User manual for TDM3885 evaluation board

4 A synchronous buck voltage regulator with integrated inductor

About this document

Scope and purpose

The TDM3885 4 A point-of-load (POL) module is an easy-to-use, fully integrated and highly efficient DC-DC module. The module's pulse width modulation (PWM) controller, MOSFETs and inductor make TDM3885 a space-efficient solution, providing accurate power delivery. The TDM3885 employs an enhanced stability engine that makes it stable with ceramic capacitors without compensation.

This user manual contains the schematic and bill of materials (BOM) for the EVAL_TDM3885_3.3Vout engineering evaluation board. The guide describes operation and use of the evaluation board itself. Detailed application information for TDM3885 is available in the TDM3885 datasheet.

Intended audience

This document is intended as a guide for design engineers evaluating the performance of TDM3885 with the engineering EVAL_TDM3885_3.3Vout demo board.

Table of contents

1 Board information

1.1 Board picture and overview

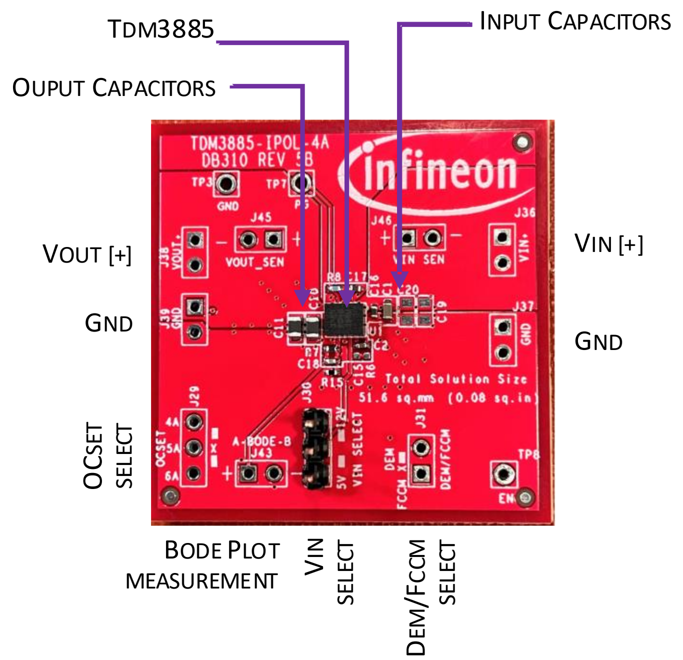


Figure 1 TDM3885 evaluation board, dimensions (width x length x thickness) = 40 mm x 40 mm x 1.5 mm

1.2 Board features

- P_{Vin} = 12 V, V_{out} = 3.3 V, I_{out} = 0 A to 4 A
- P_{Vin} = 5 V, V_{out} = 3.3 V, I_{out} = 0 A to 3 A
- F_{sw} = 600 kHz
- C_{in} = 1 x 10 µF (25 V, MLCC, 0603) + 2 x 22 µF (25 V, MLCC, 0805) + 1 x 68 µF (25 V, POSCAP) + 1 x 2.2 µF (16 V, MLCC, 0402)
- C_{out} = 3 x 47 µF (6.3 V, MLCC, 0805)
- TDM3885 IC size = 3.1 mm x 3.8 mm x 2.3 mm
- Board ID: TDM3885 EVB DB310 REV 5B

1.3 Connections and operating instructions

The TDM3885 demo board allows dual configuration +12 V or +5 V for the input power and can deliver up to 4 A load current. The operation modes and overcurrent protection (OCP) limits can be selected through jumpers.

Table 1 Connections

Label		Description
Input	V_{in}	[J36] connect input power (+12 V or +5 V) to this pin
	GND	[J37] return of input power
	V_{in} SNS	[J46] sense pins for the P_{Vin}
Output	V_{out}	[J38] connect a load (4 A max.) to this pin
	GND	[J39] return of V_{out}
	V_{out} SNS	[J45] sense pins for the V_{out}
Bode	A	Use [J43] for bode plot measurement
	B	Use [J43] for bode plot measurement
OCSET select	OC SET	Use [J29] jumper to select one of three OCP limits: 4 A; 5 A (w/o jumper); 6 A
P_{Vin} select	V_{in}	Use [J30] jumper to select PV_{IN}: +12 V or +5V
P_{good}	P_{good}	[TP7] test point, connect a scope probe to this pin to monitor power good signal
EN	Enable node	[TP8] test point, connect a scope probe to this pin to monitor EN signal
DEM/FCCM select	DEM/FCCM	Use [J31] jumper to select DEM or FCCM: DEM, FCCM (w/o) jumper

1.4 Power-on procedure

Table 2 Power-on steps

Jumper	Description
J29	Configure jumper to set OCP threshold
J30	Configure jumper to select P_{Vin}
J31	Configure jumper to select between FCCM and DEM
Load	Connect load to V_{out} [+], V_{out} [-]
Power supply	Connect power supply to V_{in} [+], V_{in} [-]
Apply P_{Vin}	$P_{Vin} \leq 14$ V
Apply load current	$I_{out} \leq 4$ A

Note: Make sure the input supply is turned off before reconfiguring any jumper placement.

1.5 PCB layout

The PCB is a six-layer board (1.5 in. x 1.5 in.) using FR4 material. Top and bottom layers use 0.5 oz. base copper plus 1.5 oz. plating. Inner layers use 2 oz. copper. The PCB thickness is 0.062 in. Layer stack-up is top – GND1 – GND2 – signal – GND3 – bottom.

The TDM3885 and other major power components are mounted on the top side of the board.

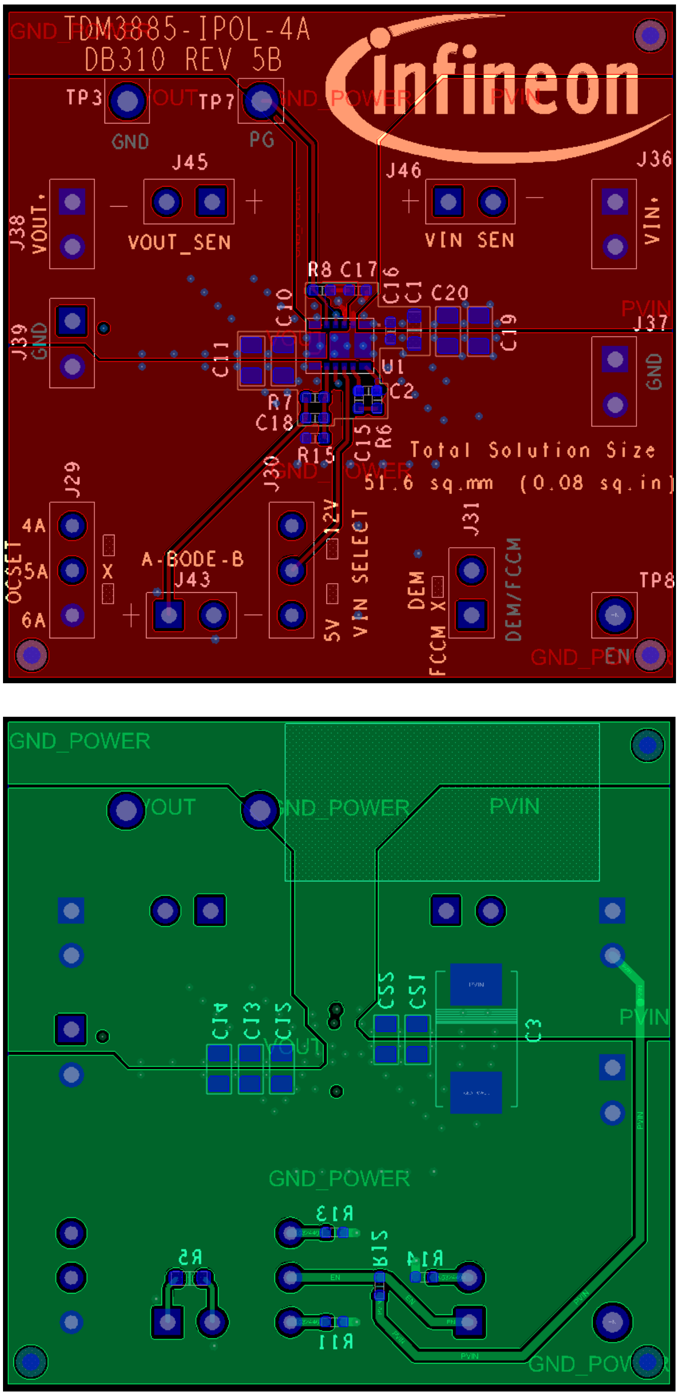


Figure 2 Layer stack-up – top and bottom

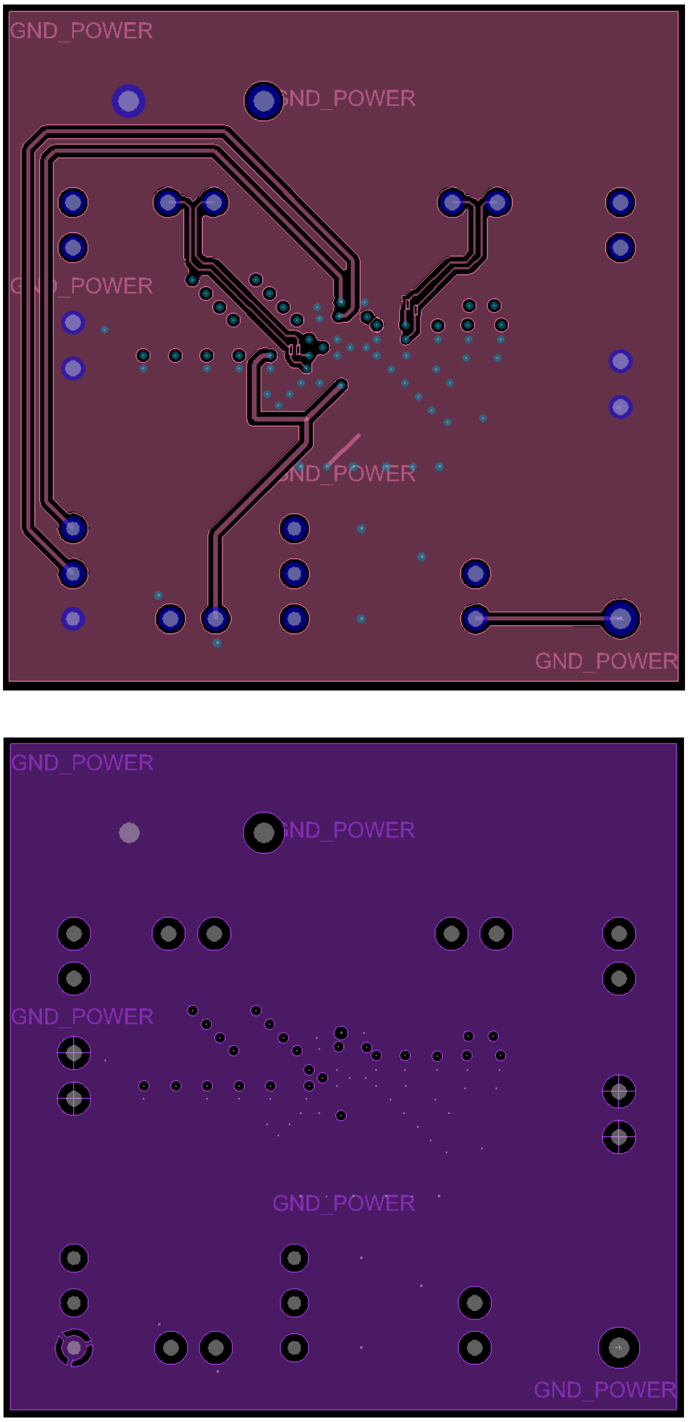


Figure 3 Layer stack-up – signal (top) and GND 1 (bottom)

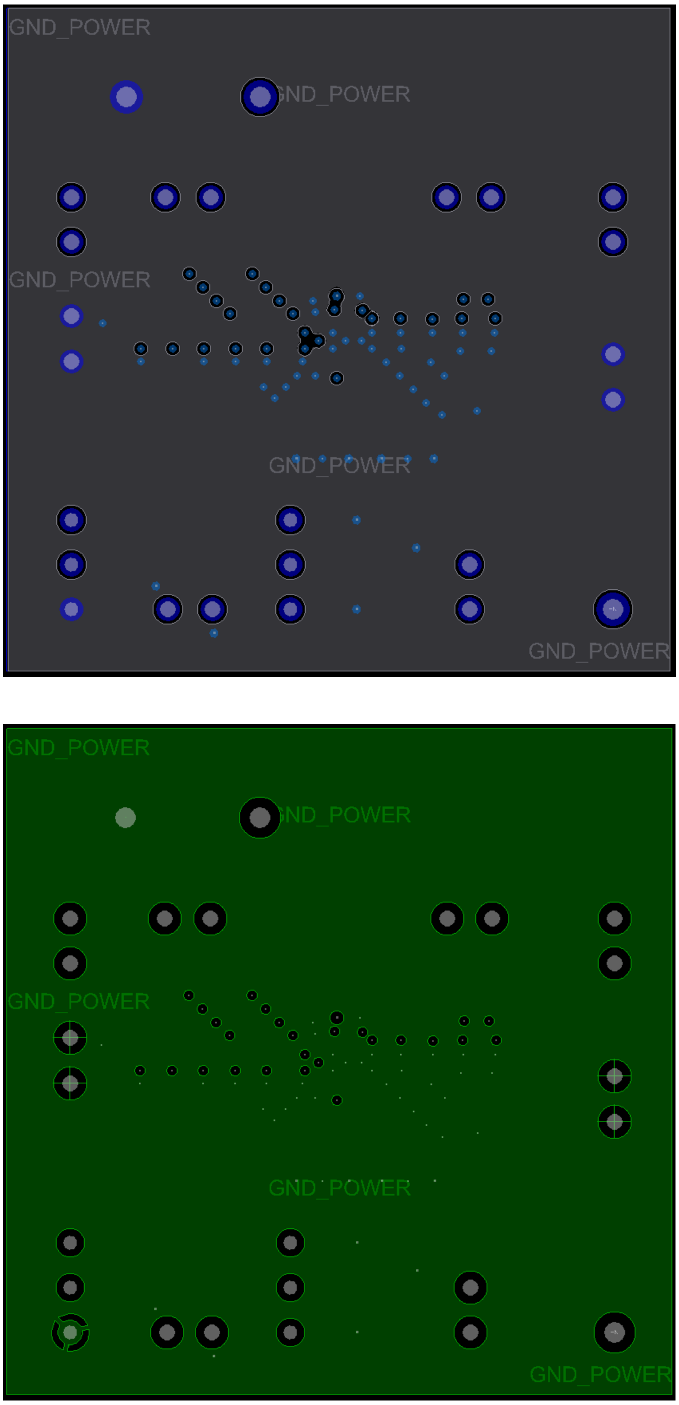


Figure 4 GND 2 (top) and GND 3 (bottom)

1.6 Schematic

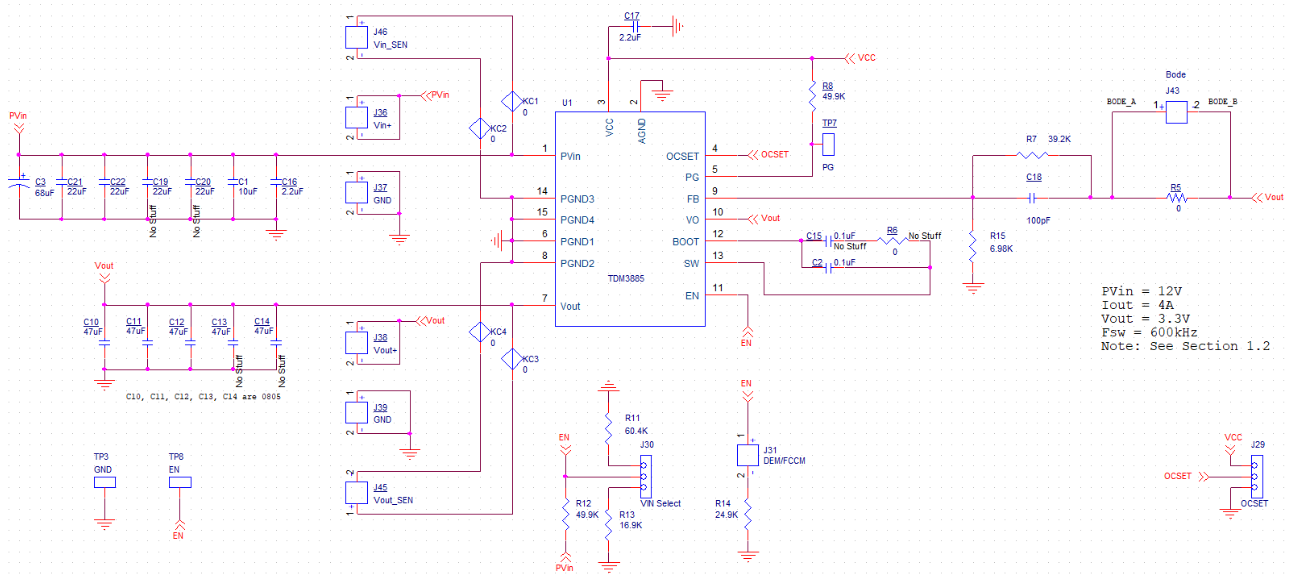


Figure 5 **Schematic of the TDM3885 evaluation board**

1.7 Bill of materials

Table 3 Bill of materials

Qty.	Part reference	Value	Manufacturer	Part number	Description
1	C1	10 µF	Murata	GRM188R61E106MA73J	Ceramic capacitor, 10 µF, 0603, 25 V, X5R, 20%
1	C2	0.1 µF	TDK	C1005X7R1C104K	Ceramic capacitor, 0.1 µF, 0402, 16 V, X7R, 10%
1	C3	68 µF	Panasonic	25TQC68MYF	POSCAP, D2L, 25 V, 20%
3	C10, C11, C12	47 µF	TDK	C2012X5R0J476M	Ceramic capacitor, 47 µF, 0805, 6.3 V, X5R, 20%
1	C16	2.2 µF	Murata	GRT155R61E225KE13D	2.2 µF, 0402, 25 V, X5R, 10%
1	C17	2.2 µF	TDK	C1005X6S1C225K050BC	Ceramic capacitor, 2.2 µF, 0402, 16 V, X6S, 10%
1	C18	100 pF	JDI	500R07N101JV4T	100 pF, 0402, 50 V, C0G, 5%
2	C21, C22	22 µF	Murata	GRM21BR61E226ME44L	Ceramic capacitor, 22 µF, 0805, 25 V, X5R, 20%
1	R5	0	Panasonic	ERJ-3GEY0R00V	Resistor, 0 Ω, 1/10 W, 5%, 0603
1	R7	39.2K	Panasonic	ERJ-2RKF3922x	Resistor, 39.2 kΩ, 1/10 W, 1%, 0402
2	R8, R12	49.9K	Panasonic	ERJ-2RKF4992X	Resistor, 49.9 kΩ, 1/10 W, 1%, 0402
1	R11	60.4K	Yageo	RC0402FR-0760K4L	Resistor, 60.4 kΩ, 1/10 W, 1%, 0402
1	R13	16.9K	Panasonic	ERJ-2RKF1692X	Resistor, 16.9 kΩ, 1/16 W, 1%, 0402
1	R14	24.9K	Panasonic	ERJ-2RKF2492X	Resistor, 24.9 kΩ, 1%, 1/10 W, 0402
1	R15	6.98K	Vishay	541-6.98KLCT-ND	Resistor, 6.98 kΩ, 1/16 W, 1%, 0402
1	U1	TDM3885	Infineon	TDM3885	4 A iPOL synchronous buck voltage regulator with integrated inductor

2 Typical operating waveforms

2.1 P_{Vin} = 5 V

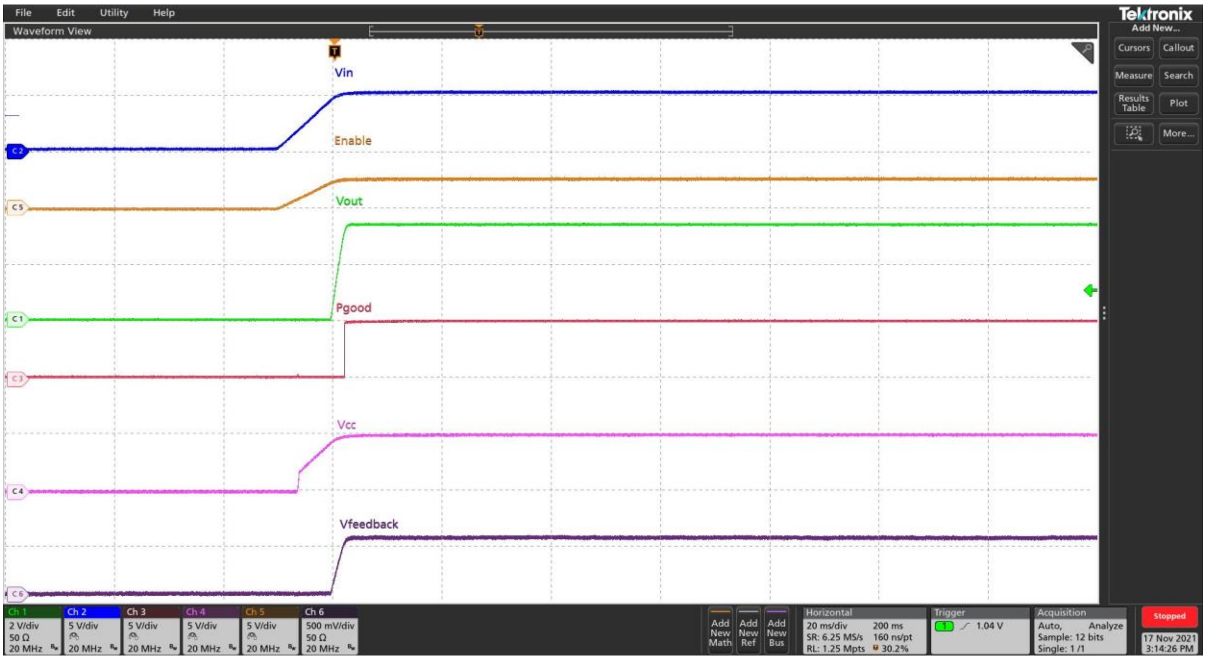


Figure 6 **Start-up, P_{Vin} = 5 V, V_{out} = 3.3 V, I_{out} = 0 A, FCCM. Ch1 = V_{out}, Ch2 = P_{Vin}, Ch3 = P_{good}, Ch4 = V_{CC}, Ch5 = enable, Ch6 = $V_{feedback}$**

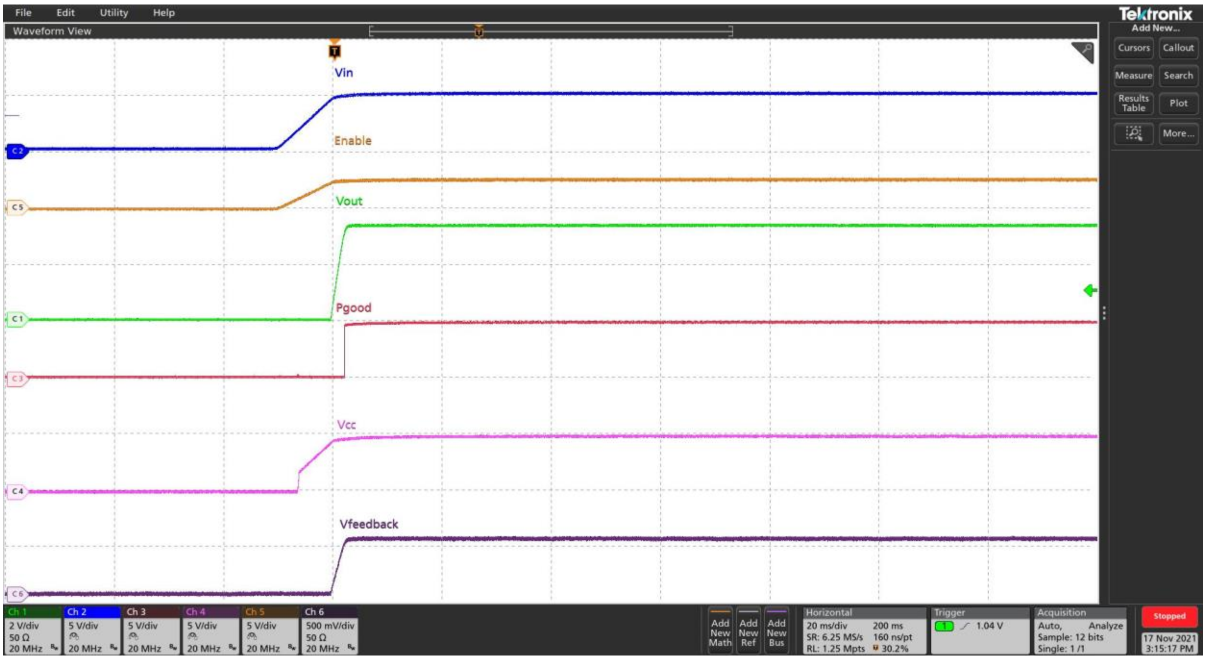


Figure 7 **Start-up, P_{Vin} = 5 V, V_{out} = 3.3 V, I_{out} = 3 A, FCCM. Ch1 = V_{out}, Ch2 = P_{Vin}, Ch3 = P_{good}, Ch4 = V_{CC}, Ch5 = enable, Ch6 = $V_{feedback}$**

2.2 P_{Vin} = 12 V

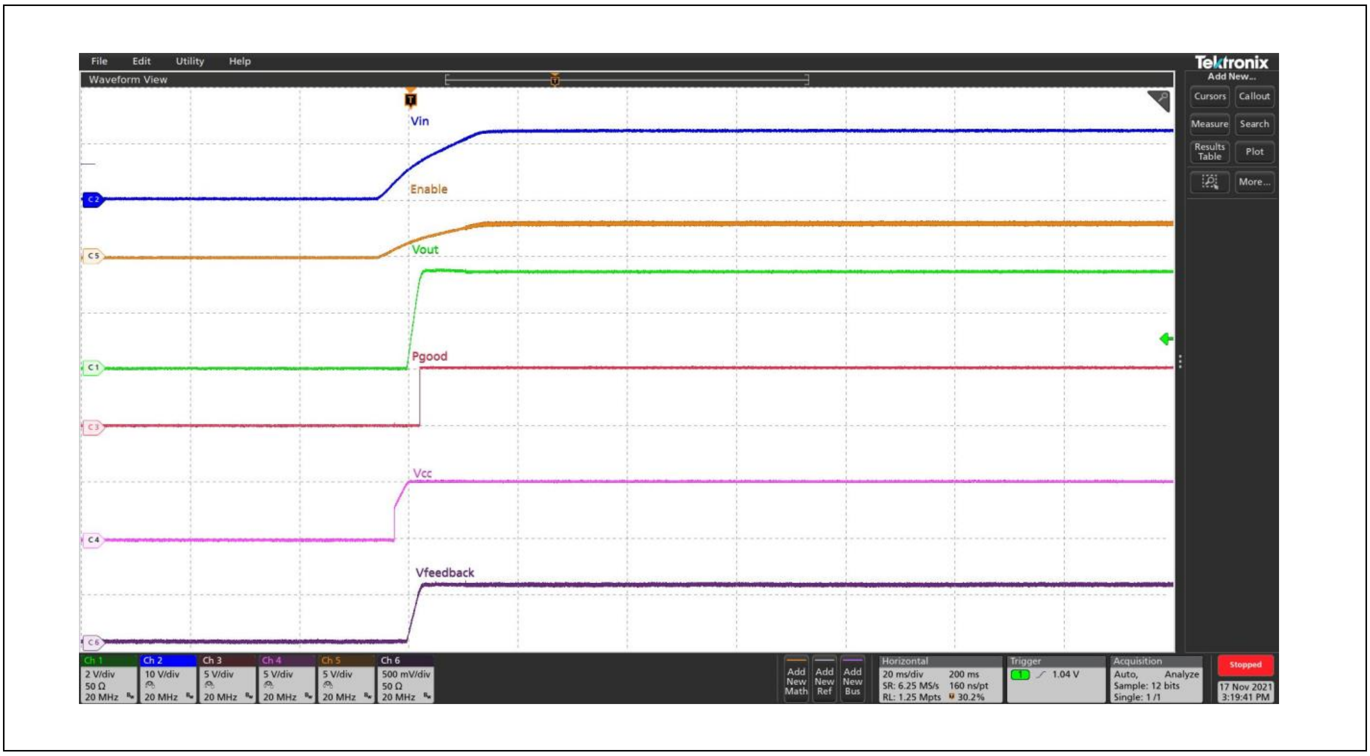


Figure 8 **Start-up, P_{Vin} = 12 V, V_{out} = 3.3 V, I_{out} = 0 A, FCCM. Ch1 = V_{out}, Ch2 = P_{Vin}, Ch3 = P_{good}, Ch4 = V_{CC}, Ch5 = enable, Ch6 = $V_{feedback}$**

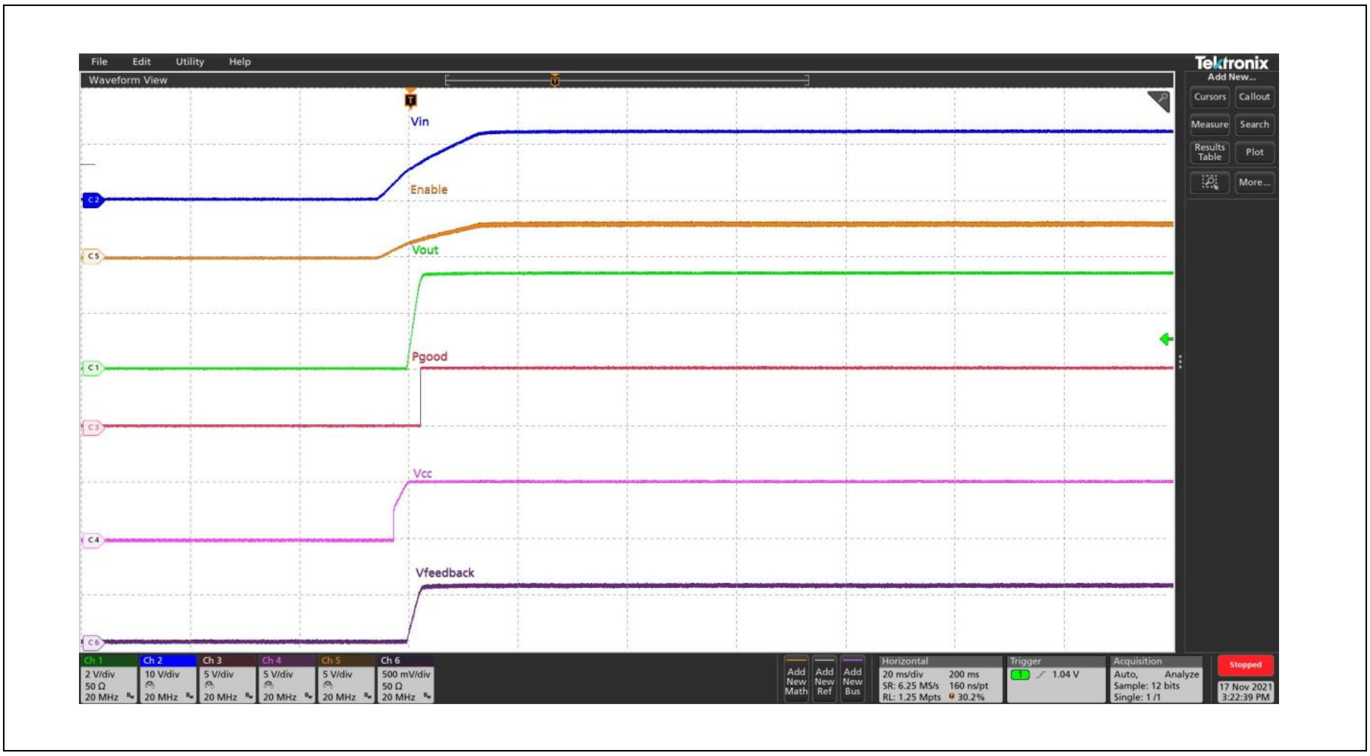


Figure 9 **Start-up, P_{Vin} = 12 V, V_{out} = 3.3 V, I_{out} = 4 A, FCCM. Ch1 = V_{out}, Ch2 = P_{Vin}, Ch3 = P_{good}, Ch4 = V_{CC}, Ch5 = enable, Ch6 = $V_{feedback}$**

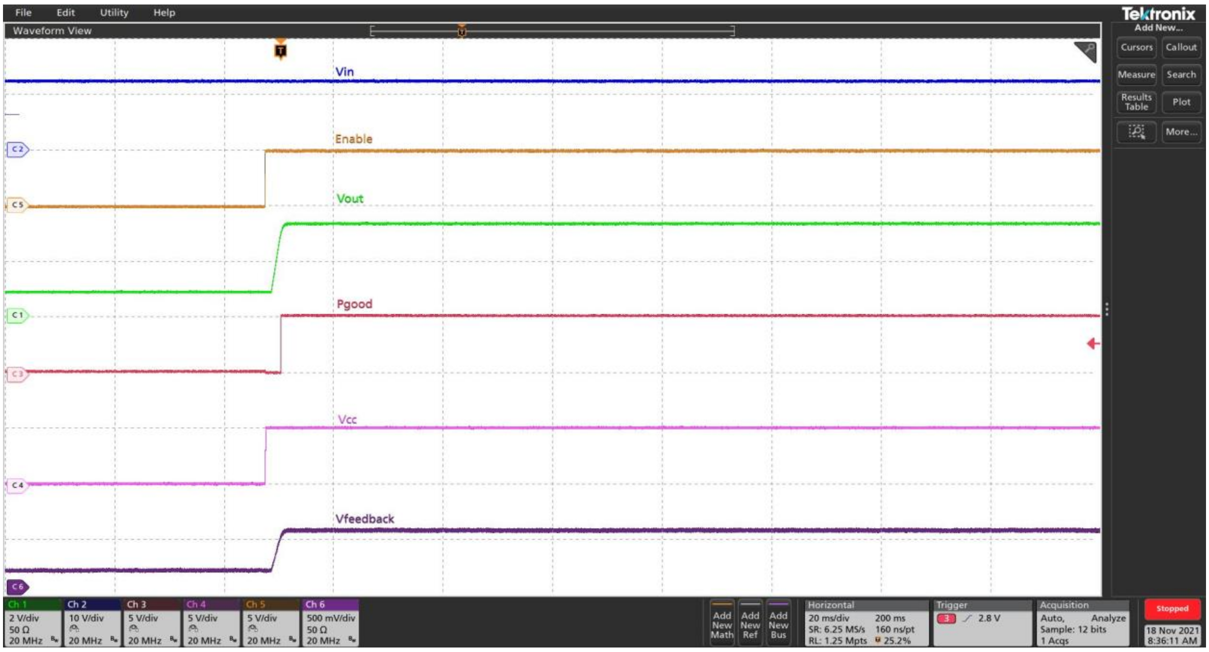


Figure 10 **Start-up pre-bias (1 V), P_{Vin} = 12 V, V_{out} = 3.3 V, I_{out} = 0 A, FCCM. Ch1 = V_{out}, Ch2 = P_{Vin}, Ch3 = P_{good}, Ch4 = V_{CC}, Ch5 = enable, Ch6 = $V_{feedback}$**

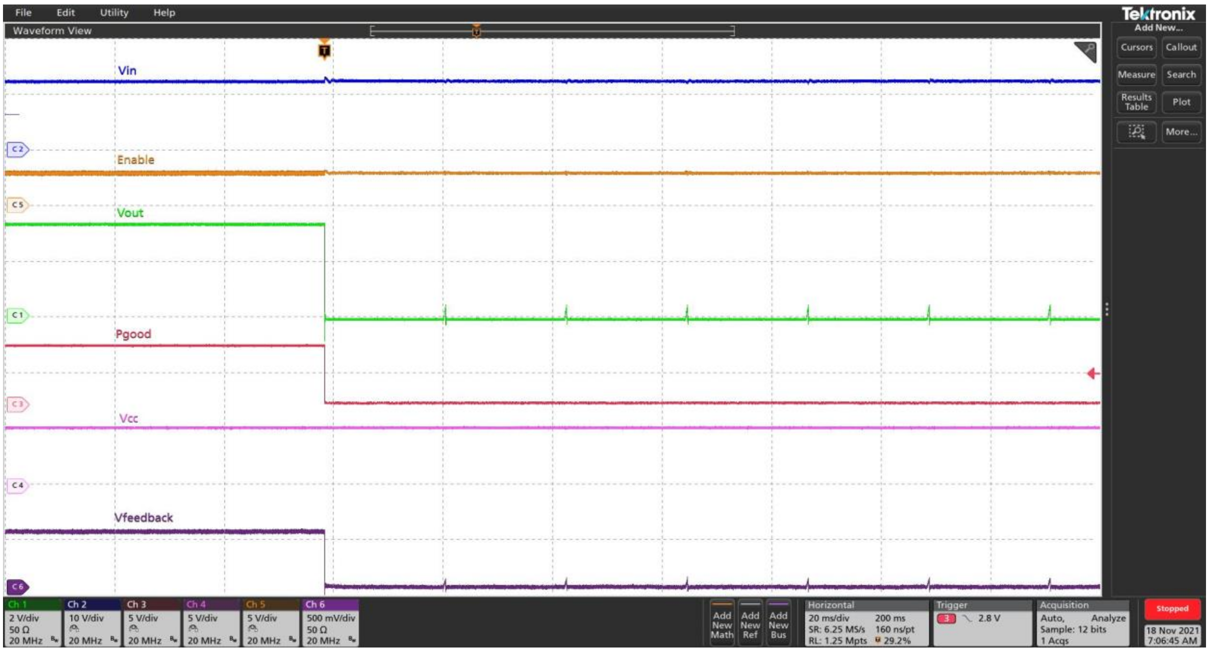


Figure 11 **Short-circuit, P_{Vin} = 12 V, V_{out} = 3.3 V, I_{out} = 4 A, FCCM. Ch1 = V_{out}, Ch2 = P_{Vin}, Ch3 = P_{good}, Ch4 = V_{CC}, Ch5 = enable, Ch6 = $V_{feedback}$**

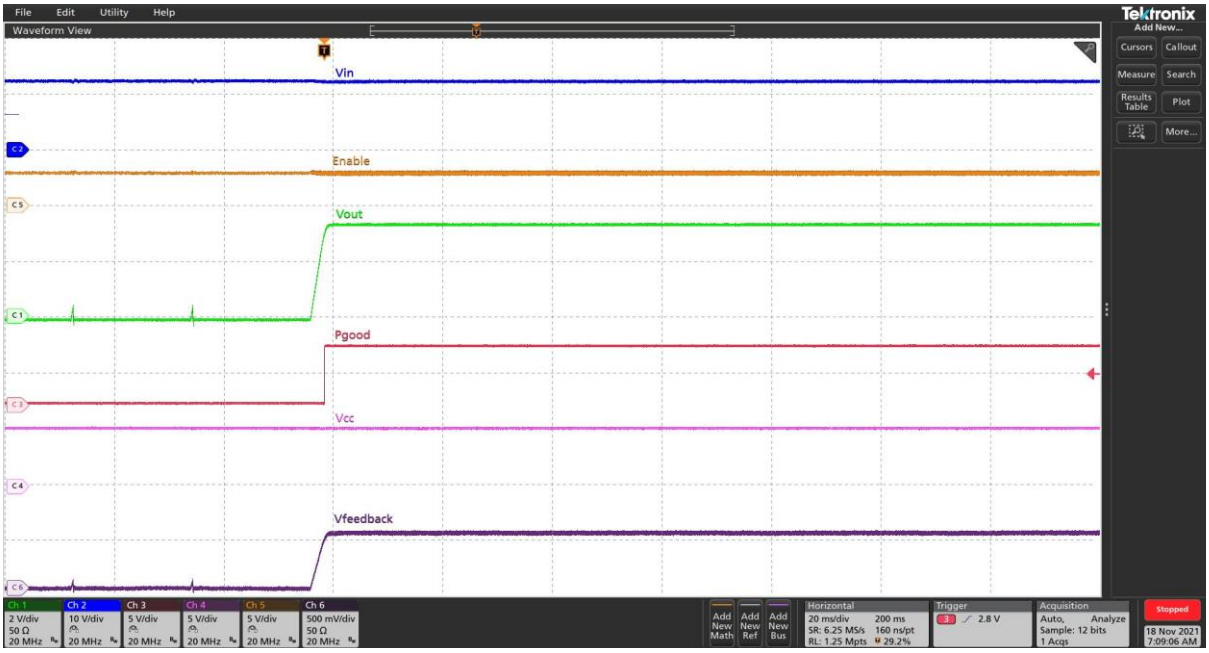


Figure 12 Recover from a shorted V_{out}, P_{Vin} = 12 V, V_{out} = 3.3 V, I_{out} = 4 A, FCCM. Ch1 = V_{out}, Ch2 = P_{Vin}, Ch3 = P_{good}, Ch4 = V_{CC}, Ch5 = enable, Ch6 = $V_{feedback}$

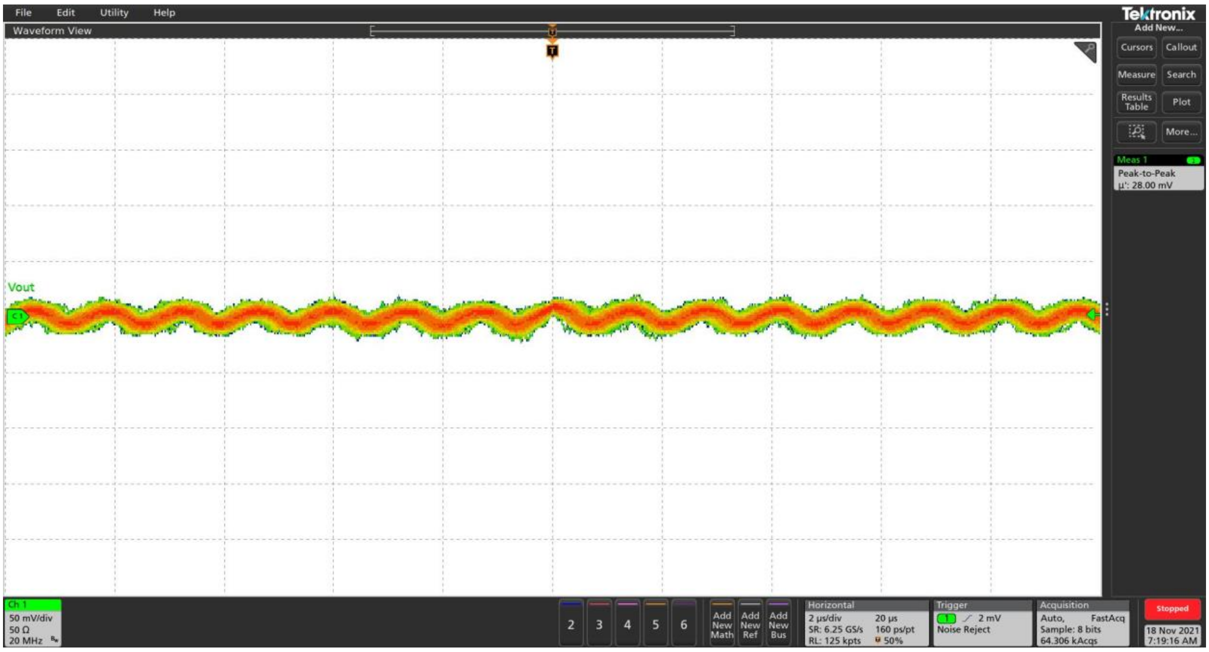


Figure 13 V_{out} ripple, P_{Vin} = 12 V, V_{out} = 3.3 V, I_{out} = 4 A, FCCM. Ch1 = V_{out}

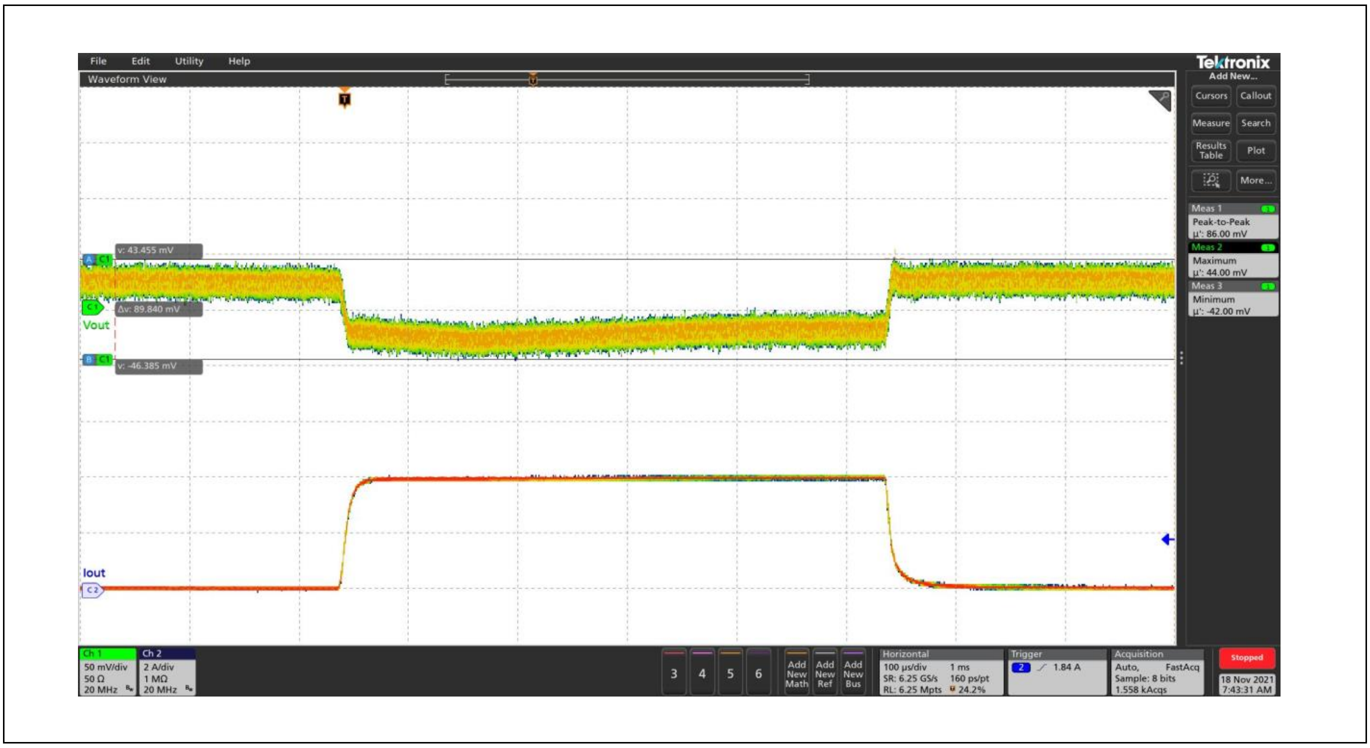


Figure 14 **Transient response, P_{Vin} = 12 V, V_{out} = 3.3 V, I_{out} = 0 A to 3 A, FCCM. Ch1 = V_{out}, Ch2 = I_{out}. Slew rate = 5 A/µS**

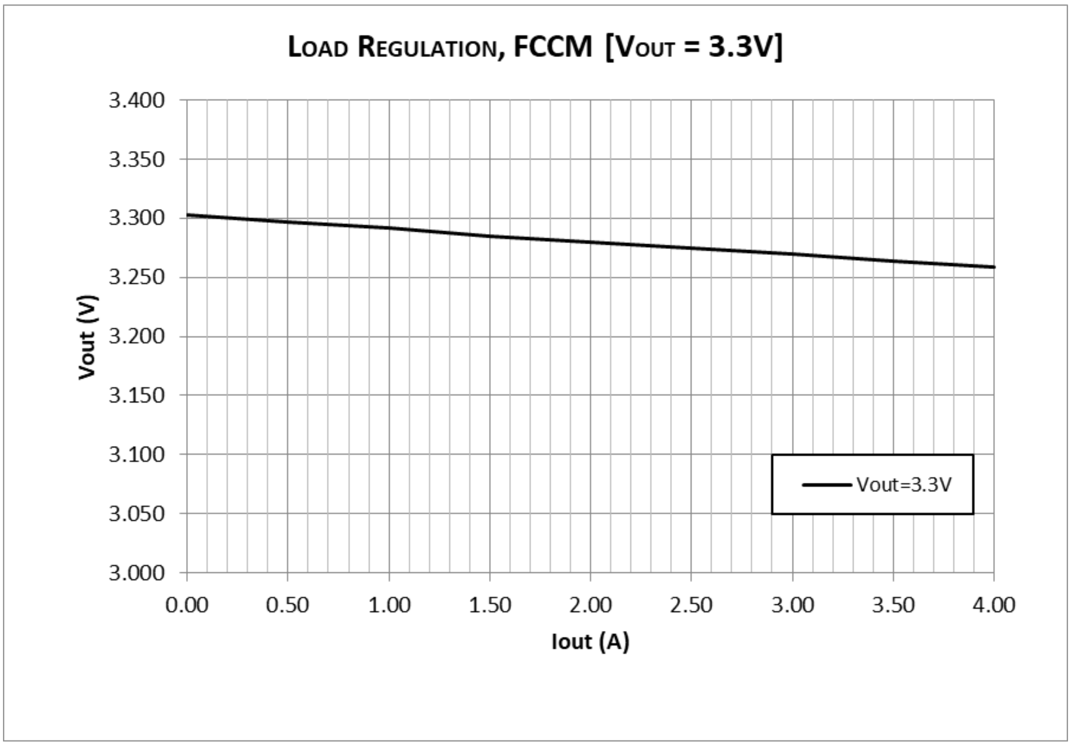


Figure 15 Load regulation, P_{Vin} = 12 V, V_{out} = 3.3 V

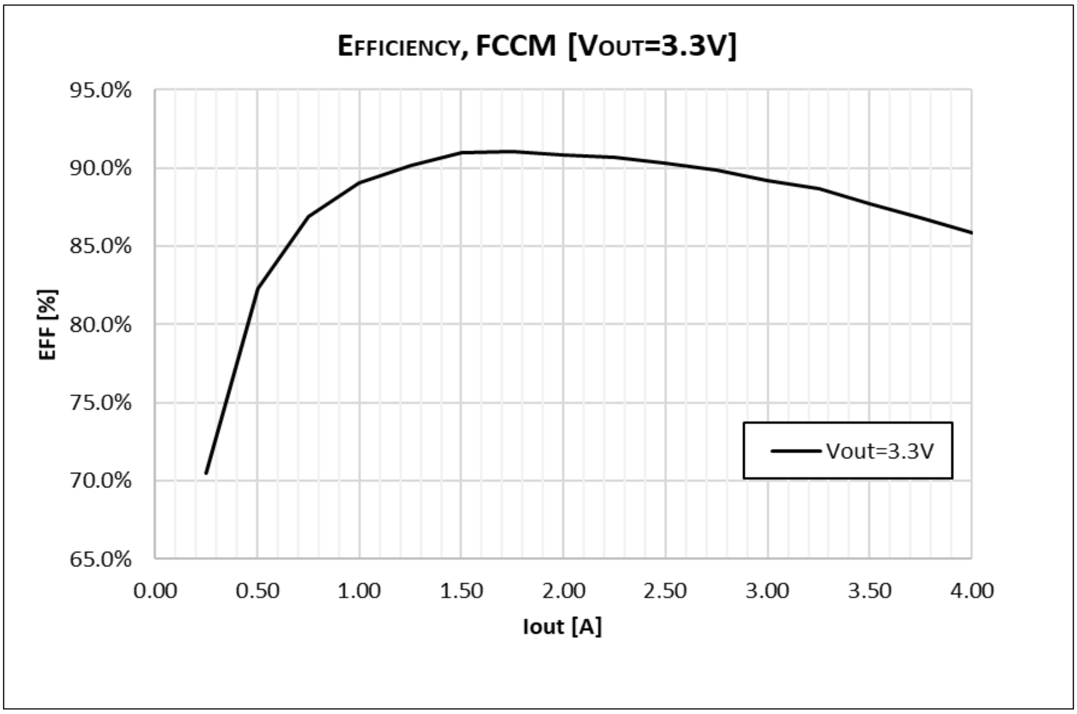
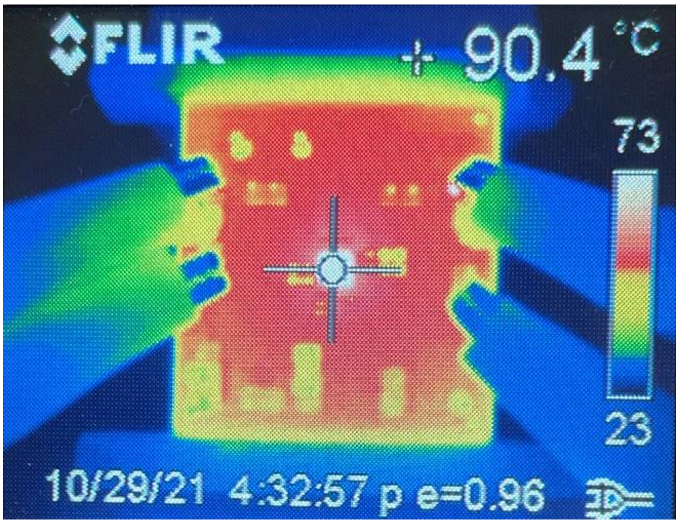


Figure 16 Efficiency, P_{Vin} = 12 V, V_{out} = 3.3 V

Room temperature, no airflow.



Board data:
TDM3885 EVB DB310 REV 5B
Dimensions (width x length x thickness) = 40 mm x 40 mm x 1.5 mm

Figure 17 Thermal image of the board at 4 A load, P_{Vin} = 12 V, V_{out} = 3.3 V, T_a = 25°C

Revision history

Document version	Date of release	Description of changes
V 1.0	2022-04-28	Initial release

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