EVAL_600W_FBFB_XDPP user guide

Digital power controller with PMBus

About this document

Scope and purpose

This document explains the hardware features and serves as the user guide for the EVAL_600W_FBFB_XDPP evaluation board, designed by Infineon Technologies. The **XDPP1100-Q024** digital controller belongs to Infineon's **XDP™ digital controller family**. It is optimized to provide high performance and design flexibility for controlling DC-DC power converters. This controller helps designers to achieve high efficiency, system control, and cost-saving goals for applications such as telecom, servers, and data centers. EVAL_600W_FBFB_XDPP offers an easy-to-use test platform for stand-alone evaluation of the 24-pin XDPP1100 controller's performance. To introduce and explore the various features of XDPP1100-Q024, this document explains how to use XDPP1100-Q024 to control an isolated hard-switching full-bridge DC-DC power converter.

Intended audience

Power supply design engineers, system engineers, embedded power designers

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1 General description

The evaluation board features the **XDPP1100-Q024** digital power controller, which is the smallest in the class available on the market. It drives Infineon's state-of-the-art MOSFETs (**OptiMOS™ 5 100 V** and **OptiMOS™ 6 40 V**) using Infineon's dual-channel gate drivers (**EiceDRIVER™ 2EDL8024G** and **EiceDRIVER™ 2EDL8124G**) in a full-bridge isolated dc-dc power supply topology.

The EVAL_600W_FBFB_XDPP evaluation kit contains the following boards which are orderable separately:

1. Isolated full-bridge DC-DC converter power-board, EVAL_600W_FBFB_XDPP
2. XDPP1100-Q024 daughterboard, EVAL_XDPP1100_Q024_DB
3. USB to I^2C dongle, USB007A1
4. Graphical user interface (the GUI can be downloaded from the Infineon website **https://softwaretools.infineon.com/tools/com.ifx.tb.tool.xdpp1100configuratortool**)

1.1 Specifications

Table 1 Specifications

	Min.	Typ.	Max.	Unit
Input voltage range	36		75	V
V_{IN} turn-on threshold	35			V
V_{IN} turn-off threshold	30			V
Maximum input current (100 percent load, 42 V_{IN})			16	A
Output voltage (at V_{IN} = 42 V to 72 V)		12		V
Output current (natural convection)			20	A
Output current (400 LFM)			50	A
Output voltage regulation (V_{IN} = 42 V to 72 V, Load 0 to 50 A, Tc = -40°C to 85°C)		±120		mV
Output voltage ripple (peak to peak at full load) With 990 µF output capacitor			300	mV
Load transient (48 V_{IN}, 990 µF and 132 µF, 1 A/µs) 50 percent to 100 percent load		±300		mV
Load-transient settling time		100		µs
Switching frequency		250		kHz
Efficiency at 48 V, 20 A		95.3		%
Operating temperature (ambient)	-40		80	°C
Isolation voltage		1500		V
Monitoring accuracy – READ_VIN	-0.75		0.75	V
Monitoring accuracy – READ_VOUT	-10		10	mV
Monitoring accuracy – READ_IOUT at 5A to 50A	-1.5		1.5	A
Monitoring accuracy – READ_TEMPERATURE	-5		5	°C

1.1 Block diagram

The block diagram of the evaluation kit is shown in **Figure 1**.

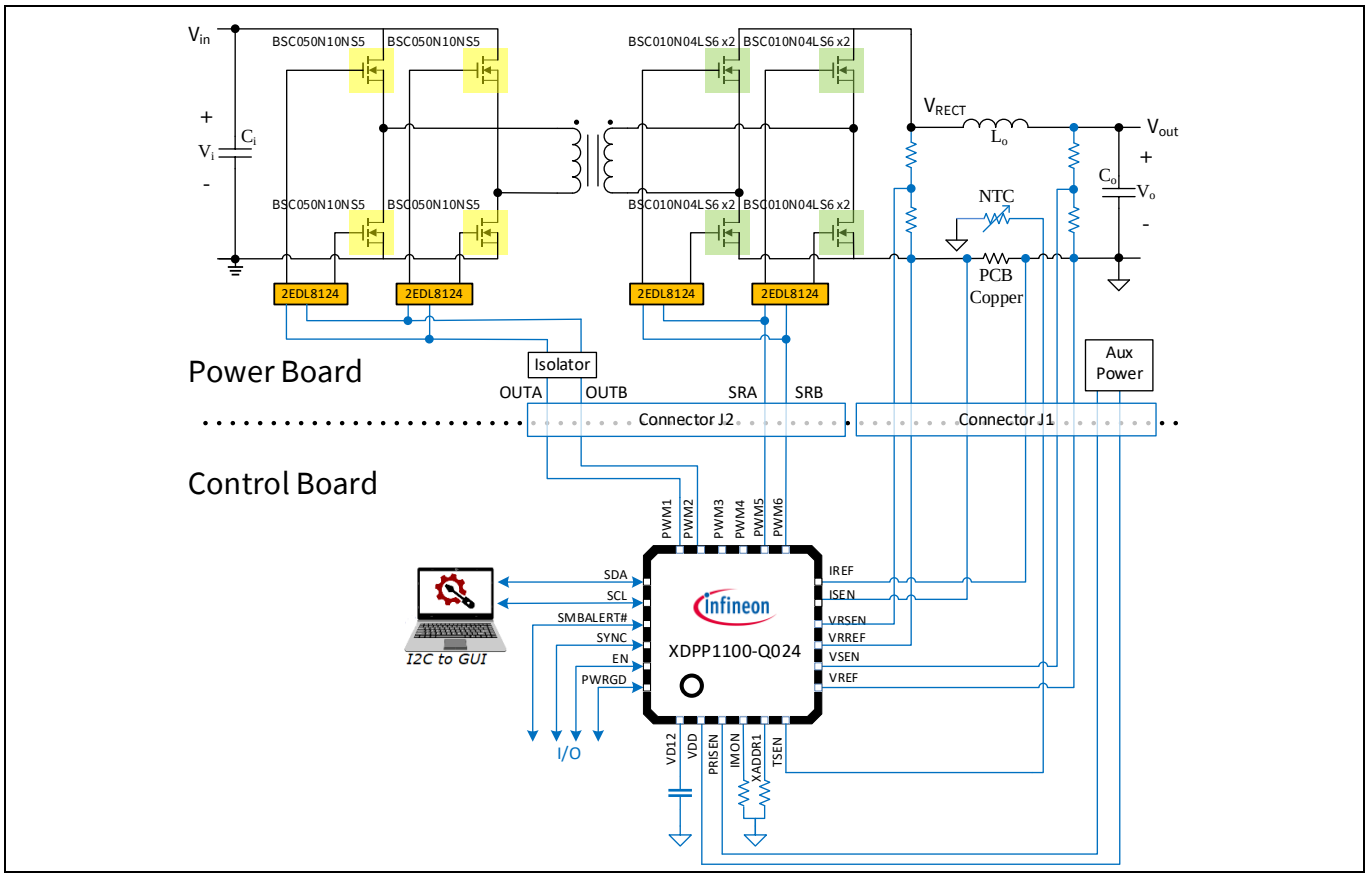


Figure 1 Block diagram

1.2 Power-board overview

The power stage is a hard-switching full-bridge to full-bridge (FB-FB) DC-DC converter (**Figure 2**). It will be connected to the XDPP1100 digital controller daughterboard through two board-to-board rectangular connectors. Voltage mode control (VMC) is implemented for output voltage regulation to convert the input voltage range of 42 V – 75 V DC to output voltage of 12 V DC. While a fan is not included in the evaluation kit, a minimum of 400 LFM air flow is required to cool down the power stage. The recommended fan part number is 04028DA-12R-AU-F0.

The power board consists of a full-bridge converter with full-bridge synchronous rectification (SR), isolated through a planar transformer, a non-dissipative snubber, and an auxiliary power supply.

The planar transformer provides isolation between the input and the output with 3:1 turns ratio. It allows versatile polarity configurations and grounding connections for the input and output terminals. Below V_{IN} = 42 V the converter will lose 12 V regulation, and the output voltage will drop to around 10.8 V at V_{IN} = 36 V. However, it can still provide the full load current.

The output current is sensed using a small PCB copper shunt, saving power loss and cost of the precision sense resistor.

The main Infineon components used in the 600 W FB-FB evaluation board are:

- **XDPP1100 XDP™** IDC digital controller

- **OptiMOS™ 5 100 V** BSC050N10NS5, 100 V 5 mΩ, SuperS08 power transistor
- **OptiMOS™ 6 40 V** BSC010N04LS6, 40 V 1 mΩ, SuperS08 power transistor
- **EiceDRIVER™ 2EDL8024G** – Infineon's isolated dual-channel junction-isolated gate driver
- **EiceDRIVER™ 2EDL8124G** – Infineon's isolated dual-channel junction-isolated gate driver

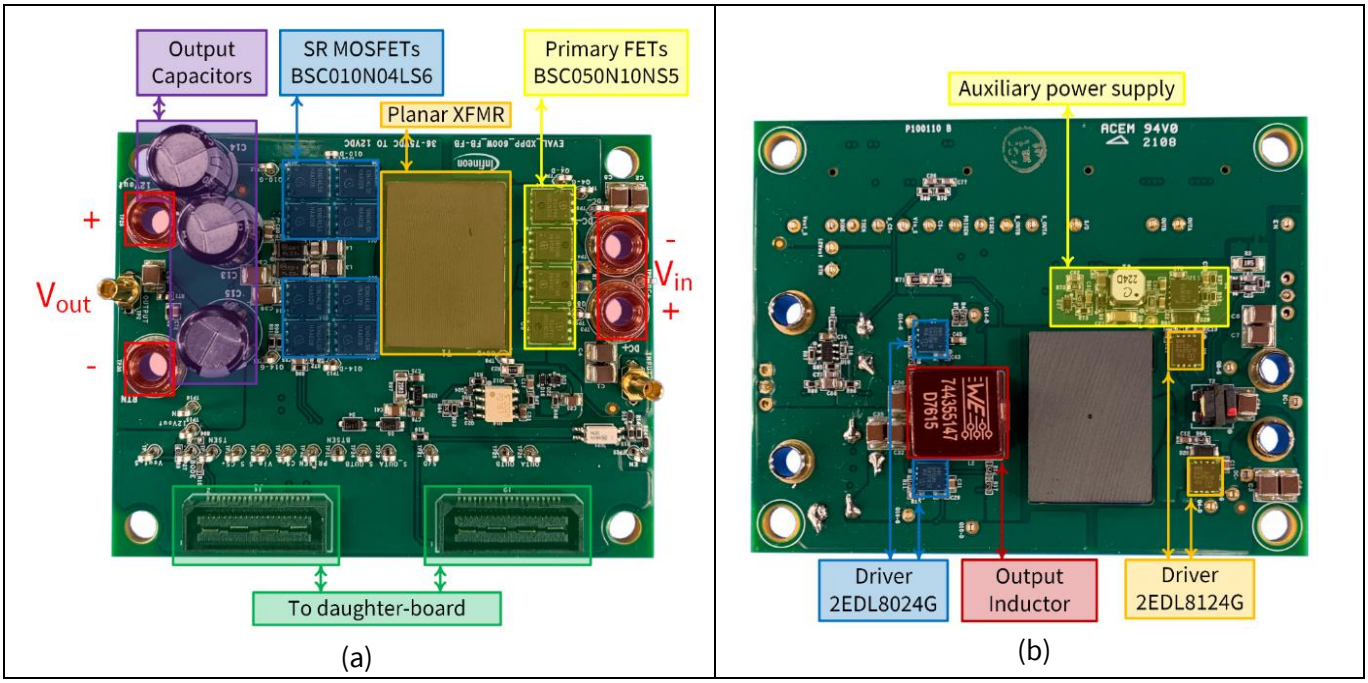


Figure 2 Power board - a) top view, b) bottom view

1.2.1 Non-dissipative snubber

An Infineon-designed non-dissipative capacitor-diode-inductor (CDL) snubber circuit is used to improve the performance of the SR stage. This CDL resonant clamp snubber circuit recycles the reverse recovery current of the SR FETs' body diodes into the output capacitors. It improves the system efficiency, reduces the high frequency ringing across the secondary SR FETs, and makes it possible to have lower voltage switches in the SR stage.

1.2.2 Auxiliary power supply

An onboard auxiliary power supply circuit on the power board (**Figure 2b**) provides 10 VDC for primary gate drivers, isolated 10 V for the secondary gate drive circuits, and 3.3 V DC to supply XDPP1100 on the daughterboard. The approximate minimum input voltage for the auxiliary power supply operation is 30 V DC.

1.3 Daughterboard overview

The control stage of this evaluation kit is on the EVAL_XDPP1100_Q024_DB daughterboard (**Figure 3**). It includes the XDPP1100-Q024 digital controller, analog filters for processing feedback signals from the power board, PWM outputs, digital inputs and outputs, I^2C connector, firmware (FW) debugger port for Lauterbach, and LED indicators. It can be supplied using an external 3.3 V DC source or from the power-board depending on the header J24 configuration (**Figure 3a**). The board-to-board rectangular header connectors are located on the bottom side of the EVAL_XDPP1100_Q024_DB daughterboard to connect to the power converter board (**Figure 3b**).

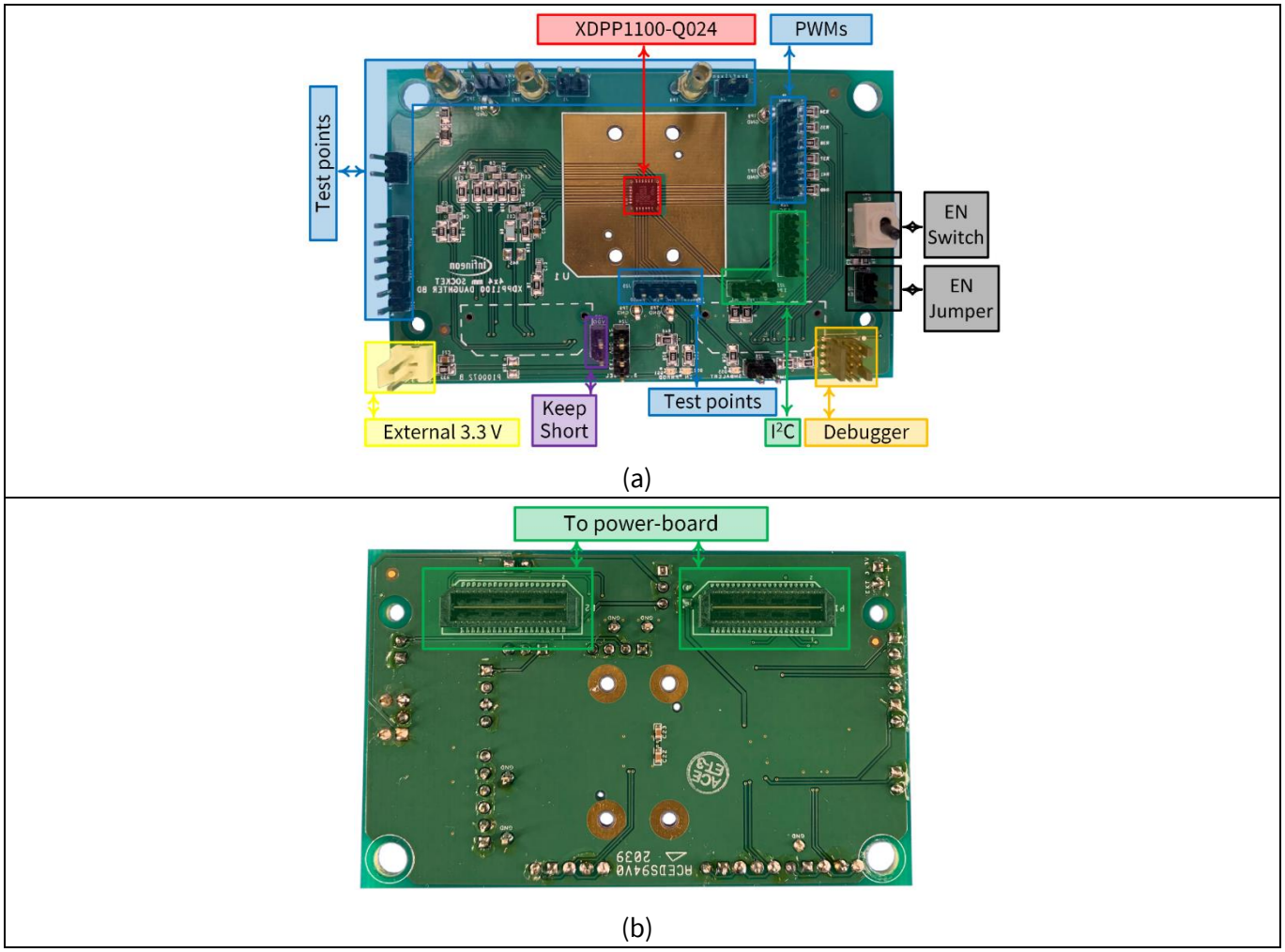


Figure 3 Daughterboard - a) top view, b) bottom view

1.3.1 Jumper settings

Table 2 Daughterboard jumper settings

Jumper	Description	Functionality
J23	External 3.3 V	External 3.3 V (0.1 A) supply should be connected to the daughterboard at J23 if external 3.3 V is selected by J24.
J24	3.3 V supply selector	- Select external 3.3 V supply by shorting pins 1 and 2. - Select power board 3.3 V supply by shorting pins 2 and 3.
J27	3.3 V jumper	Connect or disconnect 3.3 V supply to VDD of the IC. By default, this pin should be shorted.
J29	EN jumper	Control the EN pin of XDPP1100 by an onboard toggle switch (SW1) if J29 is shorted.

2 Evaluation board setup

2.1 Hardware required

- Power supply (36 V DC to 75 V DC, 16 A)
- Electronic load (600 W at 12 V DC)
- Precision shunt resistors for input and output current measurement (optional)
- Digital multimeters
- Oscilloscope (500MHz or higher bandwidth)
- Fan (suggested: 04028DA-12R-AUF) (optional at low loading)
- Infineon USB to I^2C dongle (USB007A1 or USB007B)
- Microsoft Windows 10 (32 or 64-bit)

2.2 Board setup

Figure 4 shows the XDPP1100 evaluation kit set up while the XDPP1100 daughterboard is mounted on top of the power converter board.

The board-to-board connectors provide the plug-in mechanism between the power board and the daughterboard. For connecting these two boards, align the daughterboard connectors with the power board connectors and then push it down to make sure the contact is good.

The I^2C dongle has the following color code: SCL – yellow, SDA – red, GND – black.

- For a non-isolated dongle (USB007A1), the blue wire can be used to control the EN pin of XDPP1100 through the GUI. In this case, it has to be connected to pin 2 of J29. If this wire is left floating, the EN pin cannot be controlled through the GUI.
- For an isolated dongle (USB007B), the blue wire has to be connected to 3.3 V to supply power to the dongle. In this case, the EN control could be done by the onboard switch SW1 (jumper J29 should be shorted).

The dongle can be connected to either J22 (no pin for blue wire) or J26 (has pin for blue wire), as shown in **Figure 4**.

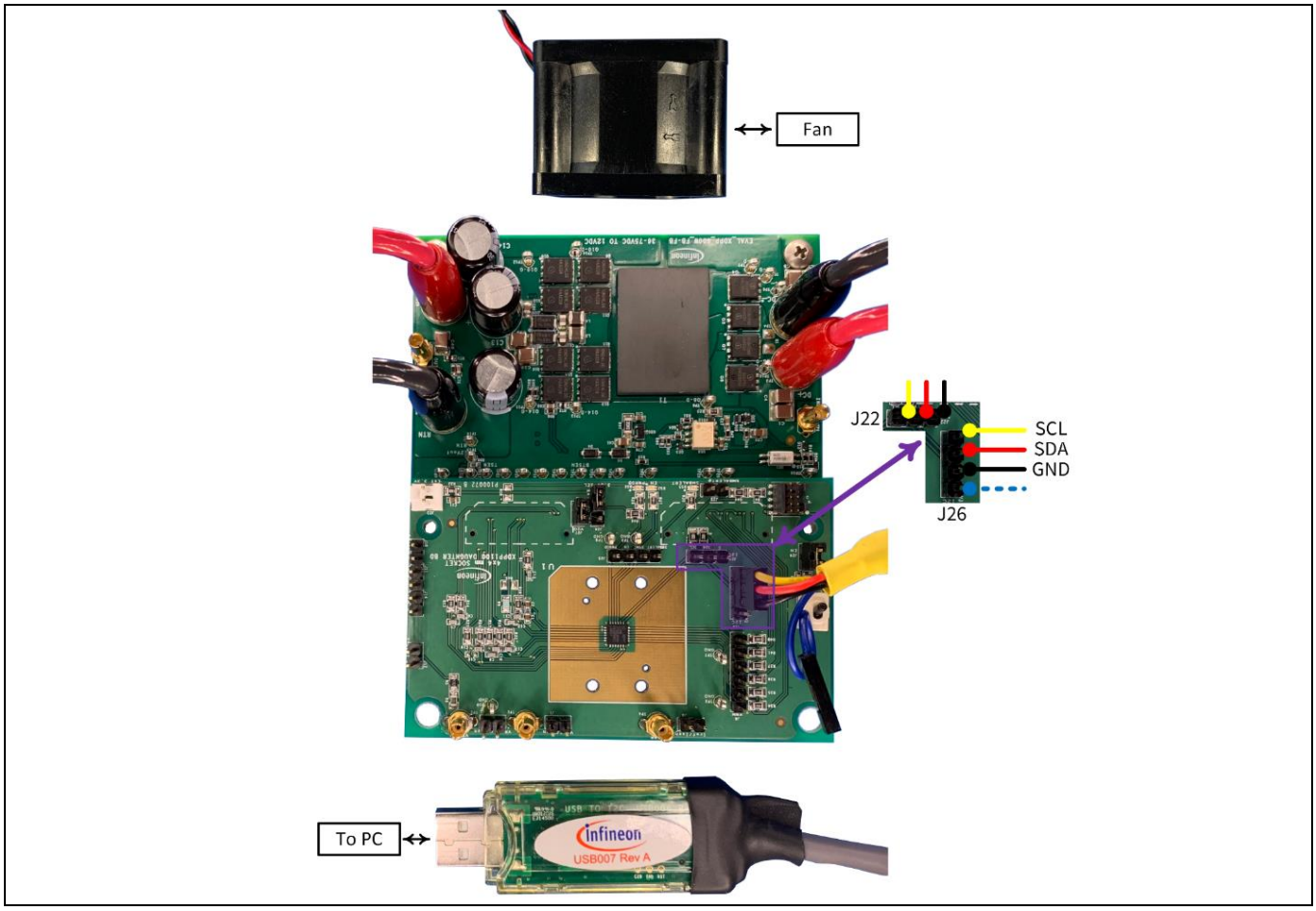


Figure 4 Evaluation test set-up

*Note: If the power board operates at room temperature with natural airflow, the maximum load current must be limited to 25 A (**Figure 5**).*

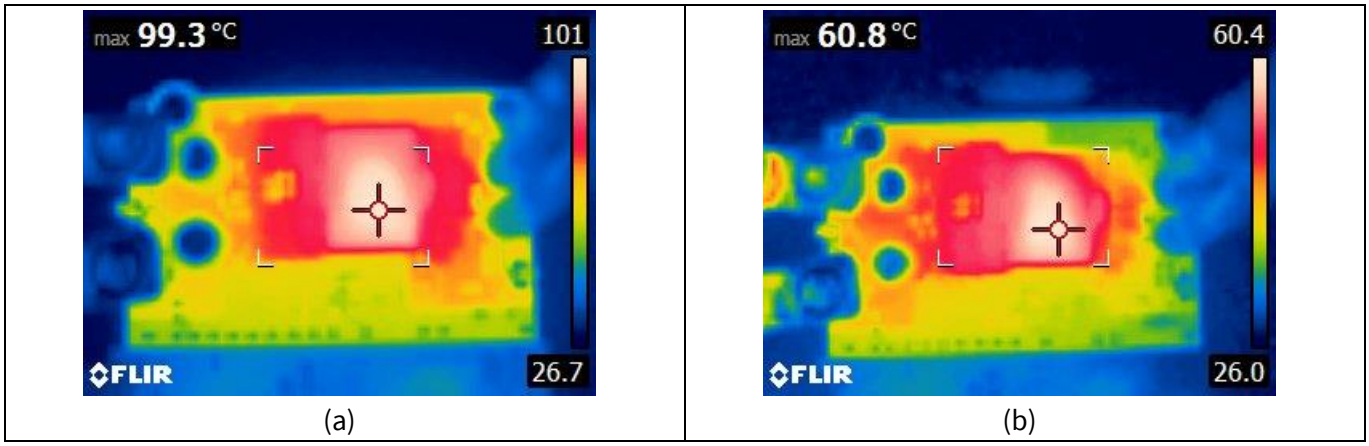


Figure 5 Thermal performance with V_{IN} = 48 V and I_{OUT} = 25 A - a) natural airflow, b) fan cooling

3 Getting started

3.1 Software GUI

Infineon provides a complimentary GUI software tool. It provides a high-level environment for users to conveniently access advanced features of the XDPP1100 digital controller without dealing with low-level programming. Online configuring, controlling and monitoring of the evaluation kit are provided through the GUI, which enhances the overall design workflow of the system. Below are the key features:

1) Step-by-step design tools to configure and optimize the XDPP1100's performance for a wide variety of DC-DC topologies
2) Fault status monitoring
3) Online telemetry reporting of V_{OUT}, I_{OUT}, V_{IN}, P_{IN}, and temperature
4) Save and load design files
5) Allows storing of PMBus configuration and I^2C registers into RAM or one-time programmable memory (OTP)
6) Allows storing of FW patch into RAM or OTP for advance customized designs and control algorithm
7) Linear11 and Linear16 Q-number format calculator tool

Detailed steps to install the GUI and initiate its communication with the XDPP1100 evaluation board are as follows:

3.1.1 System requirements

1) Ensure that the PC is connected to the internet
2) Infineon's GUI tool requires installation of *Microsoft .Net Framework 4.0* (**link to download**)
3) Security warnings during the installation should be disregarded for complete and correct installation.

3.1.2 Install GUI

Installing the GUI is the first step toward evaluating the XDPP1100. Download the installation package from the Infineon **software toolbox**. **Do not connect** the USB-to-I^2C dongle before the installation process is complete. When installing, recommend to install the XDPP1100 GUI to the default folder C:\Users\user_name\Infineon\Tools\XDPP1100-GUI.

Refer to the **XDPP1100 GUI installation guide** for any additional information about GUI installation or troubleshooting issues related to dongle connection.

3.2 Initiate the connection and communication to the XDPP1100 digital controller through the GUI

After successful installation of the GUI, USB driver, and available updates, the step-by-step procedure to connect the XDPP1100-Q024 daughterboard to the GUI for system initialization is as follows:

1) Set up the evaluation kit as shown in **Figure 4**.
2) For the power board, connect a DC power supply to the input terminals (TP 3 and TP 4), which is capable of supplying 36 V DC to 75 V DC and 16 A.

*Note: Connect the necessary digital multimeters and probes to monitor desired voltages, current signals, and waveforms **before** turning on the power supply. As a reminder, the primary and secondary sides of the power converter are isolated. Make sure to consult the circuit schematic at the end of this document and use differential probes accordingly to comply with the isolation to prevent damage to equipment and the evaluation kit! For the power board, connect an electronic load at the output terminals (TP 29 and TP 30).*

*Note: The 3.3 V VDD supply for the daughterboard is provided from an on-board auxiliary power supply in the power board. The auxiliary power supply provides 3.3 V DC bias voltage when the input voltage (TP 3 and TP 4 on the power board) is above 30 V. Alternatively, external 3.3 V DC can supply the daughterboard. In this case, the jumper placement on the J24 header has to be altered following **Figure 6**. The external bias provides flexibility, and allows the user to communicate and configure the XDPP1100 without connecting the power board to the power supply.*

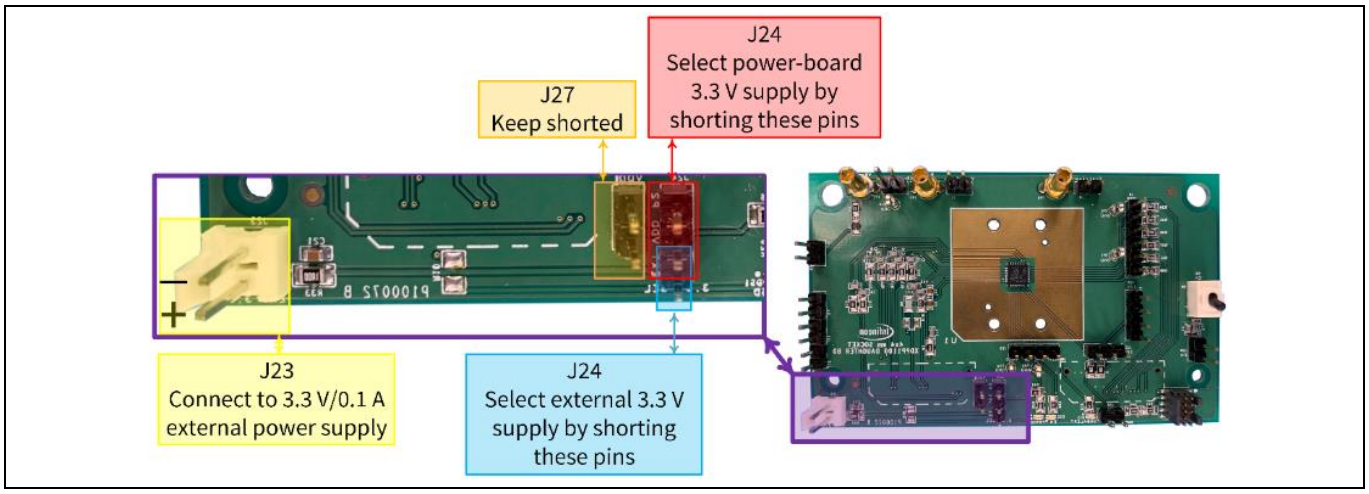


Figure 6 Daughterboard 3.3 V jumpers

3) Plug the USB dongle into the PC and the J26 header of the daughterboard (**Figure 4**).
4) If XDPP1100 is configured to operate only with the EN pin, ensure that EN switch (SW1) is in the off position (EN LED is off) for safe operation before pre-configuration. This is to avoid turning on the unit unintentionally while writing FW configuration into the memory of the digital controller.
5) Run the **XDPP1100GUI.exe**. The GUI starting window is shown in **Figure 7**.

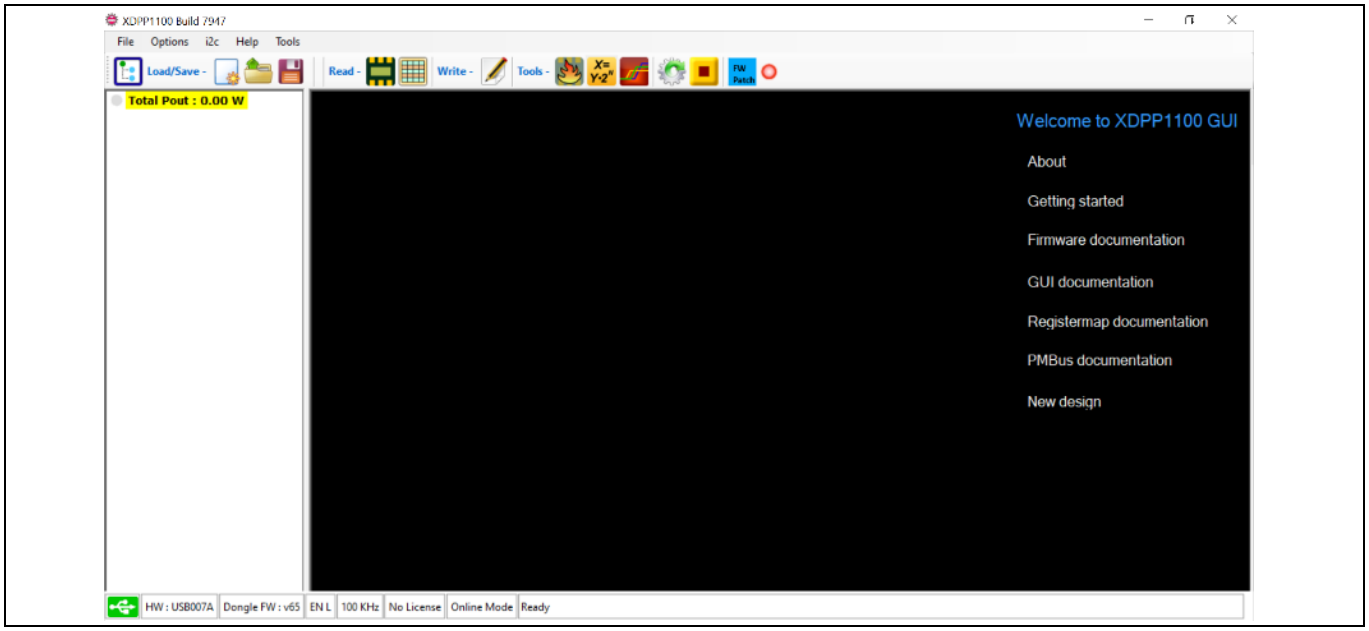


Figure 7 The XDPP1100 GUI starting window

*Note: The green USB icon at the bottom left corner of the starting window indicates that its driver is installed and updated successfully. Also, the USB hardware (HW) model and dongle FW version will be shown on the information bar at the bottom of the starting window in this case. On the other hand, the red USB icon indicates that the GUI does not recognize the dongle. A troubleshooting guide for failure in recognizing the dongle is provided in **XDP_GUI_installation_guide** (**link to download**).*

6) Use the auto-populate shortcut button to scan the device connected through the I^2C bus. If the XDPP1100 is properly biased (following step 2), the GUI will first identify the device part number and its address offset and will add the device to the design.

Note: If the XDPP1100-Q024 is pre-programmed, the GUI will read a stored program on the digital controller and restore it into the GUI. This allows users to check the configuration stored in the non-volatile memory (NVM) of the XDPP1100. The XDPP1100 has OTP NVM, with 64 kB available space for FW patch and configuration. And, if the XDPP1100 is not pre-programmed (blank IC), the registers and PMBus command have the default values, most of which are zero.

Figure 8 Auto populate

7) If the XDPP1100 is not pre-programmed;

- Click **File>Open Board Design** (**Figure 9**)
- Navigate to **..\XDPP1100_GUI\Config_files\EVAL_XDP_600W_FBFB_VMC**
- Select and open **EVAL_XDPP1100_600W_FBFB_VMC_4x4.pcd**

Figure 9 Open design file

8) The GUI will show a pop-up window (**Figure 10**). Click **Write to Device 0x10**. This will write the program into the RAM of the XDPP1100.

*Note: RAM is a volatile memory and can be used during the design phase to try different configuration settings without wasting the non-volatile OTP space. If the configuration is stored in the RAM, the configuration would be lost when the XDPP1100 is powered off. Thus, repeating steps 8 and 9 is necessary when cycling the 3.3 V VDD and restarting the MCU. Non-volatile OTP can be used to store the finalized design settings into the IC. Please refer to **Section 4.8** for storing the program in OTP.*

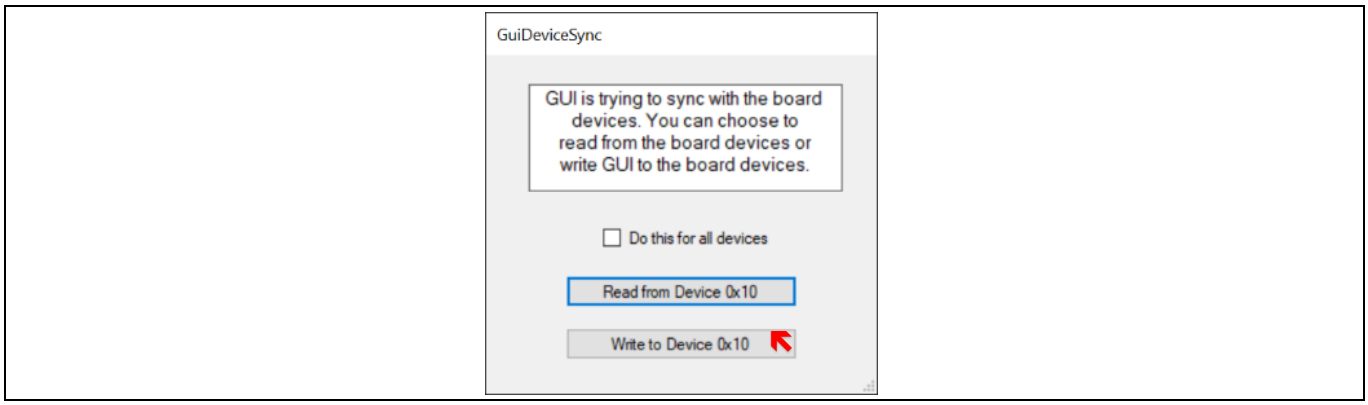


Figure 10 Write to device operation

9) For continuous monitoring of the system parameters, which are V_{IN}, V_{OUT}, I_{IN}, I_{OUT}, temperature, and P_{IN}, Click **Options>Enable Telemetry Update** (**Figure 11**). The check symbol next to each feature from the Options dropdown menu indicates that the item is enabled. Undocking the telemetry window can also be activated by enabling **Show Floating Status** (**Figure 12**) from the list.

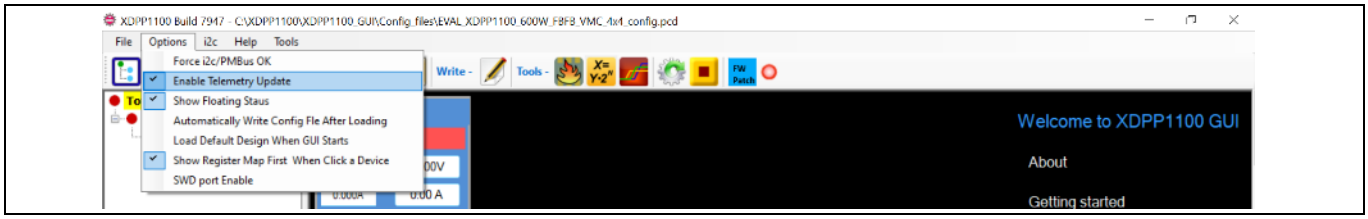


Figure 11 GUI options

Figure 12 shows the GUI after establishing communication and ensuring the configuration file is programmed to the device. To verify establishment of communication between the digital controller and the device (**Figure 12**):

- Click the **Loop0::pmbus x40** below the device part number (**XDPP1100-Q024::i2c x10**) (highlighted in yellow). It opens the PMBus configuration page of **Loop0**.

- In **PMBus Commands (Write and Read)** window, select **VOUT_COMMAND** (Code 21)
- Click **Read**. The green check indicates that reading from the device was successful.
- The **VOUT_COMMAND** should be 12 V. It shows the correct Config file is programmed into the IC.

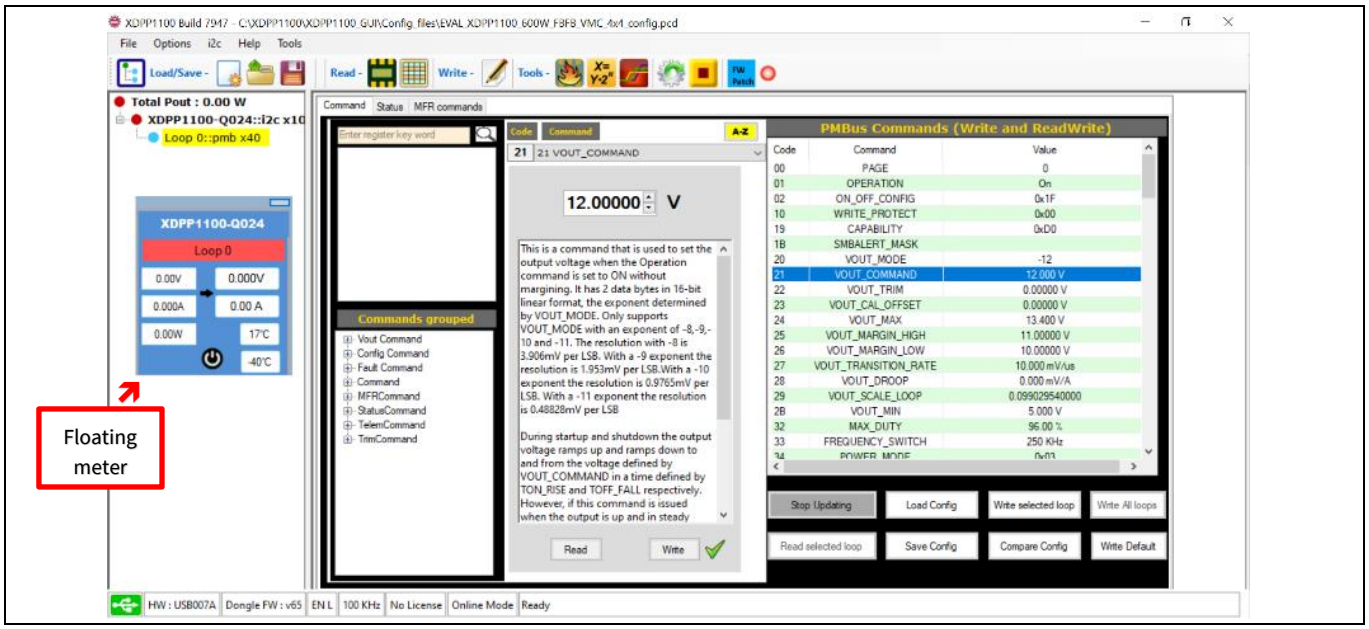


Figure 12 GUI with connected XDPP1100-Q024 and the loaded design file

The **Help** icon is located in the GUI top menu bar and provides comprehensive documentation on the wide capability of the GUI covering a number of integrated tools. These embedded tools provide an environment for fast and optimum system control design without involving in HW level programming while maintaining deep accessibility to different features of the digital controller. For more information, please refer to **Help** icon.

3.3 Powering up the converter

After successfully initiating the connection and establishing the communication between the GUI and the daughterboard (**Section 3.2**), the procedure to turn on the power converter is as follows:

*Note: Make sure all steps from **Section 3.2** are complete before moving on to the following steps!*

1) Place a fan with a minimum of 400 LFM airflow next to the power board while airflow blows over the top and the bottom of the power board where the FETs are populated. For example, supplying the recommended fan (04028DA-12R-AU-F0) with 7.5 V DC and placing it at a distance of 1 to 2 cm to the bottom side of the power board will meet the cooling criteria (**Figure 4**).
2) Set the electronic load to 5 A.
3) Enable the daughterboard using the **EN** switch (SW1) on the daughterboard.
4) To turn on the converter from the GUI:

- Click the **Loop0::pmbus x40** (highlighted in yellow in **Figure 12**). In the **Command** tab, the PMBus configuration page of Loop0 will be listed.
- In **PMBus Commands** window, select **OPERATION** (Code 01)
- Select **On** and Click **Write** (green check shows writing the PMBus command was successful) (**Figure 13**)

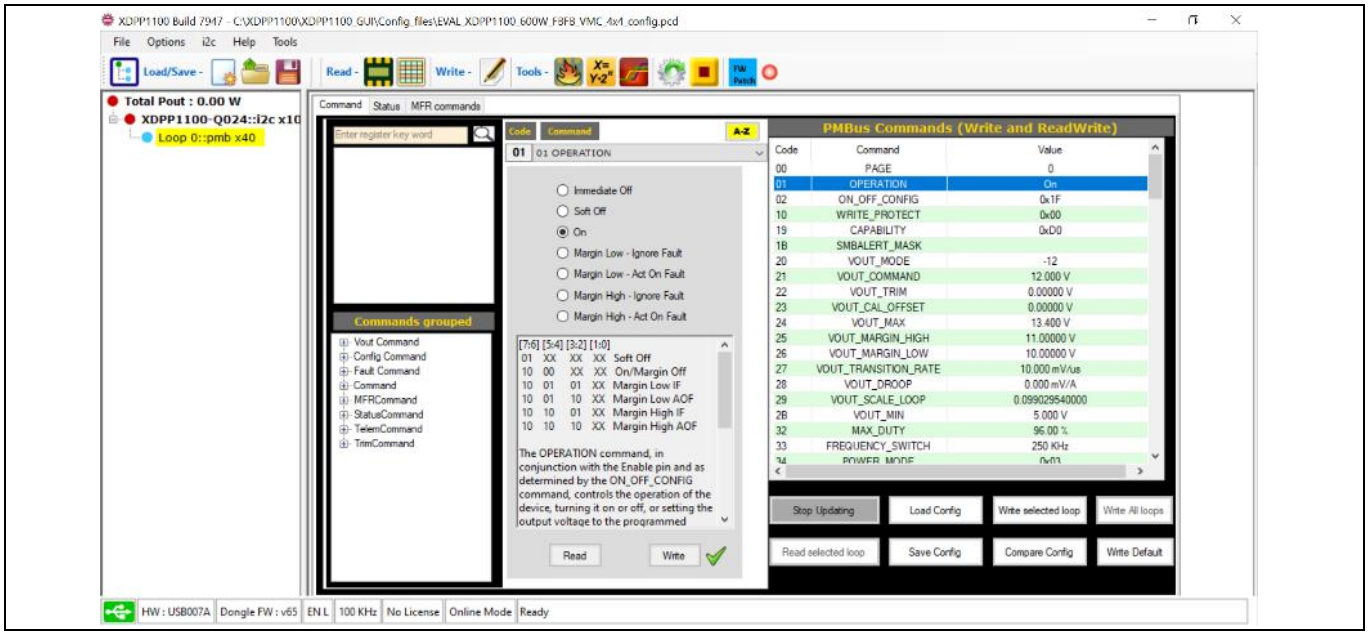


Figure 13 PMBus OPERATION command

At this point, the evaluation board should be on, and supplying the connected 5 A electronic load with 12 V DC output voltage.

The status of the power board is provided by the PWRGD (DS1) red LED on the daughterboard. This LED indicates that the output voltage of Loop0 is between the predefined thresholds. For the first 3.3 V power-up, this LED is on as it is pulled up to 3.3 V. Once the converter is enabled, the status of this LED will be determined by the output voltage level, and the polarity of the POWER_GOOD PMBus commands. While the default logic is active low, it can be modified to active high. To do so:

- Click the **Loop0::pmbus x40** below the device part number (**XDPP1100-Q024::i2c x10**) (highlighted in yellow in **Figure 12**). This opens the PMBus configuration page of Loop0.
- In the **PMBus Commands** window, select **FW_CONFIG_PMBUS** (Code C9).
- Set **GPIO polarity** to 2 and Click on **Write**.

Now, the current configuration file is programmed to active high.

If prefer to keep the POWER_GOOD signal low during the device initialization, one option is to remove the pull-up resistor at the PWRGD pin on the control board and set pwrgd_ppen =1. This enables the CMOS output of the PWRGD pin. It won't be pulled up by the external circuit and drive the logic by internal push-pull circuit.

In the **PMBus Commands** window, **Power_Good_ON** (Code 5E) and **Power_Good_OFF** (Code 5F) PMBus commands set the Power_Good thresholds. For example, with the current configuration;

- PWRGD (DS1) red LED is on if the output voltage is higher than **Power_Good_ON**.
- PWRGD (DS1) red LED is off if the output voltage is lower than **Power_Good_OFF**.

3.3.1 Measured efficiency

The power board efficiencies for V_{IN} = 36 V, 48 V, and 72 V in no-load and full-load operation conditions are shown in **Figure 14**. The efficiency results at V_{IN} = 36 V are taken with V_{OUT} set to 10 V as the power board cannot regulate due to the 3:1 turns ratio of the isolated transformer.

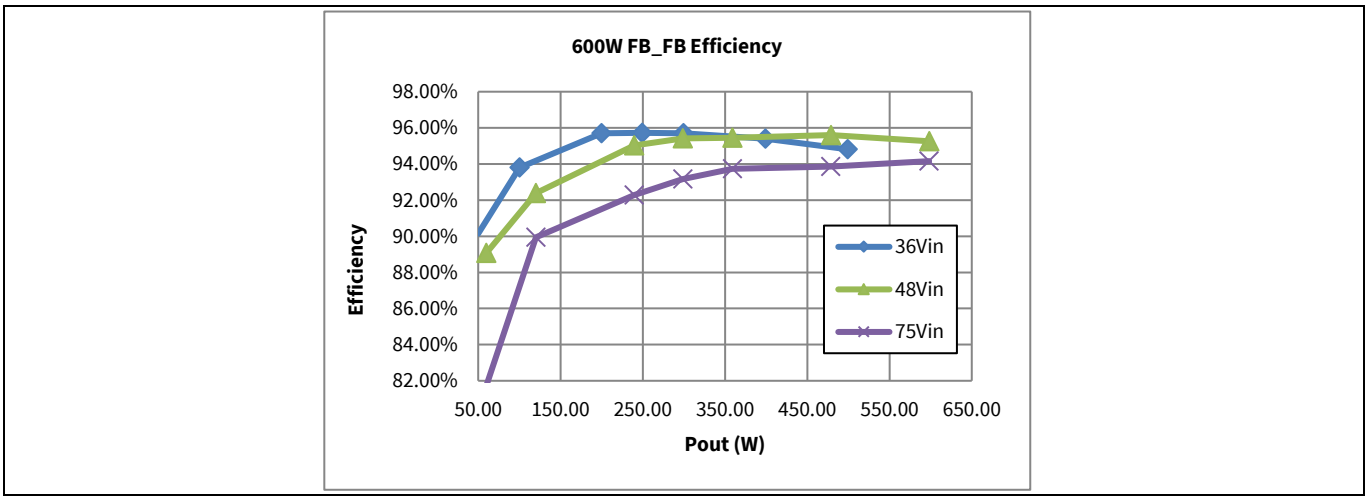


Figure 14 Efficiency results at 36 V DC, 48 V DC, and 75 V DC input

3.3.2 Output voltage ripple

Output voltage ripple waveforms of the power board with minimum V_{pk-pk} = 50 mV (at V_{IN} = 48 V, I_{OUT} = 0 A) and maximum V_{pk-pk} = 150 mV (at V_{IN} = 72 V, I_{OUT} = 50 A) are shown in **Figure 15**.

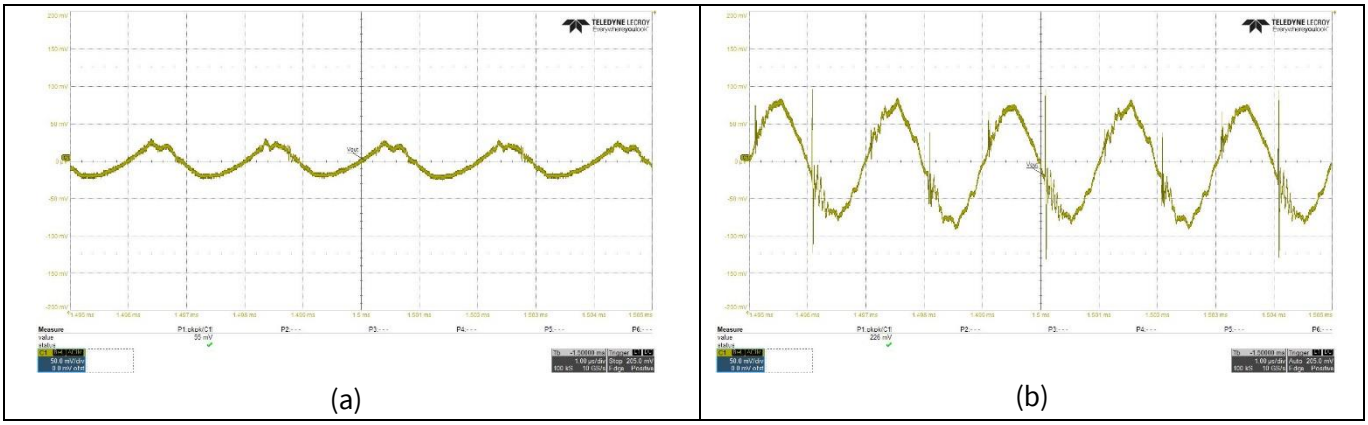


Figure 15 Output voltage ripple (AC coupled mode) - a) V_{IN} = 48 V, I_{OUT} = 0 A, b) V_{IN} = 72 V, I_{OUT} = 50 A

4 Design configuration and evaluate XDPP1100

This section presents different design tools integrated with the GUI to configure the XDPP1100 digital controller to meet system requirements. The following sections are a part of the **Design Tools** window of the XDPP1100_GUI (**Figure 16**). These sections are designed as an introduction to familiarize users with and guide them to evaluate extensive programming options and design tool features provided for the XDPP1100 family of digital controllers. More detailed and comprehensive guidelines are provided in the documents available in the **Help** dropdown menu of the GUI.

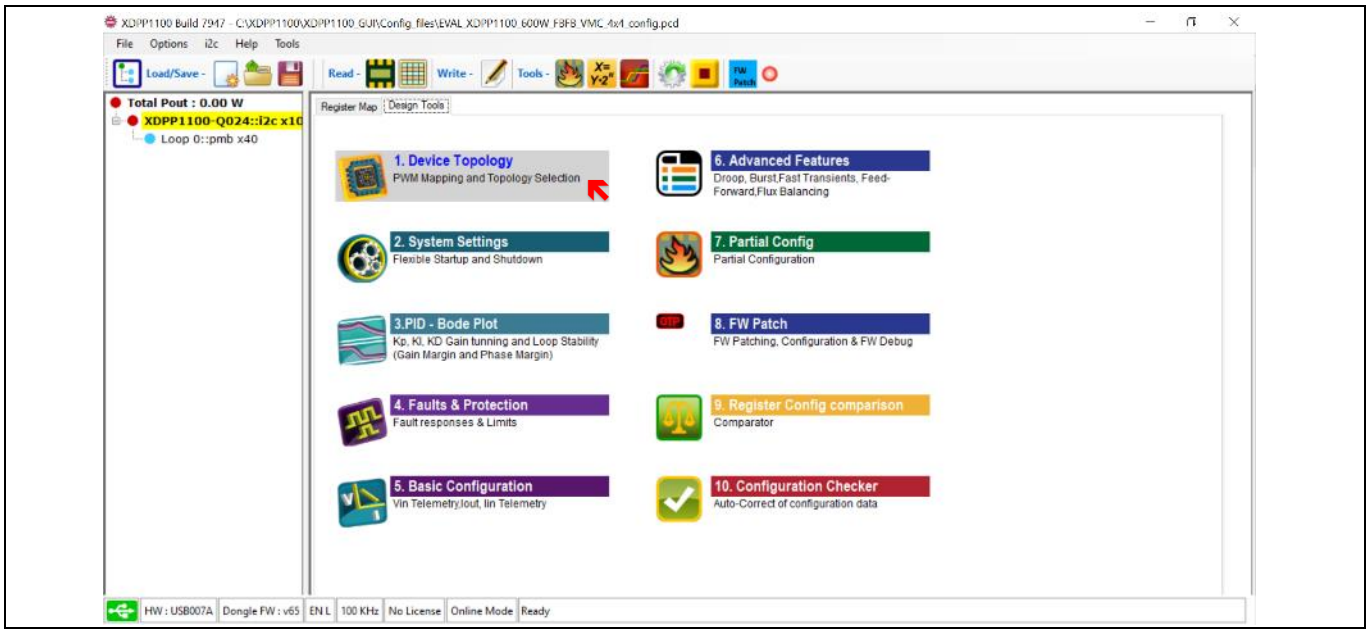


Figure 16 GUI Design Tools feature and Device Topology (PWM mapping and topology)

4.1 Device Topology (PWM mapping and topology selection)

Using the **Device Topology** tool, users can configure the XDPP1100 based on power board topology, targeted control strategy and PWM deadtimes settings. To access this tool:

- Click the **XDPP1100-Q024::i2c x10** (highlighted in yellow in **Figure 16**).
- Click the **Design Tools** and select **1. Device Topology**

The **XDPP1100 Topology** window will be opened with **Topology** and **DeadTime** tabs (**Figure 17**).

4.1.1 Topology tab

Users can select their power board topology and targeted control strategy and assign available PWMs to the switches (**Figure 17**). PWM mapping enhances the compatibility of the XDPP1100 to designed power boards and HW. They are mapped to each power switch using the drop-down list assigned for each PWM in the **Topology** tab.

The evaluation power board is a FB-FB topology. Four PWM signals from the digital controller are expanded for the diagonal switches with onboard HW. As shown in **Figure 17**, two primary switches Q2, Q3, and two secondary SR switches SR3, SR4 are left unmapped, while the other four switches are assigned to available PWM signals.

VMC is selected in this tab (**Figure 17**) as the control strategy for this evaluation kit.

4.1.2 DeadTime tab

DPWM dead time settings can be programmed in the **DeadTime** tab (**Figure 17**). In this tab, interactive PWM waveforms associated with each switch provide visual system verification for assigned deadtimes.

Three PWM techniques can be provided by the PWM module of the XDPP1100, which are trailing-edge, leading-edge, and dual-edge PWM modulation. Dual-edge PWM is the default configuration, which is shown in **Figure 17**. For more details of different modulation techniques, please refer to **Section 4.5.4**.

All settings in this tab will be applied just after clicking **Write**.

Note: Changes will be stored in RAM and stored into OTP once the program has been finalized.

(a) (b)

Figure 17 Device Topology (PWM mapping and topology selection) tool - a) Topology b) DeadTime

The deadtime unit in this module is ns. Changing dead time values will change switching waveforms accordingly and depict updated dead times. For example, the effect of increasing SR2 rising edge dead time (**DT11**) from 140 ns to 200 ns is shown in **Figure 18**.

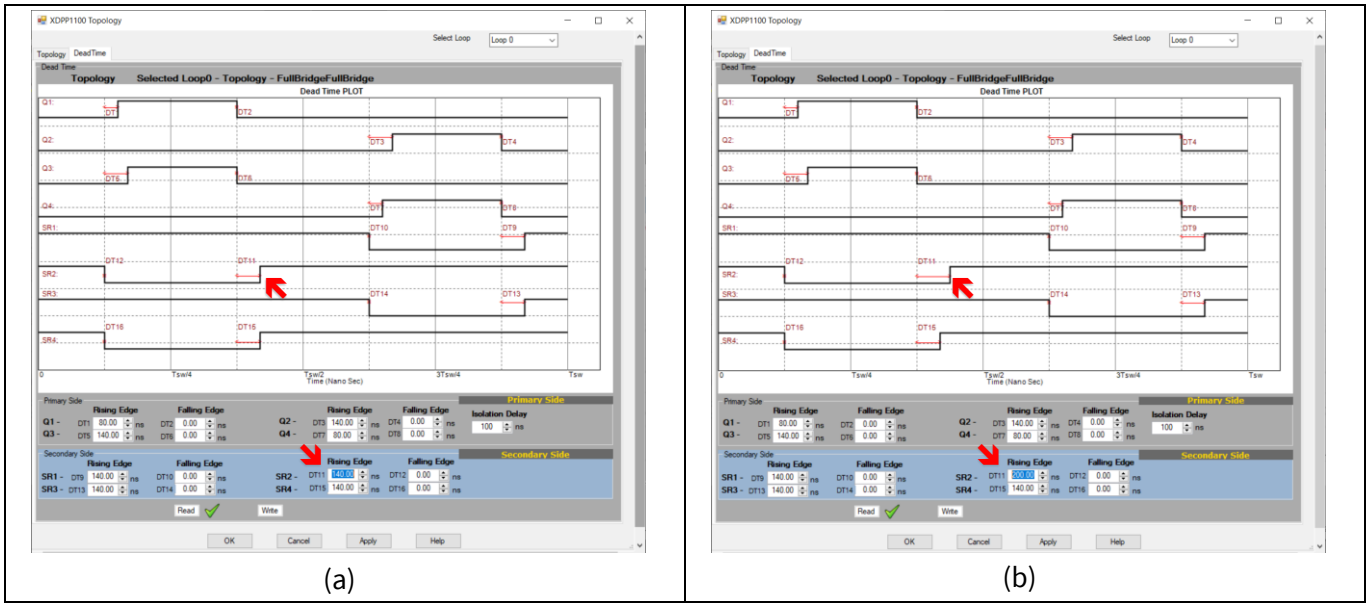


Figure 18 PWM dead time configuration - a) DT11 = 140 ns, b) DT11 = 200 ns

One of the critical factors for isolated bridge topologies is timing between the primary and the secondary opposite phases to avoid shoot-through. For this timing criteria, HW propagation delays should also be considered. As a safety measure, **Isolation Delay** reminds users to consider propagation delays between the XDPP1100 output and the gate of the primary-side switches during the configuration of the PWM rising edge of the SR switches (**Figure 19**). This is just a reminder to avoid the wrong PWM dead time configuration to avoid shoot-through, and does not have any impact on the actual PWM dead time timings. This setting only provides a warning message if dead time settings violate the **Isolation Delay** criteria. For example, if an **Isolation Delay** is considered 100 ns for the primary PWMs, GUI does not allow users to configure SR rising-edge delay less than 100 ns. GUI prompts a warning message if 100 ns criteria is violated, and does not allow the user to configure these settings (**Figure 19**).

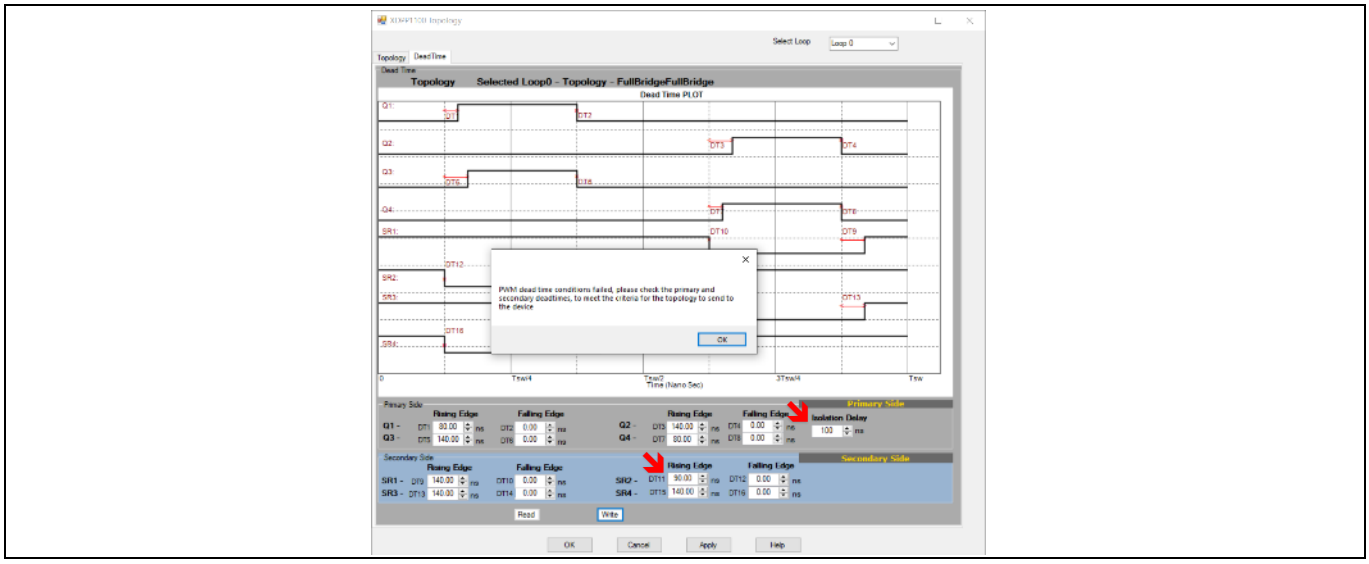


Figure 19 PWM isolation delay

For the evaluation kit programmed by the provided board design file, generated PWM signals by the daughterboard for the power board to supply 10 A load with 12 V DC output voltage are shown in (**Figure 20**).

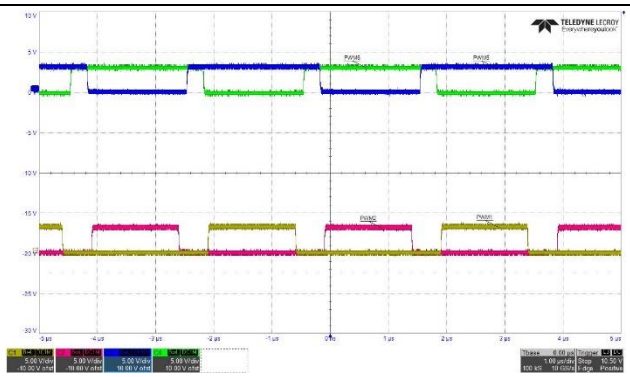


Figure 20 Evaluation kit PWM waveforms for 12 V DC output voltage and 10 A load current

4.2 System settings (flexible startup and shutdown)

Users can configure the startup, shutdown, and regulation settings of XDPP1100 using the **System Settings** tool. To access this tool,

- Click the **XDPP1100-Q024::i2c x10** (highlighted in yellow in **Figure 21**).
- Click the **Design Tools** and select **2. System Settings**

The **XDPP1100 System Settings** window will be opened with **Startup and Shutdown** and **Flexible Startup** tabs (**Figure 22**).

All settings in these tabs will be applied just after clicking on **Write**.

Note: Changes will be stored in RAM and must be stored into OTP once the program has been finalized.

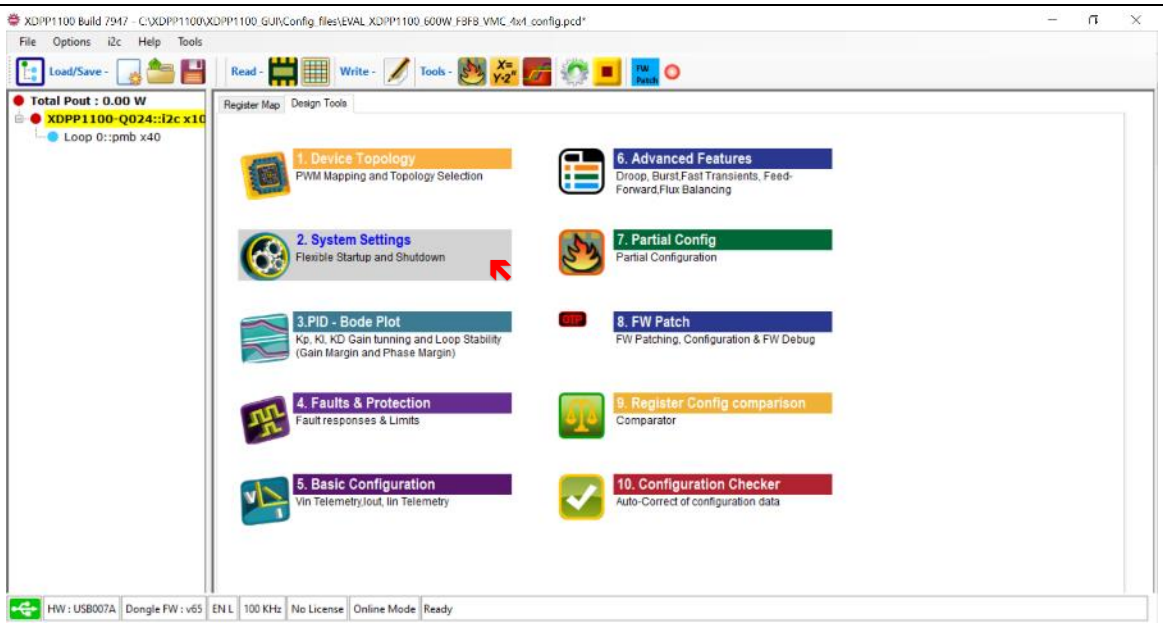


Figure 21 System settings (flexible startup and shutdown)

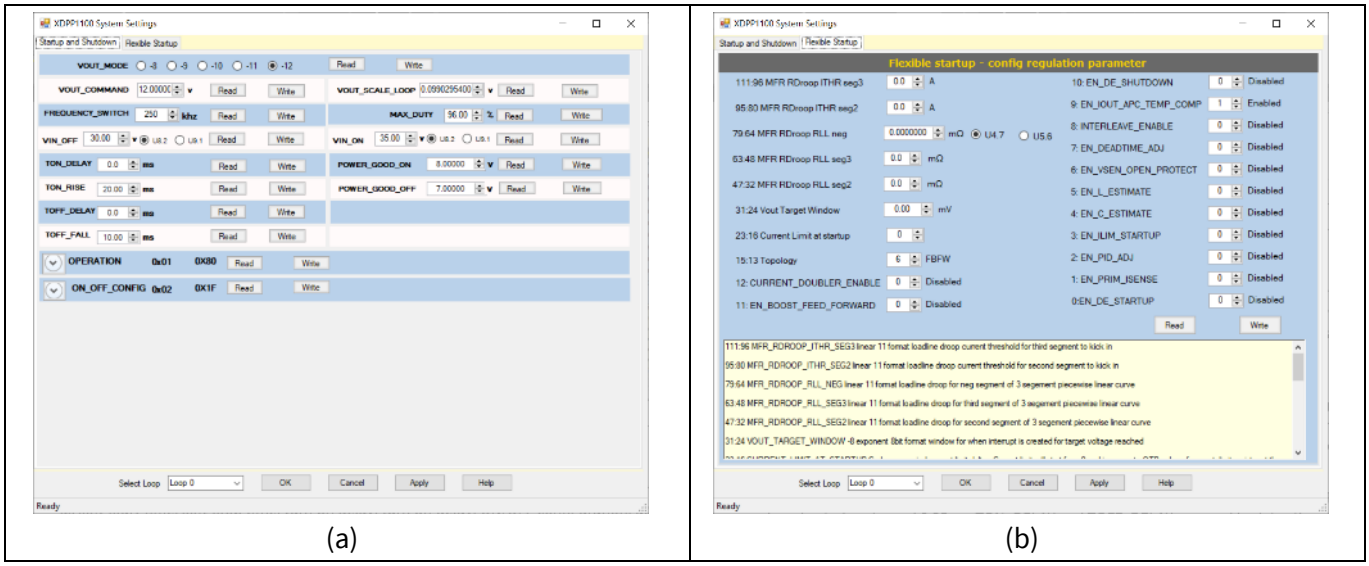


Figure 22 XDPP1100 System settings - a) startup and shutdown, b) flexible startup

4.2.1 Startup and shutdown tab

Various startup and shutdown features of the XDPP1100 such as soft-start time, soft-stop time, turn-on delay, turn-off delay, on/off configuration, and response to enable command can be configured in this tab (**Figure 22**). The PMBus commands in this tab are the standard PMBus commands, and their description can be found in PMBus specification documents.

The description of some PMBus commands in this tab are as follows:

- **TON_RISE** command sets the time, in ms, from when the output starts to rise until the voltage has entered the regulation band.
- **TOFF_FALL** sets the time, in ms, from the end of the turn-off delay time until the voltage is commanded to zero (**Figure 23**).

For shutting down the converter over the course of **TOFF_DELAY**, **Write** the **Soft Off** command in the **OPERATION** PMBus command (**Figure 23**).

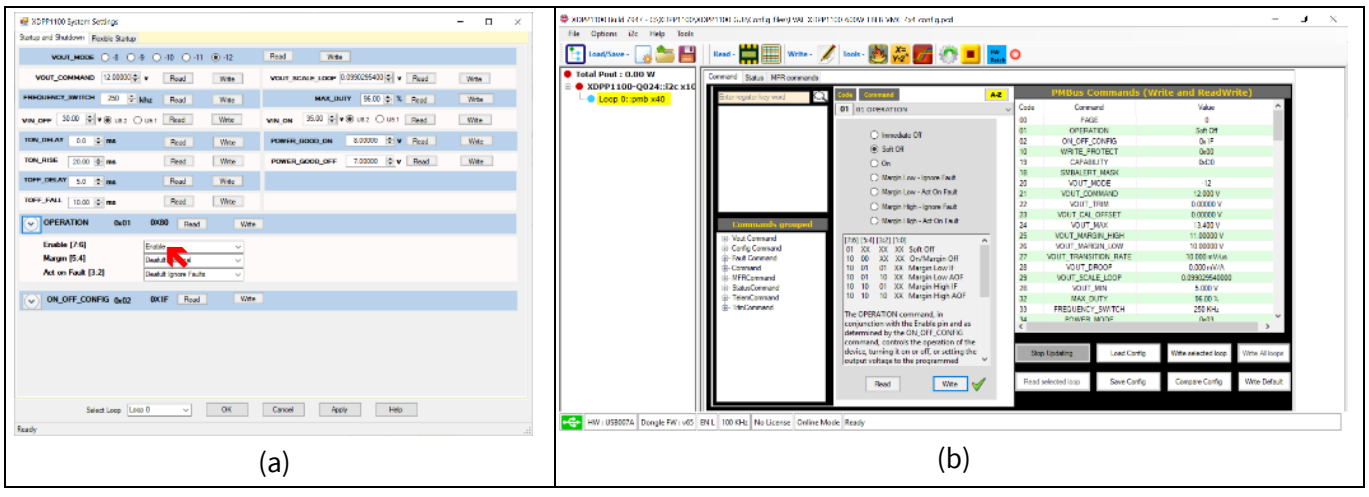


Figure 23 Soft stop feature

The evaluation kit turn-on response for TON_RISE = 20 ms and turn-off response for TOFF_FALL = 10 ms are shown in **Figure 24a** and **Figure 24b**, respectively. The load current is set to 20 A in these experiments.

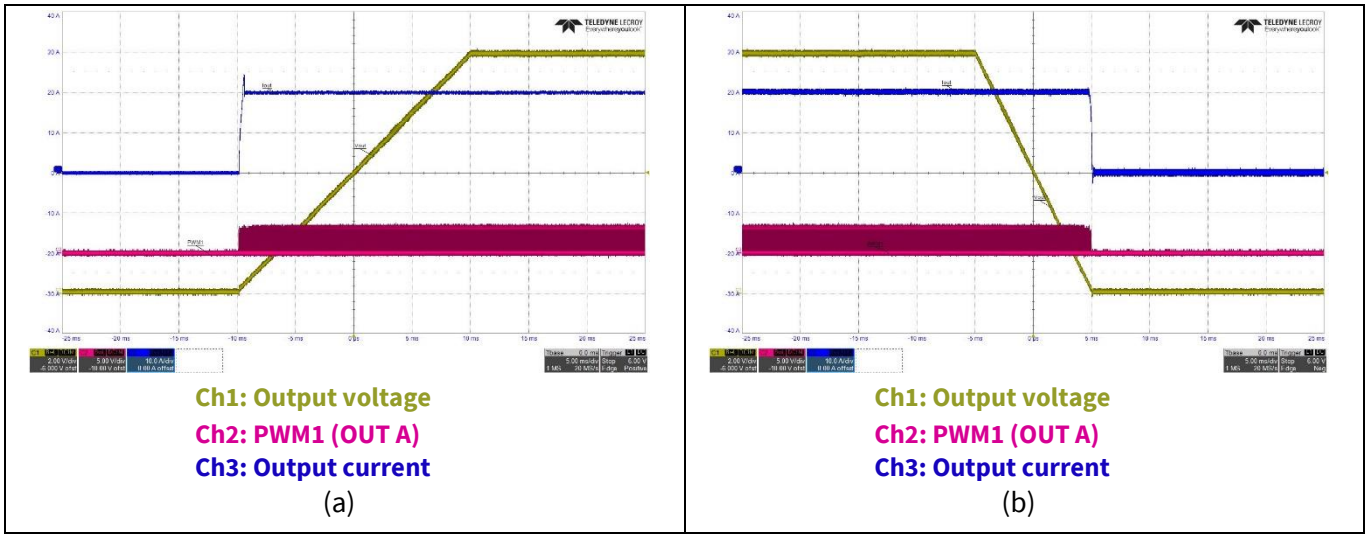


Figure 24 Evaluation kit soft start and soft stop waveforms at 20 A load - a) TON_RISE = 20 ms, b) TOFF_FALL = 10 ms

- **TON_DELAY** command sets the time, in ms, from when a start condition is received (as programmed by the ON_OFF_CONFIG command) until the output voltage starts to rise.
- **TOFF_DELAY** command sets the time, in ms, from when a stop condition is received (as programmed by the ON_OFF_CONFIG command) until the unit stops transferring energy to the output (**Figure 25**). **Write** the **Soft Stop** option for the **Stop mode** in the **ON_OFF_CONFIG PMBus** (Code 02) command to take advantage of **TOFF_DELAY** for soft shutting down (**Figure 25**).

The evaluation kit turn-on response for TON_DELAY = 5 ms, and turn-off response for TOFF_DELAY = 5 ms are shown in **Figure 26a** and **Figure 26b**, respectively. The load current is set to 20 A in these experiments.

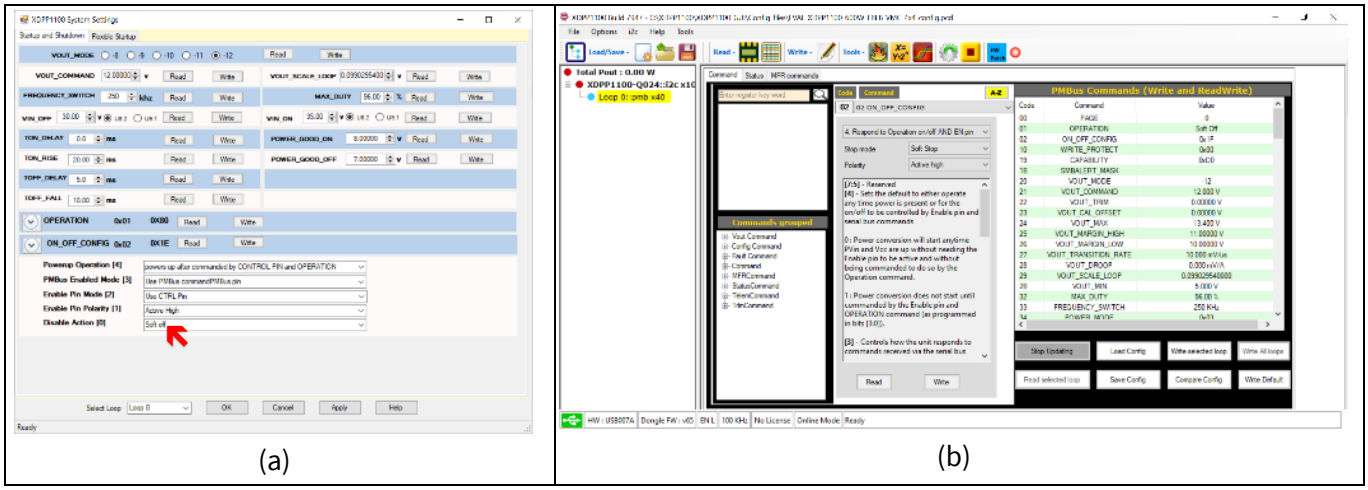


Figure 25 TOFF_DELAY feature

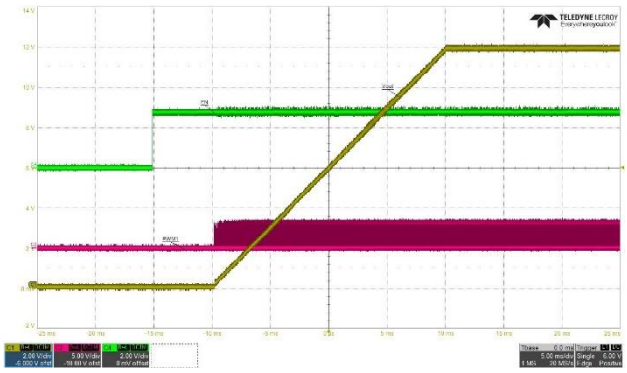


Figure 26 Evaluation kit turn-on and -off delays waveforms at 20 A load - a) TON_DELAY = 5 ms, b) TOFF_DELAY = 5 ms

4.2.2 Flexible startup

Advance startup features of the XDPP1100, such as multi-segment droop, and some FW features such as current sense (CS) temperature compensation and diode emulation startup can be configured in this tab (**Figure 22**). The PMBus commands in this tab are the Infineon-specified PMBus commands, and their description can be found in the XDPP1100 application note (**link to download**)

This evaluation board uses PCB trace as a shunt resistor to measure the output current. To achieve better current measurement accuracy over the wide temperature range, temperature compensation of the output current is enabled. To do so, **EN_IOUT_APC_TEMP_COMP** is set to 1 in **Flexible Startup** window (**Figure 22**). Temperature coefficient is set to 0.0039 internally for the copper.

4.3 PID – bode plot (K_p, K_i, K_d gain tuning and loop stability (gain margin and phase margin))

The XDPP1100 is equipped with a Type-III compensator for closed-loop control of power converters. Users can design and configure the PID compensator settings of the control loop(s) of XDPP1100 using this tool. It is also equipped with a simulation tool to predict the bode plot of the system based on power converter topology, load model, and PID parameters. To access this tool:

- Click the **XDPP1100-Q024::i2c x10** (highlighted in yellow in **Figure 27**).
- Click **Design Tools** and select **3. PID – Bode Plot.**

The **XDPP1100 PID** window will be opened with **Bode Plot** and **Load Model** tabs (**Figure 28**).

4.3.1 Bode plot tab

This tab provides an interactive closed-loop bode plot considering detailed parameters of the converter and load, parasitic, and compensator values. Users can easily and precisely tune the controller based on desired poles and zeroes locations, phase/gain margins, or PID cut-off frequencies.

4.3.2 Load model tab

In this tab, users can enter a detailed model of the converter and load, including parasitic, transformer leakages, switching deadtimes, etc. These values will be used in the **Bode Plot** tab to design and set up desired closed-loop system.

A detailed explanation of this tool and PID compensator is provided in the **XDPP1100 application note** (**link to download**).

Figure 27 PID – bode plot (K_p, K_i, K_d Gain tuning and loop stability (gain margin and phase margin))

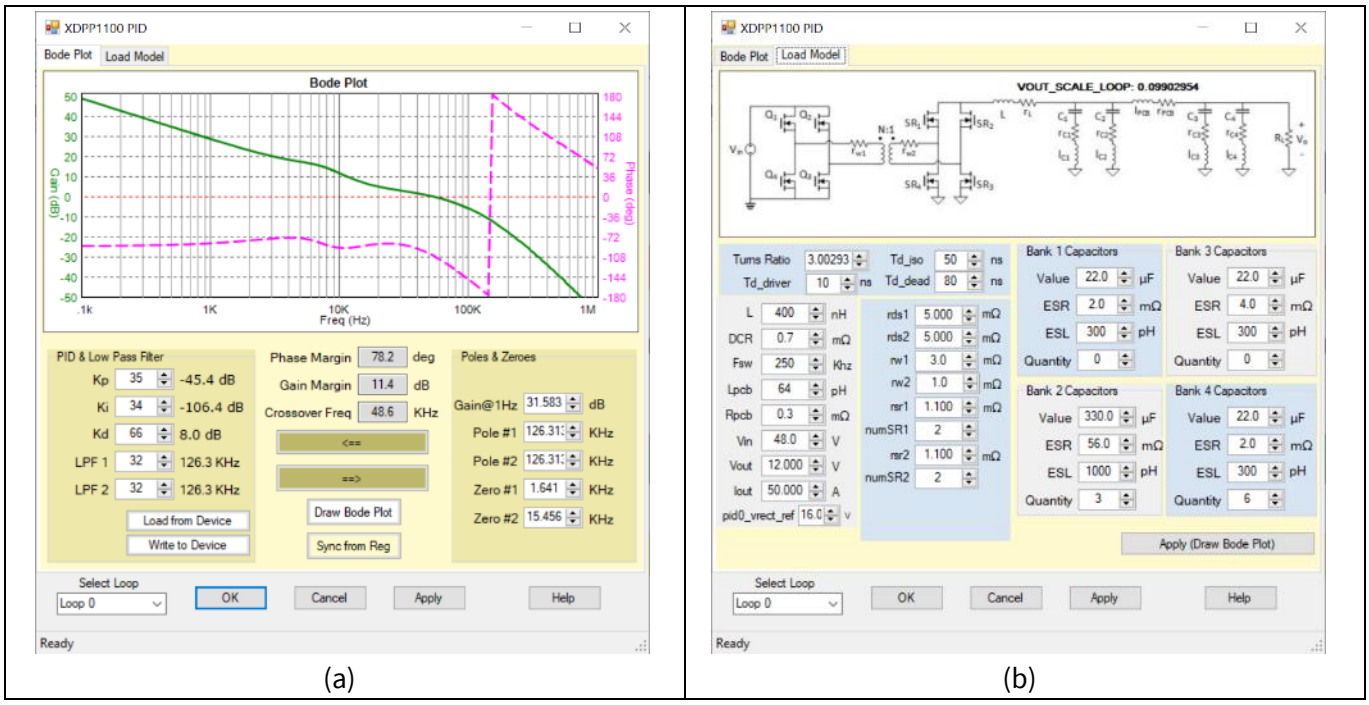


Figure 28 PID – bode plot - a) bode plot, b) load model

Some key parameters of the system listed in the load model tab are explained in **Table 3**.

Table 3 Load model parameters

Parameter	Meaning	Parameter	Meaning
Turns ratio	Transformer turns ratio Np:Ns (automatically computed by GUI based on PMBus command 0xCE)	Rds1	R_{DSON} of primary switch 1
Td_iso	Propagation delay of isolator	Rds2	R_{DSON} of primary switch 2
Td_driver	Propagation delay of primary gate driver	rw1	Transformer primary winding DCR
Td_dead	Primary PWM dead-time Td_rise	rw2	Transformer secondary winding DCR
L	Output inductor	rsr1	R_{DSON} of secondary SR1 switch
DCR	Output inductor DCR	numSR1	Number of SR1 switch in parallel
Fsw	Switching frequency	rsr2	R_{DSON} of secondary SR2 switch
Lpcb	PCB parasitic inductance	numSR2	Number of SR2 switch in parallel
Rpcb	PCB parasitic resistance	ESR	Output capacitor ESR
		ESL	Output capacitor ESL
pid_vrect_ref	Nominal V_{IN} divided by turns ratio	Quantity	Output capacitor quantity (number in parallel)

System parameters of the evaluation kit are set in its Config file as **Figure 28b**. In this case, the nominal input voltage is V_{IN} = 48 V, and turns ratio is 3. Hence, **pid0_vrect_ref** = 48 V / 3 = 16 V.

In the **Bode Plot** tab (**Figure 28a**), Kp, Ki, and Kd can be tuned to achieve desired gain and phase margin. This tab provides an automatic tool to drive PID gains by first locating poles and zeroes at desired frequencies and then clicking ==>. Also, after adjusting PID parameters, clicking on <== will show the location of poles and zeroes accordingly. In general, two zeroes (Zero #1 and Zero #2) can be placed at the double-pole of the output LC filter, and Pole #1 can be placed at half of the switching frequency.

The predicted bode plot and stability of the closed-loop system can be validated experimentally by using a loop analyzer. To connect a loop analyzer to the evaluation kit: 1) replace R96 from 0 Ω to 30 Ω on the power board, 2) inject the noise on TP 27 (bode) with respect to TP 15 (V_{OUT}) (refer to schematic **Figure 63**), 3) connect the output channel and input channel of the loop analyzer to TP 15 (V_{OUT}) and TP 27 (bode), respectively. An example of an experimental bode plot measured using an AP200 loop analyzer is shown in **Figure 29**.

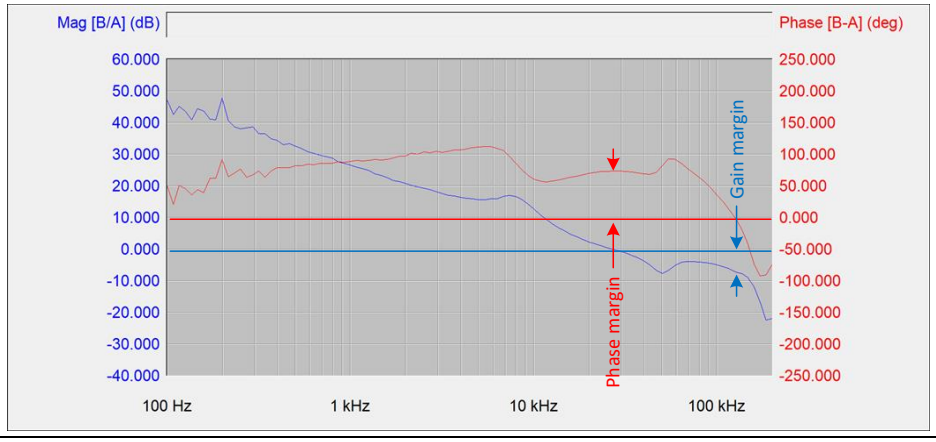


Figure 29 Experimental bode plot (phase margin = 75°, gain margin = 9 dB, crossover frequency = 28 kHz)

For the evaluation kit, load-transient responses of the closed-loop system equipped with the tuned compensator are shown in **Figure 30**.

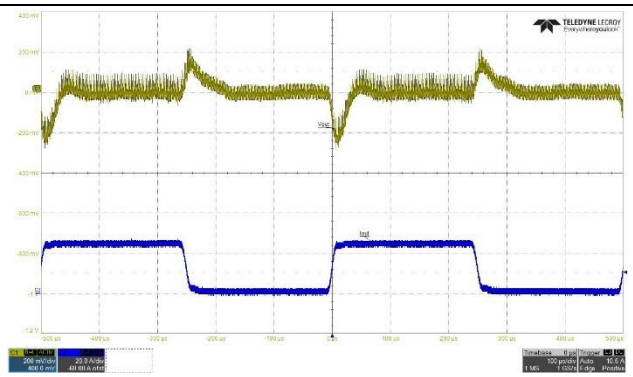


Figure 30 Load-transient response at V_{IN} = 48 V - a) load step: 5 percent ↔ 50 percent, b) load step: 50 percent ↔ 100 percent

4.4 Faults and protection (fault responses and limits)

Users can configure fault thresholds and set up protection responses of XDPP1100 to various faults (voltage, current, temperature, etc.) in the system using this tool. To access this tool:

- Click on **XDPP1100-Q024::i2c x10** (highlighted in yellow in **Figure 31**).
- Click on **Design Tools** and select **4. Faults and Protection**

The **XDPP1100 Fault Protections** window will be opened with **Protections**, **Fault Configuration**, **Common Faults**, and **Pmbus Command protections** tabs (**Figure 32**).

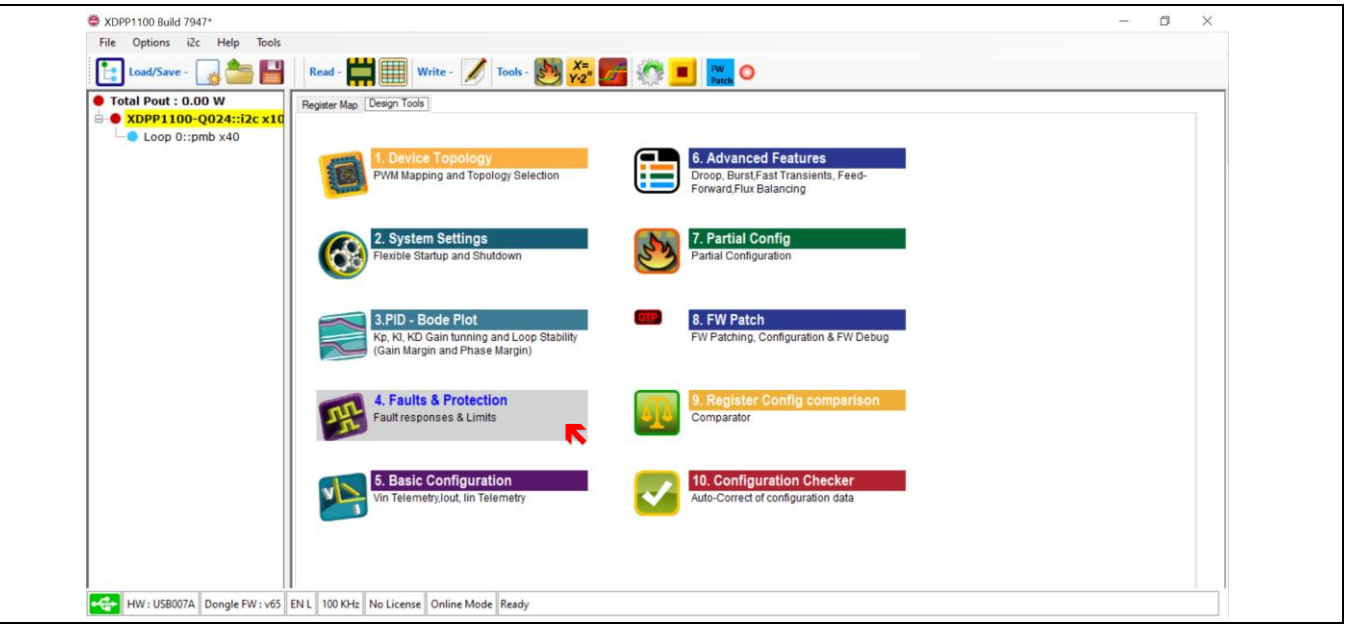


Figure 31 Faults and protection (fault responses and limits)

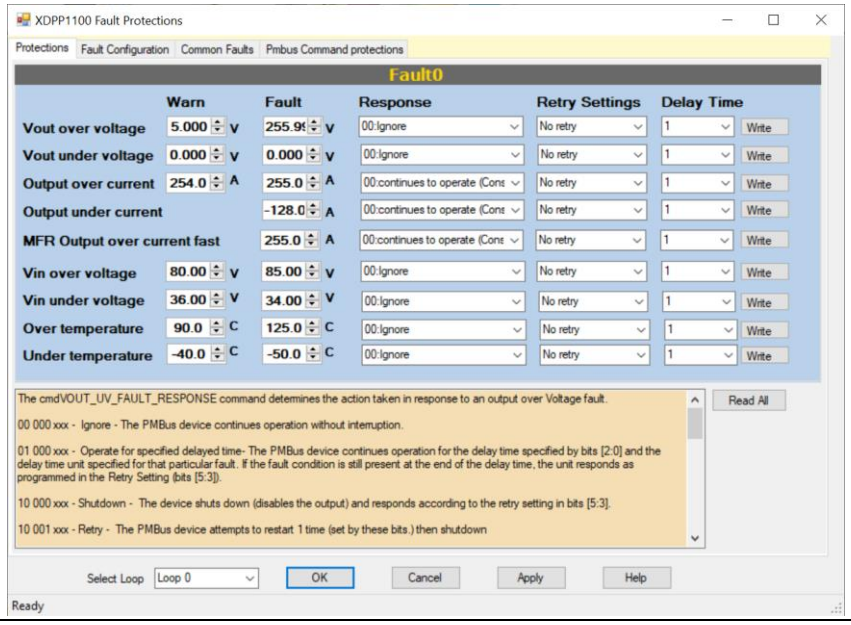


Figure 32 XDPP1100 fault protections window with Protections, Fault Configuration, Common Faults, and Pmbus Command protections tabs

4.4.1 Protections tab

This tab configures the warning threshold, fault threshold, fault response behavior, retry settings, and delay time of the fault. All settings in these tabs will be applied just after clicking on **Write**.

Note: Changes will be stored in RAM and stored into OTP once the program has been finalized.

The XDPP1100 uses a warning threshold as a hysteresis mechanism for proper response to system faults. Setting fault and warning threshold to unequal values with correct direction is necessary for proper responses to the faults. For example, V_{OUT} overvoltage fault threshold must be higher than the overvoltage warning threshold. On the other hand, the undervoltage fault threshold must be lower than undervoltage warning threshold.

For each of the faults, desired response (**Figure 33a**), the number of the retry after fault response (**Figure 33b**), and the delay time to retry after fault detection (**Figure 33c**) can be set from their dropdown menu.

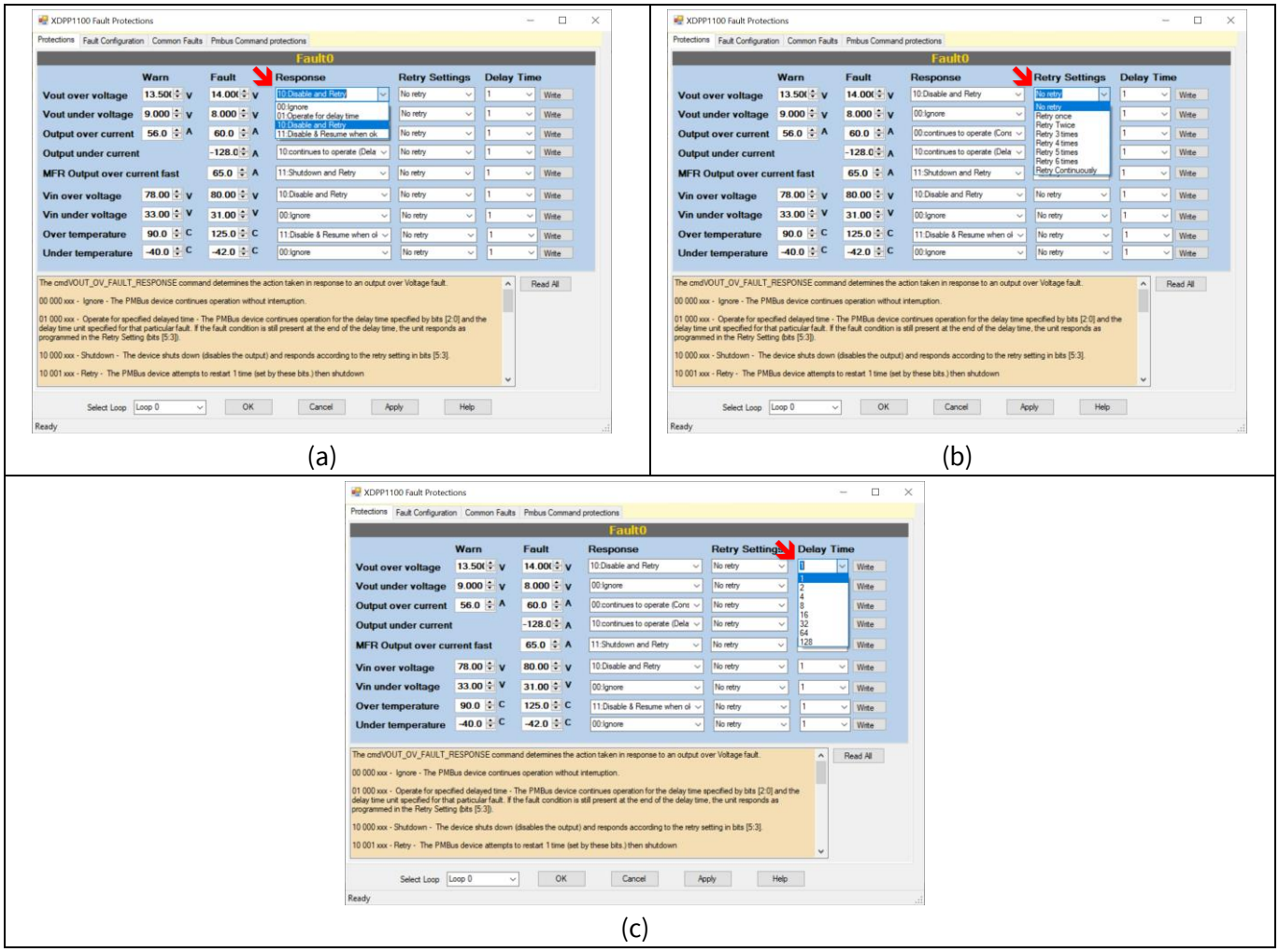


Figure 33 Protections tab; a) select response behavior to faults, b) select number of retry after a fault, c) select delay time for retry after response to a fault

Fault **Delay Time** works together with **Fault_Delay_Unit** configurable by **FW_CONFIG_FAULTS** (Code C8) PMBus command at the PMBus page shown in **Figure 34** (not in this tool). The result defines the fault operation's delay and retries delay between consecutive retries. This delay equals to (**Fault_Delay_Time** × **Fault_Delay_Unit**). For example, if the **Response** for **Over temperature** is programmed to **01: Operate for delay time**, **Delay Time** is set to **64**, and **Temperature_Delay_Unit** is set to **4ms**, the actual delay time is 64 × 4 ms = 256 ms after detecting overtemperature fault. With this setting, XDPP1100 will let the converter operate for 256 ms before shutting it down. The maximum delay time supported by XDPP1100 is 128 × 256 ms = 32.768 sec.

Note: The Delay_Unit for the input current fault is the same as the Vin_Delay_Unit.

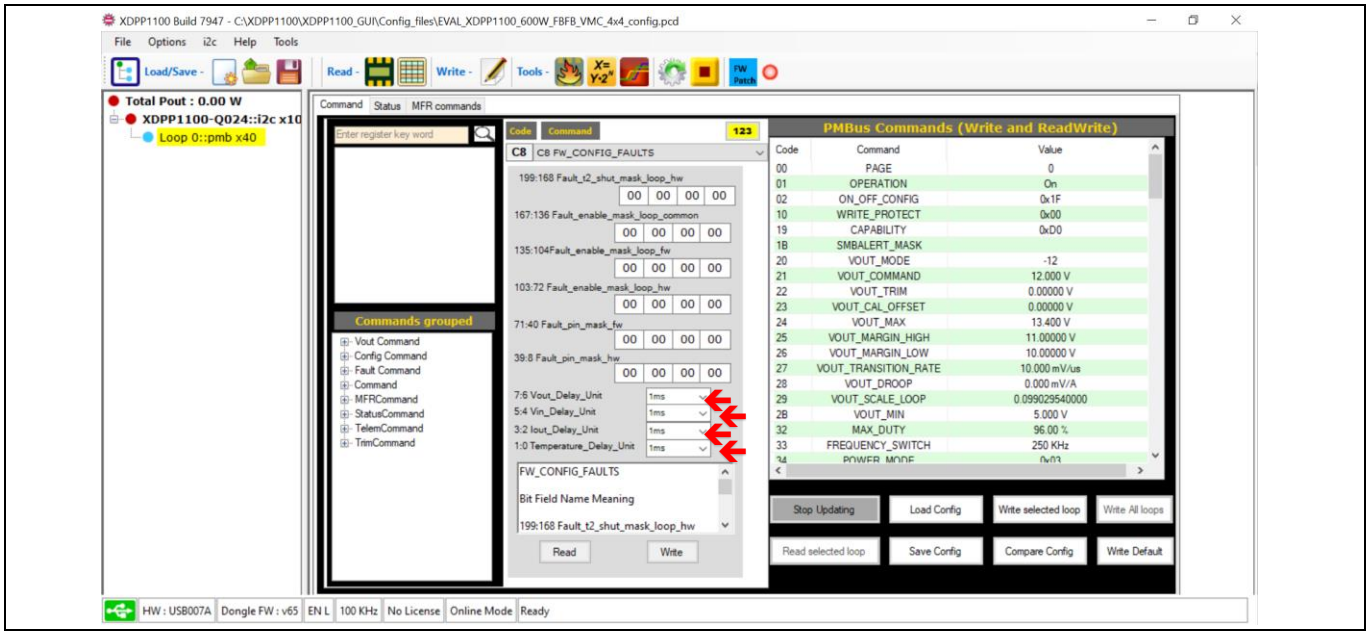


Figure 34 Setting Fault_Delay_Unit(s) in FW_CONFIG_FAULTS (Code C8) PMBus command

4.4.2 Fault Configuration tab

To avoid false fault triggering, XDPP1100 can be programmed to assert a fault/warning after the occurrence of a certain number of consecutive faults (fault count). This feature can be configured in the **Fault Configuration** tab (**Figure 35**).

Note: Setting a higher fault count reduces sensitivity to a fault and delays proper response. Configuring the correct number is essential to avoid false fault triggering while maintaining an acceptable level of sensitivity to avoid damage to the system.

In this tab, fault hysteresis registers (**fault_hyst**) set the HW hysteresis for the inputs to the fault comparators, which provides clean data for processing in the FW. It is worth mentioning that this setting is different from the FW hysteresis explained in **Section 4.4.1**. The HW hysteresis should be set higher than ripples of signals to avoid overflowing the processor due to oscillation of the output of the fault comparator.

Note: Changes in this tab are immediately applied upon making the drop-down selection. Changes will be stored in RAM and stored into OTP once the program has been finalized.

Hovering the cursor over each register name will give a more detailed its description.

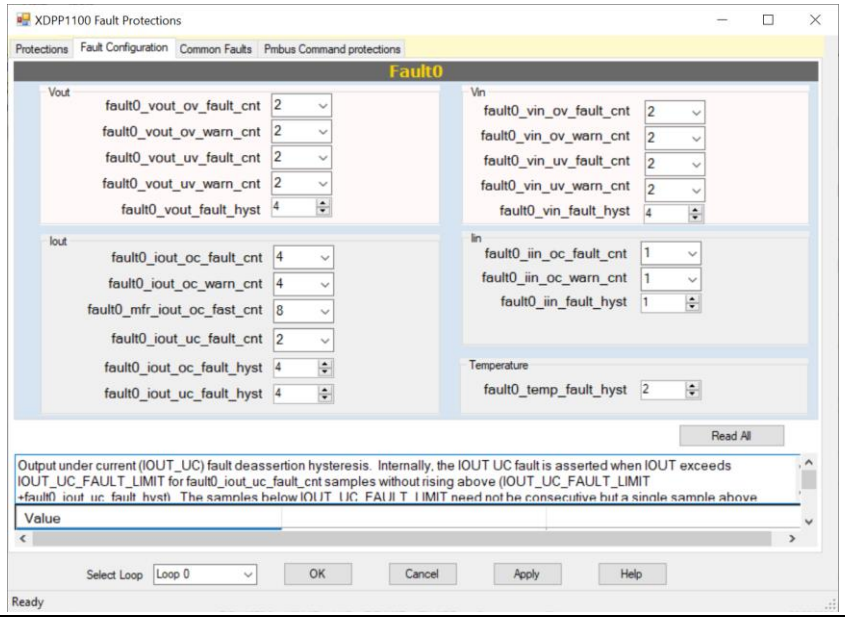


Figure 35 Fault Configuration tab

4.4.3 Common Faults tab

The XDPP1100 features a number of unique fault protections such as loop open sense fault, short-circuit protection, positive and negative cycle-by-cycle current limit, and flux balancing fault. These fault protections are grouped as a common faults in the **Common Faults** tab (**Figure 36**). The response to a common fault can be set to either ignore or shutdown. To set the shutdown response of a common fault, check the box of the associated fault in the **Common fault shutdown Configuration** section (**Figure 36**).

Note: Changes in this tab are immediately applied upon making the drop-down selection. Changes will be stored in RAM and must be stored into OTP once the program has been finalized.

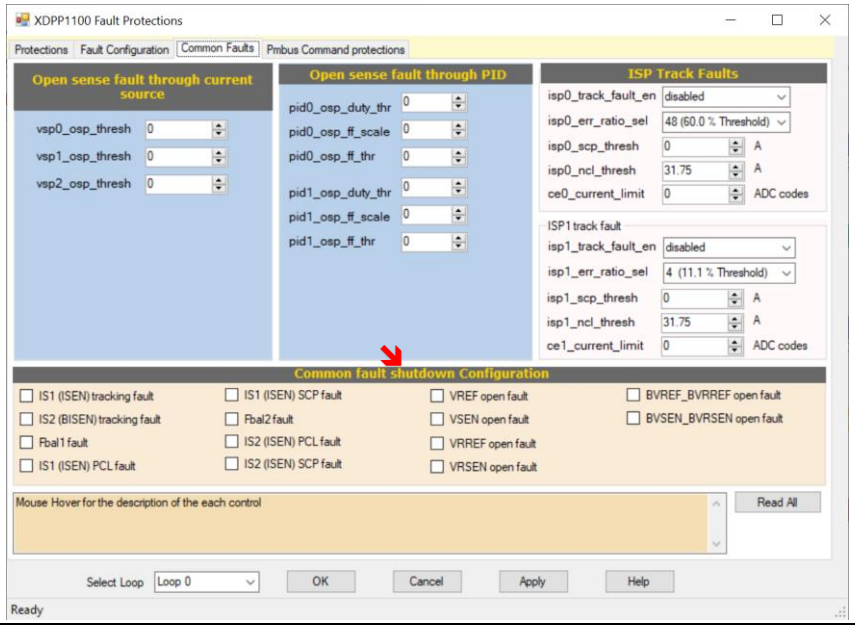


Figure 36 Common Faults tab

The **ispX_scp_thresh** defines the short circuit protection (SCP) threshold. It should be set to the highest among all over-current protection (OCP) thresholds because it requires only a single sample (at the 25 MHz ADC sample rate) above the threshold to respond and shut down the system. Setting this threshold to 0 disables the SCP fault detection. To enable SCP shutdown, check the "**IS1 (ISEN) SCP fault**" box in the **Common fault shutdown Configuration** section (**Figure 36**).

Figure 37 demonstrates differences between responses to SCP and OC using the evaluation kit. The SCP fault threshold (**ispX_scp_thresh**) is set to 22 A. For the OCP settings, the **MFR_IOUT_OC_FAST_FAULT_LIMIT** (Code D1) PMBus command is set to 20 A, and the **fault0_mfr_iout_oc_fast_cnt** in the **Fault Configuration** (**Figure 35**) tab is set to 8 to have nine counts. The OC_FAST fault count block has one switching cycle latency; thus, the shutdown happens after 10 switching cycles. Both SCP and OCP fault responses are set to shut down.

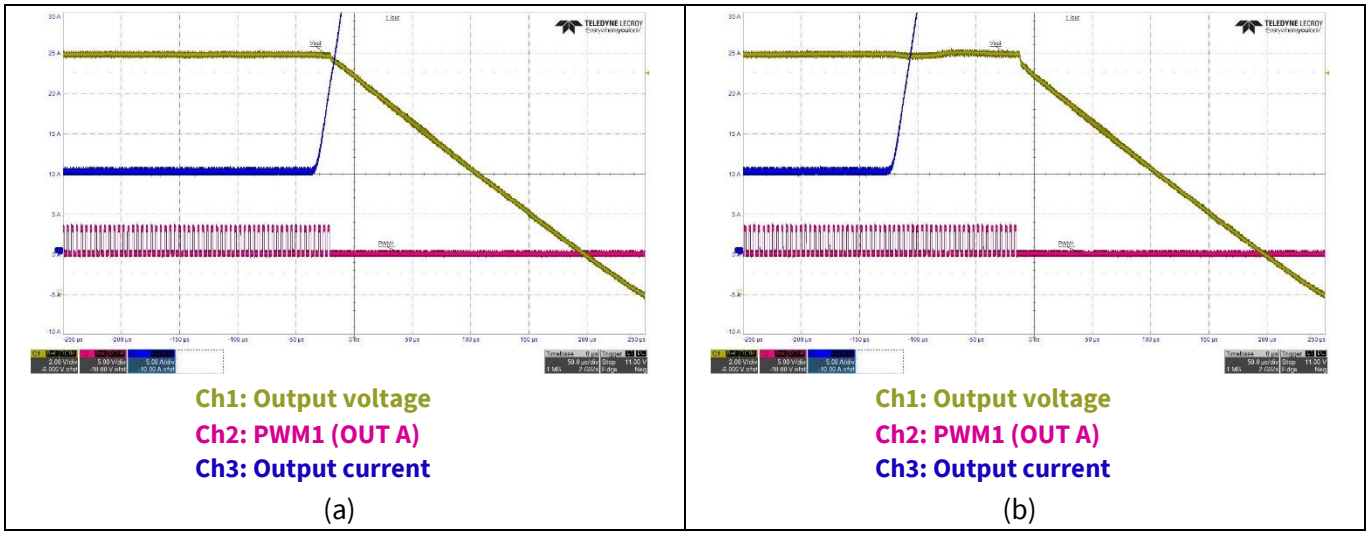


Figure 37 Responses to SCP and OCP (at 48 V input, 12 V output)- a) shutdown by SCP, which responded in one switching cycle, b) shutdown by MFR_IOUT_OC_FAST, which responded after 10 switching cycles

4.4.4 Pmbus Command protections tab

In this tab, password protection can be activated and set for the intended PMBus command to protect and prevent unauthorized modification of a selected PMBus command.

The **Pmbus Command protections** tab allows users to:

- Check if the password is set by reading **MFR_DISABLE_SECURITY_ONCE.**
- Write a new password by writing into **Mfr. SETUP password** if the **MFR_DISABLE_SECURITY_ONCE** read 00 00 00 00 00 00
- Turn off the security by writing the password to **MFR_DISABLE_SECURITY_ONCE** if the **MFR_DISABLE_SECURITY_ONCE** read 00 00 00 00 00 01.
- Select the PMBus that need to be protected.
- Set **MFR_SECURITY_BIT_MASK** by clicking **Write Protect (selected commands)** button.

If one command is selected for **Write Protect (selected commands)** and the security is activated, rewriting of this command will be prohibited, and **STATUS_CML** command reports Invalid/Unsupported data.

Please refer to the **Faults Protection** section of the XDPP1100 application note (**link to download**) for a detailed explanation.

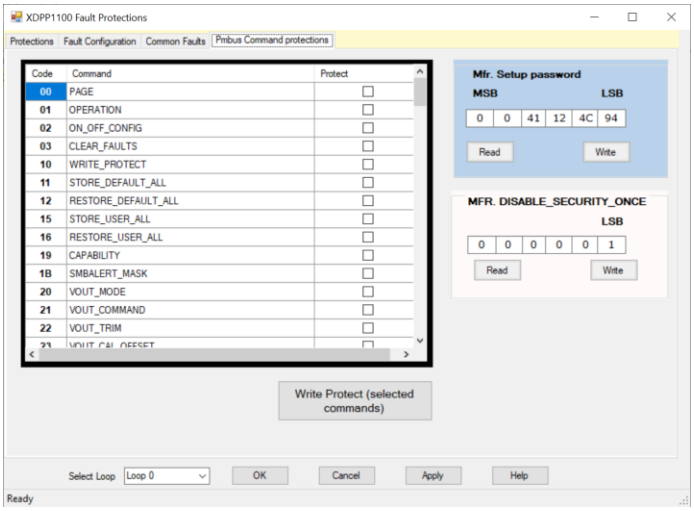
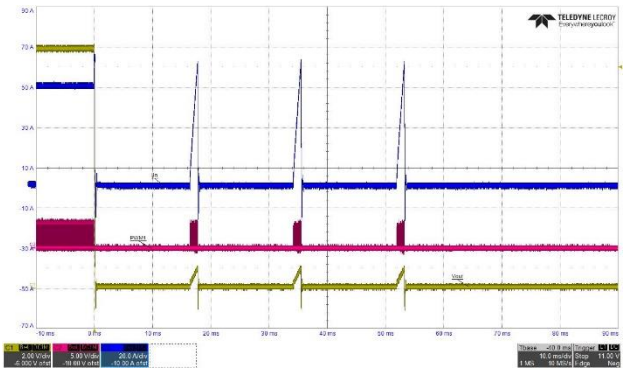


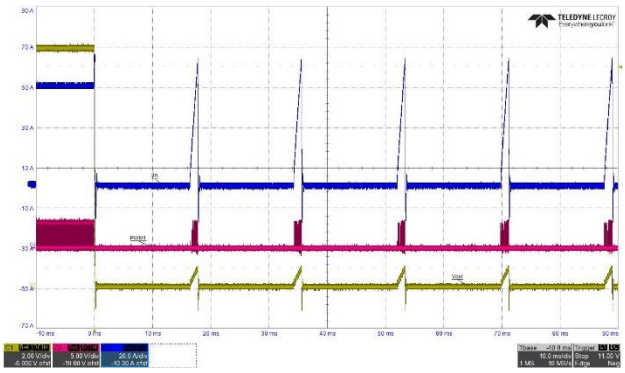
Figure 38 Pmbus Command protections tab

4.4.5 Overcurrent and short-circuit protection experimental results

Experimental results of the evaluation kit for the overload protection with different retry settings and the SCP waveforms are presented in **Figure 39** and **Figure 40**, respectively. The parameters used in this test are **IOUT_OC_FAULT_LIMIT** = 60 A, **MFR_IOUT_OC_FAST_FAULT_LIMIT** = 65 A, **fault0_iout_oc_fault_cnt** = 4, **fault0_mfr_iout_oc_fast_cnt** = 8, and **tlm0_kfp_iout** = 24. In all cases, the converter operates during normal operation condition with V_{IN} = 48 V, Vout = 12 V, and I_{OUT} = 50 A.

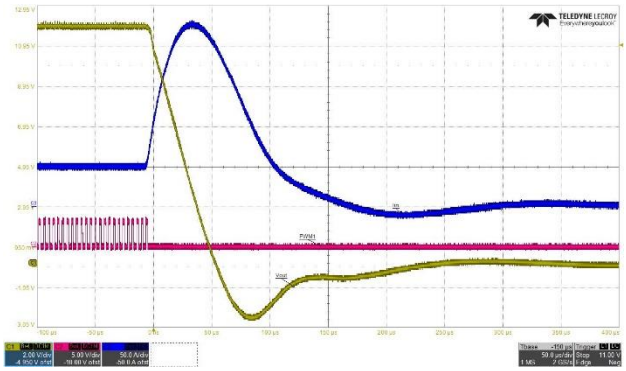


(a)



(b)

Figure 39 Overload protection - a) retry 3 times, b) retry continuously



Ch 1: Output voltage
Ch 2: PWM1 (OUT A)
Ch 3: Primary current

Figure 40 Short-circuit protection

4.5 Basic configuration (V_{IN} telemetry, I_{OUT}, I_{IN} telemetry)

Using this tool, users can program the basic configurations of the PWM ramp and telemetry-related registers of XDPP1100. To access this tool:

- Click on **XDPP1100-Q024::i2c x10** (highlighted in yellow in **Figure 41**).
- Click on **Design Tools** and select **5. Basic Configuration.**

The **Basic Configuration** window will be opened with **Output current sense**, **Input current sense**, **Vin Telemetry**, **PWM/ramp**, and **Telemetry** tabs (**Figure 42**).

Note: Changes in this tab are immediately applied on making the down selection. All changes are stored into RAM of the IC and must be stored to OTP once the changes are finalized.

Please refer to the **Input voltage sensing and feed-forward** and **Current Sense** sections of the XDPP1100 application note (**link to download**) for a detailed explanation.

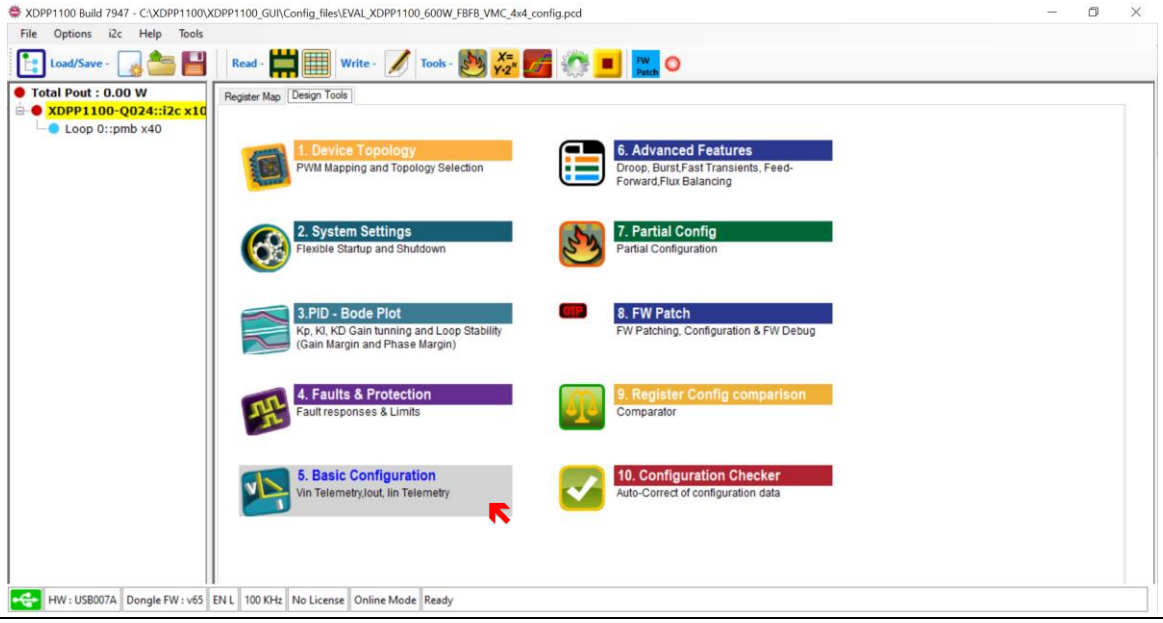


Figure 41 Basic Configuration (V_{IN} telemetry, I_{OUT}, I_{IN} telemetry)

4.5.1 Output current sense tab

In the evaluation kit, the output current is sensed by the current ADC **ISEN/IREF**. So, the **Source select** in this tab should be chosen as **ISP1 (ISEN)** (**Figure 42**).

PMBus command **MFR_IOUT_APC** (Code EA) configures the output CS gain. **MFR_IOUT_APC** is equal to **ISEN_LSB**/(**Rsns** × $\mathbf{G_{amp\_Rsns}}$) where **ISEN_LSB** is defined by the **isen_gain_mode** (**Figure 42**), which can be set as 100 µV or 1.45 mV, **Rsns** is the current sense resistor value, and $\mathbf{G_{amp\_Rsns}}$ is the amplification gain after the **Rsns**.

For this evaluation board, **ISEN_LSB** is chosen as 1.45 mV LSB by setting **isen_gain_mode** to **ISEN1 LSB 1.45mV GND IREF1** (**Figure 42**). As an external op-amp is used on the board, the Rsns is the sense resistance multiplied by the op-amp gain. For **Rsns**, the CS shunt is implemented by PCB copper, which has a resistance of 0.2 mΩ at room temperature, and $\mathbf{G_{amp\_Rsns}}$ is 20. Hence, **MFR_IOUT_APC** = 1.45 mV / (0.2 mΩ × 20) = 0.36 A.

Also, the design tool provides a calculation of the slope of the current estimator (**ce_kslope_didv**) based on the output inductor L_{OUT} value (**Figure 42**). Please refer to XDPP1100 application note (**link to download**) for more information on the current estimator module.

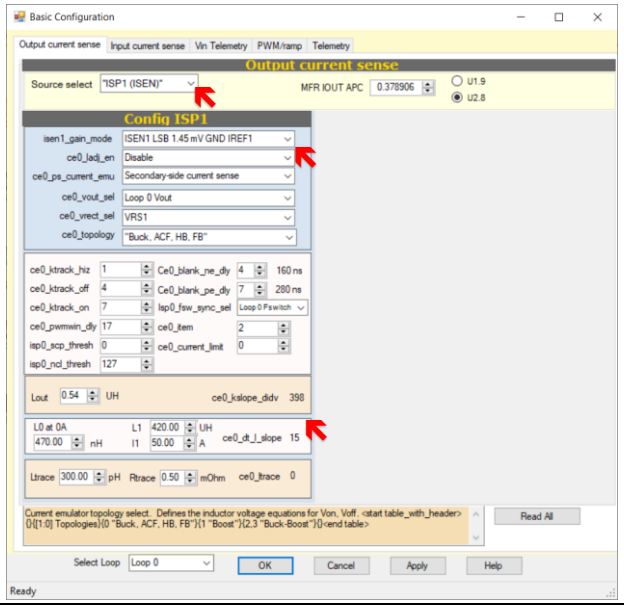


Figure 42 Output current sense tab

For more accurate current telemetry, on board trimming is required to correct the error of gain and offset from board to board. The evaluation board doesn't perform the trimming. User could trim the **MFR_IOUT_APC** and **IOUT_CAL_OFFSET** to achieve desired accuracy.

A detailed explanation of the CS registers can be found in Table 16 of **XDDP1100 technical reference manual**.

4.5.1.1 Temperature sense

XDPP1100-Q024 supports one external and one internal temperature measurement for precise measurements and protection. An optimized look-up table for the external temperature sensor is in the XDPP1100's ROM for recommended 47 kΩ negative temperature coefficients (NTCs) (Murata NCP15WB473F03RC or Panasonic ERT-J0EP473J) in parallel with a 12 kΩ resistor (**Figure 44**). Temperature sensors is connected to **TSEN** pin. Also, users can define their customized temperature look-up table for other desired sensors (e.g. V_{BE} temperature sense) by FW patch if another temperature sensing device is preferred.

The internal temperature sensor is within the XDPP1100 die and measures the controller's junction temperature.

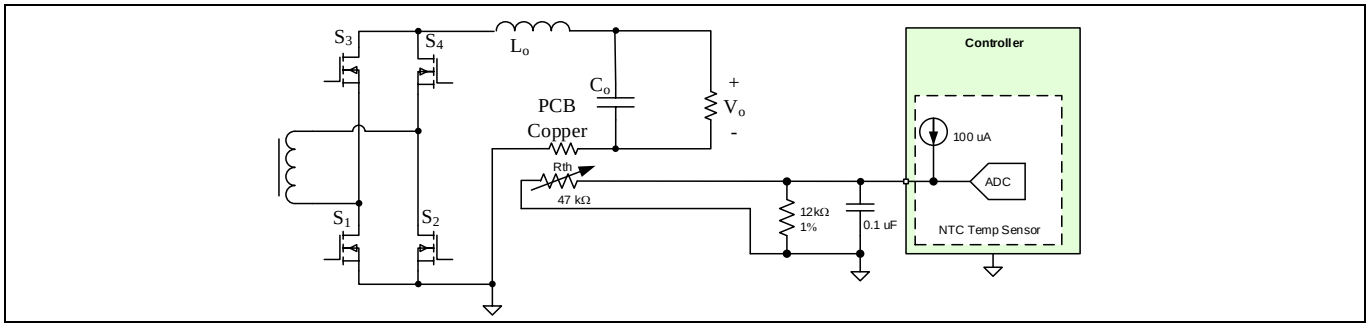


Figure 43 NTC temperature sensing circuit

On the power board of the evaluation kit, the temperature sensors RT1 and RT2 are respectively for the shunt resistance and synchronous FET temperature sensing techniques. As PCB copper trace is used as the current sensor on this board, RT1 temperature is fed back to the processor to compensate for the temperature drift of the current sensor.

Temperature sensors can be configured through the PMBus command **MFR_SELECT_TEMPERATURE_SENSOR** (Code DC) (**Figure 44**). Please note that only **Read_Temperature_1** can be set as the current source's source of temperature drift compensation. Hence, select **1: tempa tempi** as the source of temperature reading (**Read_Tempreature_1_Read_Tempreature_2**).

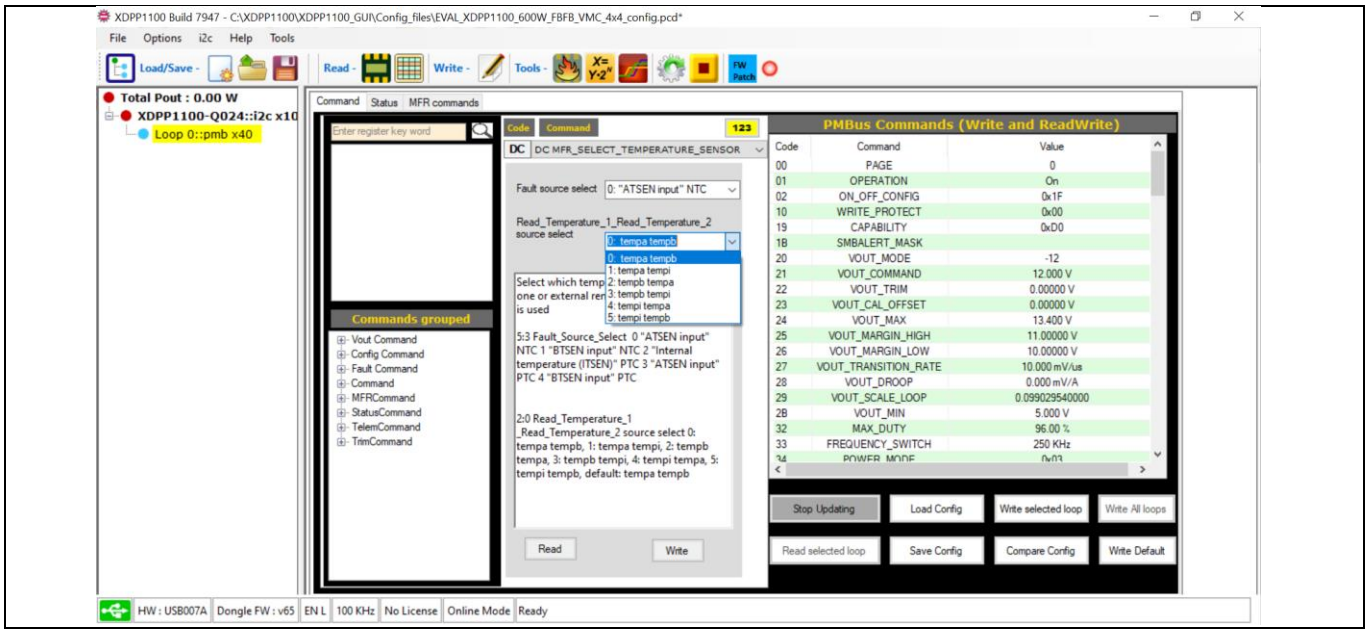


Figure 44 Configure temperature sensors through the PMBus command MFR_SELECT_TEMPERATURE_SENSOR (Code DC)

4.5.2 Input current sense tab

The XDPP1100-Q024 has one precise CS ADC. In the current configuration of the evaluation kit, this CS ADC is dedicated to measuring the output current. And for the input current, its value is estimated based on the measured V_{IN}, V_{OUT}, and I_{OUT}. In the **Input current sense** tab, the **estimated Input current** is chosen at the **Source select** as shown in **Figure 45**. The current estimate alpha coefficient defines the relative contributions of V_{OUT} / V_{IN} and duty cycle in the computing the input current estimated value.

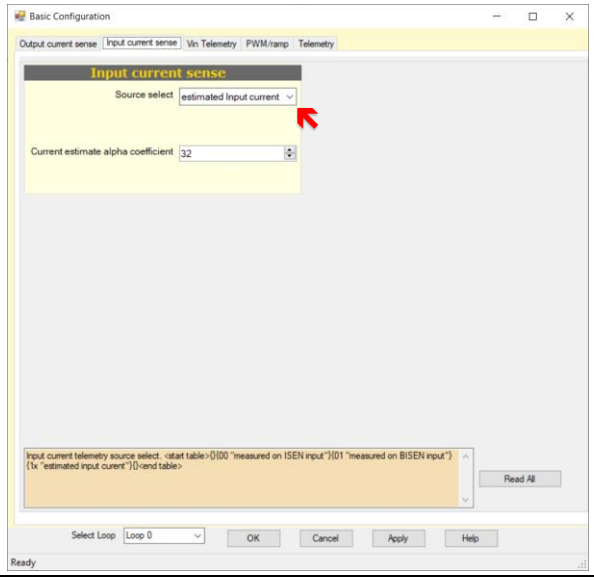


Figure 45 Input current sense tab

4.5.3 Vin Telemetry tab

The XDPP1100 offers a wide selection of sources for the input voltage measurement (**Figure 46**) which are listed and explained in **Table 4**.

Table 4 tlm_vin_src_sel configuration table

Value	Input voltage source
0	**VRSEN**. Secondary V_{RECT} sense, **vrs_init** prior to start-up
1	**BVSEN_BVRSEN**. Secondary V_{RECT} sense, **vrs_init** prior to start-up
2	**Loop 0 V_{OUT}**. Select on loop 1 when loop 1 V_{IN} provided by loop 0 V_{OUT} (e.g., post-buck).
3	**TS ADC V_{IN}**. non-pulsed/primary V_{IN} sense via telemetry ADC (PRISEN)
4	**tlm_vin_force**. Forced V_{IN} via FW (e.g., FW over-ride of HW computation)
5	**VRSEN**. Secondary V_{RECT} sense, **0 V** prior to start-up. Select on loop 1 when sharing loop 0 V_{RECT} sense
6	**VRSEN**. Non-pulsed/primary V_{IN} sense
7	**BVSEN_BVRSEN**. Non-pulsed/primary V_{IN} sense

The evaluation kit has two input voltage sense circuits. Users can select each from the Vin Telemetry tab (**Figure 46**);

1. Setting **tlm0_vin_src_sel** to **VRS1 (VRSEN, vrs_init prior to startup)** will configure the XDPP1100 to measure V_{IN} from the secondary side of the main transformer through the **VRSEN** pin. It works when the main power supply is in switching.
2. Setting **tlm0_vin_src_sel** to **TS ADC Vin** will configure the XDPP1100 to measure V_{IN} through the auxiliary power supply via the **PRISEN** pin. It works as long as the auxiliary power is in the regulation.

*Note: In general, selecting **VRSEN** is preferred for higher accuracy, faster feed-forward response, and faster fault protection.*

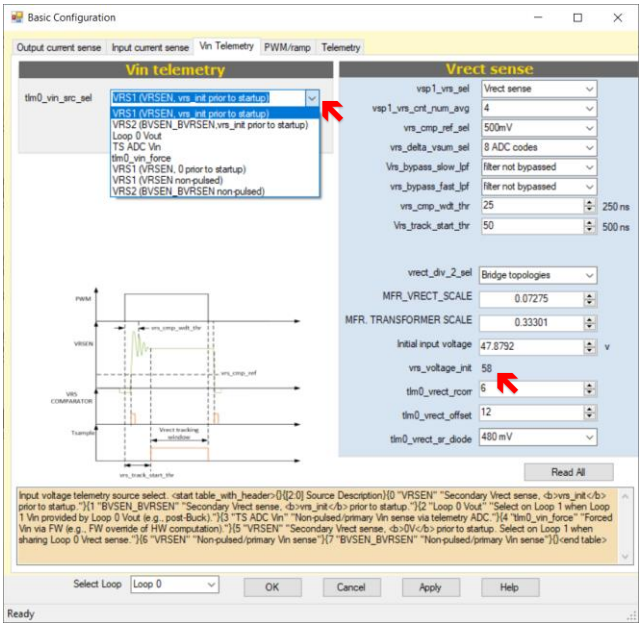


Figure 46 Vin Telemetry tab

4.5.3.1 Setting tlm0_vin_src_sel to VRS1 (VRSEN, vrs_init prior to startup)

For measuring the input voltage from the rectified voltage (V_{RECT}) at the secondary side of the isolated transformer (V_{RECT}), **VRS1 (VRSEN, vrs_init prior to startup)** has to be selected from the **tlm0_vin_src_sel** drop-down list as the input voltage source. In this case, the V_{RECT} waveform and the associated registers will be shown in the **Vin Telemetry** tab.

A detailed explanation of the VRSEN registers can be found in Table 2 and 61 of the **XDDP1100 technical reference manual**. An initial voltage for VS1 (VRSEN) when operating in VRS mode (**vrs_voltage_init**) will be calculated automatically by the design tool based on the following equations:

1. For the FB and the active clamped forward (ACF) topologies:

$$vrs\_voltage\_init = \frac{Vin\_init(V)}{20mV} \times MFR\_VRECT\_SCALE \times MFR\_TRANSFORMER\_SCALE$$

2. For the half-bridge (HB) topology:

$$vrs\_voltage\_init = \frac{Vin\_init(V)/2}{20mV} \times MFR\_VRECT\_SCALE \times MFR\_TRANSFORMER\_SCALE$$

For instance, in the FB topology of the evaluation kit with Vin = 48 V, we have:

$$vrs\_voltage\_init = \frac{48V}{20mV} \times 0.073 \times 0.333 = 58$$

4.5.3.2 Setting tlm0_vin_src_sel to TS ADC V_{IN} (PRISEN)

To measure the input voltage through the auxiliary power supply, **TS ADC Vin** has to be selected from the **tlm0_vin_src_sel** drop-down list as the input voltage source. In this case, related **PRISEN** registers will be shown in the **Vin Telemetry** tab.

A detailed explanation of PRISEN registers can be found in Table 23 of the **XDDP1100 technical reference manual**.

vin_pwl_slope and **vin_trim** are the gain and offset of a linear relationship between the TS ADC code and actual Vin value. Users can also compensate for HW measurement errors by these two registers. For the V_{IN}, we have:

$$V_{IN} = \textbf{vin\_pwl\_slope} \times ADC + \textbf{vin\_trim}$$

vin_pwl_slope can be calculated by the following equation:

$$vin\_pwl\_slope = \frac{1.2 \times 2^5}{PRISEN\_SCALE}$$

For example, in the evaluation kit, the resistor divider for PRISEN measurement has the ratio of 1.3 kΩ/ (100 kΩ + 1.3 kΩ) = 0.0128. Hence, **vin_pwl_slope** is:

$$vin\_pwl\_slope = \frac{1.2 \times 2^5}{0.0128} = 3000$$

The offset error can be compensated by the **vin_trim** register.

4.5.4 PWM/ramp tab

Users can configure PWM flavor, control mode, and maximum duty-cycle scaling for the respective loop through this tab (**Figure 47**).

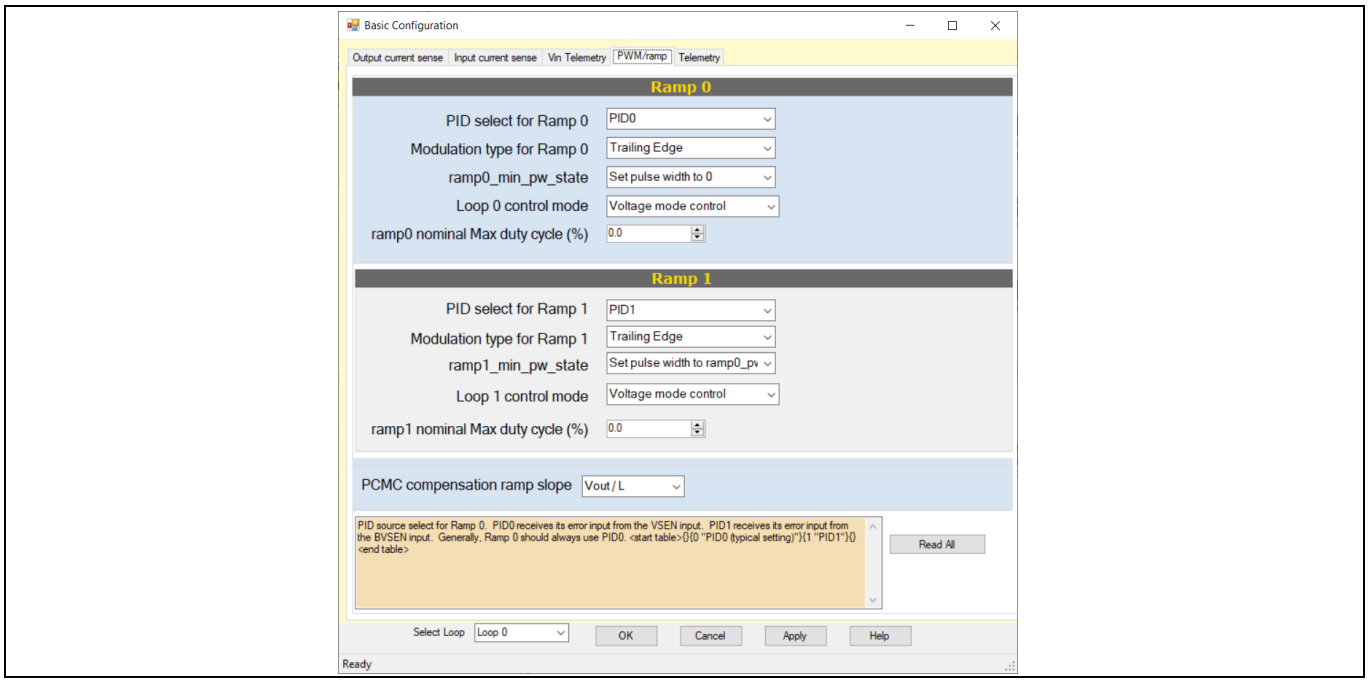


Figure 47 PWM/ramp tab

A description of the registers in this tab can be found in Table 48 of the **XDDP1100 technical reference manual**.

4.5.5 Telemetry tab

Users can set the low-pass filter (LPF) coefficients of corresponding telemetry in this tab. The LPF coefficients for output current, input current, input voltage, duty-cycle, and output voltage measurements depend on the switching frequency of the power converter. On the other hand, the filter coefficients for temperature, PRISEN, IMON, and address telemetries are independent from the switching frequency.

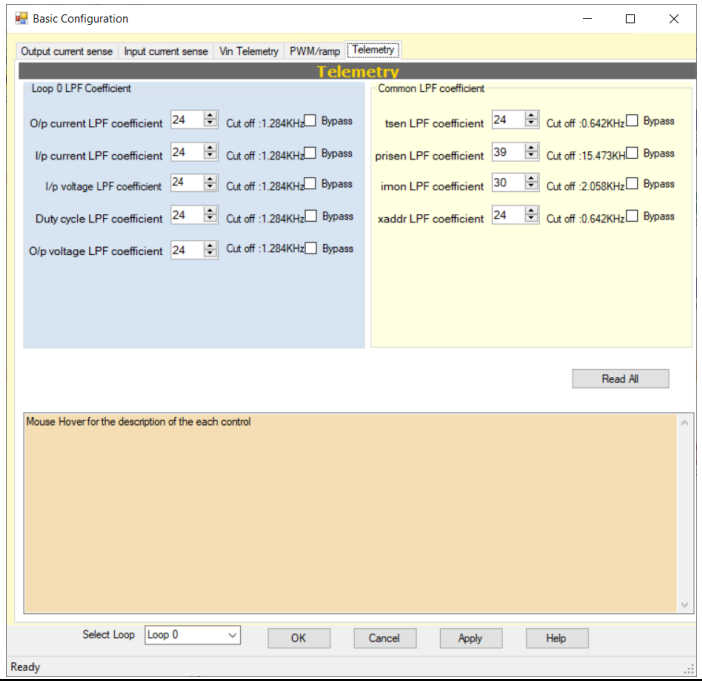


Figure 48 Telemetry tab

4.6 Advanced features (droop, burst, fast transients, feed-forward, flux balancing)

Users can program advanced features of the XDPP1100 such as feed-forward, current balancing, flux balancing, current sharing, sync in/out, droop, fast transient, and burst operation using this tool. To access this tool:

- Click on **XDPP1100-Q024::i2c x10** (highlighted in yellow in **Figure 49**).
- Click on **Design Tools** and select **6. Advanced Features.**

The **Advanced Configuration** window will be opened with **Feed-forward**, **Current balancing**, **Flux balancing**, **Current sharing**, **Sync In/Out**, **Droop**, **Fast Transient**, and **Burst** tabs.

The current balancing, current sharing, sync in/out, droop, and fast transient are not the focus of this evaluation board. Please refer to the XDPP1100 application note (**link to download**) for more information on these advanced features.

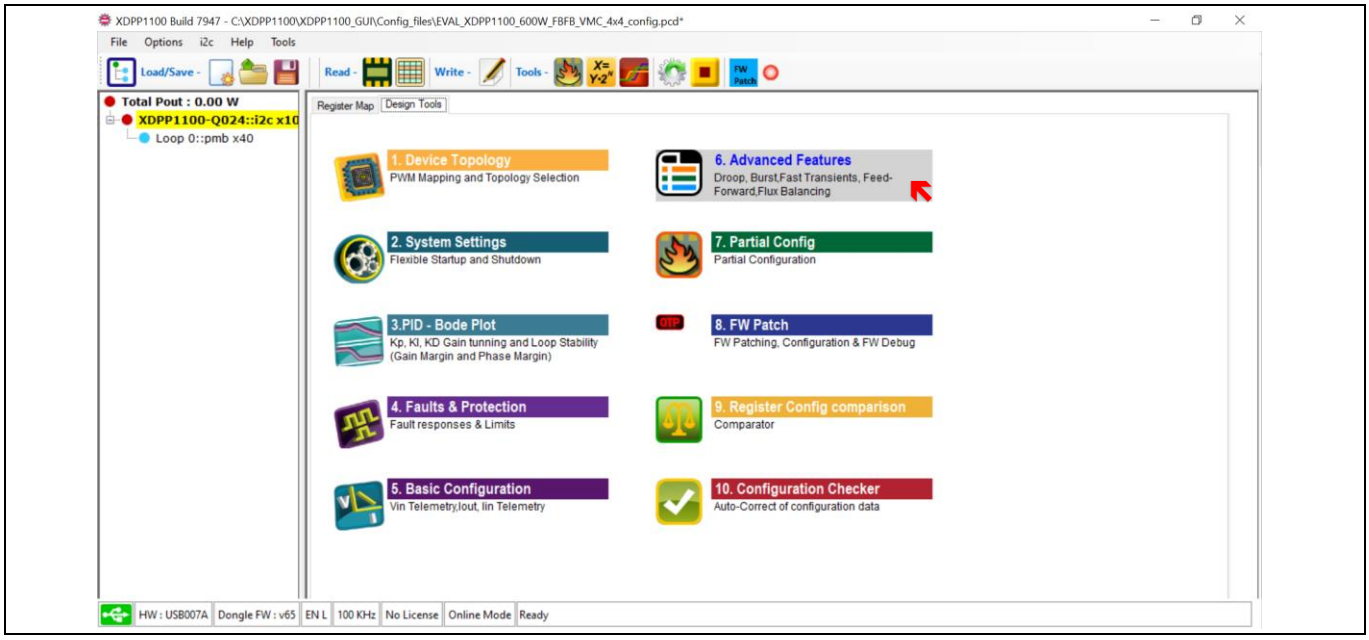


Figure 49 Advanced features (droop, burst, fast transients, feed-forward, flux balancing)

4.6.1 Feed-forward tab

The XDPP1100 is equipped with a HW-based feed-forward feature to enhance the speed of control loop response compared to the linear feedback system. The XDPP1100 adjusts power-converter duty cycle based on the updated input and output voltage values upon sensing the input voltage transient. **Feed-forward** registers are listed and explained in Table 2 and 34 in the **XDPP1100 technical reference manual**.

Register **pid_ff_vrect_sel** allows the user to select one of four sources for the V_{IN} input:

- Select **VS1 (VRSEN) Vrect**: Senses V_{RECT} on **VRSEN** inputs
- Select **VS2 (BVSEN_BVRSEN) Vrect**: Senses V_{RECT} on **BVRSEN** inputs
- Select **Telemetry Sense Vin**: Senses V_{IN} on the **PRISEN** input (telemetry sense V_{IN})
- Select **pid0_ff_vrect_override**: Overrides of sensed V_{RECT} through FW

The **pid0_ff_vrect_override** register value defines the feed-forward value to override V_{RECT}. It is calculated from PMBus commands as in the follows:

$$pid0\_ff\_vrect\_override = \frac{\mathrm{Vin(V)}}{1.25mV} \times MFR\_VRECT\_SCALE \times MFR\_TRANSFORMER\_SCALE$$

For example, in the evaluation kit, we have:

$$pid0\_ff\_vrect\_override = \frac{48V}{1.25mV} \times 0.07227 \times 0.333 = 924$$

In the evaluation kit, the provided configuration sets XDPP1100 to use the rectified voltage at the secondary side of the transformer (**VRSEN**) as the source of input voltage telemetry and feed-forward implementation. The alternative input source is using generic ADC (**PRISEN**). However, as the sample rate of the **VRSEN ADC** is considerably higher than the general-purpose ADC, selecting VRSEN as the source of the feed-forward module leads to the faster loop response.

Note: Changes in this tab are immediately applied on making the drop-down selection. All changes are stored into RAM of the IC and must be stored to OTP once the changes are finalized.

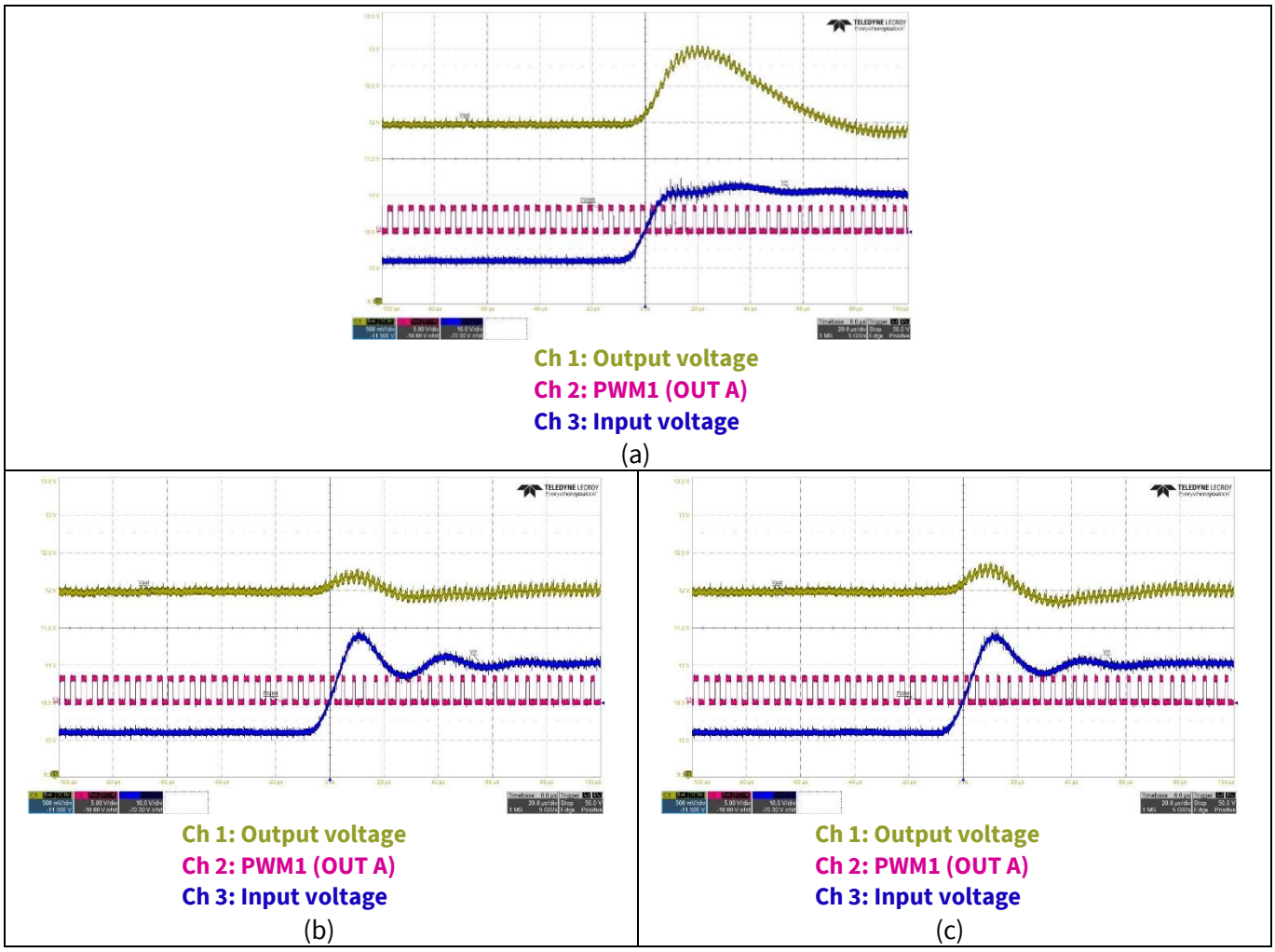


Figure 50 Feed-forward experimental results - a) feed-forward disabled by selecting pid0_ff_override_sel as pid0_ff_override and pid0_ff_overide = 0, b) same cycle enabled, c) same cycle disabled

4.6.2 Flux balancing tab

In the FB converters, timing mismatch between the gating signals can cause asymmetrical applied volt-seconds across the transformer winding from one half-cycle to its complementary half cycle. So, applied voltage will not be purely AC anymore. In this case, the excess DC voltage term across the transformer winding causes ”flux-walkaway” and leads to saturation of its ferromagnetic core. To avoid this phenomenon, PWM timing must be adjusted dynamically to compensate for practical timing mismatches and prevent the transformer core from being saturated.

The XDPP1100 volt-second balancing module will ensure symmetrical volt-seconds across the transformer winding. In each duty cycle, input voltage and timings using rectified voltage (V_{RECT}) and a high-speed edge comparator with 5 ns accuracy will be measured. Then, an error between (volt × second) of each half-cycle will be fed to a PI compensator to adjust the PWM timings and ensure flux balancing. **Flux balancing** is available just for the FB topology in voltage-mode control. This feature will be activated when register

ramp0_dutyc_lock = 1. **Flux balancing** registers are listed and explained in Table 77 of the **XDDP1100 technical reference manual**.

For correct measurement of the VRS pulse width and flux balancing, sufficient dead time before the SR rising edge is crucial. If the SR rising edge is too close to the falling edge (i.e., insufficient dead time), the XDPP1100 VRS counter might measure VRS pulse width inaccurately and fail to do the flux balancing.

Note: Changes in this tab are immediately applied on making the drop-down selection. All changes are stored in RAM of the IC and must be stored to OTP once the changes are finalized.

The XDPP1100 is capable of performing two different volt-second balance methods; flux (volt-seconds balance and time-only balance. For the evaluation kit, each method can be configured as follows:

1. To enable flux balancing using time only, set **kp_fbal** = 4, **ki_fbal** = 24, **vbal_mode_sel** = **flux balance mode (select for FB primary)**, **fbal_time_only** = **Enable** and **ramp0_dutyc_lock** = checked.
2. To enable flux balancing using volt-second, set **kp_fbal** = 4, **ki_fbal** = 24, **vbal_mode_sel** = **flux balance mode (select for FB primary)**, **fbal_time_only** = **disable** and **ramp0_dutyc_lock** = checked.

To evaluate the experimental performance of the **Flux balancing** module, 30 ns is added to one side of the primary side gate pulse (**Figure 51**) in order to create imbalanced volt-seconds. These PWM settings can be done using the PMBus command **PWM_DEADTIME** (Code CF). Steady-state experimental results of the evaluation kit without flux balancing, with flux balancing enabled but operating in discontinuous conduction mode (DCM), with flux balancing enabled and time-only mode, and with enabled flux-balancing and volt-seconds technique, are shown in **Figure 52a to d**, respectively. As shown in **Figure 52b**, XDPP1100 disables flux-balancing under the predefined DCM threshold, because predicting the primary voltage from the transformer secondary winding is not feasible in DCM operation. Similarly, experimental results for the line transient and the load transient are shown in **Figure 53** and **Figure 54**, respectively.

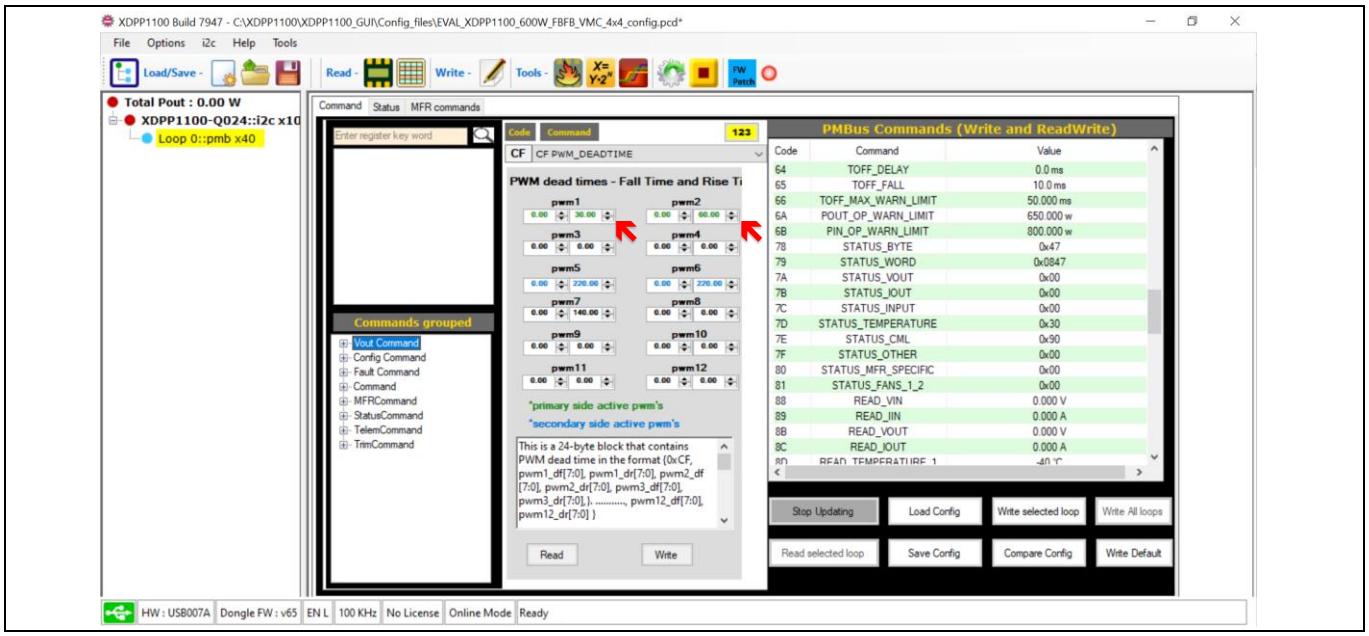
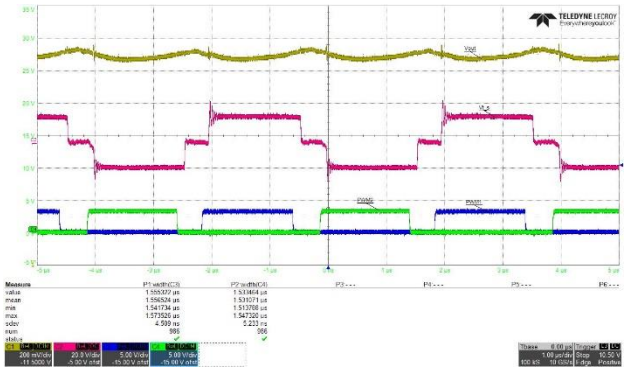
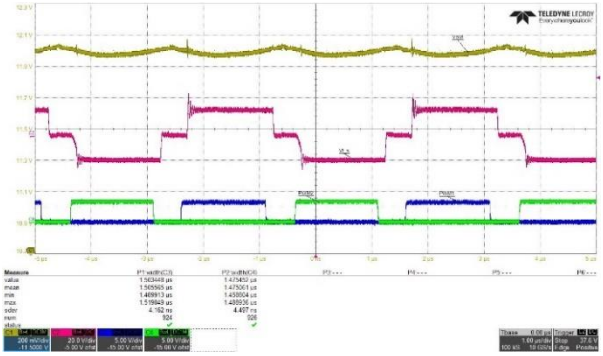


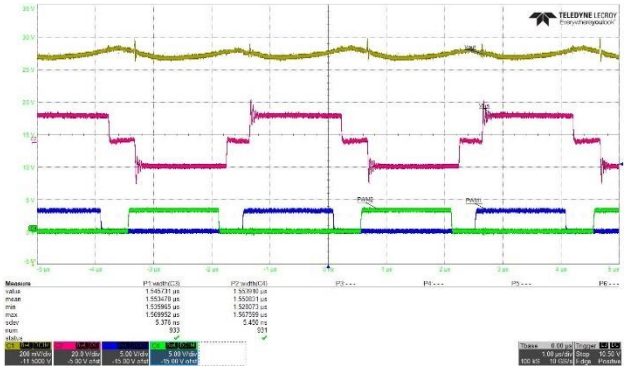
Figure 51 Mismatching the gate driver signals



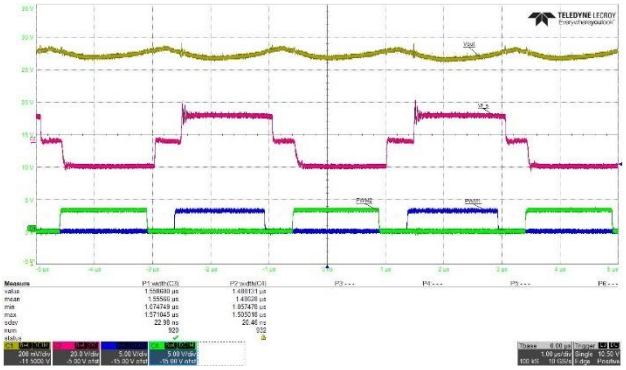
Ch 1: Output voltage
Ch 2: Transformer secondary voltage
Ch 3: OUT A PWM
Ch 4: OUT B PWM
(a)



Ch 1: Output voltage
Ch 2: Transformer secondary voltage
Ch 3: OUT A PWM
Ch 4: OUT B PWM
(b)

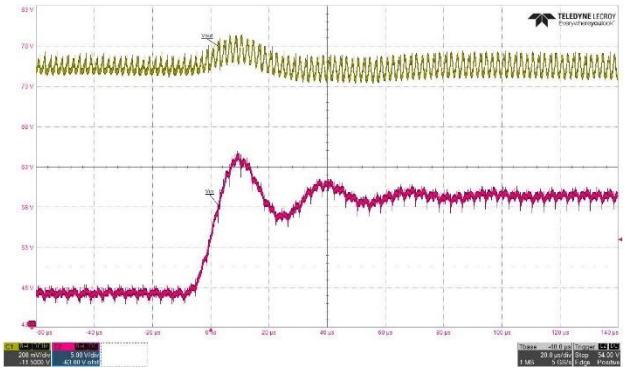


Ch 1: Output voltage
Ch 2: Transformer secondary voltage
Ch 3: OUT A PWM
Ch 4: OUT B PWM
(c)



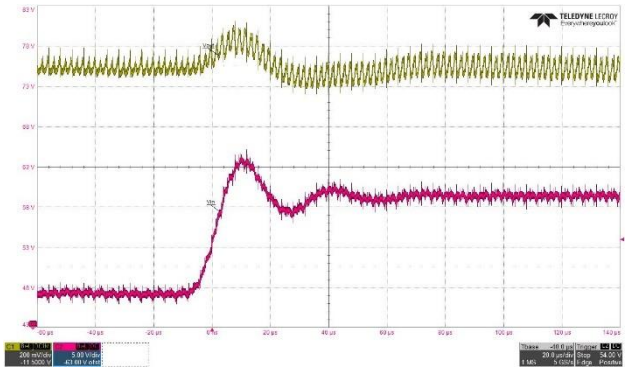
Ch 1: Output voltage
Ch 2: Transformer secondary voltage
Ch 3: OUT A PWM
Ch 4: OUT B PWM
(d)

Figure 52 **Flux balancing steady-state result - a) ramp0_dutyc_lock = unchecked (flux balancing disabled), b) ramp0_dutyc_lock = checked and I_{OUT} = 10 A (flux balancing is disabled due to DCM), c) ramp0_dutyc_lock = checked and fbal_time_only = enable (flux balancing is disabled due to DCM), d) ramp0_dutyc_lock = checked and fbal_time_only = disable (flux balancing enabled with volt × seconds technique)**



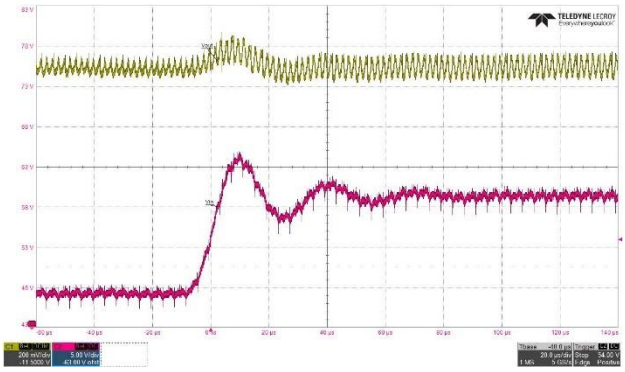
Ch 1: Output voltage
Ch 2: Input voltage

(a)



Ch 1: Output voltage
Ch 2: Input voltage

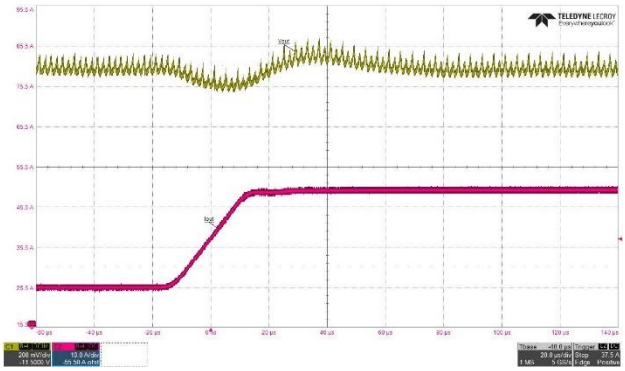
(b)



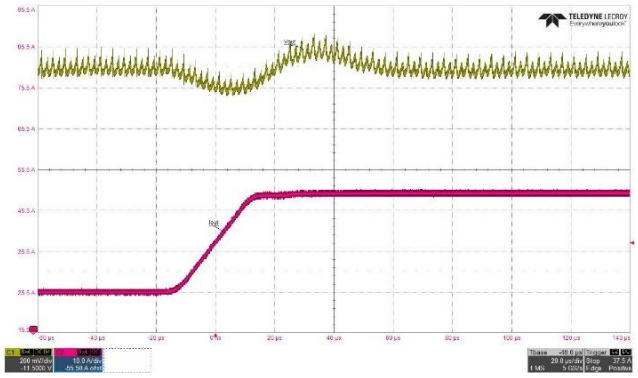
Ch 1: Output voltage
Ch 2: Input voltage

(c)

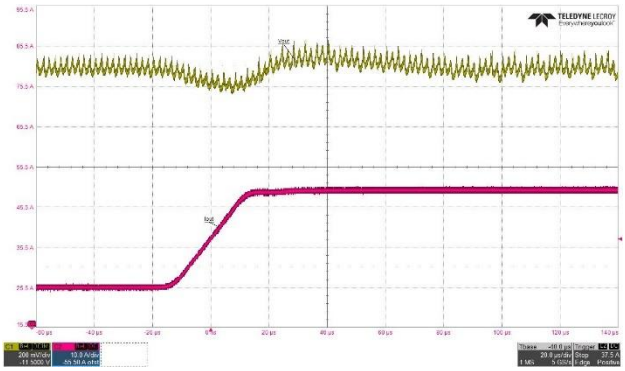
Figure 53 **Flux balancing line transient results - a) ramp0_dutyc_lock = unchecked (flux balancing disabled), b) ramp0_dutyc_lock = checked and fbal_time_only = enable (flux balancing is disabled due to DCM), c) ramp0_dutyc_lock = checked and fbal_time_only = disable (flux balancing enabled with volt × seconds technique)**



Ch 1: Output voltage
Ch 2: Output current
(a)



Ch 1: Output voltage
Ch 2: Output current
(b)



Ch 1: Output voltage
Ch 2: Output current
(c)

Figure 54 Flux balancing load transient results - a) ramp0_dutyc_lock = unchecked (flux balancing disabled), b) ramp0_dutyc_lock = checked and fbal_time_only = enable (flux balancing is disabled due to DCM), c) ramp0_dutyc_lock = checked and fbal_time_only = disable (flux balancing enabled with volt × seconds technique)

4.6.3 Burst mode tab

Burst mode is a common technique to reduce switching losses of switched-mode power-converters in the light-load operation condition. This mode of operation can be enabled by setting PMBus command **POWER_MODE** (Code 34) to 0. By enabling this feature, XDPP1100 enters burst mode and stops switching the power converters (burst-off) when the load current falls below the burst-entry threshold. After that, when the output voltage drops to a target level (burst-on), switching will be resumed. SRs are also off during the burst mode (burst-on). Those target levels define output voltage ripple in this mode of operation. In the burst mode, PID output is frozen to its value right before entering burst mode. Thus, during the burst-on period, the converter works with a constant duty cycle. **Burst mode** registers are listed and explained in **Table 5**.

Table 5 Burst mode registers (loop0, pid 0)

Register name	Module name	Description
en_burst0	pid0	FW driven, the burst mode is enabled when PMBus command POWER_MODE = 0

Register name	Module name	Description
Pid0_burst_mode_ith	pid0	Burst mode entry current threshold. When burst mode is enabled (POWER_MODE= 0), the controller will enter burst mode upon the sensed current dropping below pid0_burst_mode_ith. Note LSB = (Qadc / 2) where Qadc is the value of MFR_IOUT_APC in A
Pid0_burst_mode_err_thr	pid0	Burst mode error voltage threshold where the error voltage is defined as (target voltage - sense voltage) at VSEN. When the controller is in burst mode (error voltage greater than pid0_burst_mode_err_thr) it will trigger the start of a new burst sequence. Note: This threshold is always positive, indicating the controller triggers the start of a new burst sequence at or below the target voltage. LSB = 1.25 mV. Range = 0 to 18.75 mV
pid_burst_reps	pid0	Burst mode cycle count. In burst mode, one cycle corresponds to one even half-cycle pulse followed by one odd half-cycle pulse. This register defines the number of burst cycles in each burst event. A higher cycle count can be used to increase the inductor peak current in a burst event, which will increase the time between burst events at a given load current. 0 = 1 cycle 1 = 2 cycles 2 = 4 cycles 3 = 8 cycles

Experimental results of the burst mode operation of the evaluation kit are shown in **Figure 55** with different burst mode cycle counts (**pid0_burst_reps**). The power board operates at V_{IN} = 48 V, V_{OUT} = 12 V, and I_{OUT} = 4 A. Burst mode registers are configured as **pid0_burst_mode_ith** = 25 and **pid0_burst_mode_err_thr** = 8. With PMBus commands **VOUT_SCALE_LOOP** (Code 29) = 0.09902954 and **MFR_IOUT_APC** (Code EA) = 0.400391, the output voltage minimum threshold in burst mode is:

$$Burst\ mode\ output\ voltage\ minimum\ threshold = \frac{pid0\_burst\_mode\_err\_thr \times 1.25\ mV}{VOUT\_SCALE\_LOOP} = 100\ mV$$

And, for the output current threshold to enter the burst mode of operation, we have:

$$Burst\ mode\ output\ current\ entry\ threshold = \frac{pid0\_burst\_mode\_ith \times MFR\_IOUT\_APC}{2} = 5\ A$$

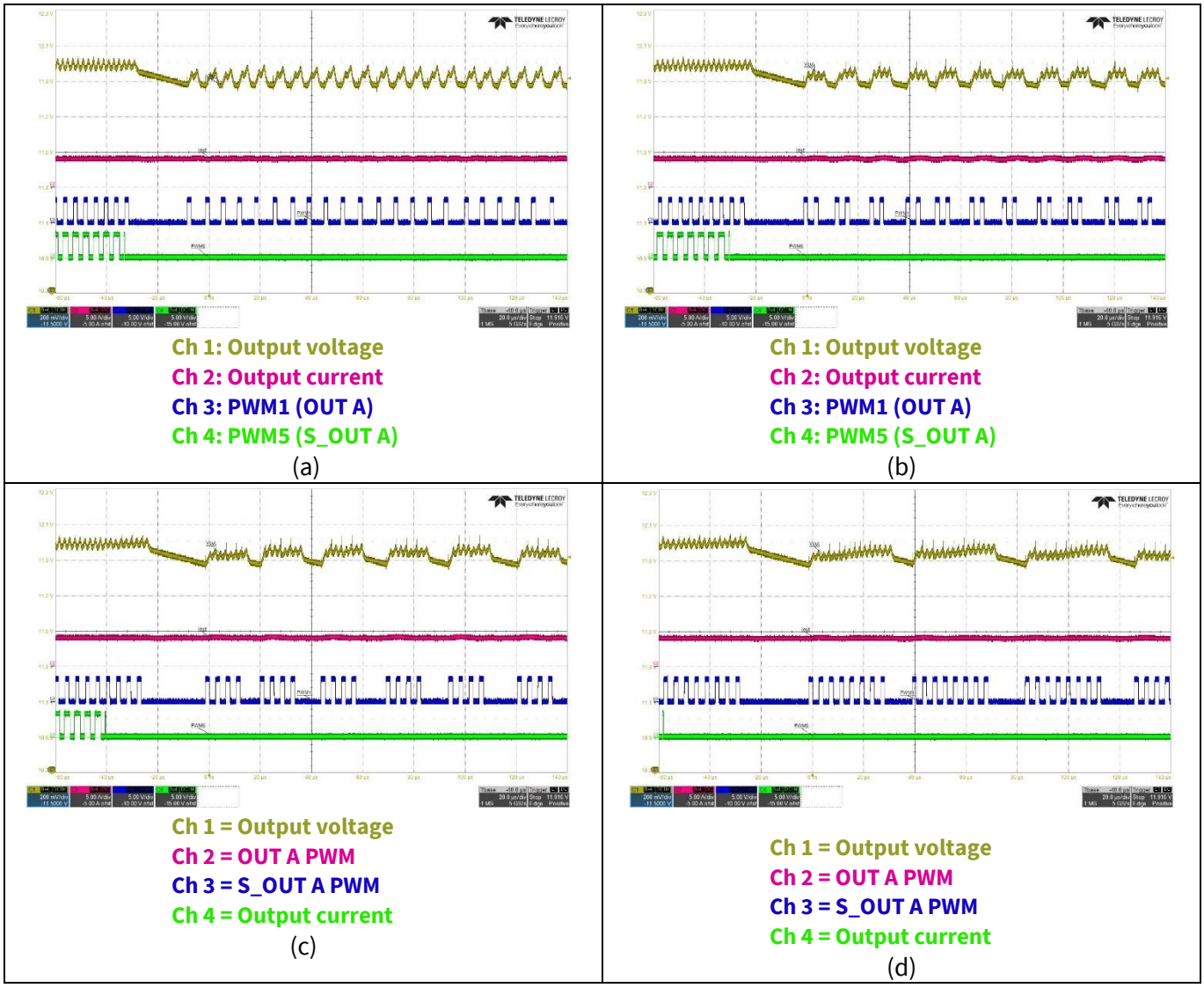


Figure 55 Burst mode experimental waveforms - a) pid0_burst_reps = 0, b) pid0_burst_reps = 1, c) pid0_burst_reps = 2, d) pid0_burst_reps = 3

4.7 FW patch (FW patching, configuration and FW debug)

While the GUI provides a variety of control scenarios, users can customize them by patching their own executable programs into the XDPP1100. This powerful feature of the XDPP1100 provides full flexibility to customize ROM programs or add new functions. User can store codes into the RAM or OTP of the XDPP1100 and manage those memories using the **FW Patch** tool. To access this tool:

- Click on **XDPP1100-Q024::i2c x10** (highlighted in yellow in **Figure 56**).
- Click on **Design Tools** and select **8. FW Patch.**

The **FW Patch** window will be opened with **OTP Partition**, **FW Patch**, **FW Patch Handler**, **FW Config**, and **FW Debug** tabs.

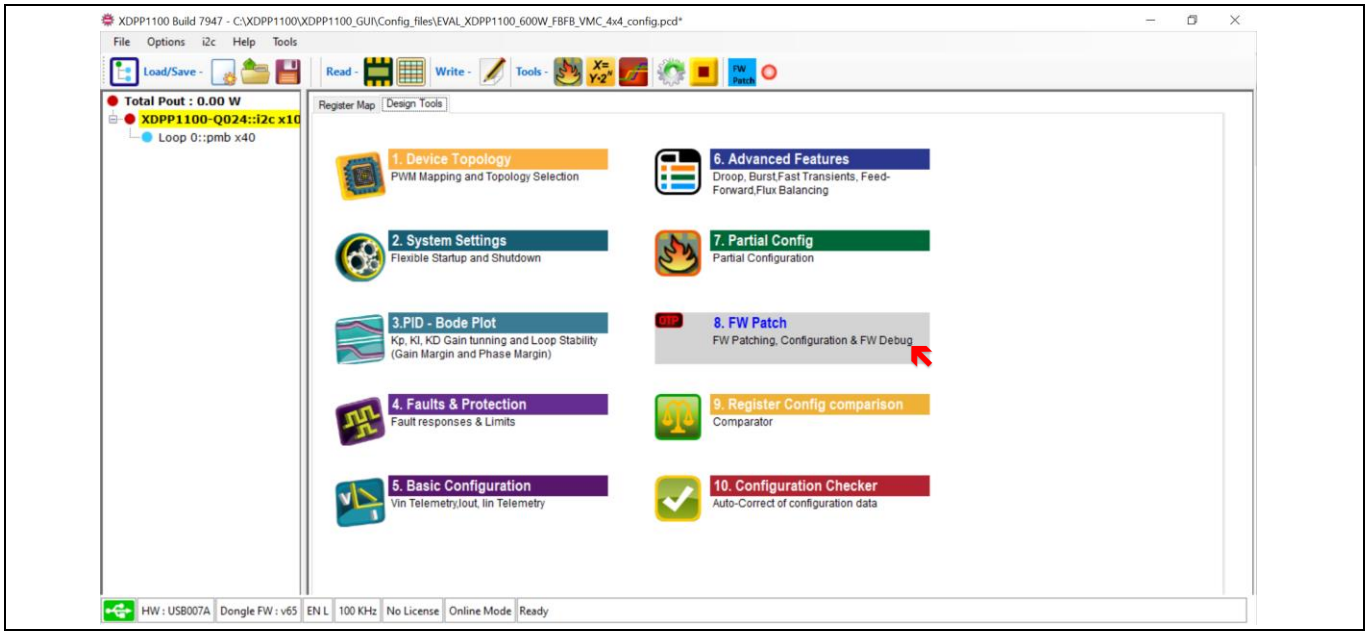


Figure 56 FW patch (FW patching, configuration and FW debug)

Please refer to the **XDPP1100 Firmware User Guide** documentation for detailed information. Information about tools required for FW development can be found in the GUI folder \XDPP1100_fw\doc\ shasta_fw_getting_started.pdf.

4.7.1 OTP Partition tab

Using this tab, users can review and manage OTP partitions to satisfy the program requirements (**Figure 57**). The XDPP1100 has 64 kB OTP and can be partitioned in up to 17 sections. By default, OTP is partitioned into two sections; 1) data which takes 16 kB (0x4000, i.e., 16 kB) and 2) FW patch which is reserved (0xC000, i.e., 48 kB). The OTP Section 0 (**Data Partition**) is used for storing user data such as design configuration which can be set up to 0x7C00 or 31kB, and **Sections 1** to **16** are for storing FW patch. After configuring the desired partition sizes, clicking on **Store Trim** will store the new memory allocation.

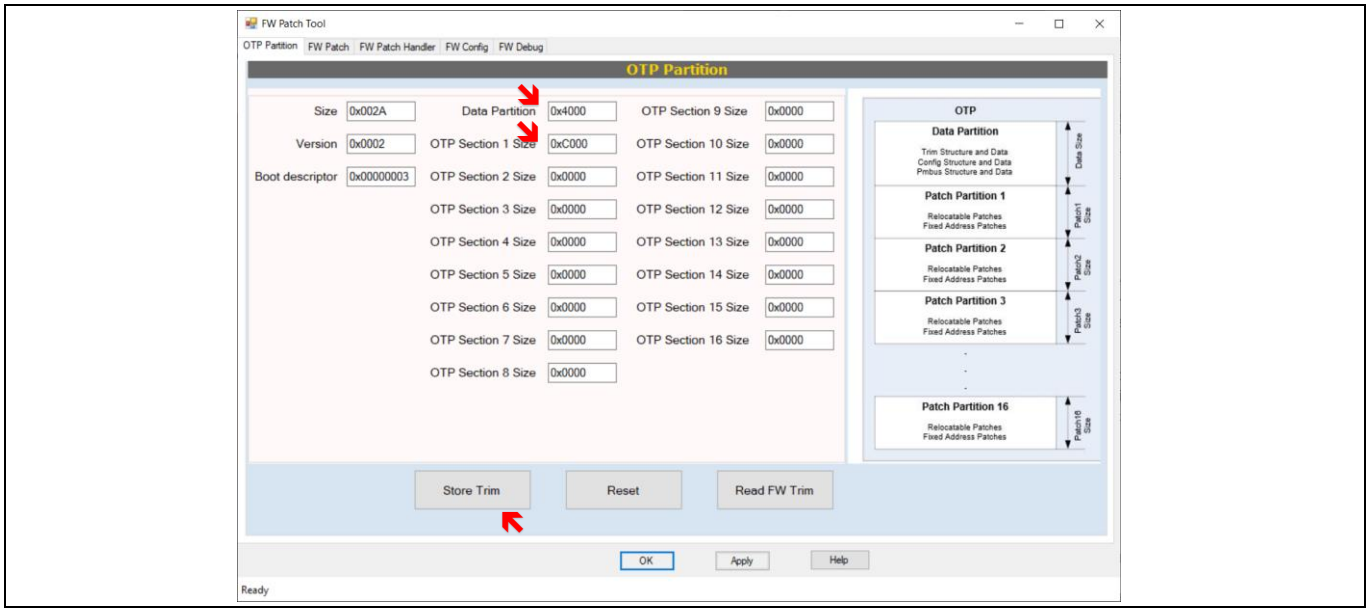


Figure 57 OTP Partition tab

4.7.2 FW patch tab

The FW patch file (compiled .bin file) can be loaded and stored into the XDPP1100 RAM or OTP through this tab. For patch verification and debugging, storing the patch into RAM is recommended to allow unlimited modification while avoiding wasting the OTP capacity. Once the FW patch code is verified and finalized, it can be stored into the OTP to be available and executable after power cycling of the XDPP1100. The XDPP1100 has 8 kB RAM available for FW patch execution. For debugging a patch file with larger size, it can be broken into small modules to make it possible to be stored into RAM. While all the patch modules are tested, they can be unified to the original program and be stored in the OTP.

Note: It is recommended to disable the automatic telemetry update when storing OTP.

Note: Users should always store their patch file first and then store their configuration file, as the patch might alter the PMBus commands.

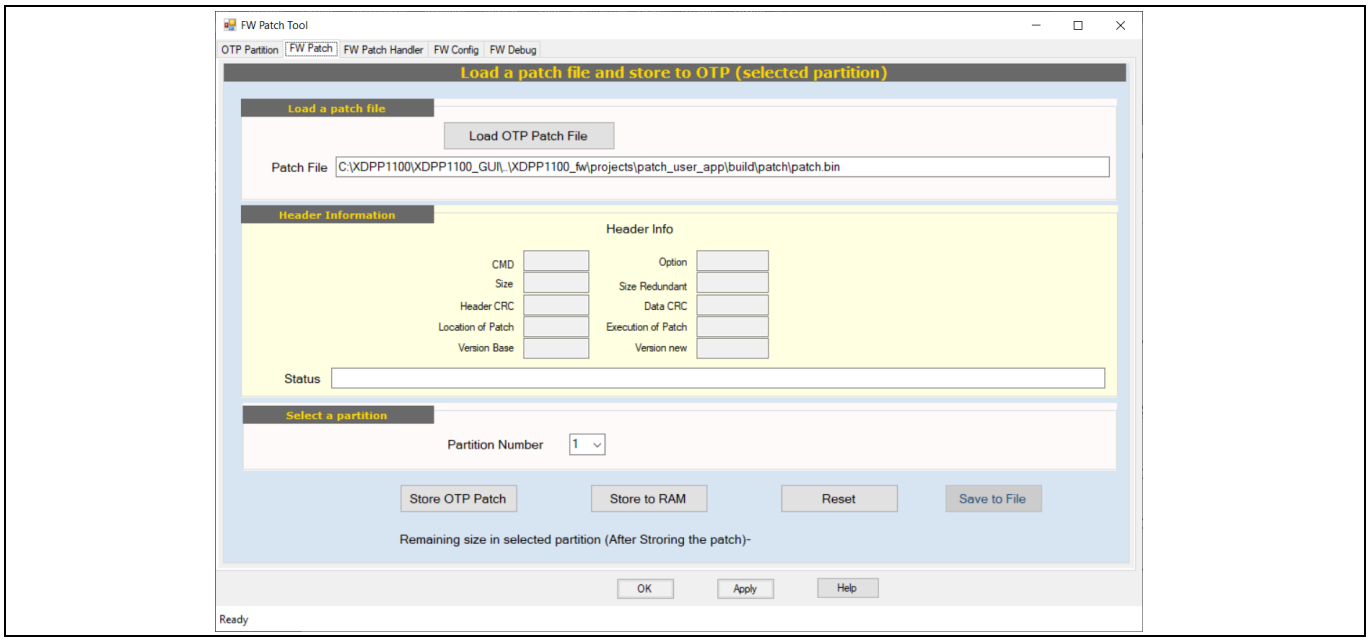


Figure 58 FW Patch tab

4.7.2.1 Load PMBus spreadsheet

If users develop customized manufacturer (MFR) PMBus commands in their patch program, the new MFR-commands must be defined in the **shasta_pmbus.xlsx**. This sheet is available in the **src** folder of the patch project and should be incorporated the final changes before compiling the patch code. The newly generated MFR commands should be loaded into the GUI from the **MFR commands** tab. To access this tab:

- Click the **Loop0::pmbus x40** (highlighted in yellow in **Figure 59**) and select the MFR commands tab.

Clicking the Load **PMBus Spreadsheet** button will load the newly generated PMBus commands sheet (including MFR commands). The patched MFR commands can be configured in this tab by **Write** individually or **Write All** for all MFR commands together.

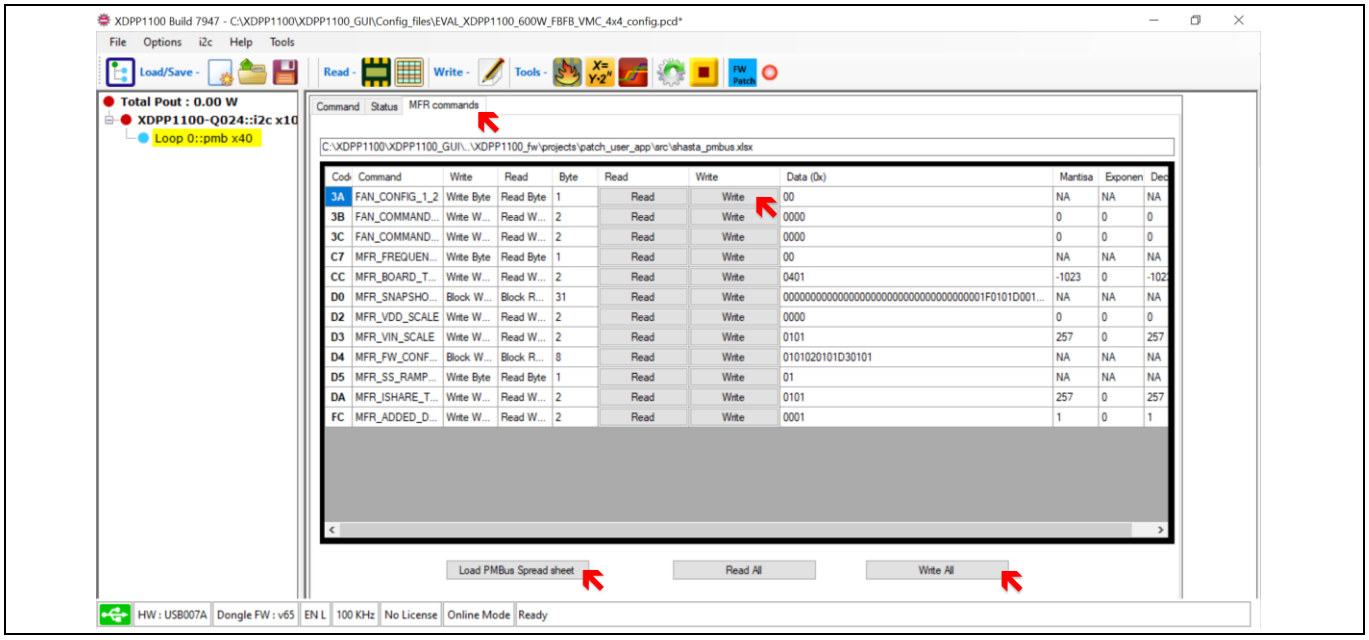


Figure 59 MFR commands tab

4.7.3 FW Patch Handler tab

In this tab, users can search through OTP to find stored active patches and configuration (PMBus commands and registers) using **Find Active patch** and **Find Trim and Config** (**Figure 60**), respectively.

Only one active patch is allowed in each OTP partition, and a warning message will pop up if the user tries to load the patch to a section that already has an active patch. In this case, the user can deactivate an unwanted FW patch before loading a new one. First, **Find Active patch** has to be performed, and then clicking on **Invalidate a patch in a partition** will deactivate the old patch program.

Similarly, an unwanted PMBus or configuration can also be invalidated by first performing **Find Trim and Config** and then clicking on the respective Invalidate button in **Trim and Config(Finder and Invalidate)** window in the **FW Patch Handler** tab (**Figure 60**).

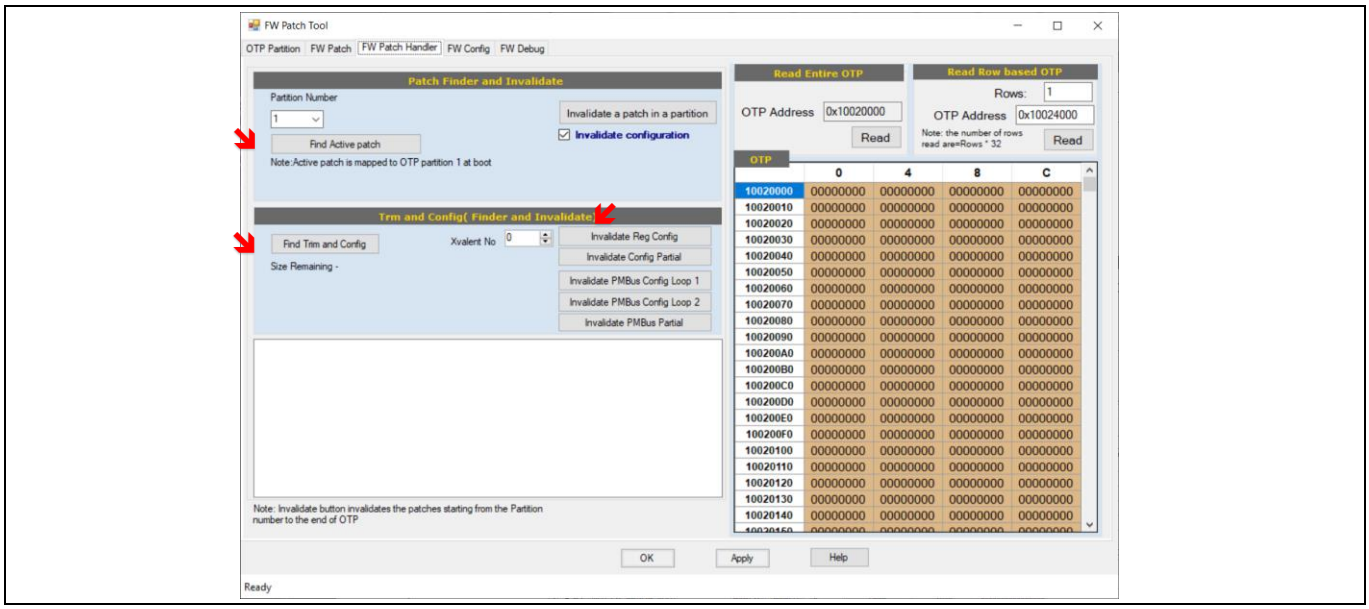


Figure 60 FW Patch Handler tab

4.8 Store user configuration to OTP

Users can save or open a configuration file (**Board Design**) from the **File** menu (**Figure 61**), including configured registers and PMBus commands. Before storing a **Board Design** into the OTP, it must be stored into XDPP1100 RAM. After opening a Config file (**Open Board Design**), GUI will write the opened file into XDPP1100 RAM (**Figure 10**). Also, the **Write all** button (shown with a pencil symbol in **Figure 61**) can store an opened **Board Design** file into RAM and update the most recent configuration file changes.

Figure 61 Open and save a configuration file (board design)

To store a **Board Design** into the XDPP1100 OTP, the user can use the **Multi Device Programmer** tool accessible through the GUI (**Figure 62**). A stored **Board Design** in the RAM will be burned into the OTP by clicking on **Program Configuration To OTP** (**Figure 62**). Successful storing of the **Board Design** into the OTP will be acknowledged with a green check next to **Program Configuration To OTP** button.

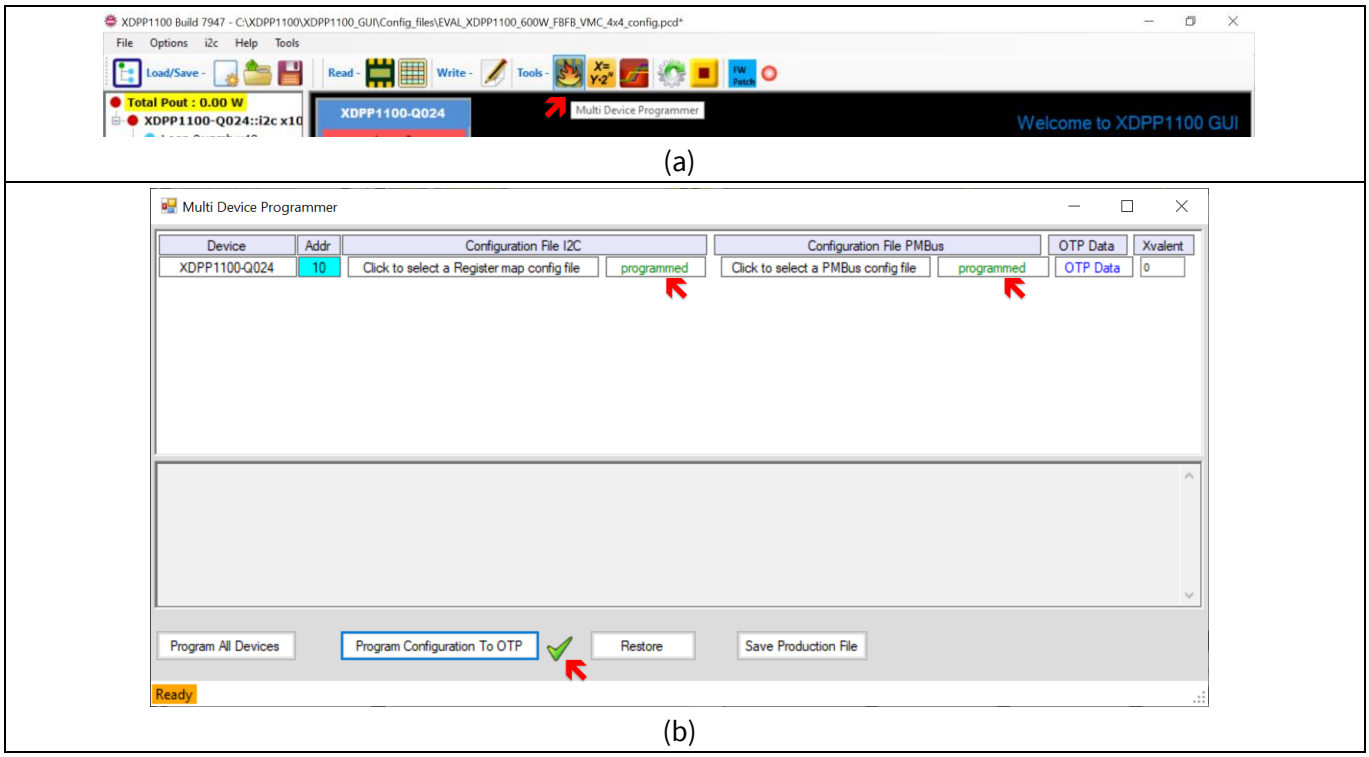


Figure 62 Multidevice Programmer - a) access button, b) successful programming of the Config file into the OTP

5 Schematic and bill of materials

5.1 Schematic

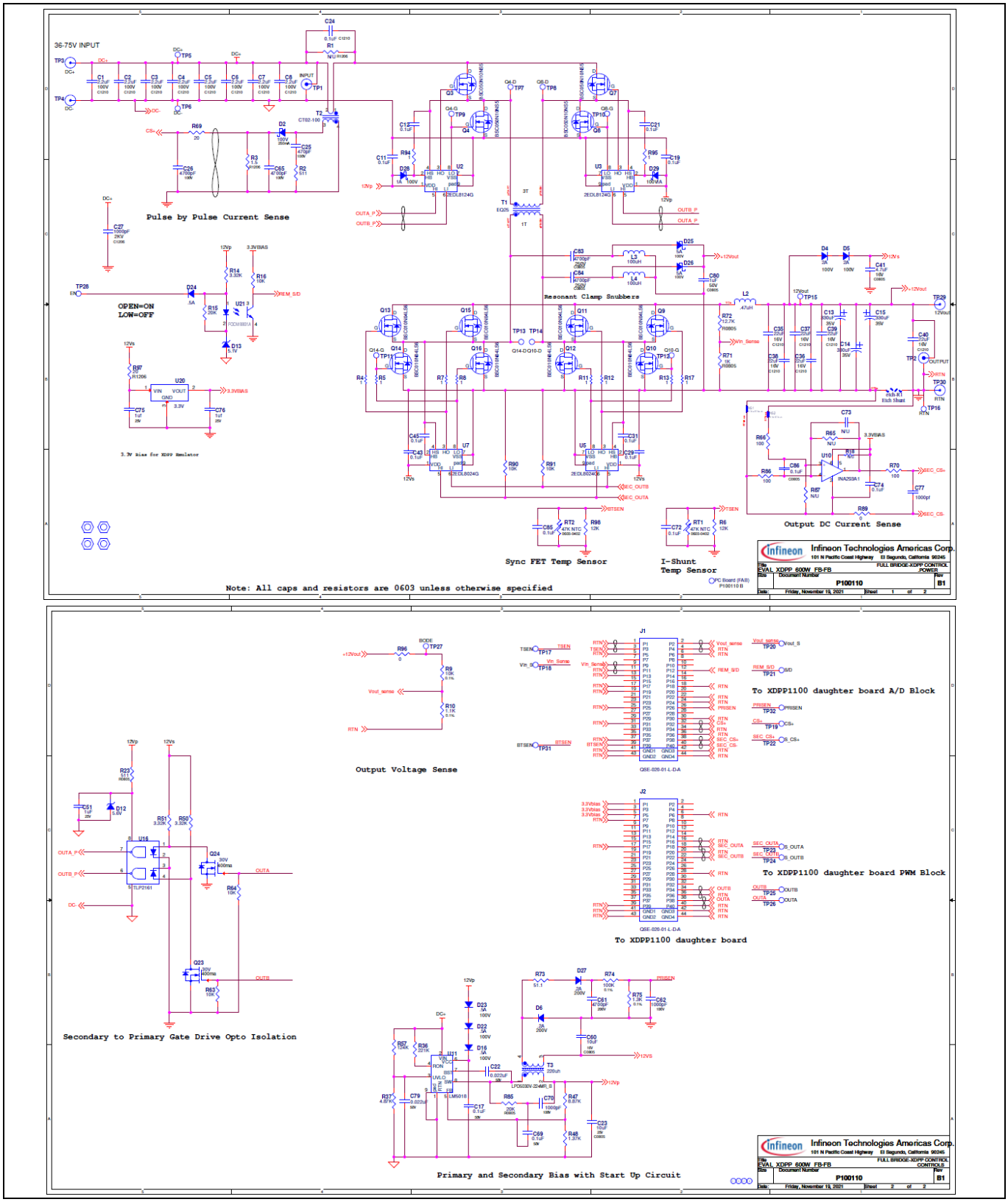


Figure 63 Power board schematic

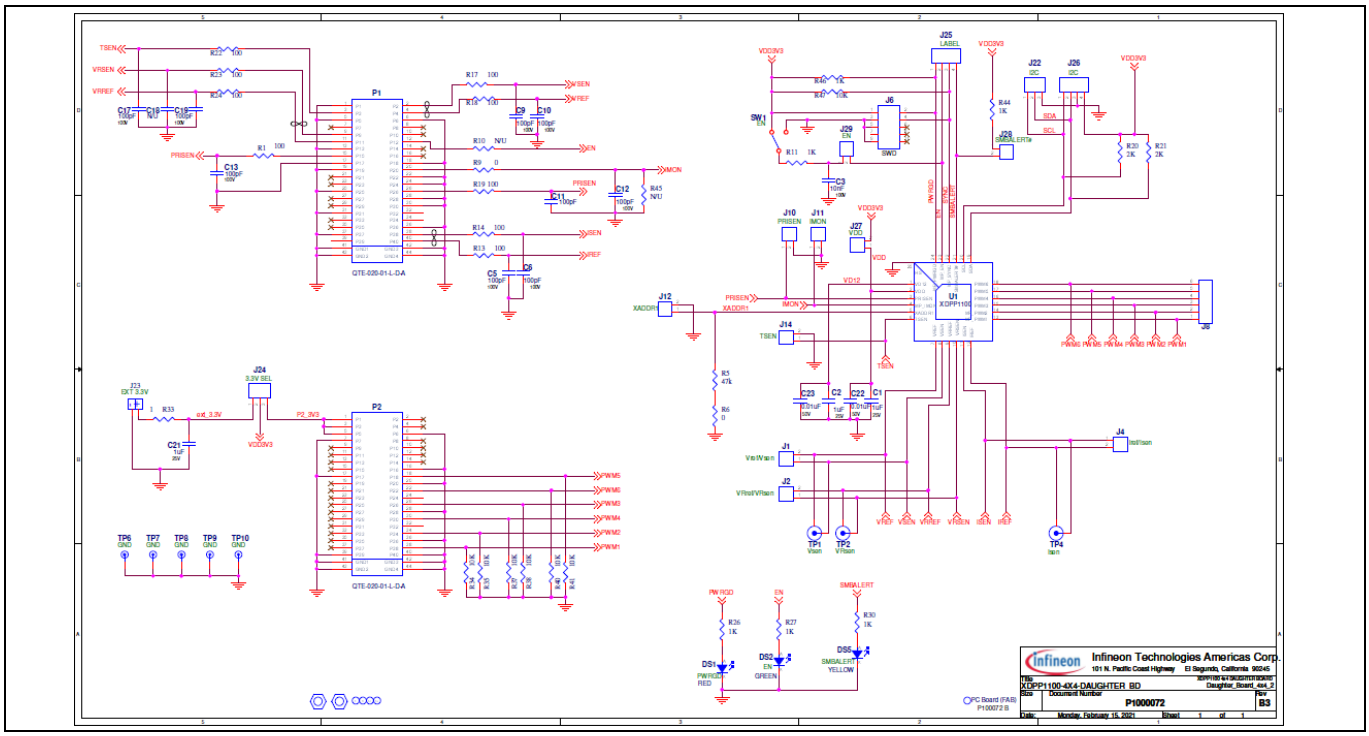


Figure 64 Daughterboard schematic

5.2 Bill of materials

Table 6 BOM for Power Board

Item	Qty.	Ref.	Manufacturer	Part number
1	1	BRD1	Shenzhen Tongyuexin Technology/ Krypton	P100110 A
2	8	C1, C2, C3, C4, C5, C6, C7, C8	TDK	C3225X7R2A225K230
3	13	C11, C12, C17, C19, C21, C29, C31, C43, C45, C69, C72, C74, C85	TDK	C1608X7R1H104K080
4	3	C13, C14, C15	Panasonic	EEU-FR1V331U
5	2	C22, C79	TDK	C1608X7R1H223K080
6	1	C23	TDK	C2012X5R1E106K125AB
7	1	C24	TDK	C3225C0G1H104J
8	1	C25	TDK	C1608C0G2A471K
9	2	C26, C65	TDK	C1608C0G2A472K
10	1	C27	Kemet	C1206C102JGR
11	6	C35, C36, C37, C38, C39, C40	TDK	CGA6P1X8L1C226M250AC
12	1	C41	TDK	C2012X7R1C475K125
13	3	C51, C75, C76	TDK	C1608X7R1E105M
14	1	C60	Samsung	CL21B106KOQNNNE
15	1	C61	Kemet	C0603C472K2RACTU
16	3	C62, C70, C77	TDK	C1608C0G2A102J
17	1	C80	TDK	C2012X7R1H105K085
18	2	C83, C84	TDK	C2012C0G2E472J

Item	Qty.	Ref.	Manufacturer	Part number
19	1	C86	TDK	C2012X7R1H104M085AA
20	1	D2	NXP	BAT46WJ,115
21	2	D4, D5	On	MBR2H100SFT3G
22	2	D6, D27	On	BAS20HT1G
23	1	D12	On Semi	MM5Z5V6T1G
24	1	D13	On Semi	MM5Z5V1T1G
25	4	D16, D22, D23, D24	NXP	BAS516,135
26	2	D25, D26	On	NRVTSAF5100ET3G
27	2	D28, D29	Diodes Inc.	DFLS1100Q-7
28	2	J1, J2	Samtec	QSE-020-01-L-D-A
29	1	L2	Würth	744355147
30	2	L3, L4	Taiyo Yuden	CBC3225T101KR
31	4	M1, M2, M3, M4	Keystone	8833
32	4	Q3, Q4, Q7, Q8	Infineon	BSC050N10NS5ATMA1
33	8	Q9, Q10, Q11, Q12, Q13, Q14, Q15, Q16	Infineon	BSC010N04LS6ATMA1
34	2	Q23, Q24	Toshiba	SSM3K15AMFV
35	2	RT1, RT2	Murata	NCP15WB473F03RC
36	3	R1, R65, R87	Panasonic	Not Used
37	1	R2	Panasonic	ERJ-3EKF5110V
38	1	R3	Panasonic	ERJ-8RQF1R5V
39	10	R4, R5, R7, R8, R11, R12, R13, R17, R94, R95	Panasonic	ERJ-3RQF1R0V
40	2	R6, R98	Panasonic	ERJ-3EKF1202V
41	1	R9	Panasonic	ERA-3AEB103V
42	1	R10	Panasonic	ERA-3AEB112V
43	3	R14, R50, R51	Panasonic	ERJ-3EKF3321V
44	1	R15	Panasonic	ERJ-3EKF2002V
45	5	R16, R63, R64, R90, R91	Panasonic	ERJ-3EKF1002V
46	3	R18,R89,R96	Panasonic	ERJ-3GEY0R00V
47	1	R23	Panasonic	ERJ-6ENF5110V
48	1	R36	Panasonic	ERJ-3EKF2213V
49	1	R37	Panasonic	ERJ-3EKF4871V
50	1	R47	Panasonic	ERJ-3EKF8871V
51	1	R48	Panasonic	ERJ-3EKF1371V
52	1	R57	Panasonic	ERJ-3EKF1243V
52	3	R66, R70, R86	Panasonic	ERJ-3EKF1000V
53	1	R69	Panasonic	ERJ-3EKF20R0V
54	1	R71	Panasonic	ERJ-6ENF1001V
55	1	R72	Panasonic	ERJ-6ENF1272V
56	1	R73	Panasonic	ERJ-3EKF51R1V
57	1	R74	Panasonic	ERA-3AEB104V
58	1	R75	Panasonic	ERA-3AEB132V
59	1	R85	Panasonic	ERJ-6ENF2002V
60	1	R97	Panasonic	ERJ-8ENF1500V
61	2	TP1, TP2	Cinch Connectors	129-0701-202
62	4	TP3, TP4, TP29, TP30	Keystone	575-4
63	26	TP5, TP6, TP7, TP8, TP9, TP10, TP11, TP12, TP13, TP14, TP15, TP16, TP17, TP18, TP19, TP20, TP21, TP22, TP23, TP24, TP25, TP26, TP27, TP28, TP31, TP32	Keystone	5020

Item	Qty.	Ref.	Manufacturer	Part number
64	1	T1	Ferroxcube	EQ25-3F36 and PLT25/18/2-3F36
65	1	T2	ICE	CT02-100
66	1	T3	Coilcraft	LPD5030V-224MR_B
67	2	U2, U3	Infineon	2EDL8124GXUMA1
68	2	U5, U7	Infineon	2EDL8024GXUMA1
69	1	U10	Texas Instruments	OPA140AIDBVT
70	1	U11	Texas Instruments	LM5018SD/NOPB
71	1	U16	Toshiba	TLP2161(TP,F)
72	1	U20	LT	LT1460KCS3-3.3#TRMPBF
73	1	U21	Fairchild	FODM8801A

Table 7 BOM for daughterboard

Item	Qty.	Ref.	Manufacturer	Part number
1	1	BRD1	Shenzhen Tongyuexin Technology/ Krypton	P100072 B
2	3	C1, C2, C21	TDK	C1608X7R1E105K
3	1	C3	TDK	C1608C0G2A103J080AC
4	9	C5, C6, C9, C10, C12, C13, C17, C18, C19	TDK	C1608C0G2A101K
5	1	C11	TDK	C1608C0G2A101K080AA
6	2	C22, C23	TDK	C1608X7R1H103K080
7	1	DS1	Würth	150060RS75000
8	1	DS2	Würth	150060GS75000
9	1	DS5	Würth	150060YS75000
10	10	J1, J2, J4, J10, J11, J12, J14, J27, J28, J29	Würth	613 002 111 21
11	1	J6	Samtec	FTSH-105-01-L-DV-007-K
12	1	J8	Würth	61300611121
13	2	J22, J24	Würth	613 003 111 21
14	1	J23	TE Connect	640456-2
15	2	J25, J26	Würth	613 004 111 21
16	2	M1, M2	Keystone	8833
17	2	P1, P2	Samtec	QTE-020-01-L-D-A
18	8	R1, R13, R14, R17, R18, R22, R23, R24	Panasonic	ERJ-6ENF1000V
19	1	R5	Panasonic	ERJ-6ENF4702V
20	3	R6, R9, R10	Panasonic	ERJ-6GEY0R00V
21	6	R11, R26, R27, R30, R44, R46	Panasonic	ERJ-6ENF1001V
22	1	R19	Panasonic	Not Used
23	2	R20, R21	Panasonic	ERJ-6ENF2001V
24	1	R33	Panasonic	ERJ-6RQF1R0V
25	7	R34, R35, R37, R38, R40, R41, R47	Panasonic	ERJ-6ENF1002V
26	1	R45	Panasonic	ERJ-6ENF3001V
27	1	SW1	C&K	GT11MCBE
28	3	TP1, TP2, TP4	Cinch Connectors	129-0701-202
29	5	TP6, TP7, TP8, TP9, TP10	Keystone	5020

Item	Qty.	Ref.	Manufacturer	Part number
30	1	U1	Infineon	XDPP1100-Q024

6 Nomenclature

Table 8 Definitions of acronyms, symbols, and terms

Symbol, acronym, or term	Definition
APC	Amperes per code
F_s	Sampling frequency (inverse of sampling period)
F_{sw}	Switching frequency (inverse of switching period)
FB	Full-bridge
FW	Firmware
GUI	Graphical user interface
N	Transformer turns ratio (N_p/N_s)
N_p	Number of turns of the transformer primary winding
N_s	Number of turns of the transformer secondary winding
OTP	One-time programmable memory
PCMC	Peak-current mode control
PWM	Pulse-width modulation
SR	Synchronous rectifier
VMC	Voltage-mode control

References

[1] Infineon Technologies AG: *XDPP1100 datasheet*; **Available online**

[2] Infineon Technologies AG: *XDPP1100 GUI installation guide*; **Available online**

[3] Infineon Technologies AG: *XDPP1100 technical reference manual*; **Available online**

[4] Infineon Technologies AG: *The XDPP1100 digital power supply controller*; **Available online**

[5] Infineon Technologies AG: *XDPP1100 PMBus command set*; **Available online**

[6] System Management Interface Forum, Inc.: *PMBus™ Power System Management Protocol Specification Part II – Command Language*; **Available online**

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