User manual for TDA38820 evaluation board

20 A single-phase buck regulator with 1.0 V output

About this document

Scope and purpose

The TDA38820 is a synchronous buck converter, providing a compact, high-performance and flexible solution in a small 4 mm x 5 mm power QFN package.

Key features offered by the TDA38820 include internal digital soft-start, precision 0.6 V reference voltage, power good, thermal protection, programmable switching frequency, enable input, input undervoltage lockout for proper start-up, latched off or unlatched overvoltage protection, and pre-bias start-up.

The output overcurrent protection (OCP) function is implemented by sensing the voltage developed across the on-resistance of the synchronous MOSFET for optimum cost and performance, and the current limit is thermally compensated.

This user manual contains the schematic and bill of materials (BOM) for the EV119-001 engineering evaluation board. The manual describes operation and use of the evaluation board itself. Detailed application information for TDA38820 is available in the TDA38820 datasheet.

Intended audience

This document is intended as a guide for design engineers who are evaluating TDA38820 performance with the engineering of EV119-001 demo board.

Table of contents

1 Board information

1.1 Board features

V_{in} = +12 V, V_{out} = +1 V at 0 to 20 A

F_s = 600 kHz/800 kHz/1000 kHz

L = 215 nH (10.4 mm x 8.0 mm x 7.5 mm, DCR = 0.29 mΩ)

C_{in} = 10 x 22 µF (25 V, ceramic 0805) + 1 x 330 µF (25 V, electrolytic, optional)

C_{out} = 9 x 47 µF (6.3 V, ceramic 0805) + 1 x 470 µF (2 V, 6 mΩ, SP-cap)

1.2 Connections and operating instructions

The TDA38820 demo board requires a single +12 V for the input power and can deliver up to 20 A load current. The operation modes and OCP limits can be selected through jumpers.

Table 1 Connections

Label		Descriptions
Input	PV_{in}	Connect input power (+12 V) to this pin
	GND	Return of input power
	PV_{in}, GND	Sense pins for the input voltage
Output	V_{out}	V_{out} (+1 V), connect a load (20 A max.) to this pin
	GND	Return of V_{out}
	V_{out}, GND	Sense pins for the output voltage
Enable	Enable, GND	Connect a scope probe to this pin to monitor enable signal Or, an external enable signal can be applied to this pin to over-drive the on-board enable signal
Bode	A, B	For bode plot measurement
SS/Latch	OVP latch	Use a jumper to select one of four soft-start time selections (1 ms, 2 ms, 4 ms and 8 ms), and latched OVP or unlatched OVP
	OVP no latch	
Internal LDO or External VCC	PV_{in}, V_{in}, VCC	To use the internal LDO, connect PV_{in} and V_{in} with a jumper. To use an external VCC voltage, connect V_{in} and VCC with a jumper.
	VCC, GND	When using the internal LDO, connect a scope probe to this pin to monitor the output of the internal LDO. When using using an external VCC voltage, apply +5 V between VCC and GND.
Ton/Mode	FCCM	Use a jumper to select FCCM or DEM, and switching frequency. The available switching frequencies are: 600 kHz, 800 kHz, 1000 kHz and 1200 kHz
	DEM	
ILIM		Use a jumper to select one of four OCP limits. OCP 1 is the lowest OCP limit and OCP4 is the highest OCP limit.
P_{Good}	P_{Good}, GND	Connect a scope probe to this pin to monitor power good signal
	EPGb	External P_{Good} pull-up bias pin. P_{Good} pin is pulled up to V_{CC} through R4 on the standard demo board. By removing R4 and populating R42 with 49.9 kΩ, an external P_{Good} pull-up bias can be applied to the EPGb pin.

1.3 Layout

The PCB is a six-layer board (3.0 in. x 3.75 in.) using FR4 material. Top and bottom layers use 1.5 oz. copper and inner layers use 2 oz. copper. The PCB thickness is 0.062 in. The TDA38820 and other major power components are mounted on the top side of the board.

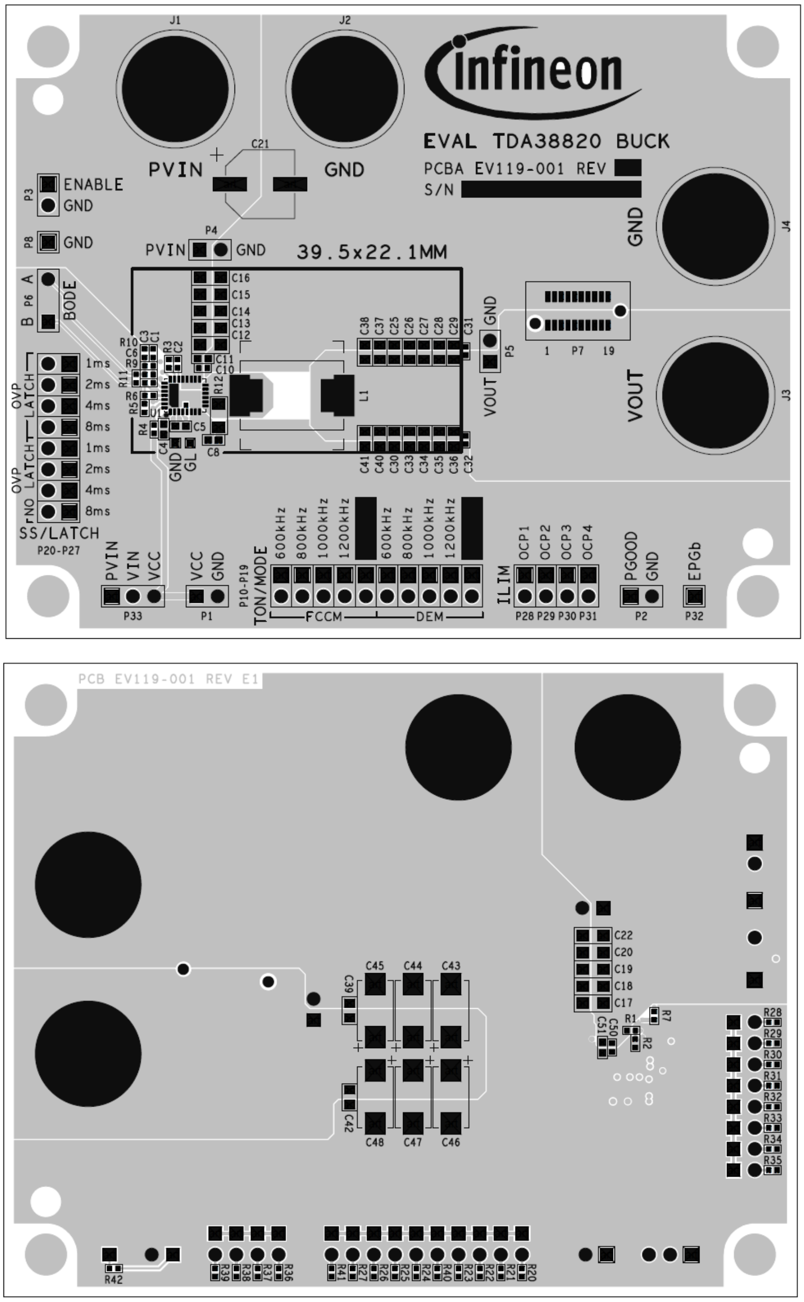

Figure 1 Top and bottom view of TDA38820 evaluation board

1.4 PCB layout

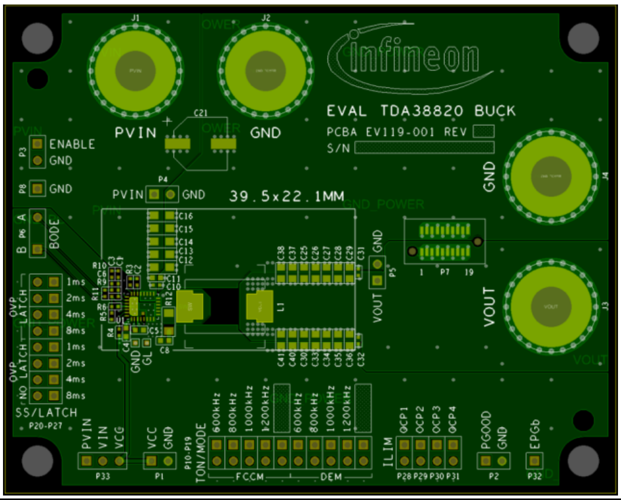

Figure 2 Top layer

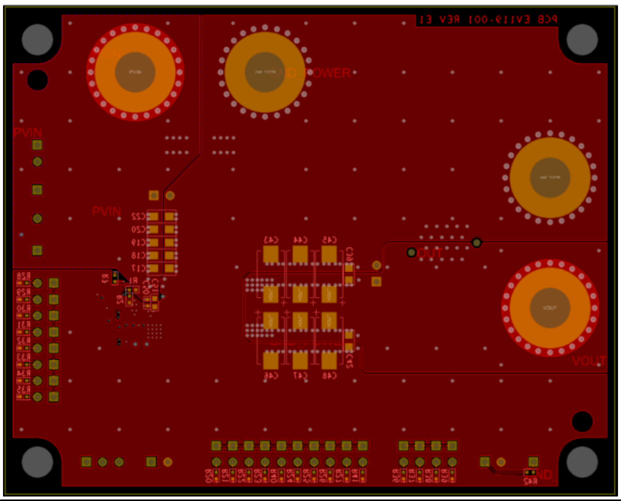

Figure 3 Bottom layer

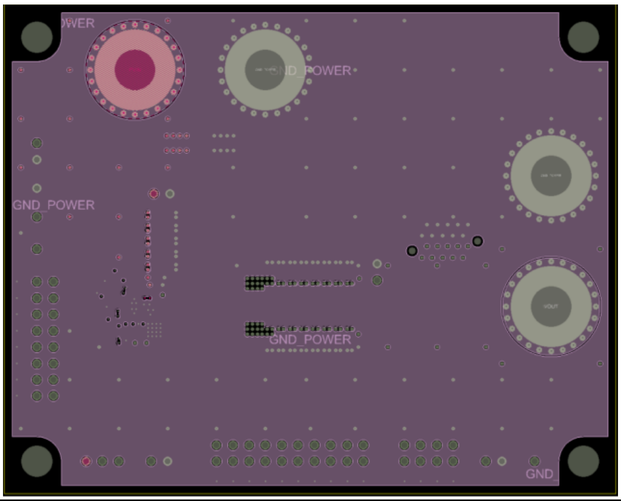

Figure 4 Mid layer 1

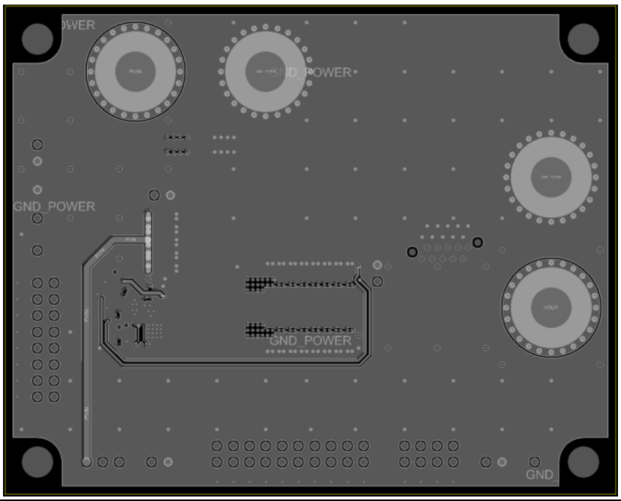

Figure 5 Mid layer 2

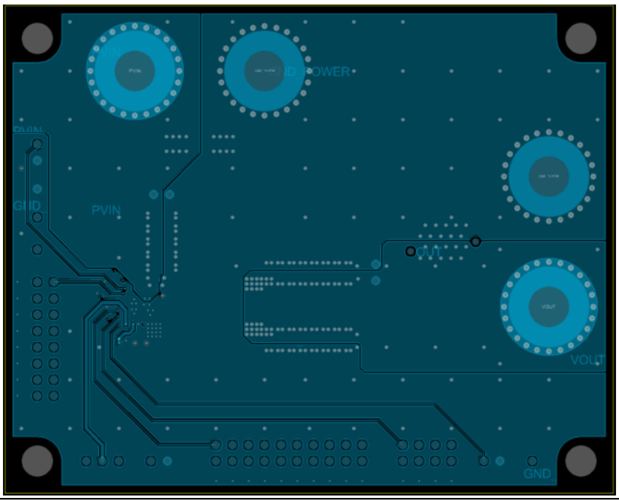

Figure 6 Mid layer 3

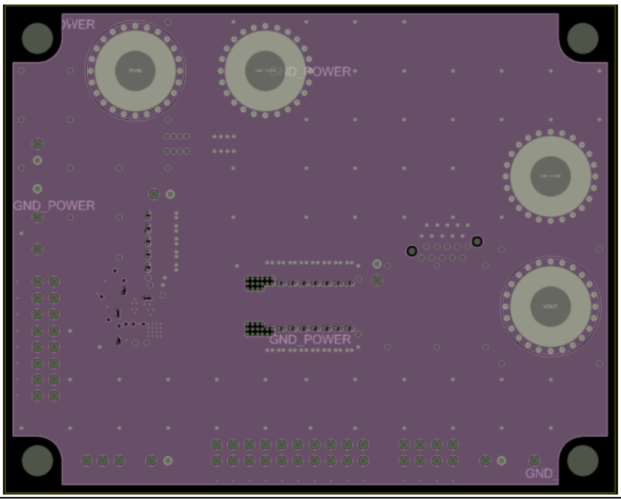

Figure 7 Mid layer 4

1.5 Schematic

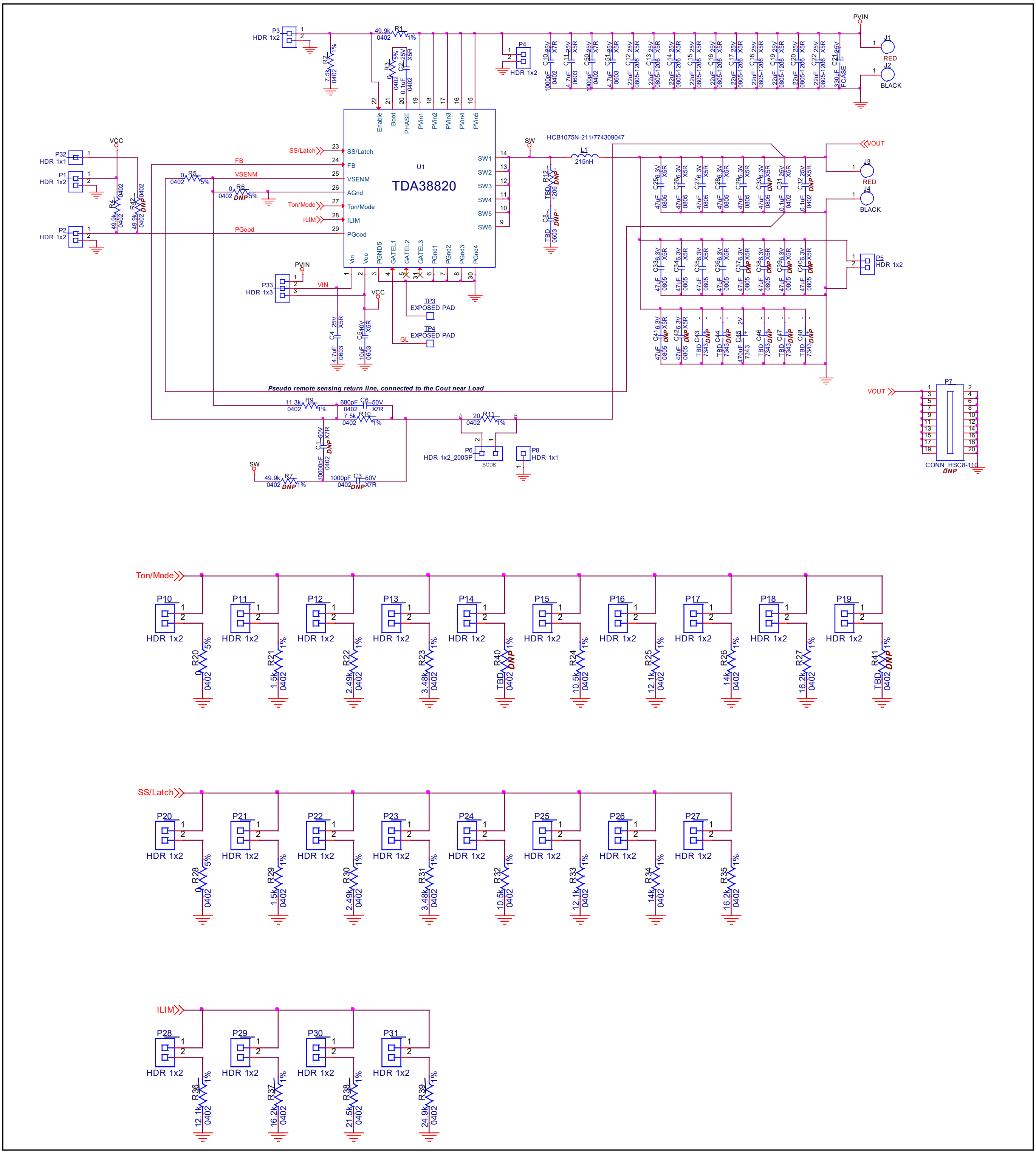

Figure 8 **Schematic of the TDA38820 evaluation board V_{in} = 12 V, V_{out} = 1 V, I_{outmax} = 20 A, fsw = 600 kHz/800 kHz/1000 kHz. See Note 1**

Note 1: The inductor selection here does not consider overcurrent protection (OCP) limit requirement. Please refer to the sections 9.8 and 10.4 in the **TDA38820 datasheet** for the guideline of inductor selection for a desired OCP limit.

1.6 Bill of Materials (BOM)

Table 2 Bill of materialss

Item	Qty.	Reference	Value	Manufacturer	Manufacturer part no.	Description
1	2	C10,C50	1000 pF	Kemet	C0402C102K3RAC TU	Ceramic capacitor 1000 pF 25V 10% X7R 0402
2	10	C12,C13,C14,C15 C16,C17,C18,C19 C20,C22	22 µF	Murata	GRM21BR61E226 ME44L	Ceramic capacitor 22 µF 25V 20% X5R 0805
3	2	C2,C31	0.1 µF	Taiyo Yuden	TMK105BJ104KV-F	Ceramic capacitor 0.1 µF 25V 10% X5R 0402
4	1	C21	330 µF	Panasonic	EEE-FK1E331P	CAP ALUM 330 µF 20% 25V SMD
5	9	C25,C26,C27,C28 C29,C33,C34,C35 C36	47 µF	Murata	GRM21BR60J476M E11	Ceramic capacitor 47 µF 6.3V 20% X5R 0805
6	3	C4,C11,C51	4.7 µF	Murata	GRM188R61E475K E15D	Ceramic capacitor 4.7 µF 25V 10% X5R 0603
7	1	C5	10 µF	Murata	GRM188R61A106K E69D	Ceramic capacitor 10 µF 10V 10% X5R 0603
8	1	C45	470 µF	Panasonic	EEF-SX0D471XE	CAP ALUM POLY 470 µF 20% 2V SM
9	1	C6	680 pF	Yageo	CC0402KRX7R9BB 681	Ceramic capacitor 680 pF 50V 10% X7R 0402
10	1	L1	215 nH	Delta	HCB1075N-211	Inductor 215 nH, 48 A, 0.29 mΩ 10.4 x 8.0 x 7.5 mm, SMD
11	2	R1,R4	49.9 k	Panasonic	ERJ-2RKF4992X	Resistor 49.9 kΩ 1/10W 1% 0402 SMD
12	1	R11	20	Vishay Dale	CRCW040220R0FK ED	Resistor 20.0 Ω 1/16W 1% 0402 SMD
13	2	R2,R10	7.5 k	Panasonic	ERJ-2RKF7501X	Resistor 7.50 kΩ 1/10W 1% 0402 SMD
14	2	R21,R29	1.5 k	Rohm	MCR01MZPF1501	Resistor 1.50 kΩ 1/16W 1% 0402 SMD
15	2	R22,R30	2.49 k	Vishay Dale	CRCW04022K49FK ED	Resistor 2.49 kΩ 1/16W 1% 0402 SMD
16	2	R23,R31	3.48 k	Vishay Dale	CRCW04023K48FK ED	Resistor 3.48 kΩ 1/16W 1% 0402 SMD
17	2	R24,R32	10.5 k	Panasonic	ERJ-2RKF1052X	Resistor 10.5 kΩ 1/10W 1% 0402 SMD
18	3	R25,R33,R36	12.1 k	Panasonic	ERJ-2RKF1212X	Resistor 12.1 kΩ 1/10W 1% 0402 SMD
19	2	R26,R34	14 k	Panasonic	ERJ-2RKF1402X	Resistor 14.0 kΩ 1/10W

						1% 0402 SMD
20	3	R27,R35,R37	16.2 k	Panasonic	ERJ-2RKF1622X	Resistor 16.2 kΩ 1/10W 1% 0402 SMD
21	4	R3,R5,R20,R28	0	Panasonic	ERJ-2GE0R00X	Resistor 0.0 Ω 1/10W 0402 SMD
22	1	R38	21.5 k	Panasonic	ERJ-2RKF2152X	Resistor 21.5 kΩ 1/10W 1% 0402 SMD
23	1	R39	24.9 k	Panasonic	ERJ-2RKF2492X	Resistor 24.9 kΩ 1/10W 1% 0402 SMD
24	1	R9	11.3 k	Panasonic	ERJ-2RKF1132X	Resistor 11.3 kΩ 1/10W 1% 0402 SMD
25	1	U1	TDA38820	Infineon	TDA38820	20 A Single input voltage, synchronous buck regulator

2 Typical operating waveforms

V_{in} = 12.0 V, V_{out} = 1 V, I_{out} = 0 to 20 A, room temperature, no airflow.

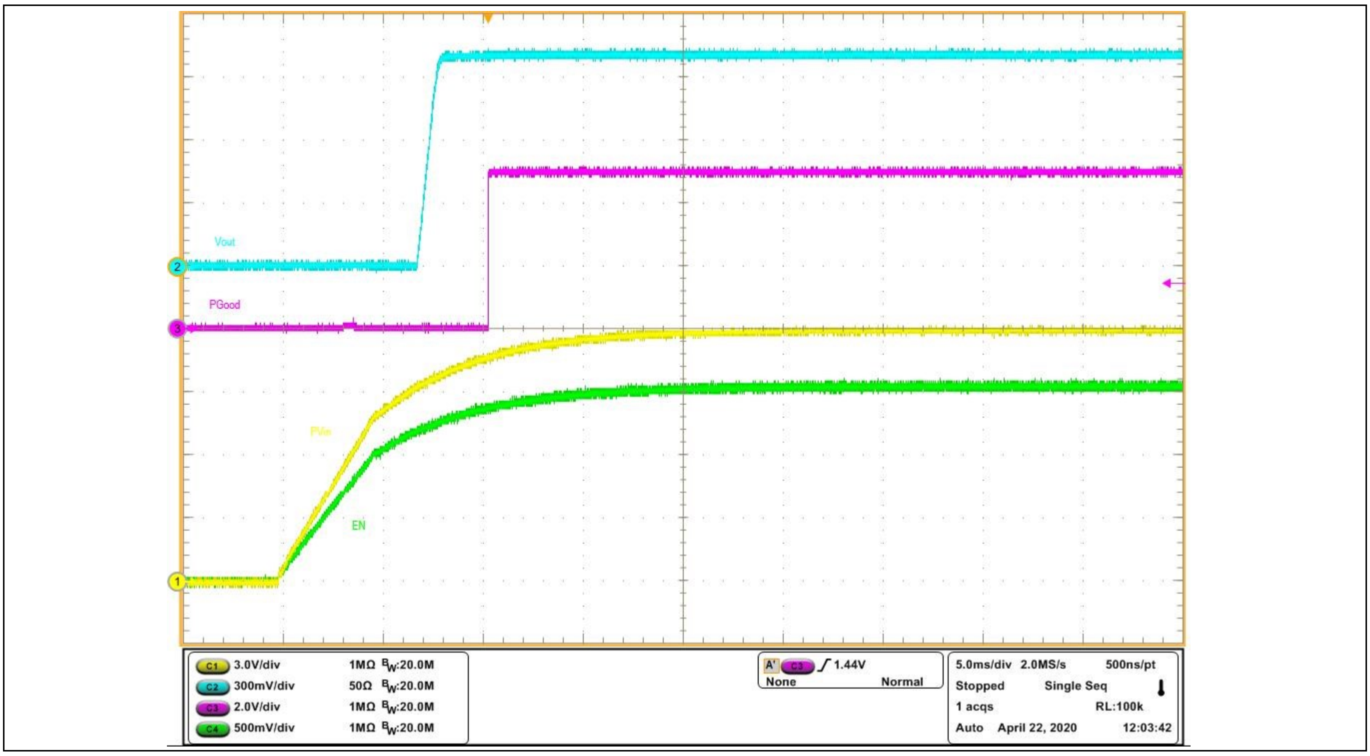

Figure 9 **Start-up at 20 A load (Ch_1: PV_{in}, Ch_2: V_{out}, Ch_3: P_{Good}, Ch_4: Enable)**

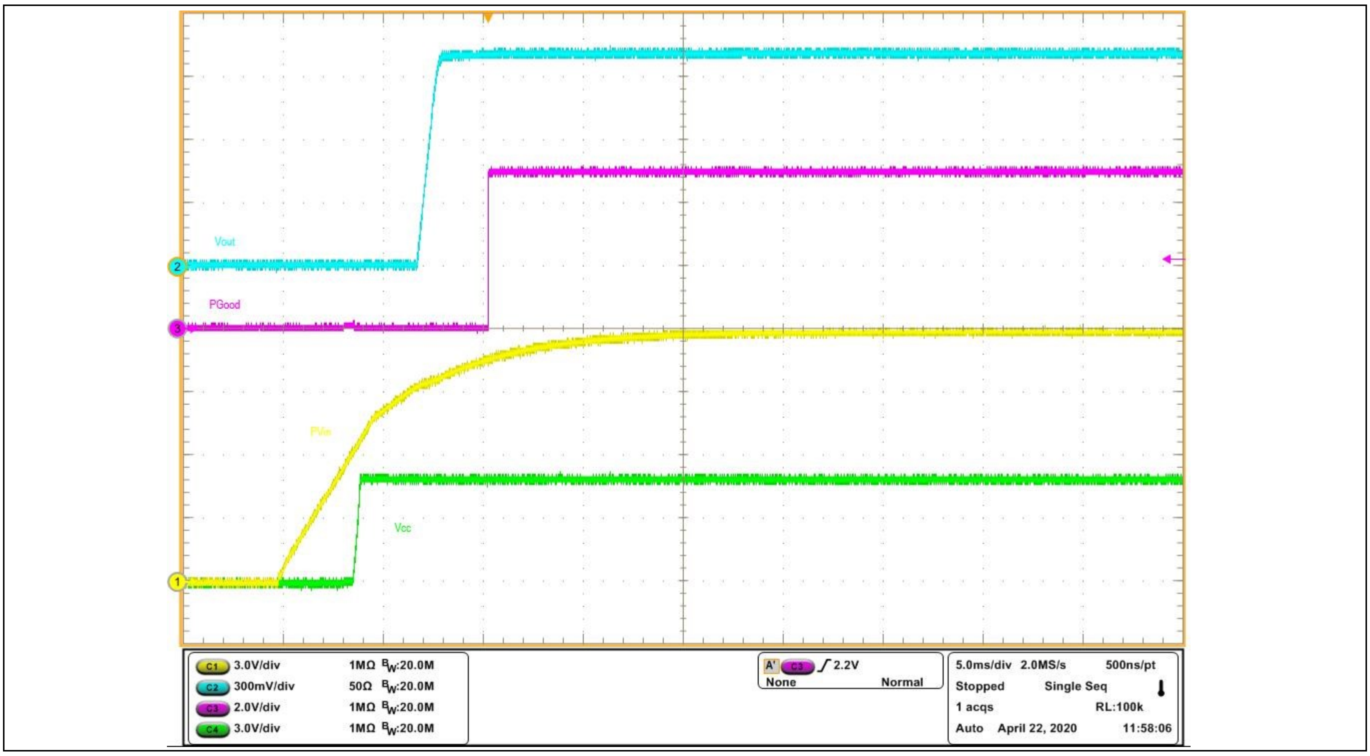

Figure 10 **Start-up at 20 A load (Ch_1: PV_{in}, Ch_2: V_{out}, Ch_3: P_{Good}, Ch_4: V_{cc})**

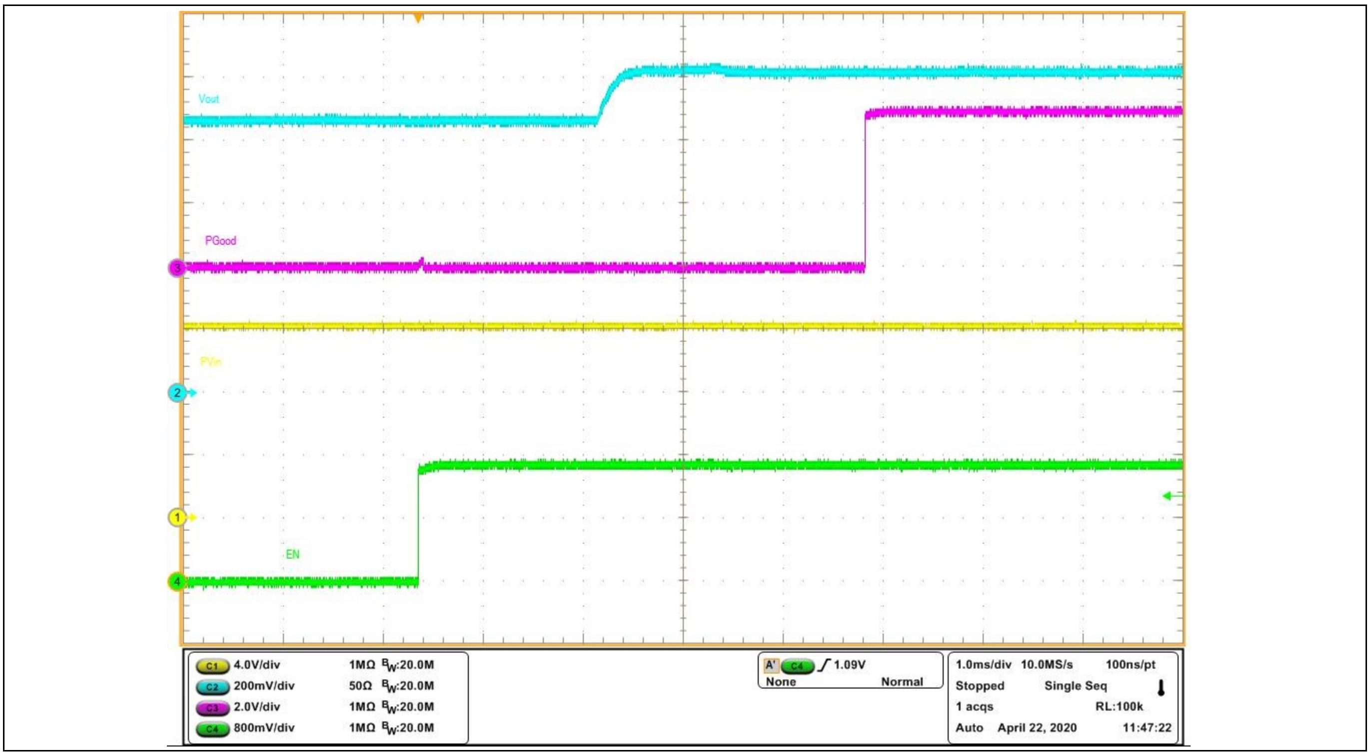

Figure 11 Pre-bias start-up at 0 A load (Ch_1: PV_{in}, Ch_2: V_{out}, Ch_3: P_{Good}, Ch_4: Enable)

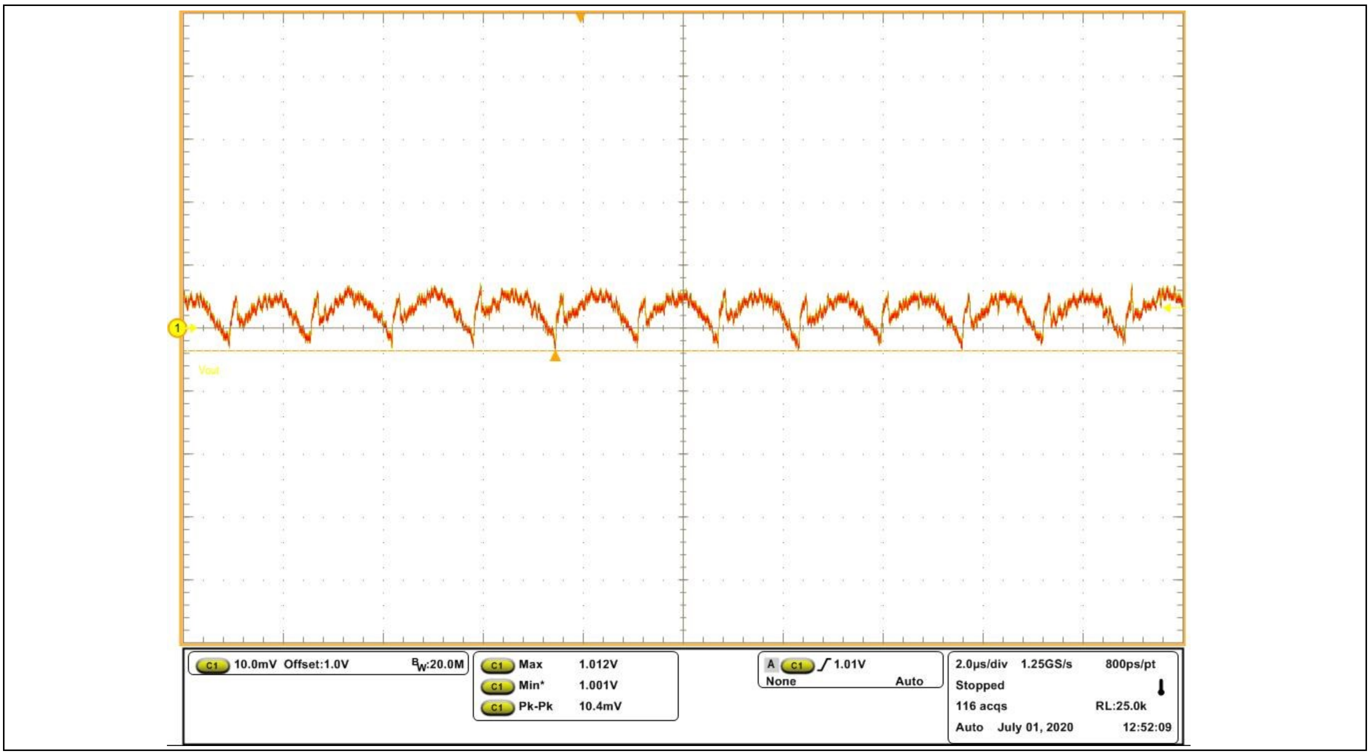

Figure 12 V_{out} ripple at 20 A load, fsw = 600 kHz (Ch_1: V_{out})

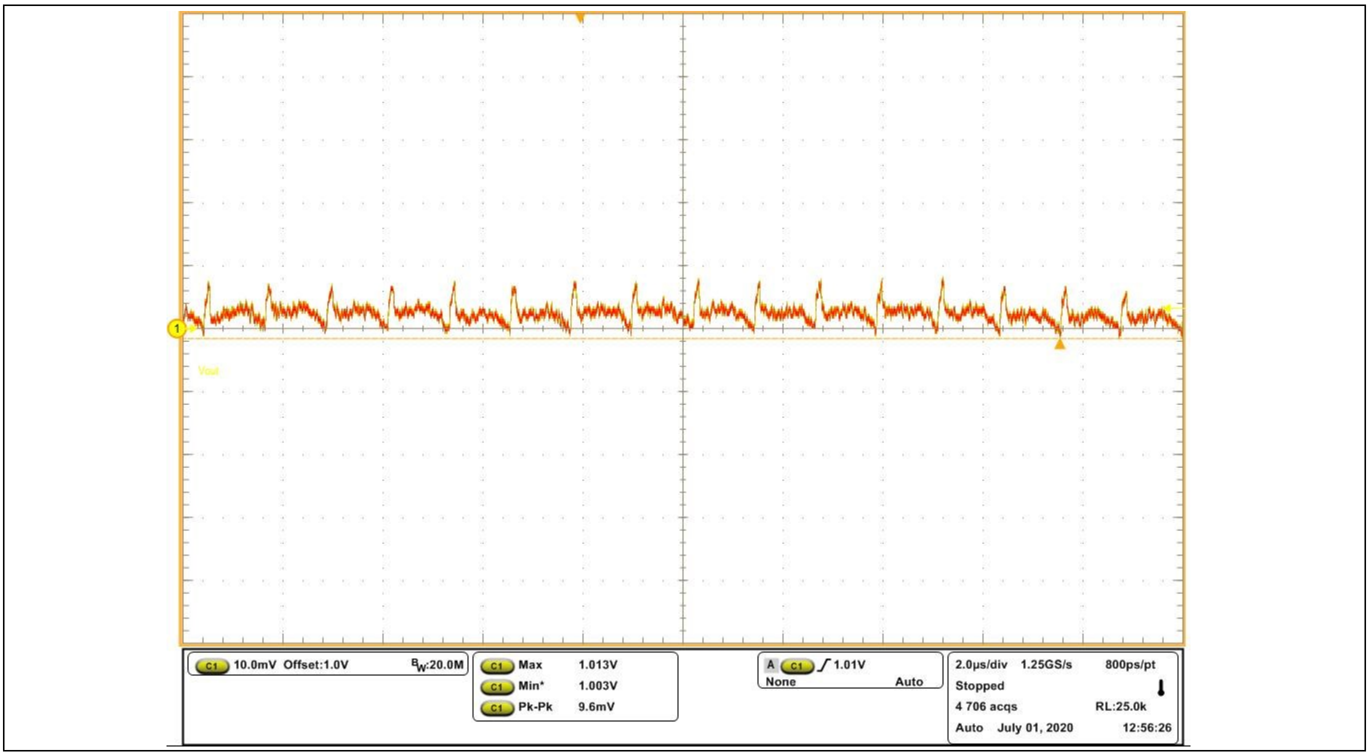

Figure 13 V_{out} ripple at 20 A load, fsw = 800 kHz (Ch_1: V_{out})

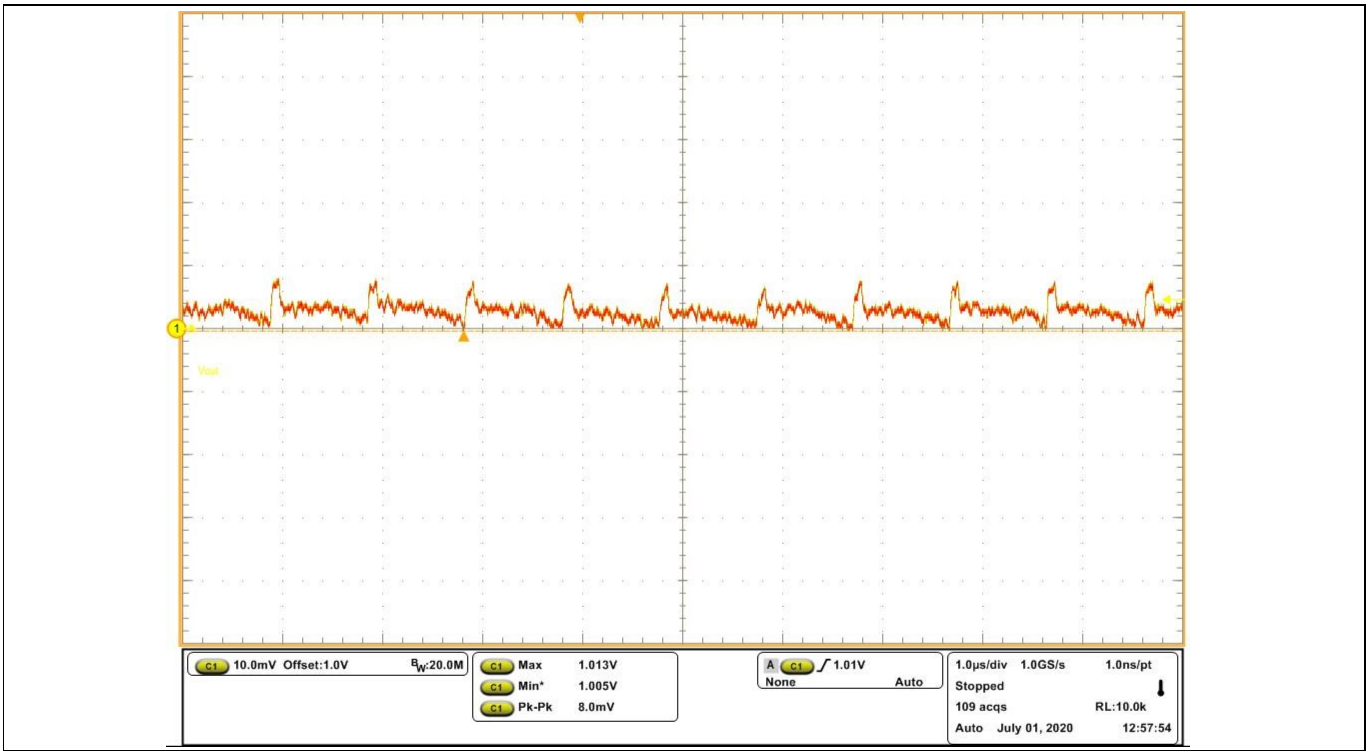

Figure 14 V_{out} ripple at 20 A load, fsw = 1000 kHz (Ch_1: V_{out})

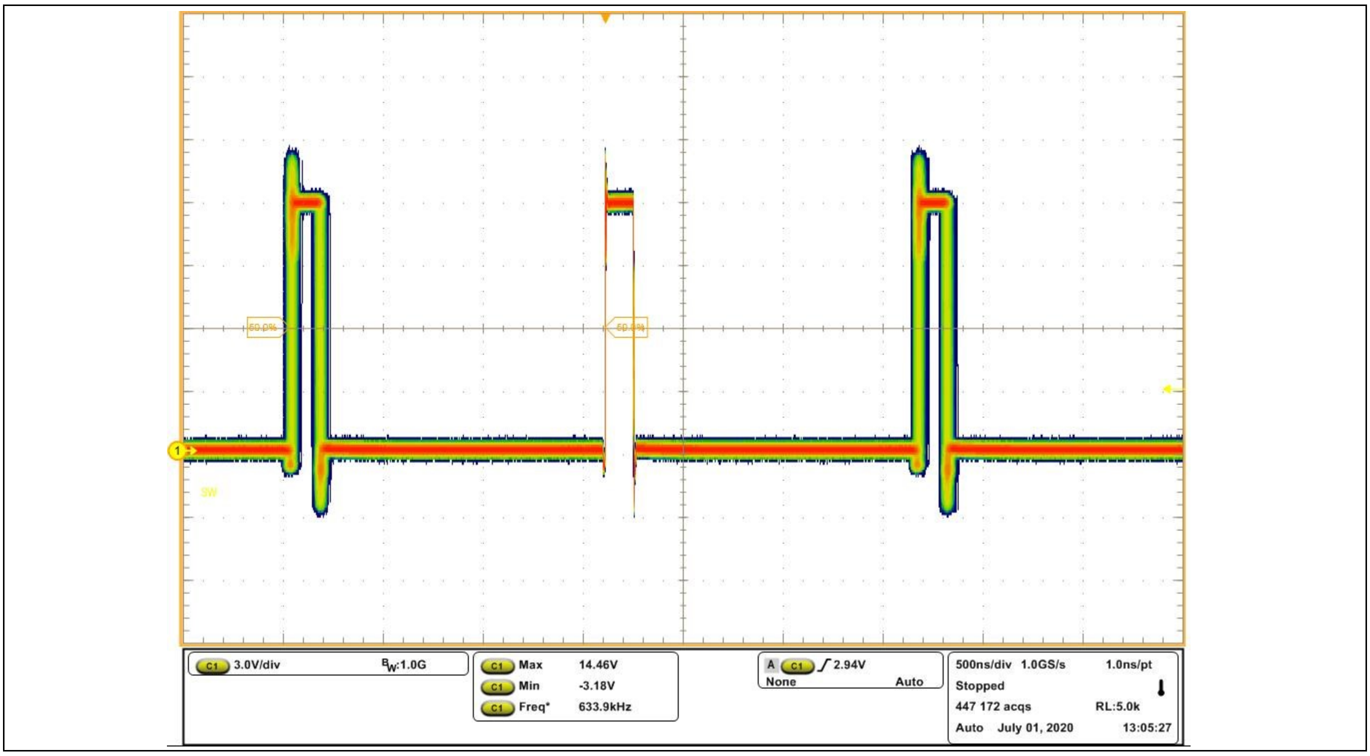

Figure 15 SW node, 20 A load, fsw = 600 kHz

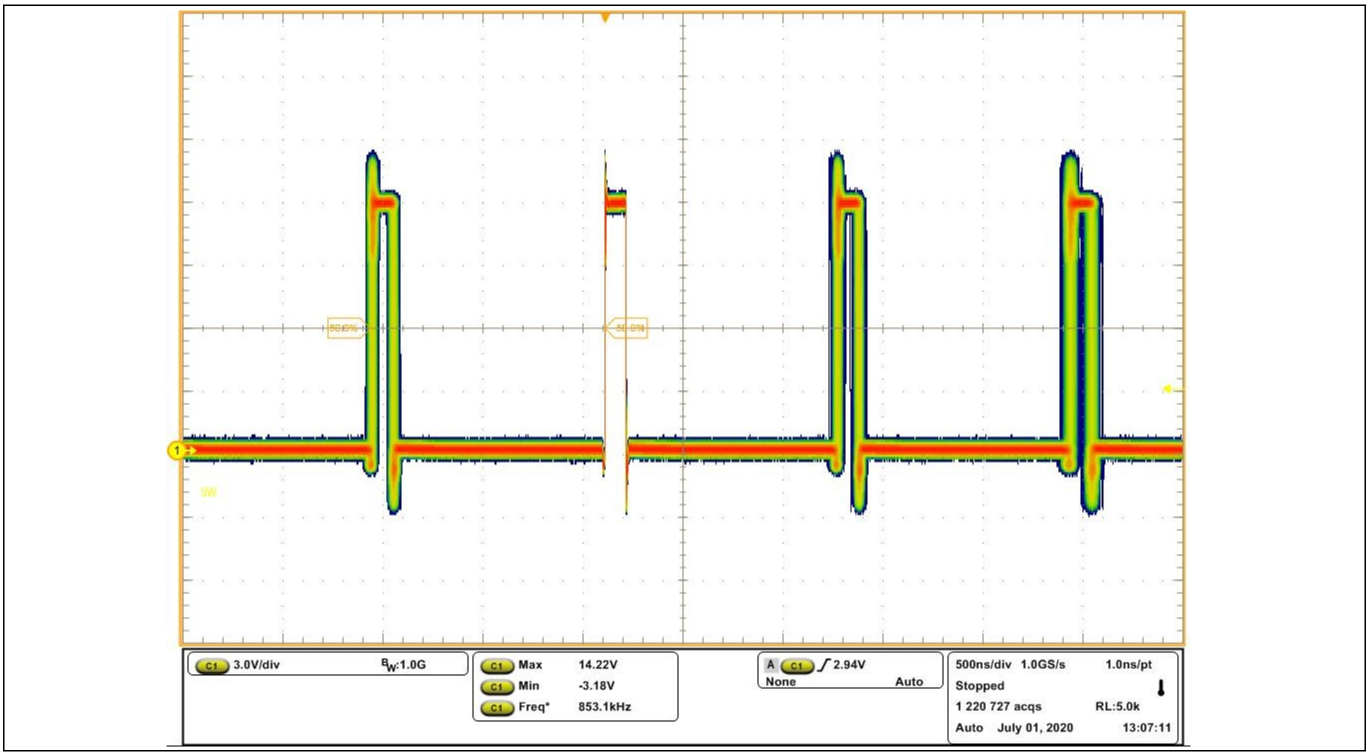

Figure 16 SW node, 20 A load, fsw = 800 kHz

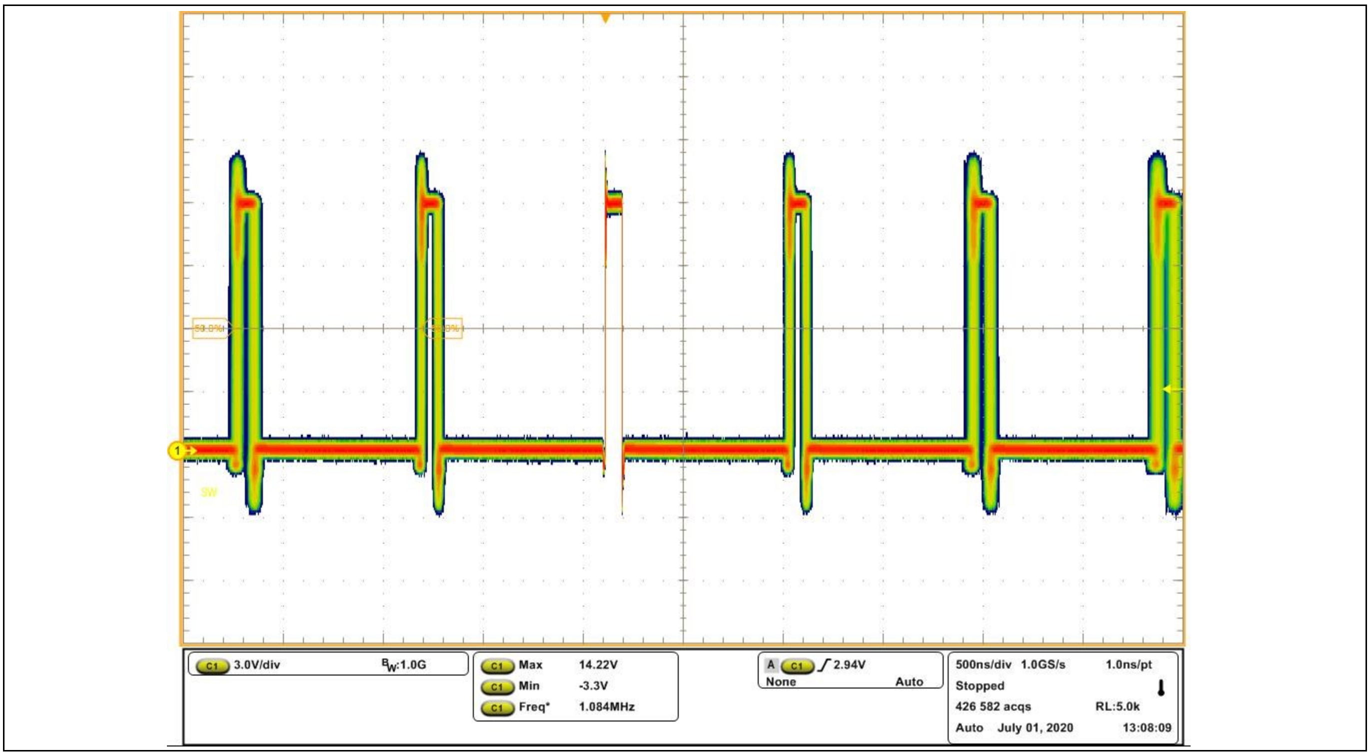

Figure 17 SW node, 20 A load, fsw = 1000 kHz

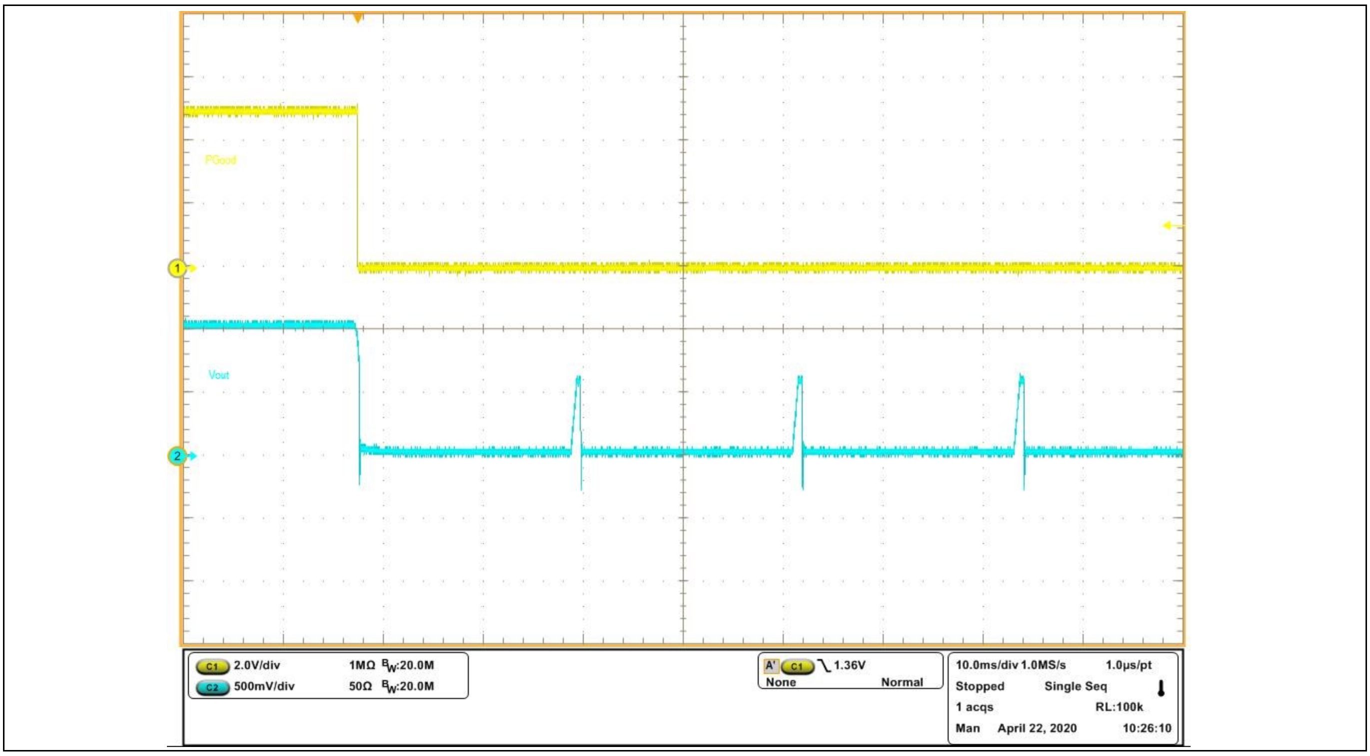

Figure 18 Short-circuit and UVP (hiccup), (Ch_2: V_o, Ch_1: P_{Good})

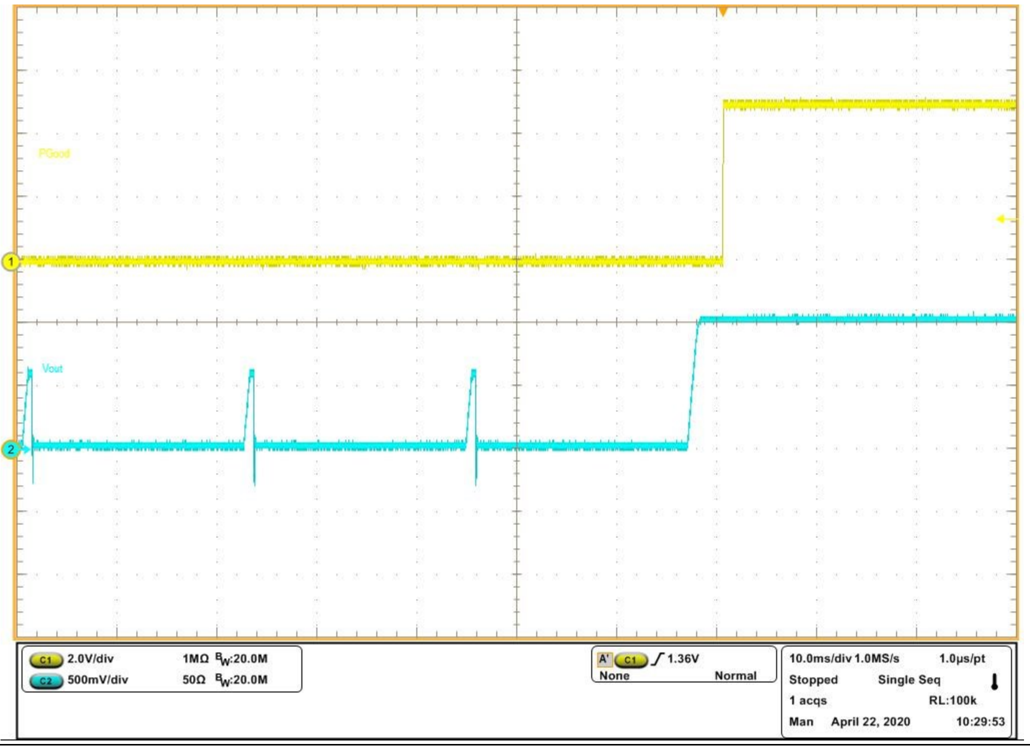

Figure 19 Short-circuit and UVP (hiccup) recover (Ch_2: V_{out}, Ch_1: P_{Good})

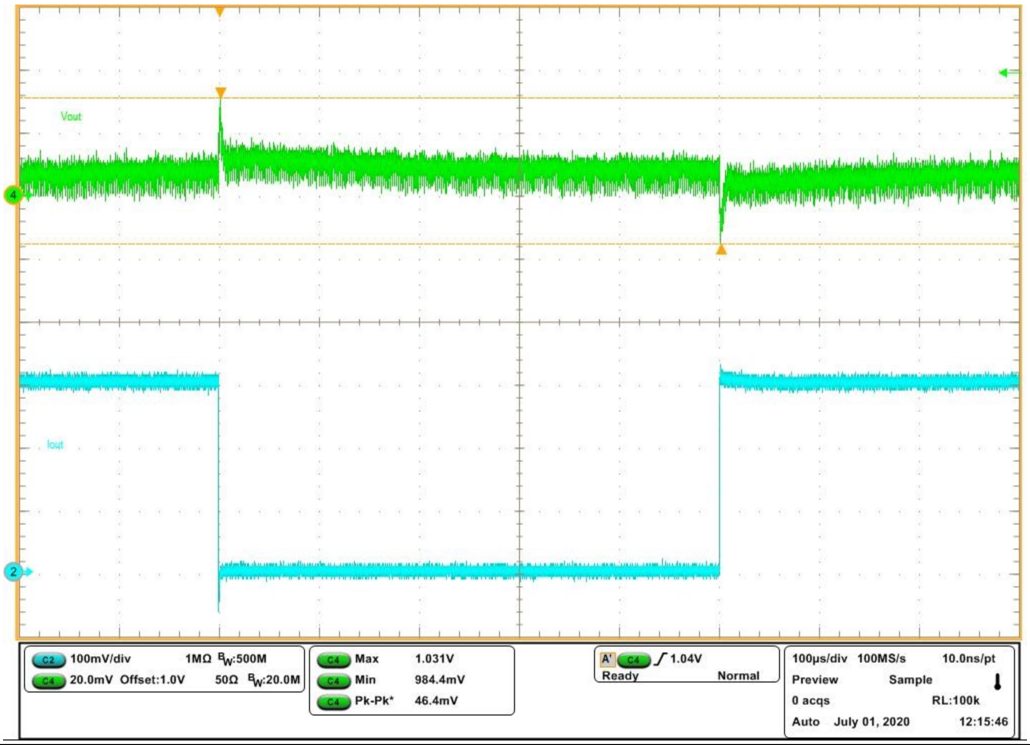

Figure 20 Transient response at 6 A step load current at 30 A/µs slew rate: I_{out} = 0 to 6 A (Ch_4: V_{out}, Ch_2: I_{out}, 50 mV/A) pk-pk: 46.4 mV, fsw = 600 kHz

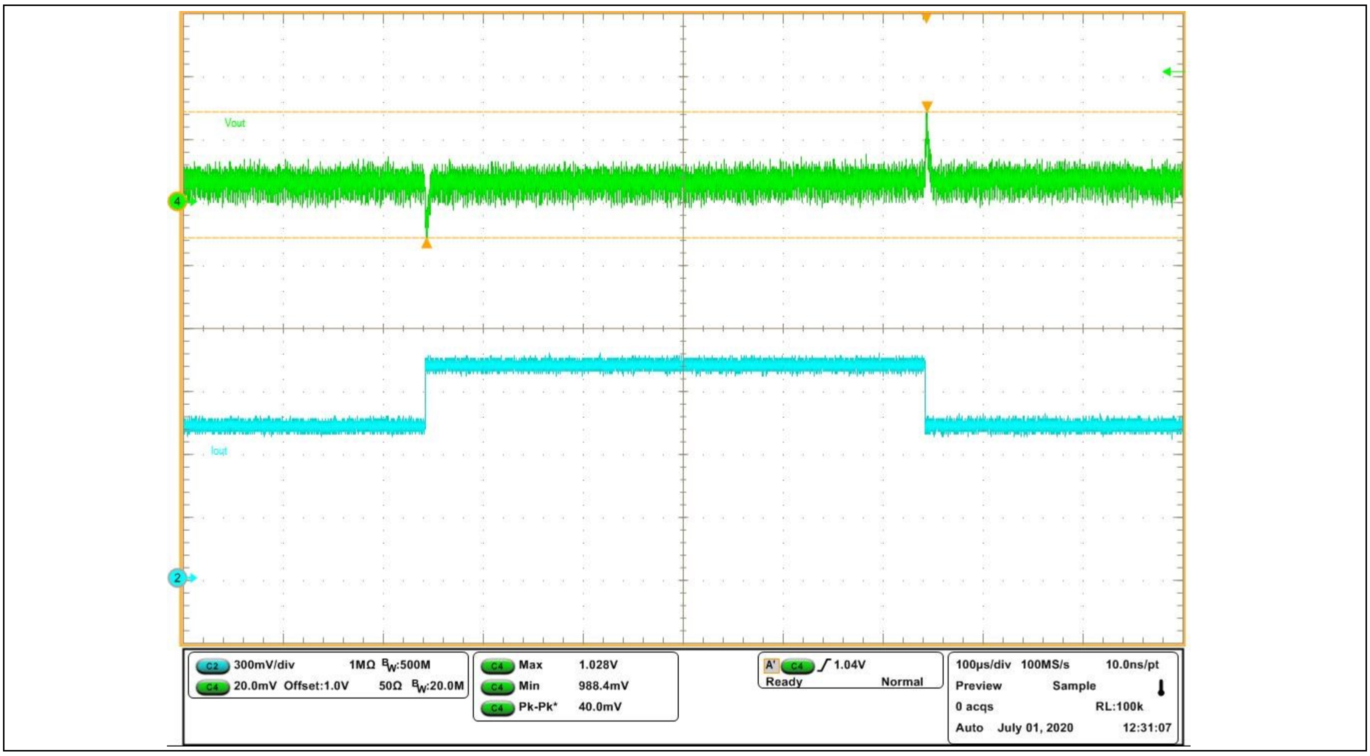

Figure 21 **Transient response at 6 A step load current at 30 A/µs slew rate: I_{out} = 14 to 20 A (Ch_4: V_{out}, Ch_2: I_{out}, 50 mV/A), pk-pk: 40 mV, fsw = 600 kHz**

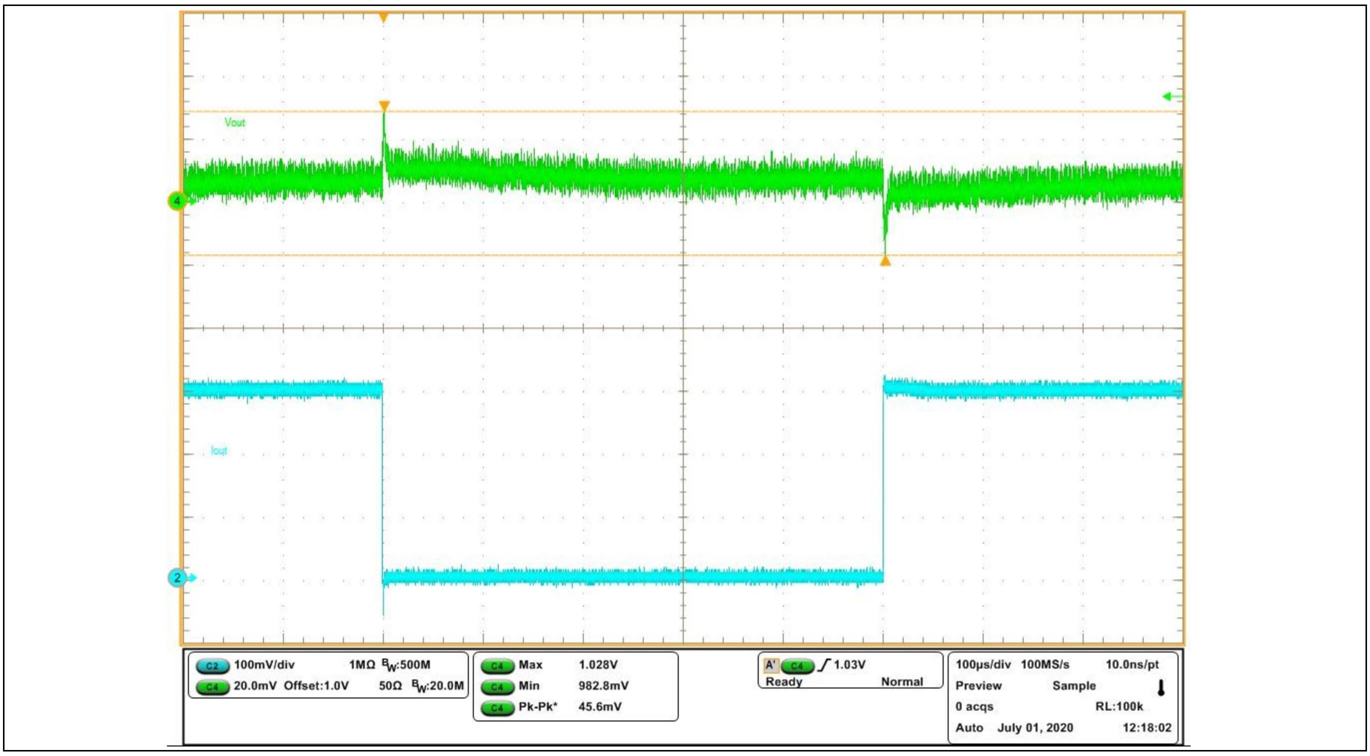

Figure 22 **Transient response at 6 A step load current at 30 A/µs slew rate: I_{out} = 0 to 6 A (Ch_4: V_{out}, Ch_2: I_{out}, 50 mV/A) pk-pk: 45.6 mV, fsw = 800 kHz**

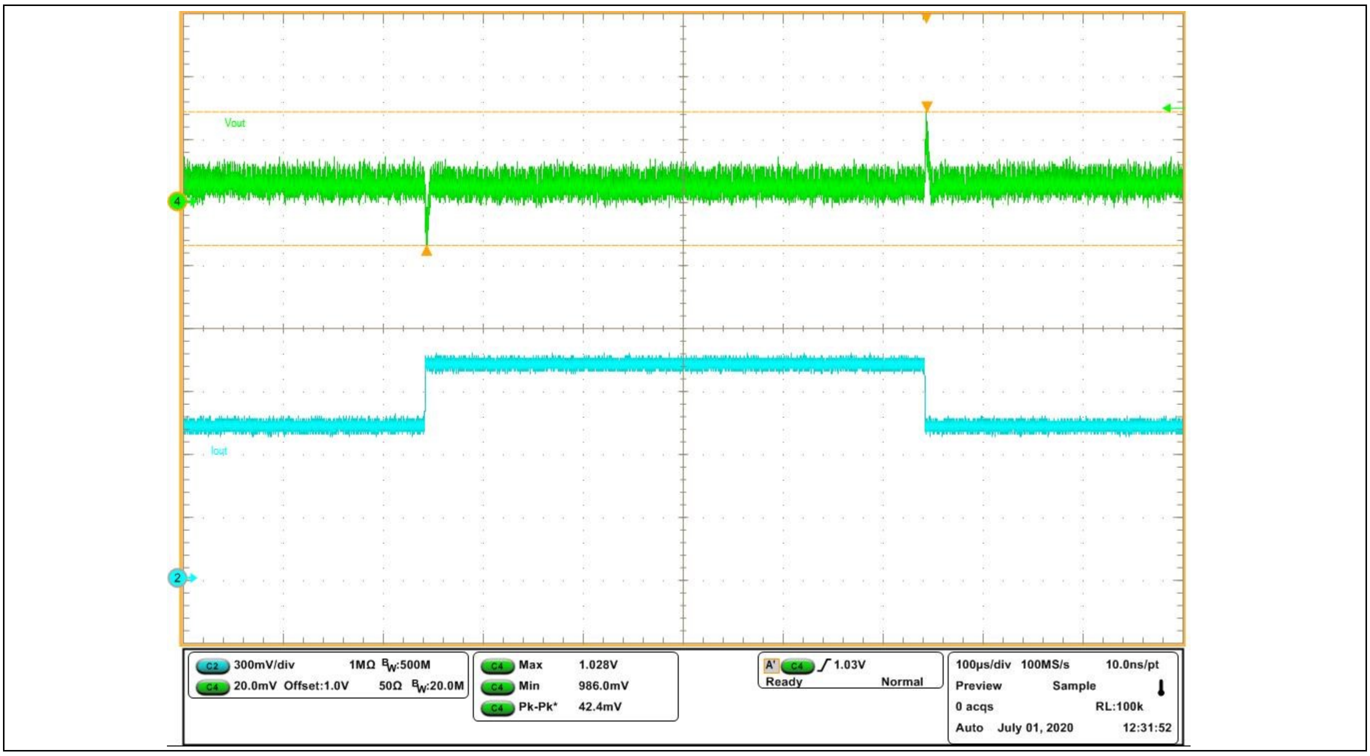

Figure 23 **Transient response at 6 A step load current at 30 A/µs slew rate: I_{out} = 14 to 20 A (Ch_4: V_{out}, Ch_2: I_{out}, 50 mV/A), pk-pk: 42.4 mV, fsw = 800 kHz**

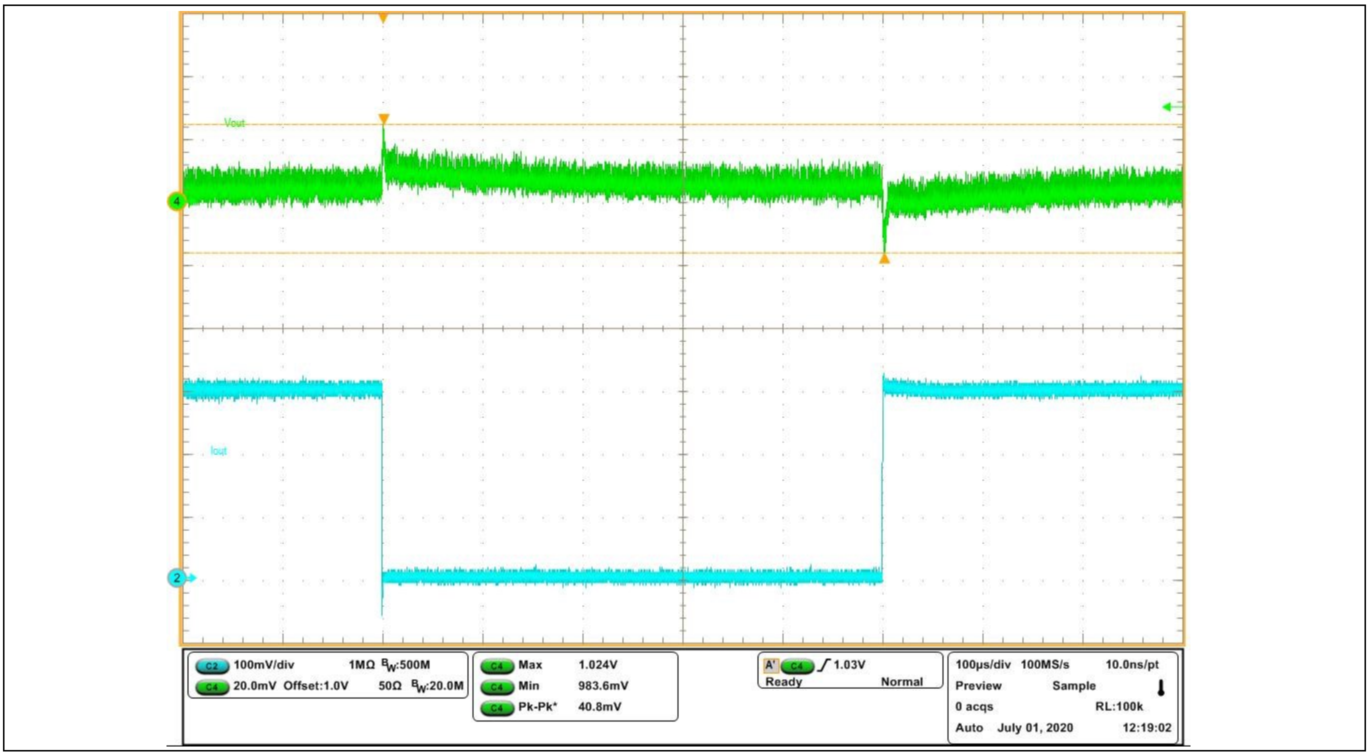

Figure 24 **Transient response at 6 A step load current at 30 A/µs slew rate: I_{out} = 0 to 6 A (Ch_4: V_{out}, Ch_2: I_{out}, 50 mV/A) pk-pk: 40.8 mV, fsw = 1000 kHz**

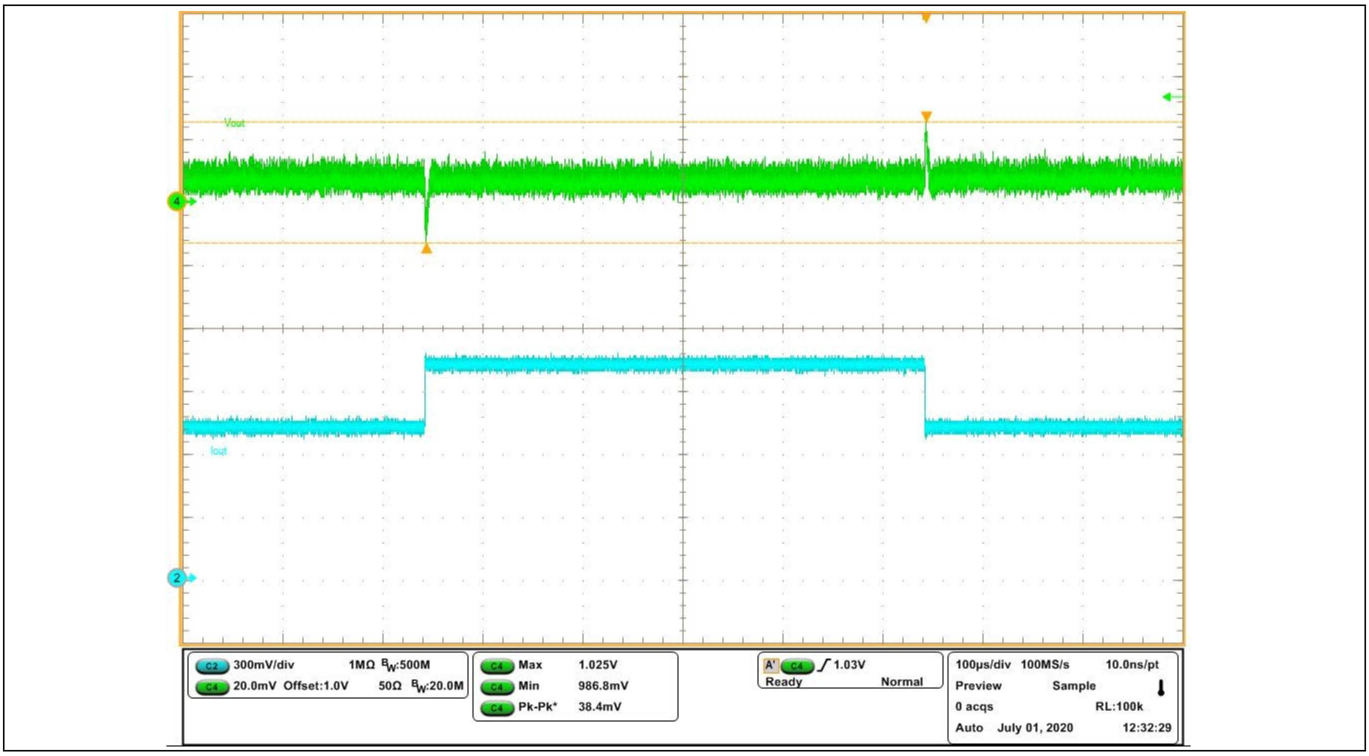

Figure 25 Transient response at 6 A step load current at 30 A/µs slew rate: I_{out} = 14 to 20 A (Ch_4: V_{out}, Ch_2: I_{out}, 50 mV/A) pk-pk: 38.4 mV, fsw = 1000 kHz

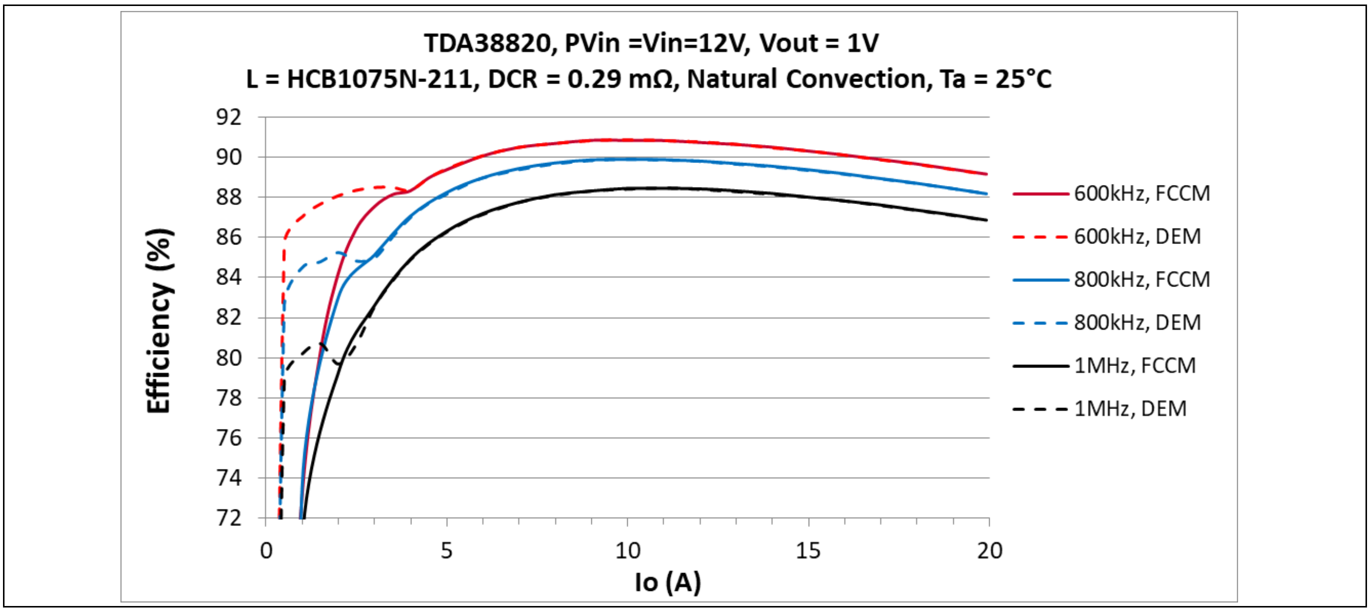

Figure 26 Efficiency with natural convection (12 V_{in}, 1 V_{out}, 215 nH, 600 kHz, 800 kHz and 1000 kHz, T_a = 25°C)

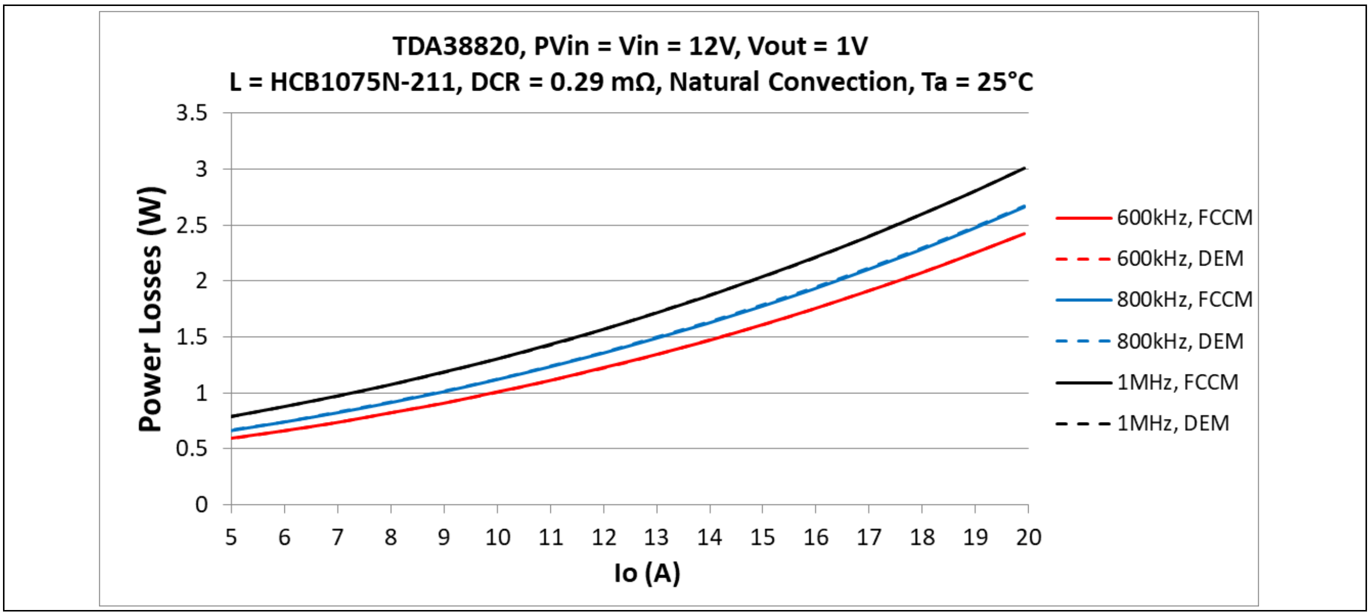

Figure 27 **Power loss with natural convection (12 V_{in}, 1 V_{out}, 215 nH, 600 kHz, 800 kHz and 1000 kHz, T_a = 25°C)**

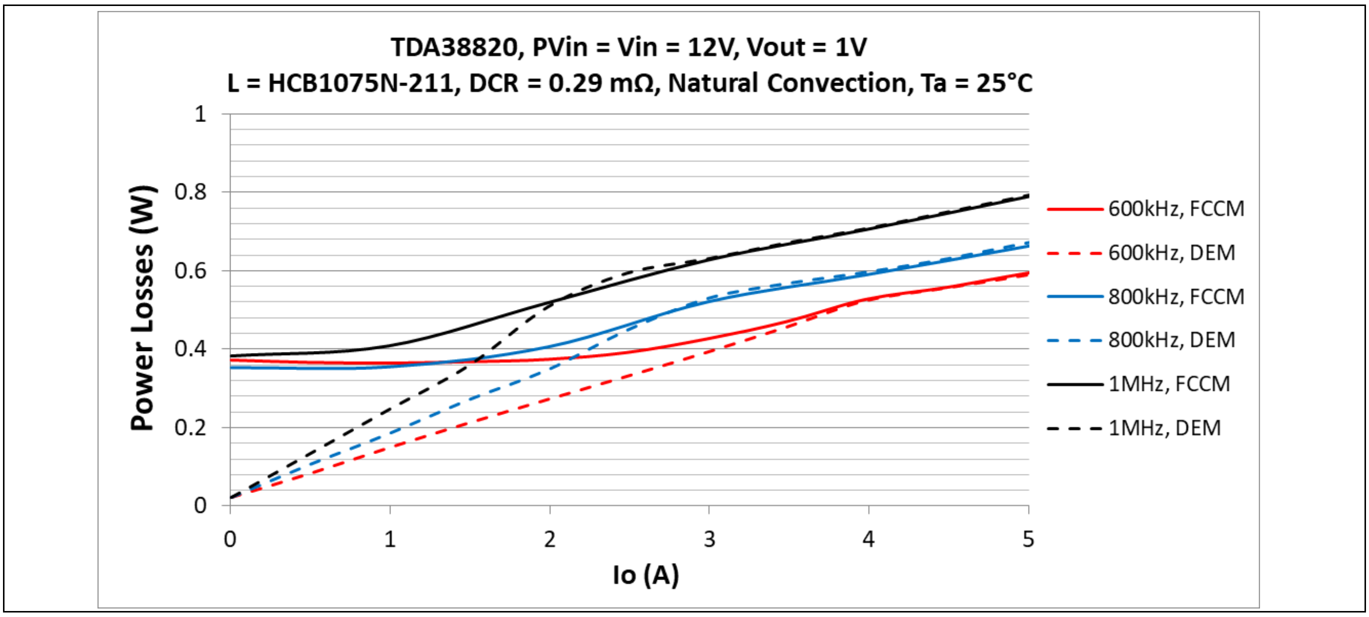

Figure 28 **Power loss with natural convection (12 V_{in}, 1 V_{out}, 215 nH, 600 kHz, 800 kHz and 1000 kHz, T_a = 25°C)**

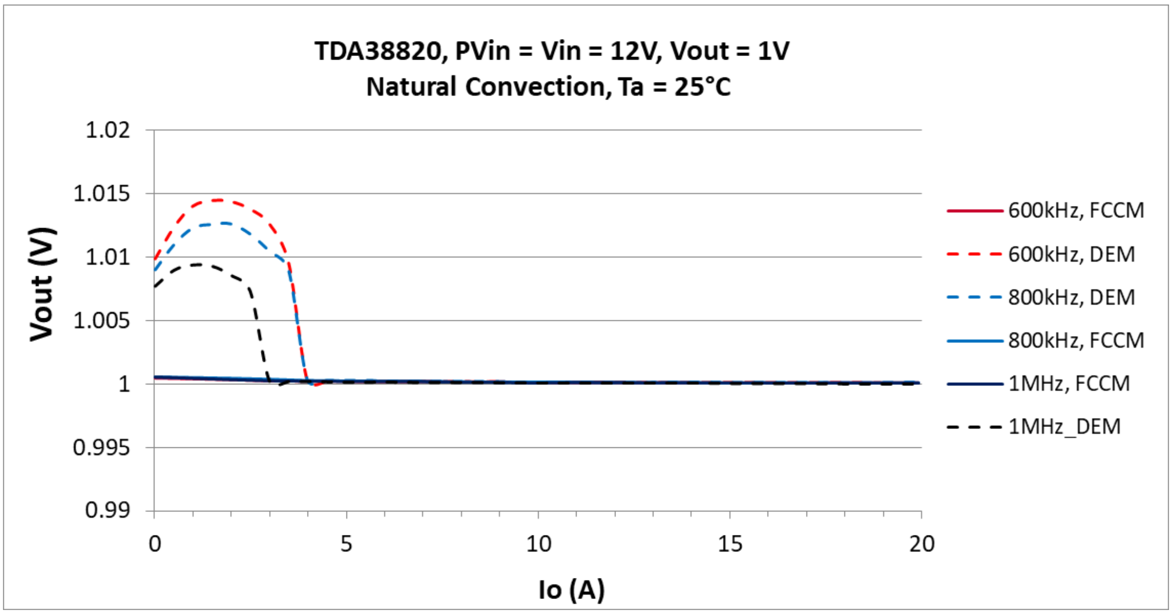

Figure 29 TDA38820 V_{out} regulation (12 V_{in}, 1 V_{out}, 215 nH, 800 kHz and 1000 kHz, T_a = 25°C)

Figure 30 Thermal image at 20 A load TDA38820 = 58°C, L = 49°C, fsw = 600 kHz, T_a = 25°C, natural convection

Figure 31 Thermal image at 20 A load TDA38820 = 63°C, L = 52°C, fsw = 800 kHz, T_a = 25°C, natural convection

Figure 32 Thermal image at 20 A load TDA38820 = 68°C, L = 53.3°C, fsw = 1000 kHz, T_a = 25°C, natural convection

3 Revision history

Document version	Date of release	Description of changes
V 1.0	11-09-2020	First release
V 1.1	01-13-2021	Added Note 1
V 1.2	04-28-2022	Title and subtitle updated

Trademarks
All referenced product or service names and trademarks are the property of their respective owners.

Edition 2022-04-28

Published by

Infineon Technologies AG

81726 Munich, Germany

Do you have a question about this document?

Email: erratum@infineon.com

Document reference
UM_2008_PL12_2009_003801