

User manual for TDA38740 evaluation board

40 A single-phase buck regulator

About this document

Scope and purpose

The TDA38740 is a synchronous buck converter with PMBus communication interface, providing a compact, high-performance and flexible solution in a small 5 mm x 6 mm power QFN package.

Key programmable features offered by the TDA38740 include soft-start, thermal protection, switching frequency, enable input, input undervoltage lockout (UVLO), overvoltage protection (OVP), overcurrent protection (OCP), output undervoltage, overtemperature protection (OTP), high-side short detection, load-line and pre-bias start-up. All faults have configurable responses via the XDP™ Designer GUI available from Infineon.

Output OCP function is implemented by sensing the voltage developed across the on-resistance of the synchronous (low-side) MOSFET for optimum cost and performance, and the current limit is thermally compensated.

This user manual contains the schematic and bill of materials (BOM) for the EVAL_TDA38740_1.2VOUT and EVAL_TDA38740_3.3VOUT evaluation boards. It describes operation and use of the evaluation board itself. Detailed application information for TDA38740 is available in the TDA38740 data sheet.

Intended audience

This document is intended as a guide for design engineers evaluating TDA38740 performance with EVAL_TDA38740_1.2VOUT and EVAL_TDA38740_3.3VOUT evaluation boards.

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1 Board information

1.1 Default board features

$V_{IN} = +12\text{ V}$

$f_{SW} = 800\text{ kHz}$ (default, but it is configurable using the GUI)

$C_{IN} = 8 \times 22\text{ }\mu\text{F}$ (25 V, ceramic 0805) + $1 \times 2.2\text{ }\mu\text{F}$ (25 V, ceramic 0402) + $1 \times 4.7\text{ }\mu\text{F}$ (25 V, ceramic 0603) + $1 \times 390\text{ }\mu\text{F}$ (20 V, electrolytic, optional)

Table 1 Default output inductor and capacitor bank for each output voltage

Output voltage	Inductor	Output capacitors (C_{out})
1.2 V	150 nH	1880 μF (2 x 470 μF SP capacitor + 20 x 47 μF ceramic)
3.3 V	470 nH	1880 μF (2 x 470 μF SP capacitor + 20 x 47 μF ceramic)

1.2 Connections and operating instructions

The EVAL_TDA38740_1.2VOUT and EVAL_TDA38740_3.3VOUT demo boards require a single +12 V for the input power and can deliver up to 40 A load current. The operation modes and OCP limits are programmable via the XDP™ Designer GUI.

Table 2 Connections

Label		Descriptions
Input	PVIN	Connect input power (+12 V) to this pin
	GND	Return of input power
	VIN_Eff	Sense pins for the input voltage
	VIN_SNS	Sense pins for the input voltage
Output	VOUT	V_{OUT} , connect a load (40 A max.) to this pin
	GND	Return of V_{OUT}
	VOUT_Eff	Sense pins for the output voltage
	VOUT_SNS	Sense pins for the output voltage
Enable	ENABLE	Connect a scope probe to this pin to monitor the enable signal.
	GND	An external enable signal can be applied to this pin to overdrive the onboard enable signal by connecting a jumper on EXT-EN header J668. Alternatively, the enable signal can be generated using P_{VIN} using a resistor divider by connecting a jumper on PVIN-EN header J668.
BODE	A	For bode plot measurement
	B	
SM_ADDR/PROG	I ² C slave address offset	Use this jumper to add an offset to the I ² C slave base address of 0x10h. By default, this is set to zero.
PMBus	J659	This is used to establish communication with the Infineon XDP™ Designer GUI, which is used to change the default configuration of the part. The USB005 dongle is used for communication.

VRRDY	TP101	This signal is used to indicate that the V_{OUT} has reached a threshold set by POWER_GOOD_ON PMBus command
SM_ADDR/PROG	J665	This jumper is used to select between 16 programmed files stored in the part. By default, it is set to accept the most recent programmed config file into the part.
ILIM	J671	This jumper is used to select the resistor-programmable current limit
TON/MODE	J672	This jumper is used to select the resistor-programmable switching frequency and FCCM or DCM mode
VBT	J674	This jumper is used to set the resistor-programmable boot voltage
VIN-PVIN	VCC	Connecting a jumper to J654 generates the V_{CC} onboard, but removing this jumper and connecting a 5 V external supply to TP104 will also work
EN ON/OFF	SW3	This switch is used to enable the part on and off. The switch is pulled up to an onboard 3.3 V regulator.

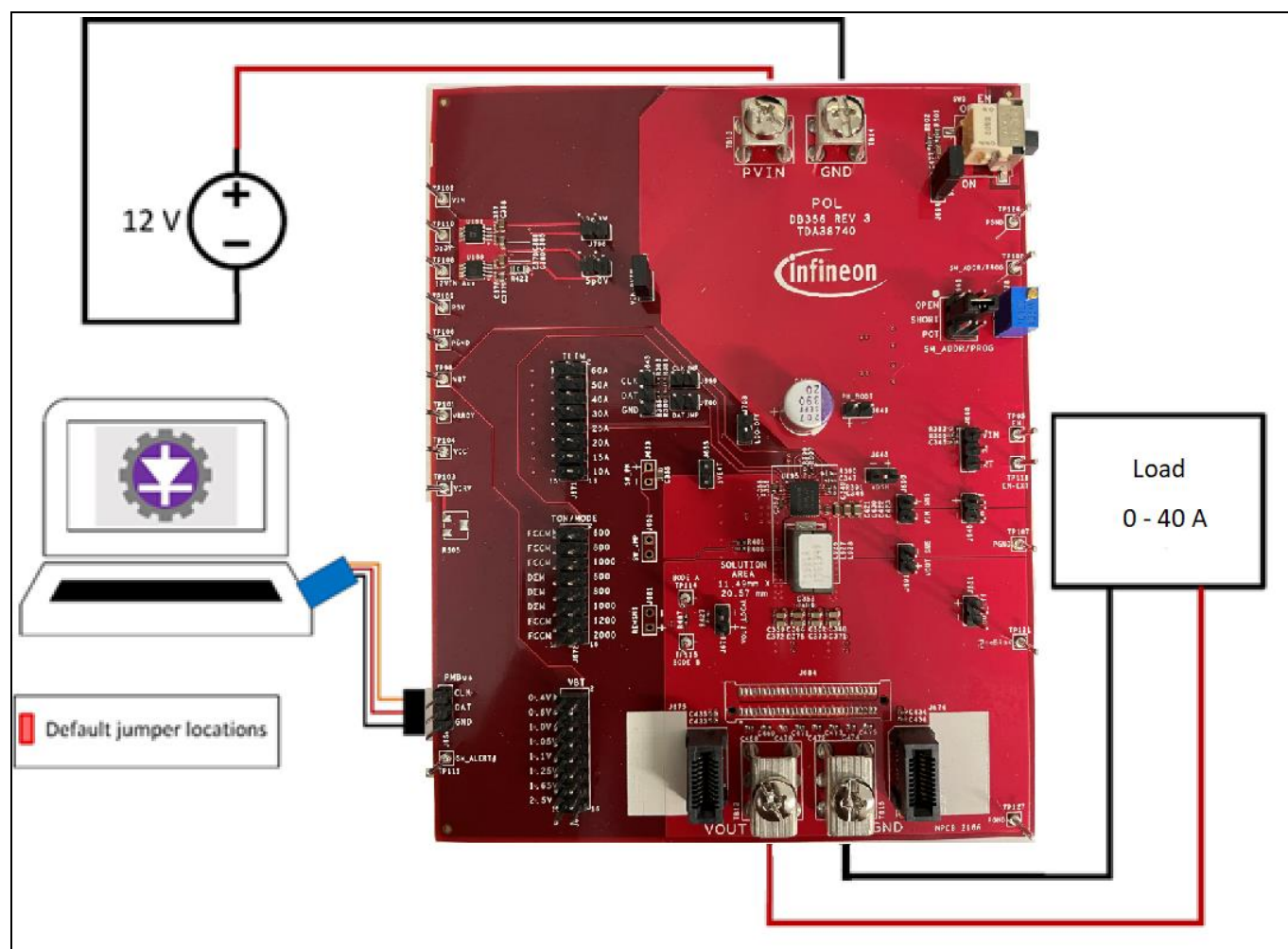


Figure 1 Default bench setup block diagram

Figure 1 depicts a default bench setup to start the demo board. The 12 V input voltage and USB dongle connected to a computer running the XDP™ Designer GUI are necessary to begin to communicate with the part. Section **1.6** covers installing and starting the GUI. A load may then be connected to the output terminals.

1.3 Layout

The PCB is an eight-layer board (5.25 in. x 4.1 in.) using FR4 material. The PCB thickness is 0.062 in. The TDA38740 and other major power components are mounted on the top side of the board. **Table 2** details the layer stack-up order and copper weight for each layer.

Table 3 PCB layer stack-up

Layer	Layer description	Trace material
1	Top	0.5 oz. copper + 1.5 oz. plating
2	Ground 1	2 oz. copper
3	Signal 1	2 oz. copper
4	Power 1	2 oz. copper
5	Power ground	2 oz. copper
6	Signal 2	2 oz. copper
7	Ground 2	2 oz. copper
8	Bottom	0.5 oz. copper + 1.5 oz. plating

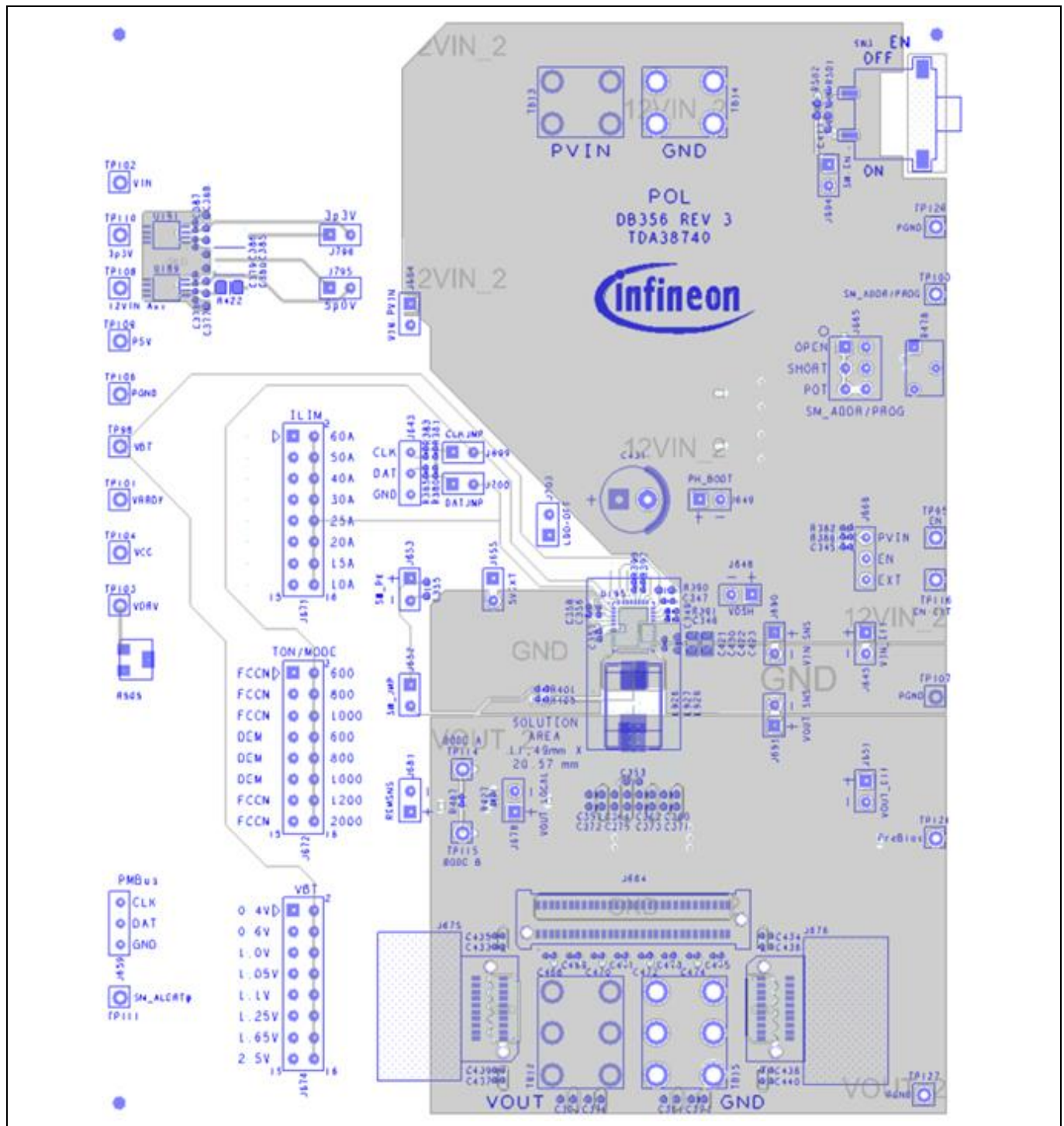


Figure 2 Top view of TDA38740 evaluation board

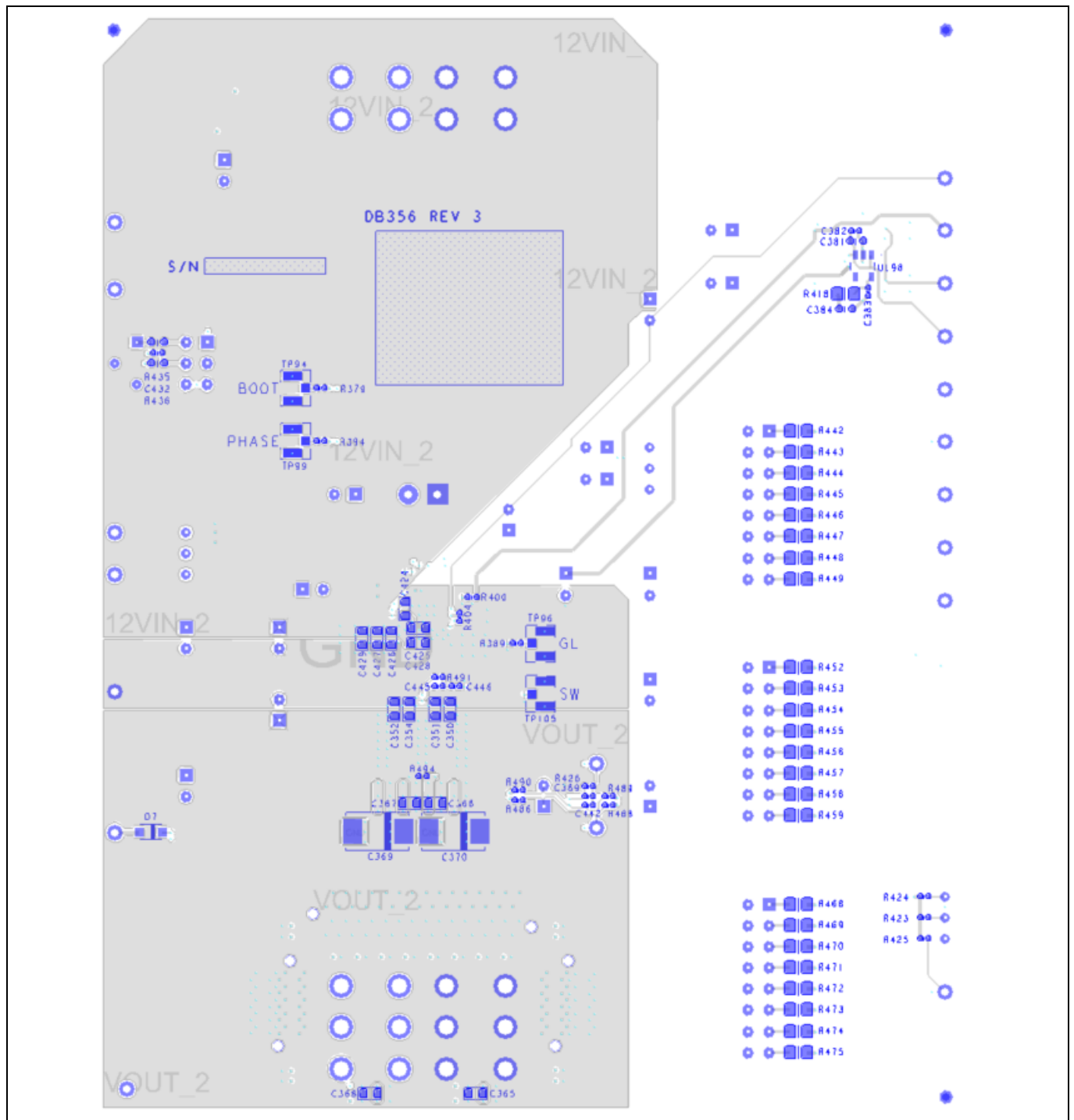


Figure 3 **Bottom view of TDA38740 evaluation board**

1.4 PCB layout

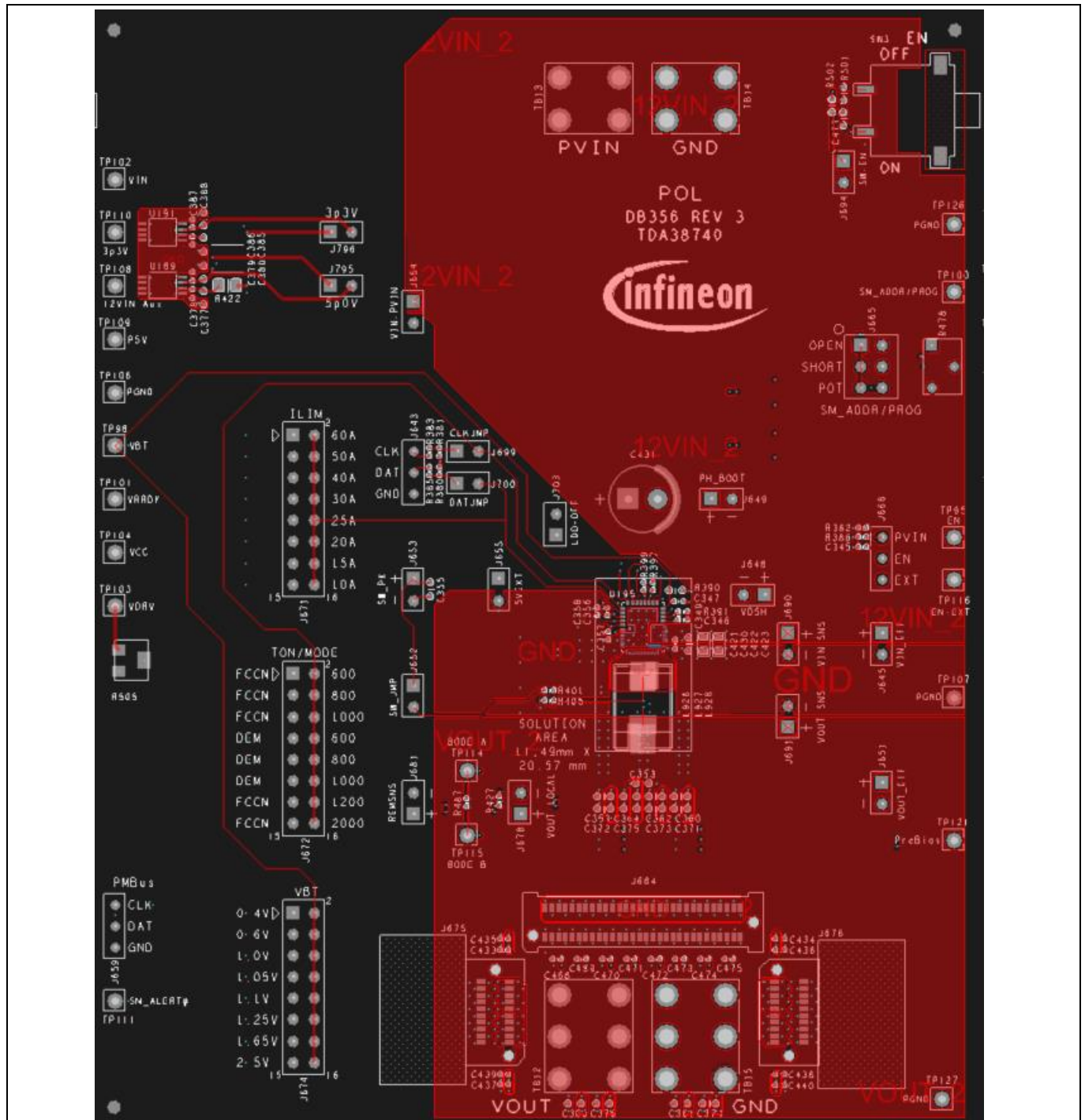


Figure 4 Top layer

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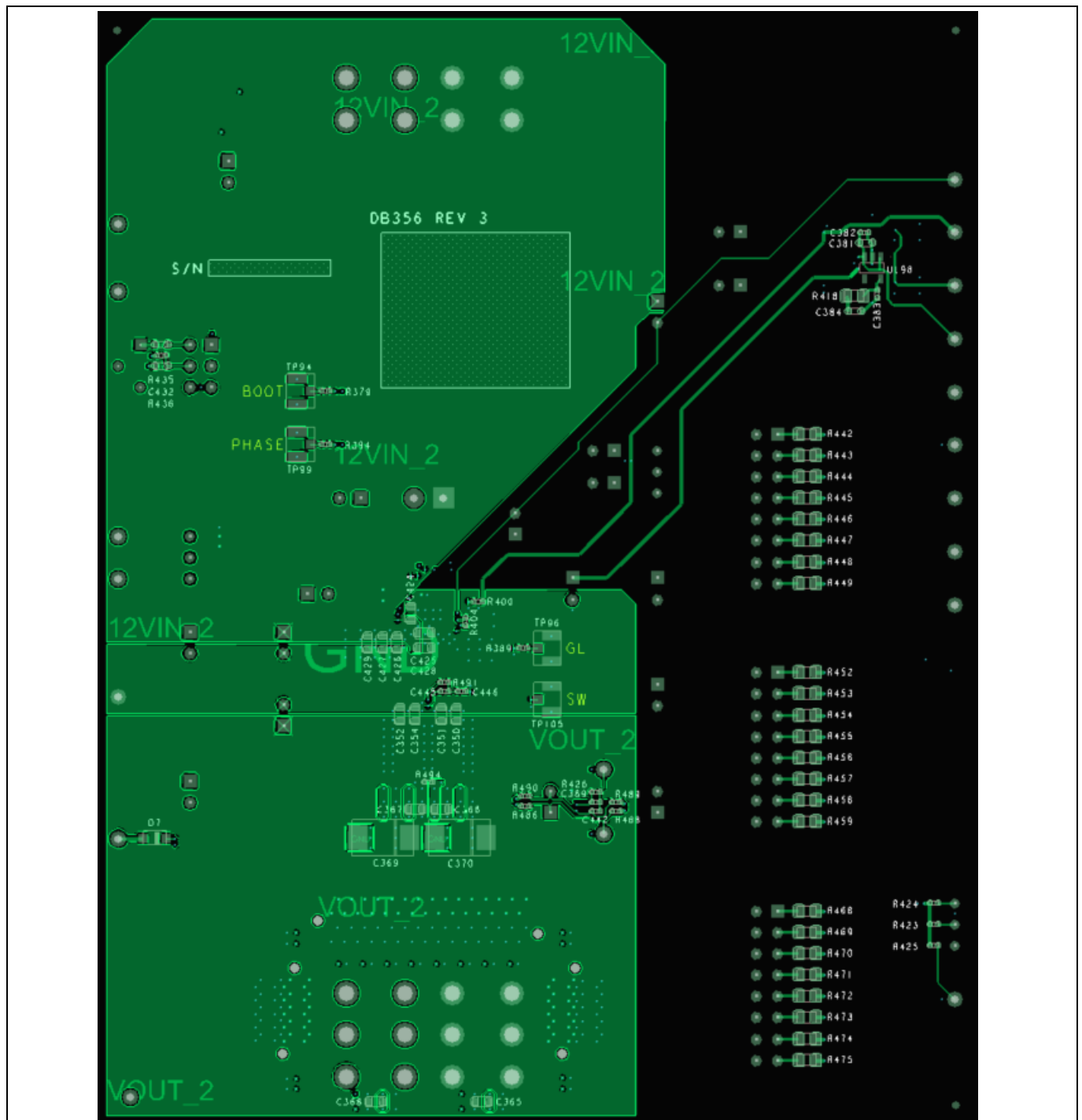


Figure 5 Bottom layer

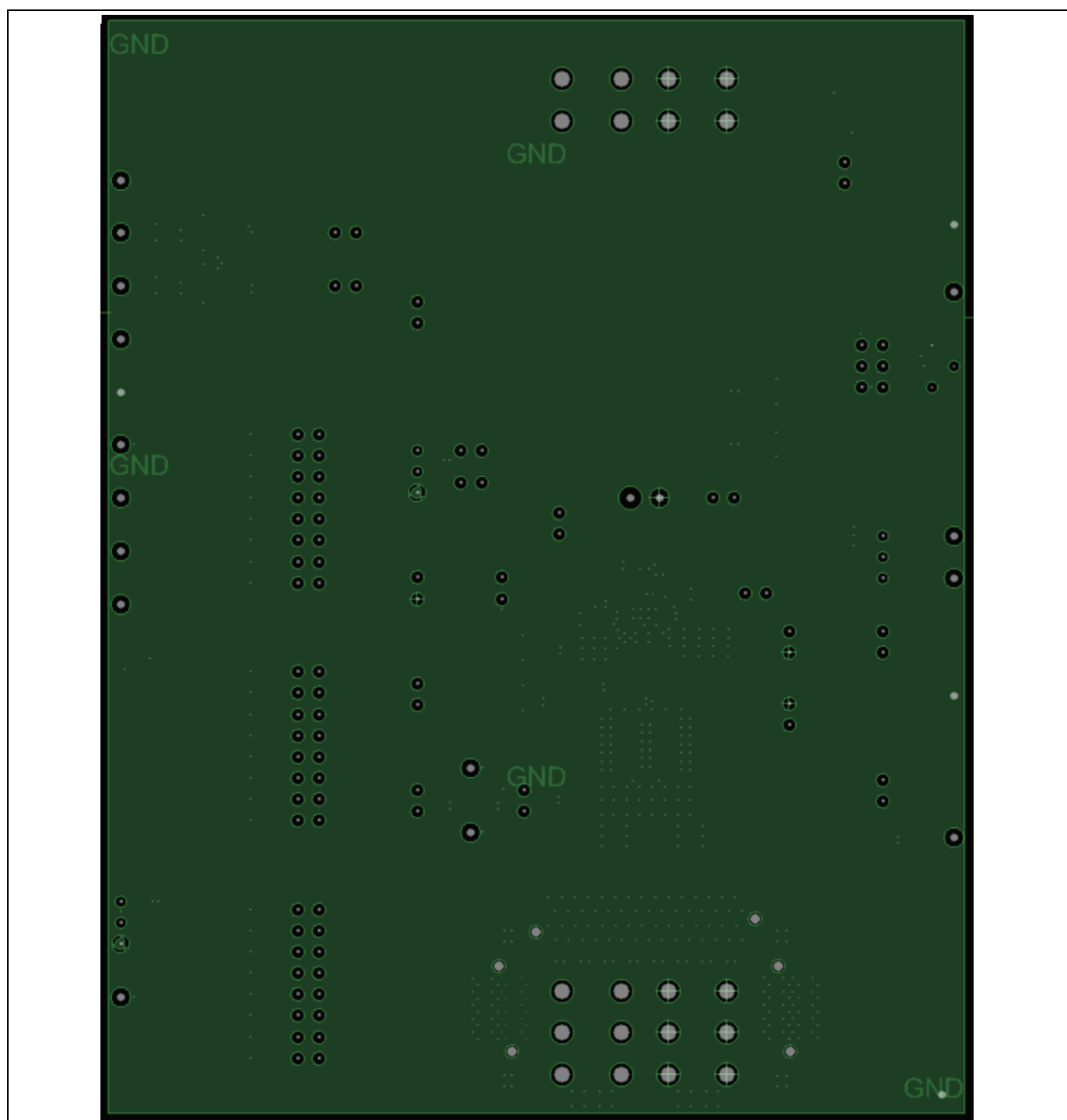


Figure 6 Mid layer 1 (ground 1)

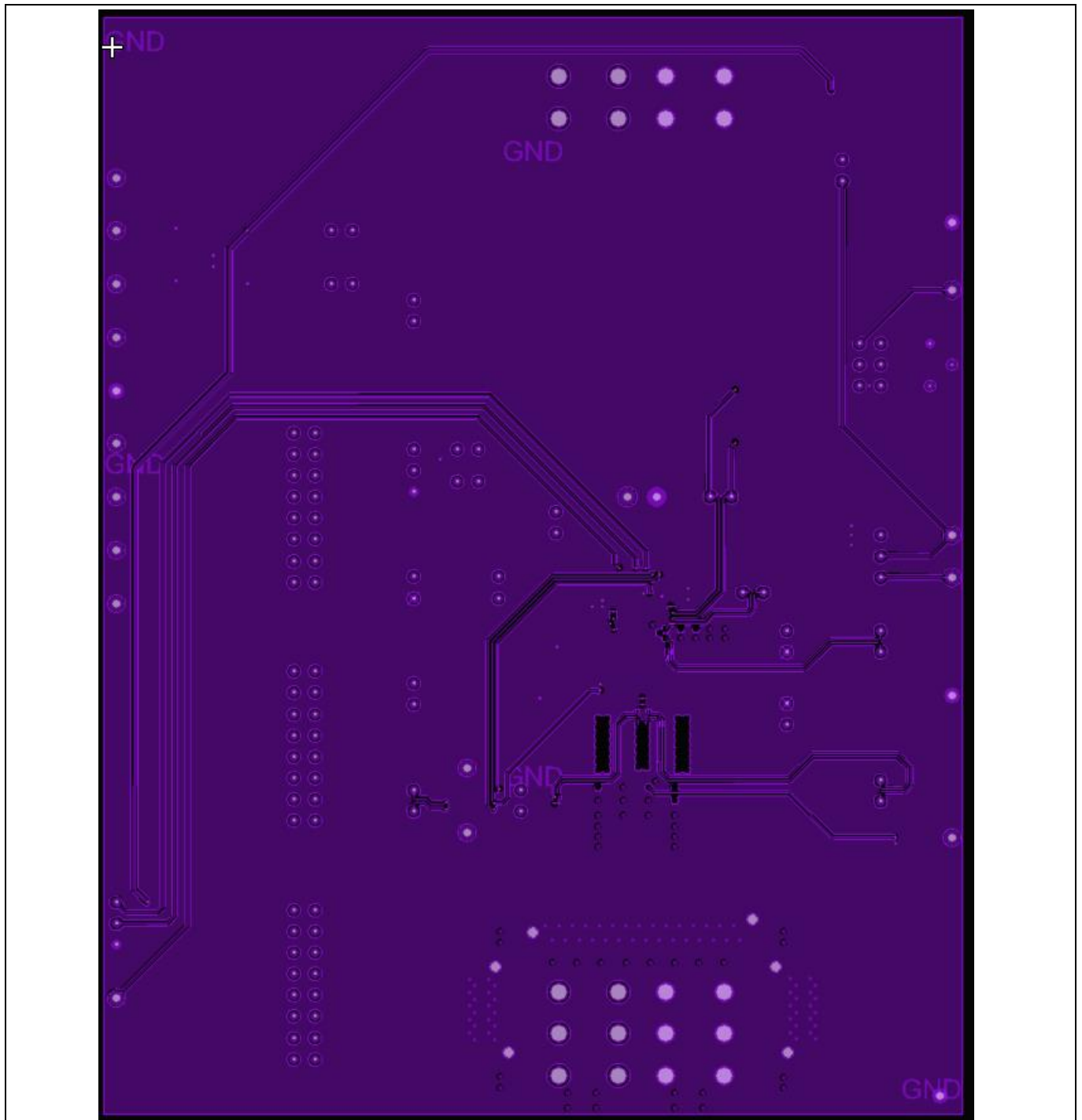


Figure 7 Mid layer 2 (signal 1)

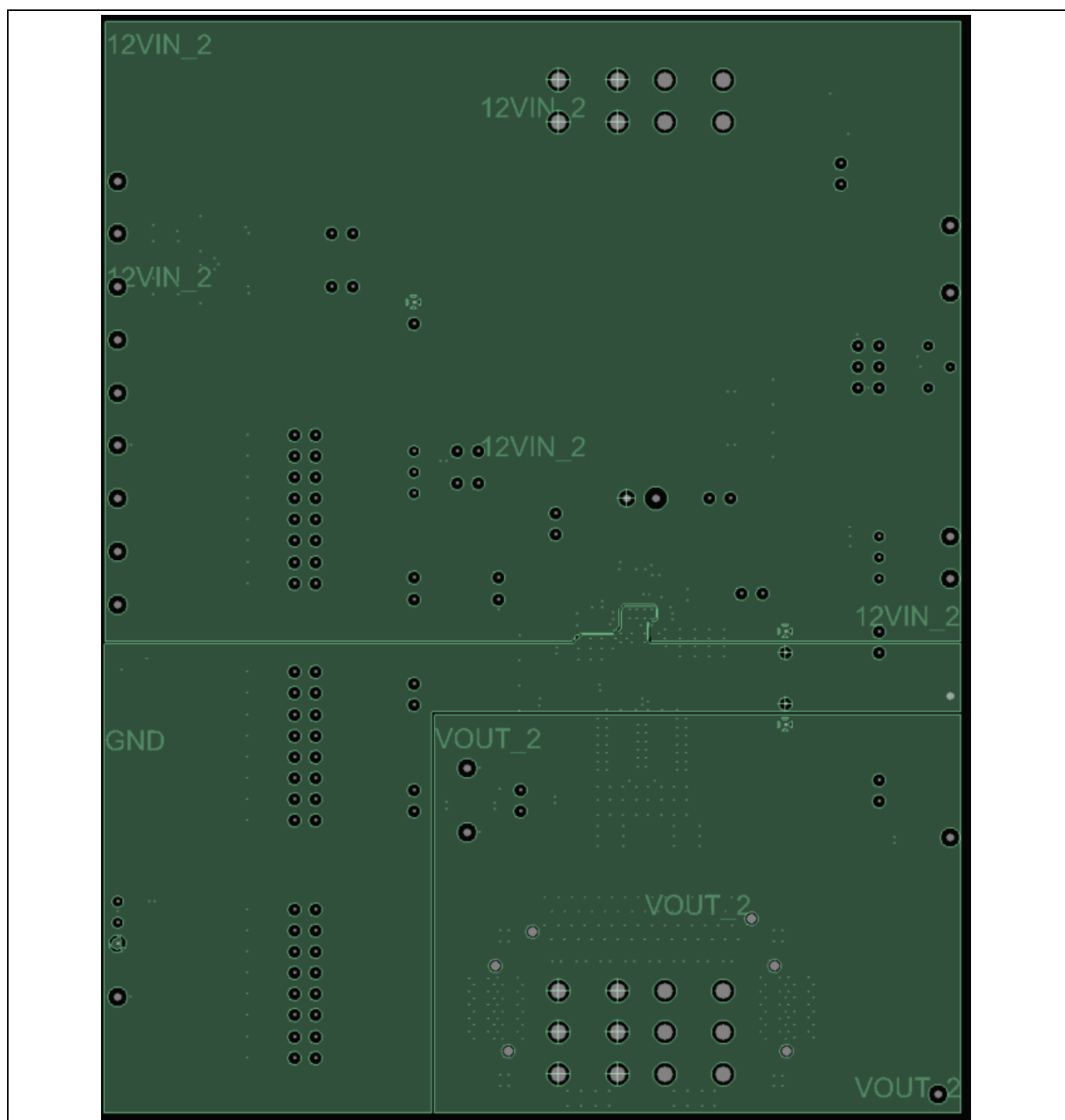


Figure 8 Mid layer 3 (power 1)

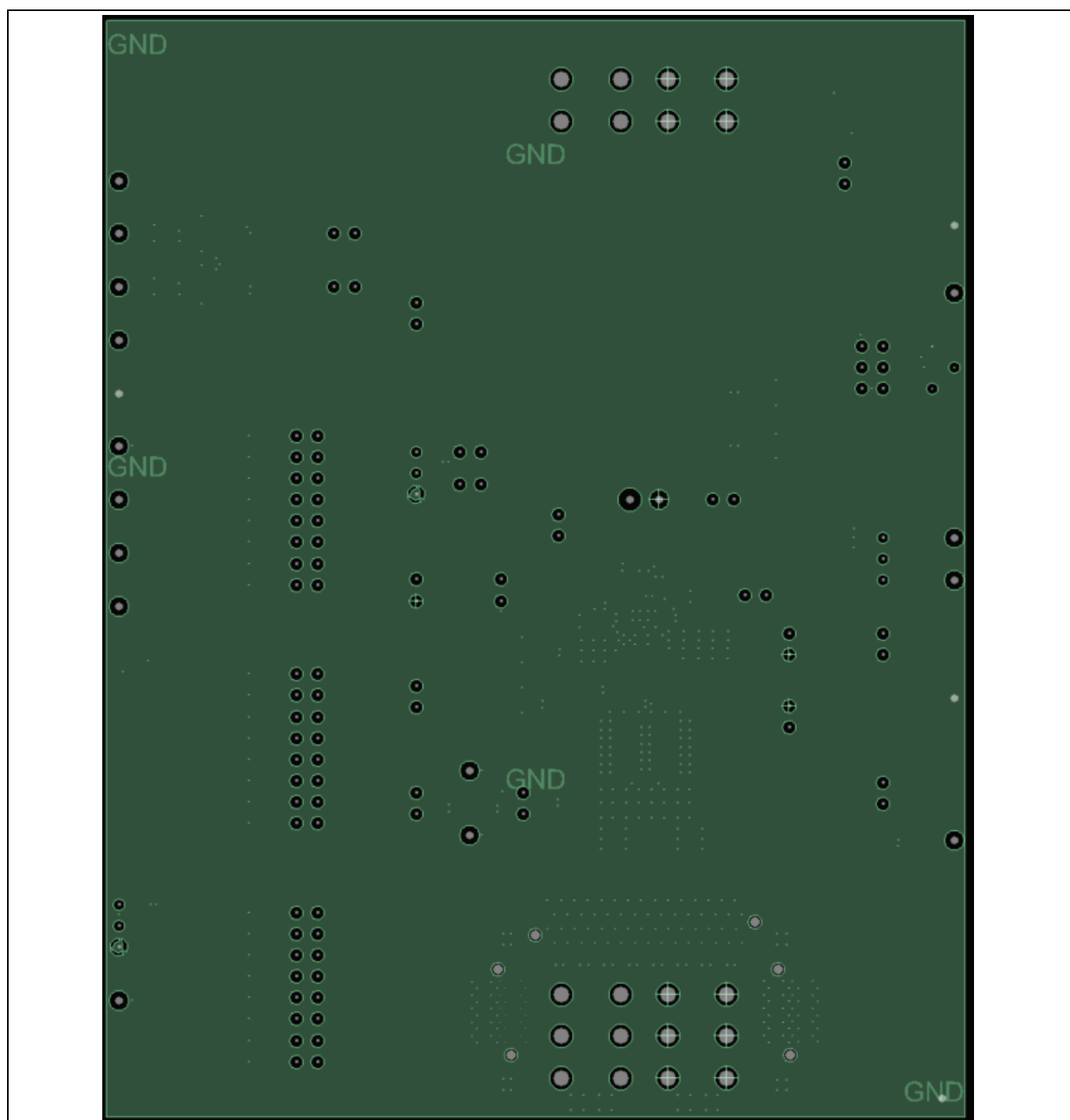


Figure 9 Mid layer 4 (power 2)

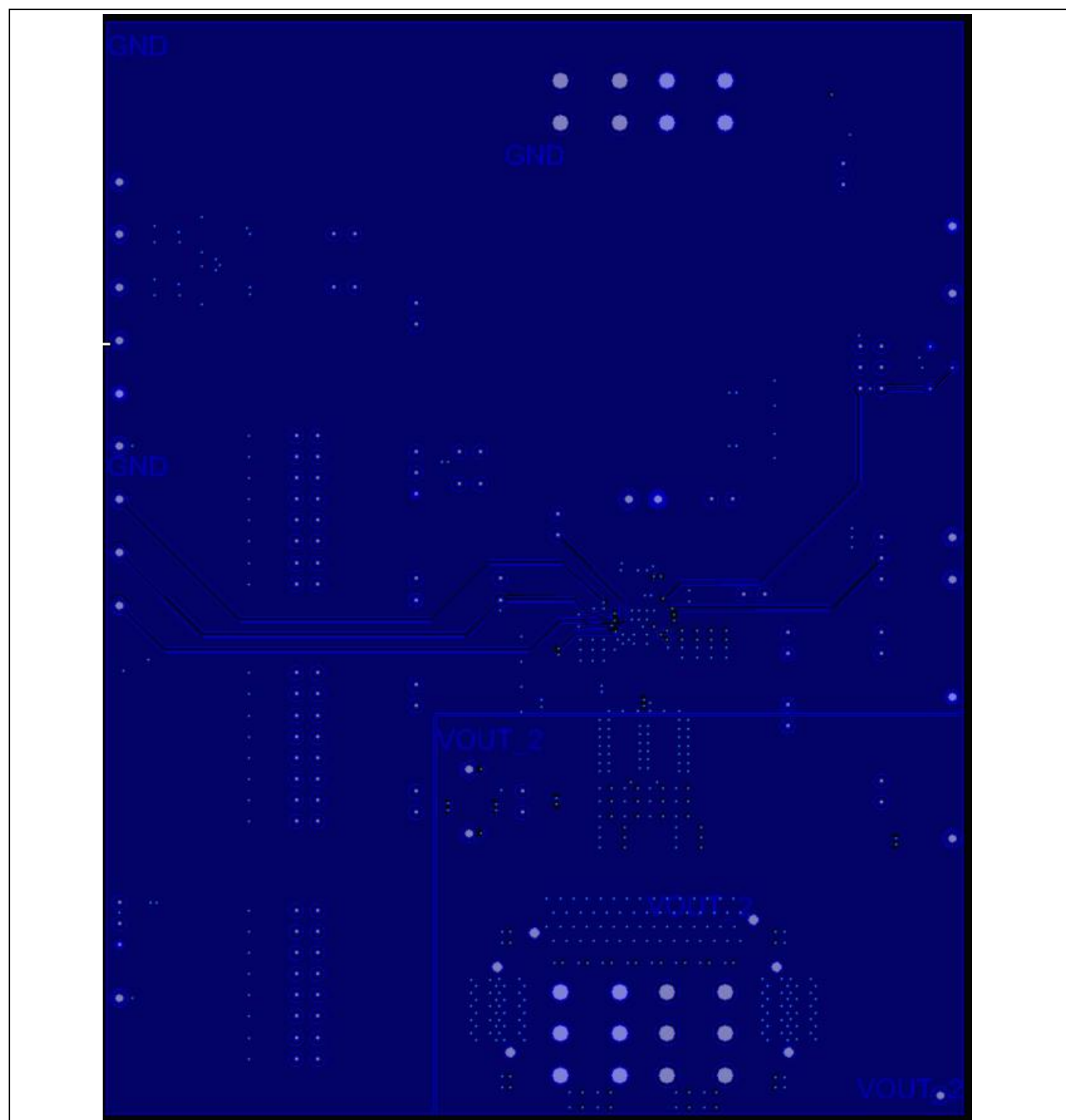


Figure 10 Mid layer 5 (signal 2)

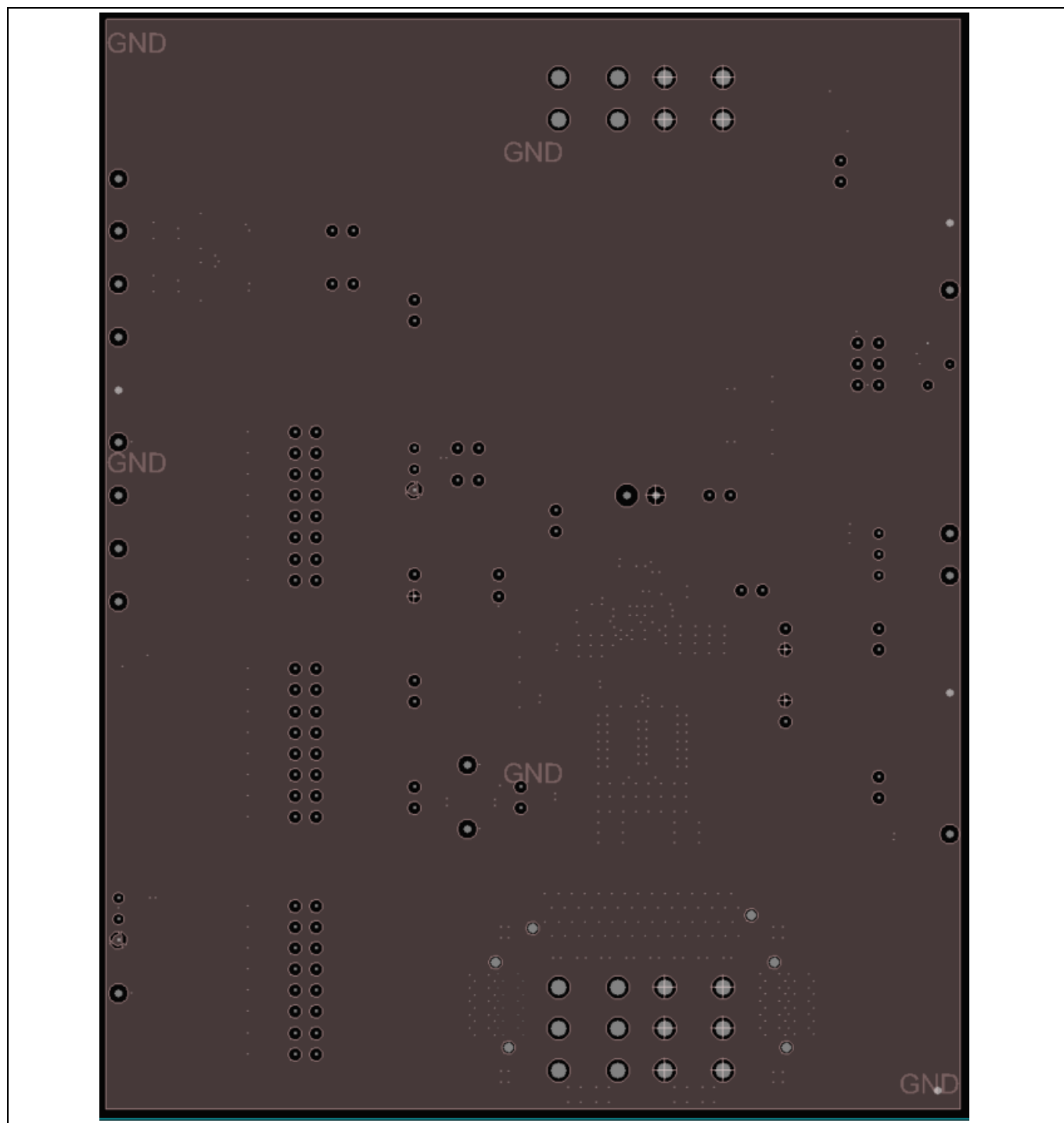


Figure 11 Mid layer 6 (ground 2)

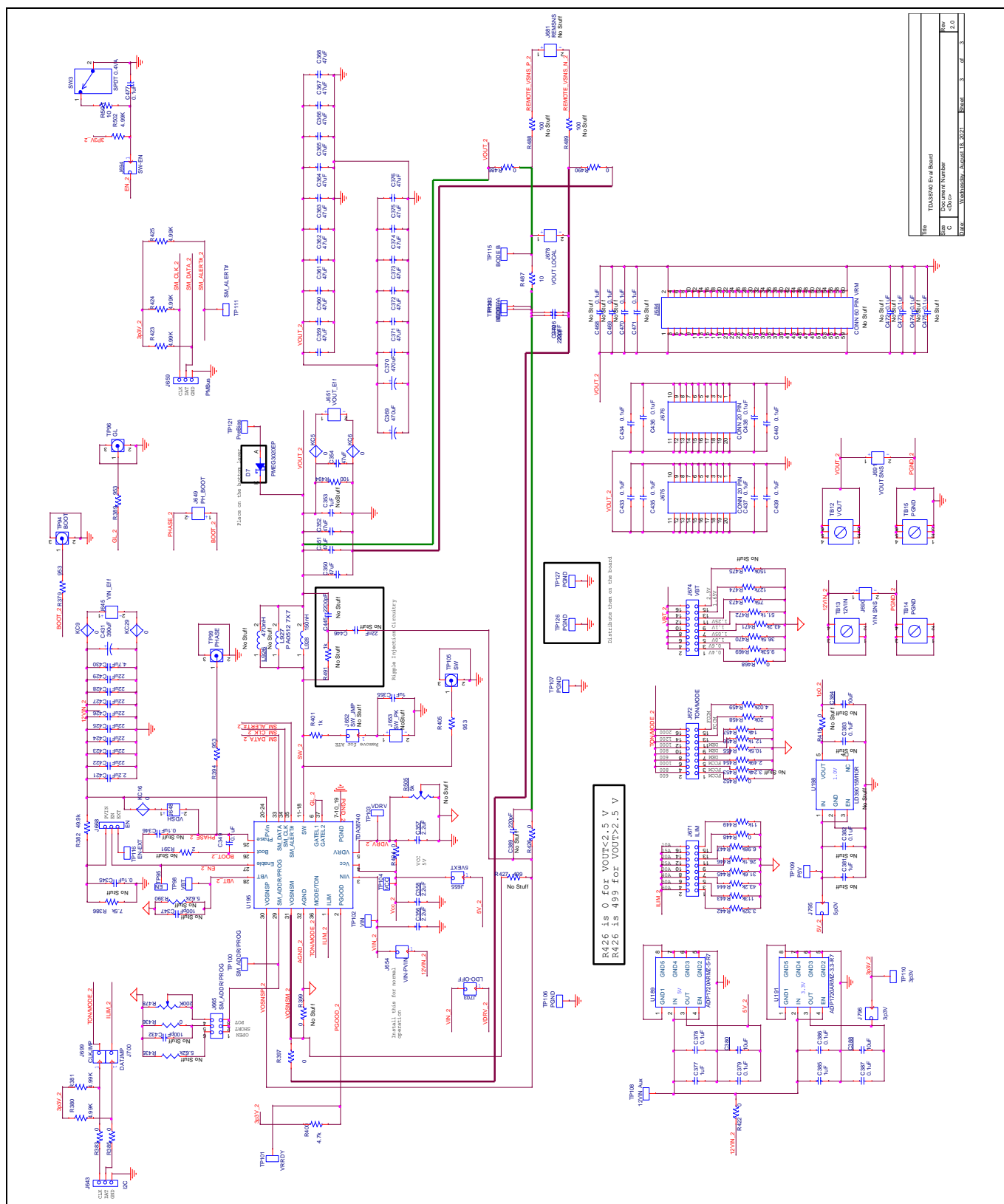


Figure 12 Schematic of the EVAL_TDA38740_1.2VOUT and EVAL_TDA38740_3.3VOUT evaluation board BOM

1.5 Bill of materials

Table 4 Optimized BOM, with components necessary for point-of-load (POL) function

Item	Qty.	Reference	Value	Description	Manufacturer	Part number
1	1	C349	0.1 μ F	0.1 μ F 0402 25 V X7R 10%	TDK	C1005X7R1E104K
2	2	C347, C342	100 pF	100 pF 0402 50 V COG 5%	JDI	500R07N101JV4T
3	1	C353	1 μ F	1 μ F 0603 25 V X5R 10%	Samsung	CL10A105KA8NNNC
4	3	C356, C357, C358	2.2 μ F	2.2 μ F 0402 16 V X6S 10%	TDK	C1005X6S1C225K050BC
5	1	C421	2.2 μ F	2.2 μ F 0402 25 V X5R 10%	Murata	GRT155R61E225KE13D
6	8	C422, C423, C424, C425, C426, C427, C428, C429	22 μ F	22 μ F 0805 25 V X5R 20%	Murata	GRM21BR61E226ME44L
7	1	C430	4.7 μ F	4.7 μ F 0603 25 V X6S 20%	Murata	GRM188C81E475KE11
8	1	C431	390 μ F	Capacitor 8 mm 20 V 20%	Panasonic	20SEPF390M
9	1	R382	49.9 k	Resistor 0402 1/16 W 1%	Yageo	RC0402FR-07####L
10	2	R404	0	Resistor 0402 1/16 W 1%	Yageo	RC0402FR-07####L
11	1	R386	7.5 k	Resistor 0402 1/16 W 1%	Yageo	RC0402FR-07####L
12	2	R390, R435	5.62 k	Resistor 0603 1/10 W 1%	Yageo	RC0603FR-07####L
13	1	R391	2	Resistor 0402 1/16 W 1%	Yageo	RC0402FR-07####L
14	1	R400	4.7 k	Resistor 0402 1/16 W 1%	Yageo	RC0402FR-07####L
15	1	R436	0	Resistor 0603 1/10 W 1%	Yageo	RC0603FR-07####L
16	1	R487	10	Resistor 0402 1/16 W 1%	Yageo	RC0402FR-07####L
17	2	R488, R489	100	Resistor 0402 1/16 W 1%	Yageo	RC0402FR-07####L
18	1	U195	TDA38740	TDA38740 20 A single-voltage synchronous buck regulator	Infineon	TDA38740-0000

Table 5 Optimized BOM, with components that differ for different output voltages

V _{OUT}	Item	Qty.	Reference	Value	Description	Manufacturer	Part number
Less than 2.5 V	1	8	C350, C351, C352, C354, C365, C366, C367, C368	47 µF	47 µF 0805 4 V X6S 20%	Murata	GRT21BC80G476ME13L
	2	12	C359, C360, C361, C362, C363, C364, C371, C372, C373, C374, C375, C376	47 µF	47 µF 0603 6.3 V X5R-10%	Murata	GRM188R60J476ME15D
	3	1	C369	470 µF	POSCAP Dcase 2.5 V 20%	Panasonic	EEFGX0E471R
	4	1	C370	470 µF	POSCAP Dcase 2.5 V 20%	Panasonic	EEFGX0E471R
	5	1	L928	150 nH	Inductor SMT 10 x 6.4 mm 78 A, 0.125 mΩ	Inter-technical	L101247A-150L
	6	1	R426	0	Resistor 0402 1/16 W 1%	Yageo	RC0402FR-07####L
	7	1	R444	43.2 k	Resistor 0805 1/8 W 1%	Panasonic	ERJ6ENF####V
	8	1	R427	–	Resistor 0402 1/16 W 1%	Yageo	RC0402FR-07####L
	9	1	R452	0	Resistor 0805 1/8 W 1%	Panasonic	ERJ6ENF####V
More than 2.5 V	1	8	C350, C351, C352, C354, C365, C366, C367, C368	47 µF	47 µF 0805 6.3 V X5R 20%	TDK	C2012X5R0J476M
	2	12	C359, C360, C361, C362, C363, C364, C371, C372, C373, C374, C375, C376	47 µF	47 µF 0603 6.3 V X5R 10%	Murata	GRM188R60J476ME15D
	3	1	C369	470 µF	POSCAP Dcase 6.3 V 20%	Panasonic	6TPF470MAH
	4	1	C370	470 µF	POSCAP Dcase 6.3 V 20%	Panasonic	6TPF470MAH
	5	1	L928	470 nH	Inductor, SMT, 10 x 7.3 mm, 30 A, 0.81 mΩ	Inter-technical	L101158A-R47LH
	6	1	R426	499	Resistor 0402 1/16 W 1%	Yageo	RC0402FR-07####L
	7	1	R444	26.1 k	Resistor 0805 1/8 W 1%	Panasonic	ERJ6ENF####V
	8	1	R427	499	Resistor 0402 1/16 W 1%	Yageo	RC0402FR-07####L
	9	1	R452	0	Resistor 0805 1/8 W 1%	Panasonic	ERJ6ENF####V

1.6 XDP™ designer GUI

Infineon's XDP™ Designer GUI is needed to communicate with the TDA38740 part via I²C. The GUI is part of the Infineon Toolbox. The **Toolbox** can be downloaded from Infineon's website by navigating to the "Tools/Utilities" tab, then scrolling to the "**Infineon Developer Center Launcher**" section. The page has more detailed instructions on how to install the Toolbox. Dongle driver v59.4 or higher is necessary to communicate with the TDA38740.

Once the Toolbox is installed the user must launch it and navigate to the "Manage tools" section. Search this section for "XDP™ Designer" and click to install. Launch XDP™ Designer, and with the evaluation board powered (+12 V P_{VIN}) and connected via the USB005 dongle, click the "tuning and debugging" button. This should update the system section with this device and its configuration, or alternatively click the "scan devices" button. The device will show with the part number and I²C address, with green circles (if the connection is correct and there are no faults). Click on the device name and navigate the options on the toolbar to alter any system configurations or read the telemetry. See **Figure 13** for an annotated version of the XDP™ Designer home screen.

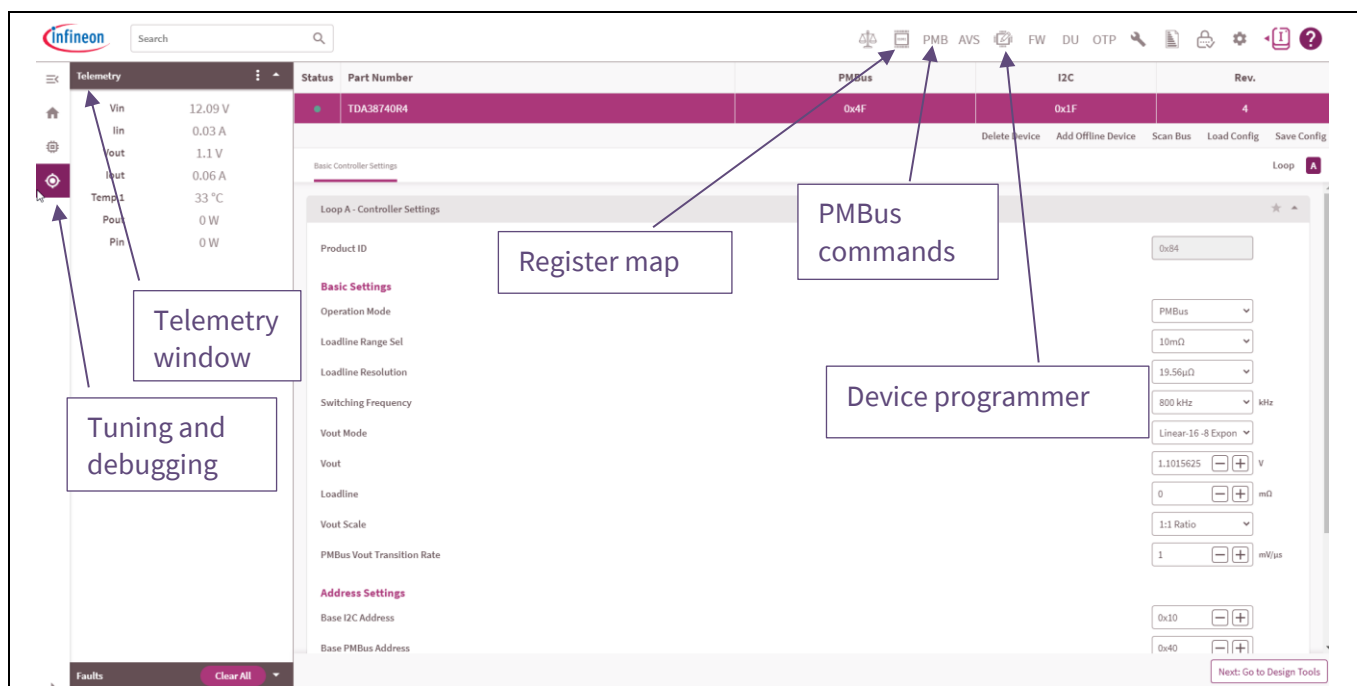
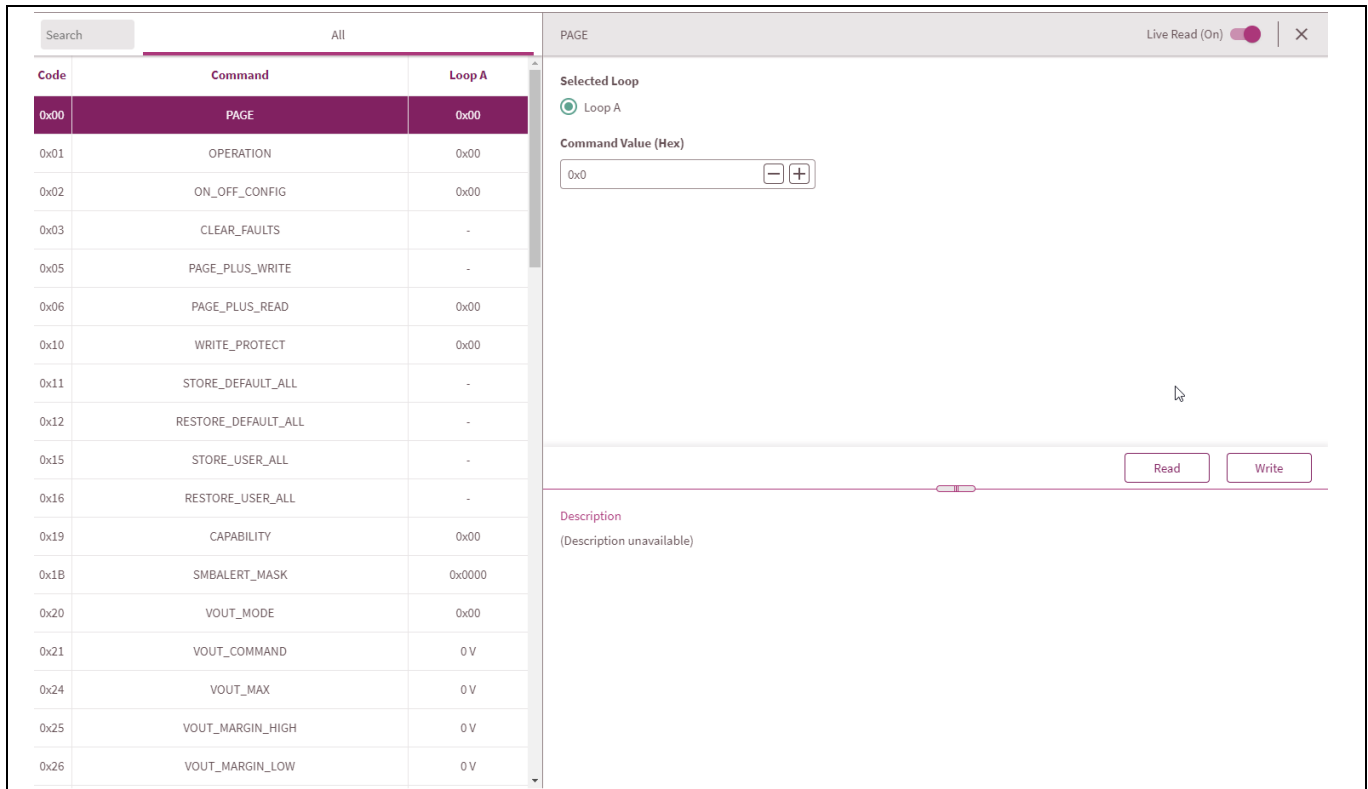


Figure 13 XDP™ designer GUI home screen

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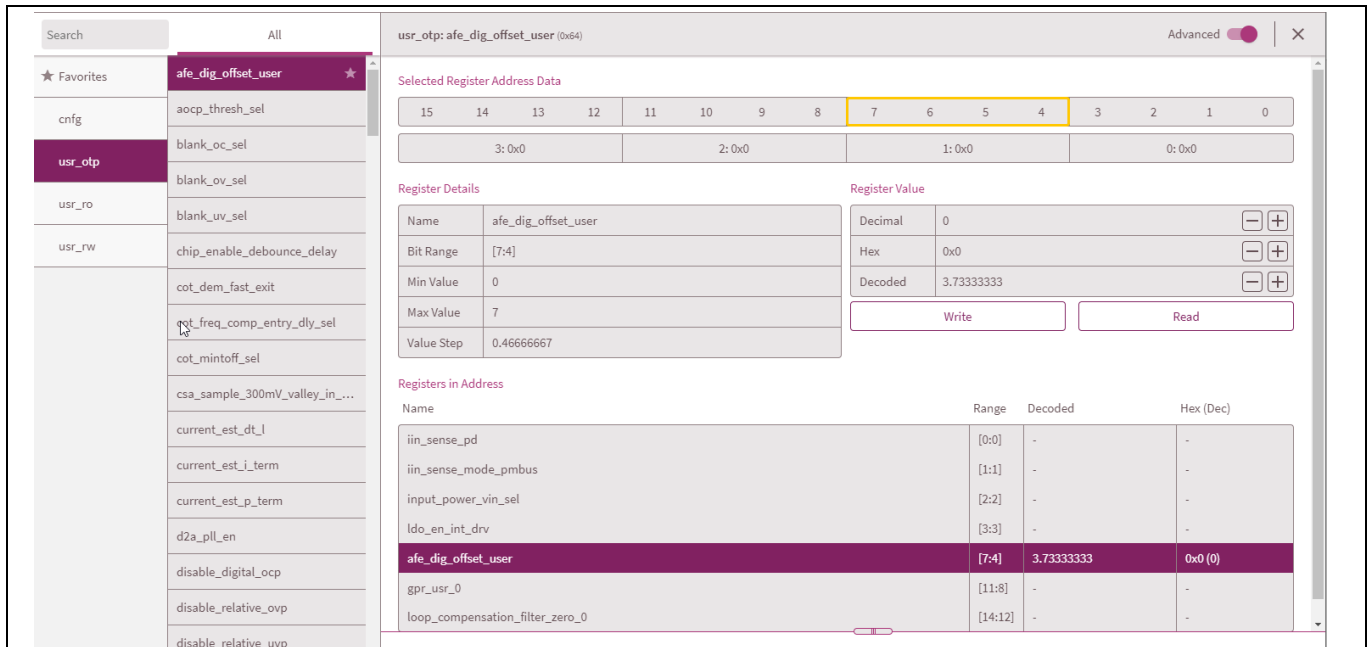
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The screenshot shows the PMBus command window. On the left, a table lists PMBus commands with their codes and loop addresses. The 'PAGE' command (0x00) is selected. On the right, the 'Selected Loop' is 'Loop A', and the 'Command Value (Hex)' is '0x0'. Below this, there are 'Read' and 'Write' buttons. A description field shows '(Description unavailable)'.

Code	Command	Loop A
0x00	PAGE	0x00
0x01	OPERATION	0x00
0x02	ON_OFF_CONFIG	0x00
0x03	CLEAR_FAULTS	-
0x05	PAGE_PLUS_WRITE	-
0x06	PAGE_PLUS_READ	0x00
0x10	WRITE_PROTECT	0x00
0x11	STORE_DEFAULT_ALL	-
0x12	RESTORE_DEFAULT_ALL	-
0x15	STORE_USER_ALL	-
0x16	RESTORE_USER_ALL	-
0x19	CAPABILITY	0x00
0x1B	SMBALERT_MASK	0x0000
0x20	VOUT_MODE	0x00
0x21	VOUT_COMMAND	0 V
0x24	VOUT_MAX	0 V
0x25	VOUT_MARGIN_HIGH	0 V
0x26	VOUT_MARGIN_LOW	0 V

Figure 14 PMBus command window



The screenshot shows the Register map window. On the left, a tree view shows the register map structure. The 'afe_dig_offset_user' register is selected. On the right, the 'Selected Register Address Data' is shown as a 16-bit bus. Below this, the 'Register Details' table shows the register's name, bit range, and value. The 'Register Value' section shows the decimal, hex, and decoded values. At the bottom, the 'Registers in Address' table lists all registers in the address space.

Name	Bit Range	Min Value	Max Value	Value Step
afe_dig_offset_user	[7:4]	0	7	0.46666667

Name	Range	Decoded	Hex (Dec)
iiin_sense_pd	[0:0]	-	-
iiin_sense_mode_pmbus	[1:1]	-	-
input_power_vin_sel	[2:2]	-	-
ldo_en_int_drv	[3:3]	-	-
afe_dig_offset_user	[7:4]	3.73333333	0x0 (0)
gpr_usr_0	[11:8]	-	-
loop_compensation_filter_zero_0	[14:12]	-	-

Figure 15 Register map window

2 Typical operating waveforms

2.1 $P_{VIN} = 12.0\text{ V}$, $V_{OUT} = 1.2\text{ V}$, $I_{OUT} = 0\text{ A}$, room temperature, no airflow

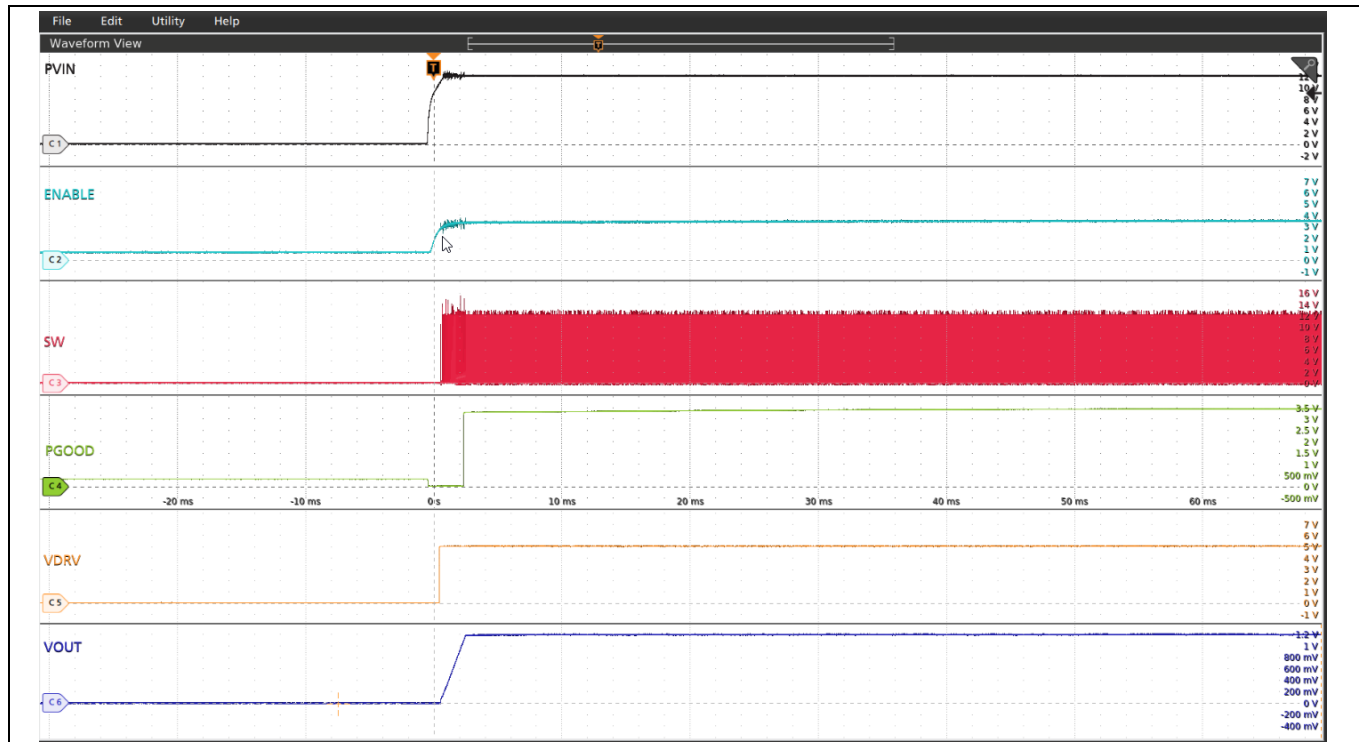


Figure 16 Start-up at 1.2 V V_{OUT} 0 A load (Ch1: P_{VIN} , Ch2: enable, Ch3: switch node, Ch4: P_{GOOD} , Ch5: V_{DRV} , Ch6: V_{OUT})

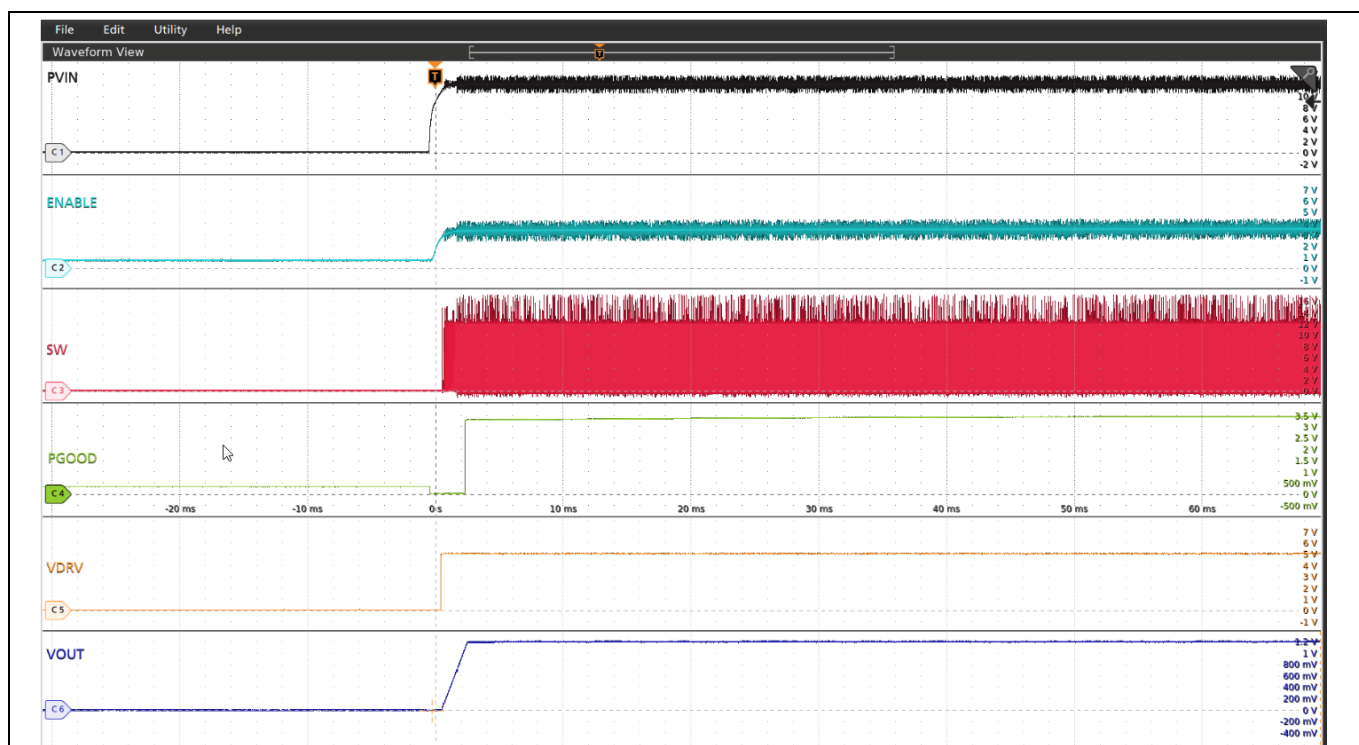


Figure 17 Start-up at 1.2 V V_{OUT} 20 A load (Ch1: P_{VIN} , Ch2: enable, Ch3: switch node, Ch4: P_{GOOD} , Ch5: V_{DRV} , Ch6: V_{OUT})

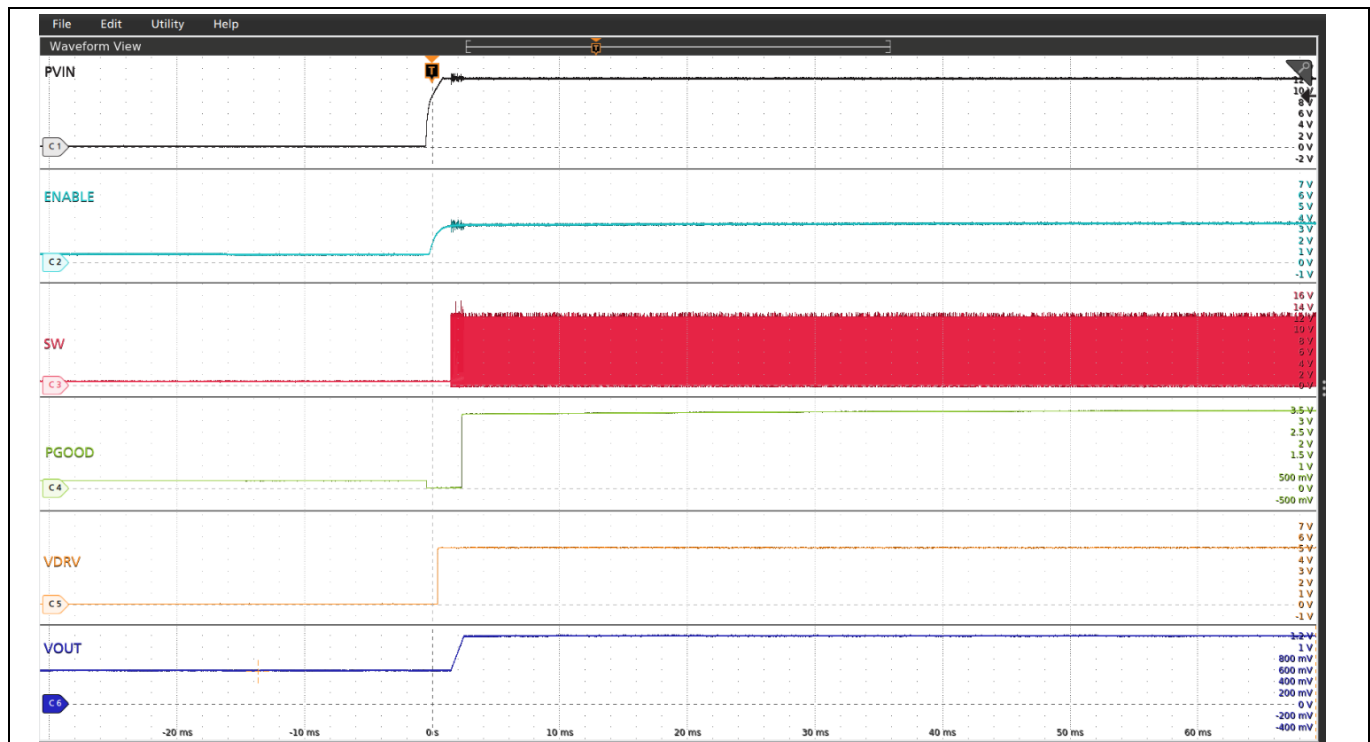


Figure 18 Pre-bias start-up 1.2 V V_{OUT} at 0 A, pre-bias voltage = 0.6 V (Ch₁: P_{VIN} , Ch₂: enable, Ch₃: switch node, Ch₄: P_{GOOD} , Ch₅: V_{DRV} , Ch₆: V_{OUT})

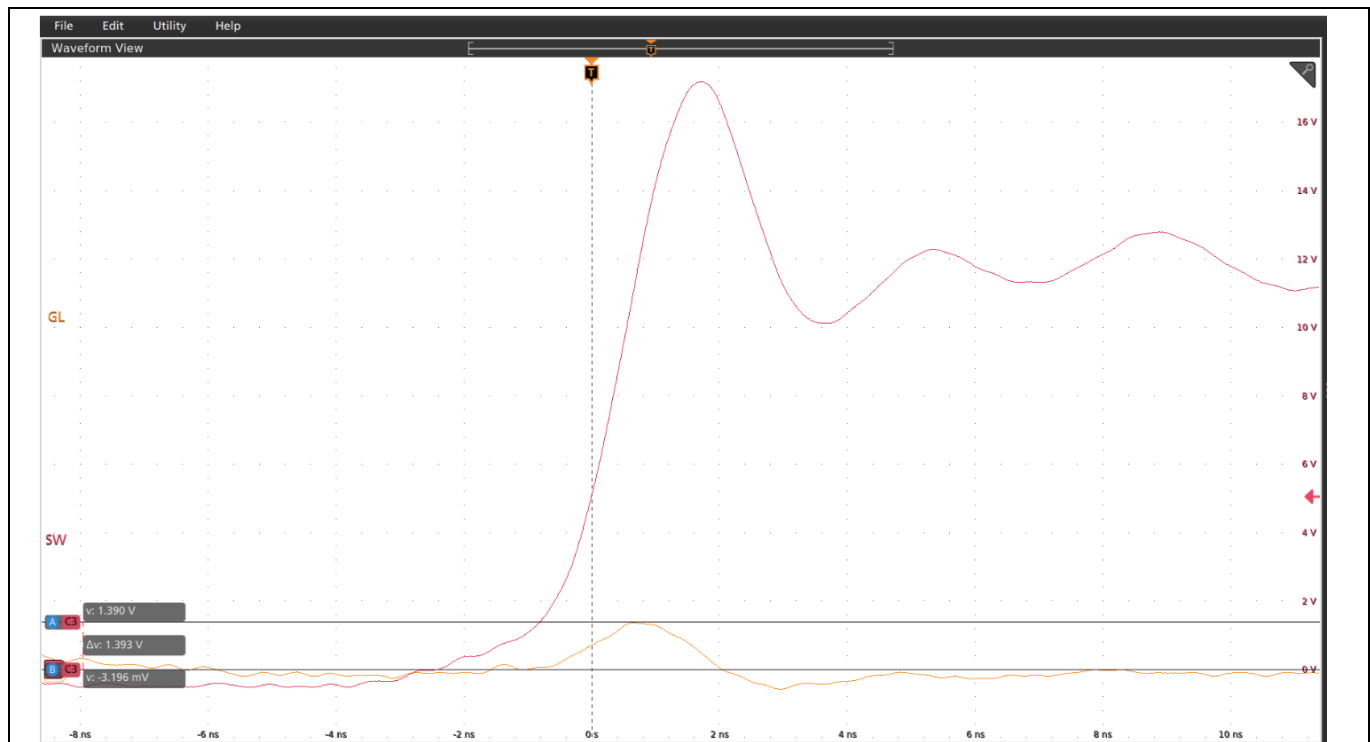


Figure 19 SW and GL, 25 A load, $f_{SW} = 800$ kHz

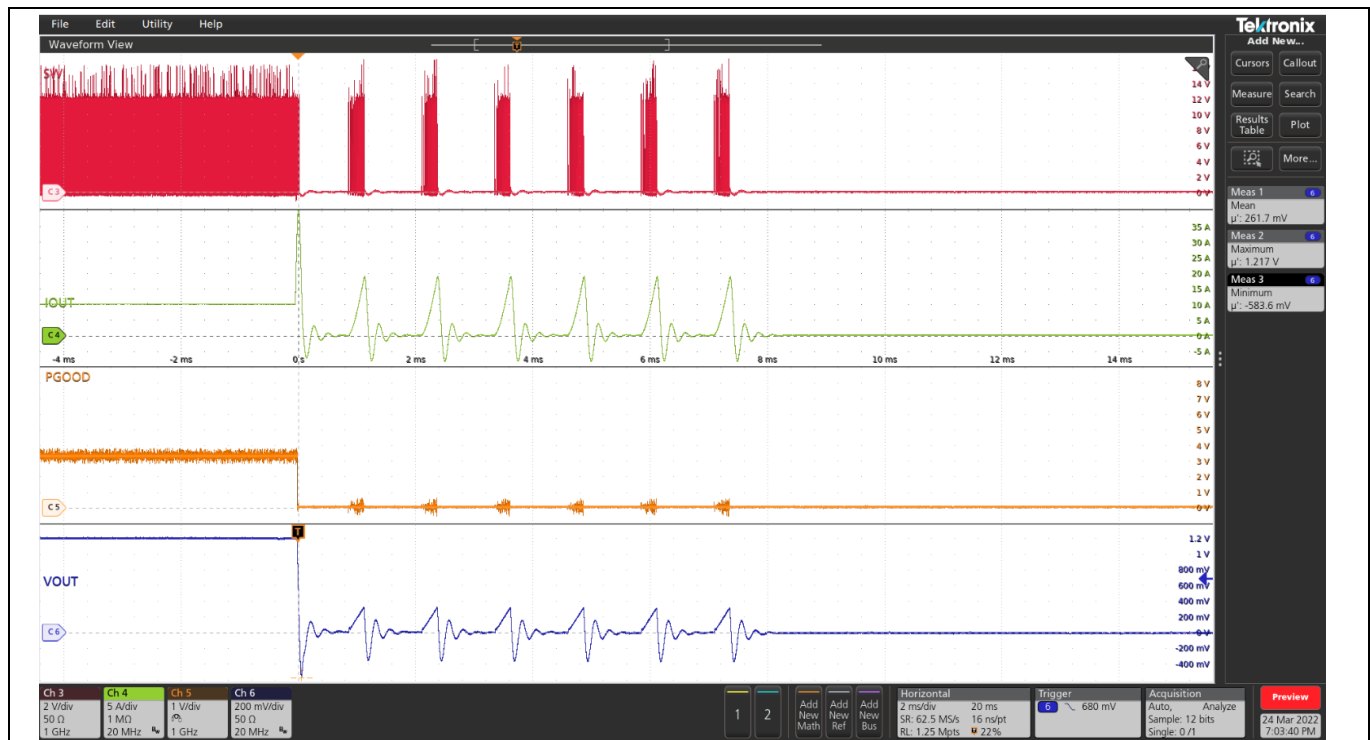


Figure 20 Short-circuit and retry six times and shut down (Ch₃: SW, Ch₄: I_{OUT}, Ch₅: P_{GOOD}, Ch₆: Vout)

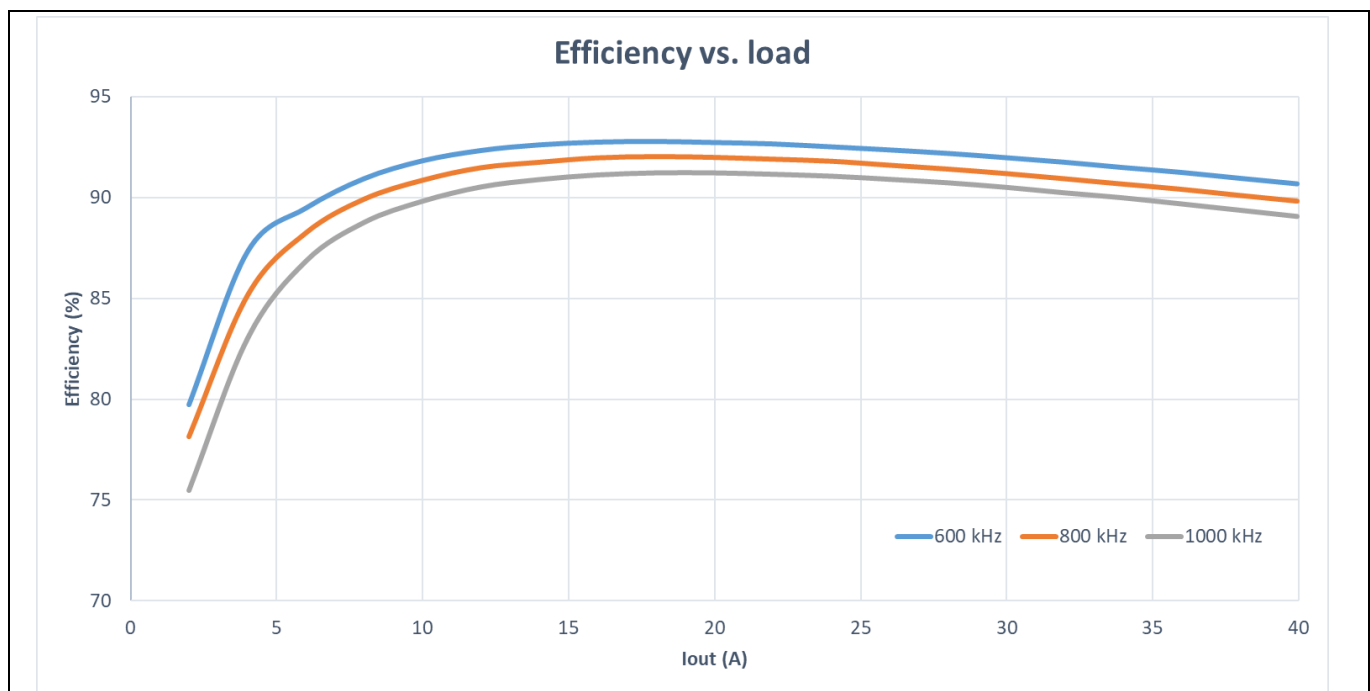


Figure 21 Efficiency vs. load current without airflow in FCCM with external V_{CC} (12 V P_{VIN}, V_{OUT} = 1.2 V, no airflow, 150 nH, 600 kHz/800 kHz/1000 kHz, T_a = 25°C)

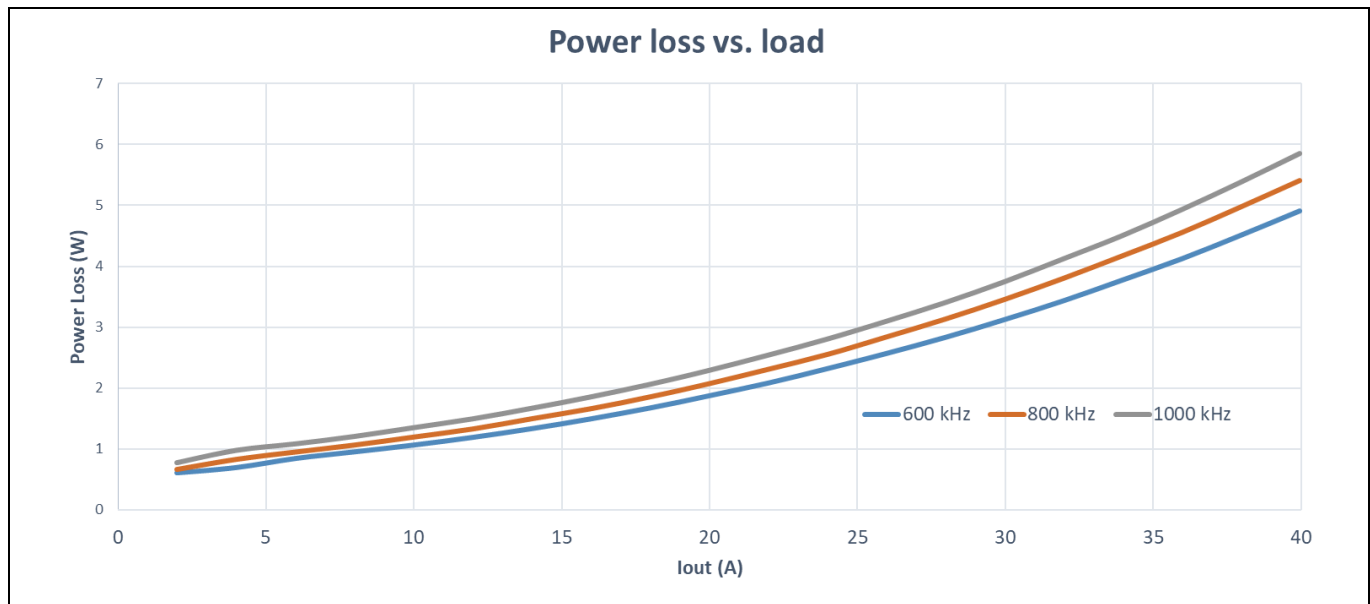


Figure 22 Power loss vs. load current without airflow in FCCM with external V_{CC} (12 V P_{VIN} , 1.2 V V_{OUT} , no airflow, 150 nH, 600 kHz/800 kHz/1000 kHz, $T_a = 25^\circ\text{C}$)

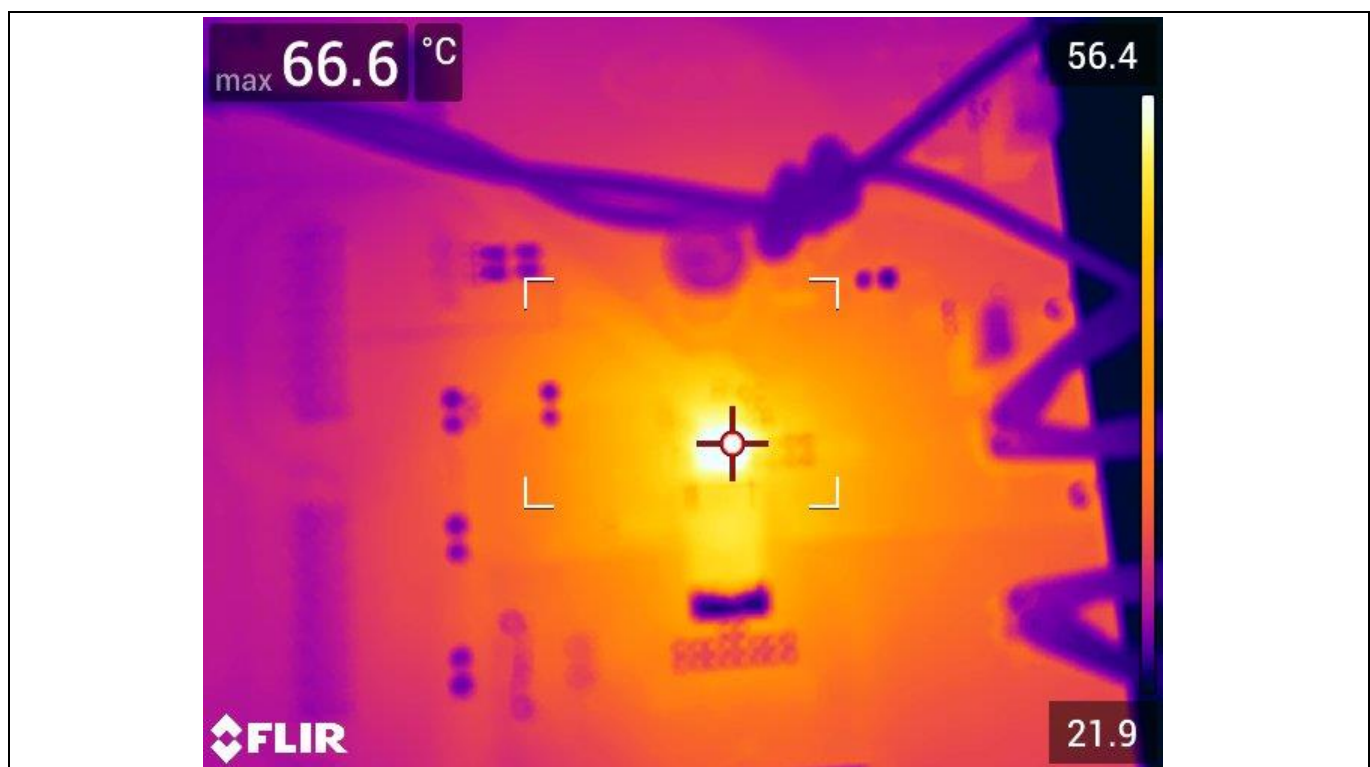


Figure 23 Thermal image of the board at 1.2 V 40 A load TDA38740 = 66.6°C, L = 47.3°C, $T_a = 21.9^\circ\text{C}$, natural convection, $f_{sw} = 1000$ kHz

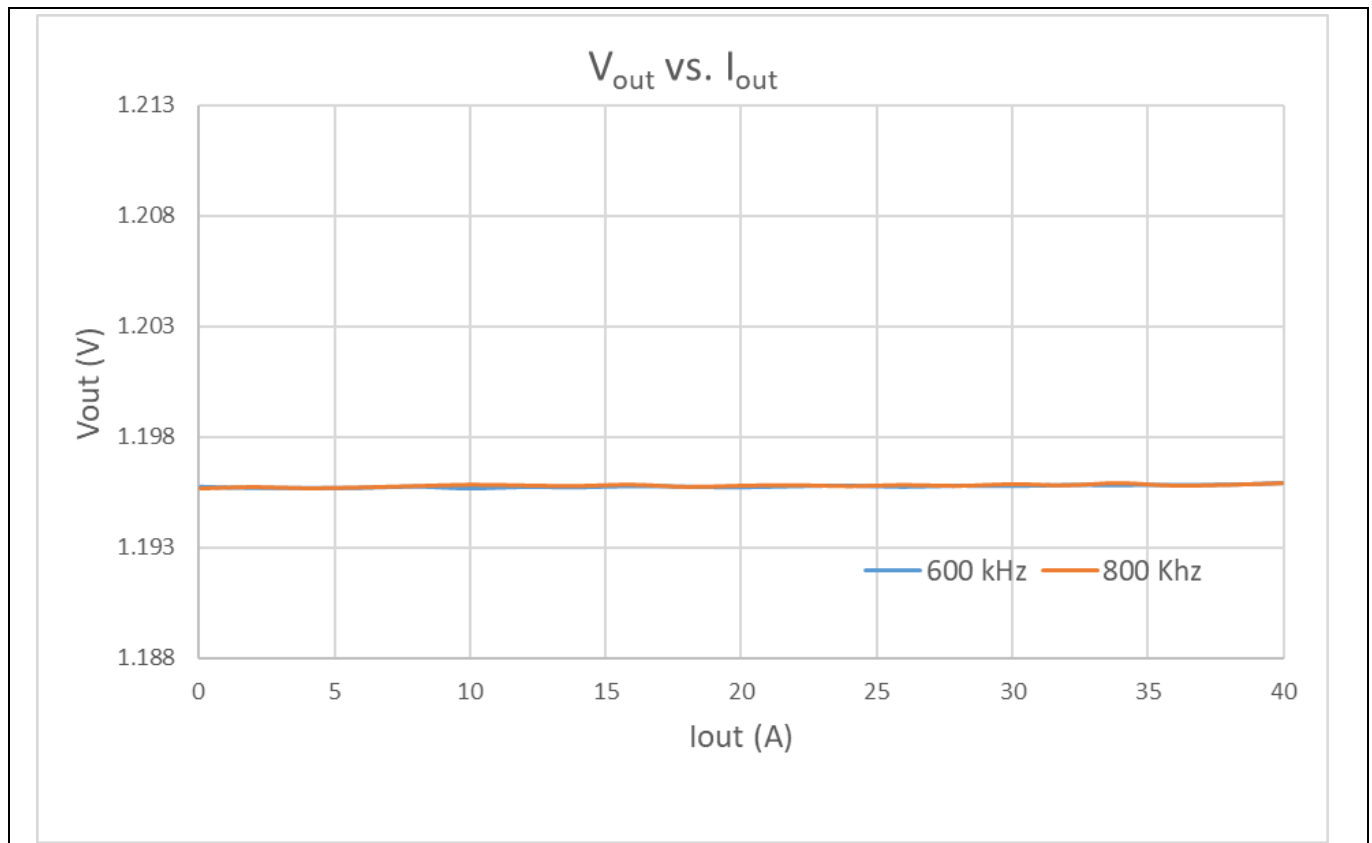


Figure 24 TDA38740 V_{OUT} regulation (12 V P_{VIN}, 1.2 V V_{OUT}, no airflow, 150 nH, 600/800 kHz, T_a = 25°C)

2.2 $P_{VIN} = 12.0\text{ V}$, $V_{OUT} = 3.3\text{ V}$, $I_{OUT} = 0\text{ to }25\text{ A}$, room temperature, no airflow

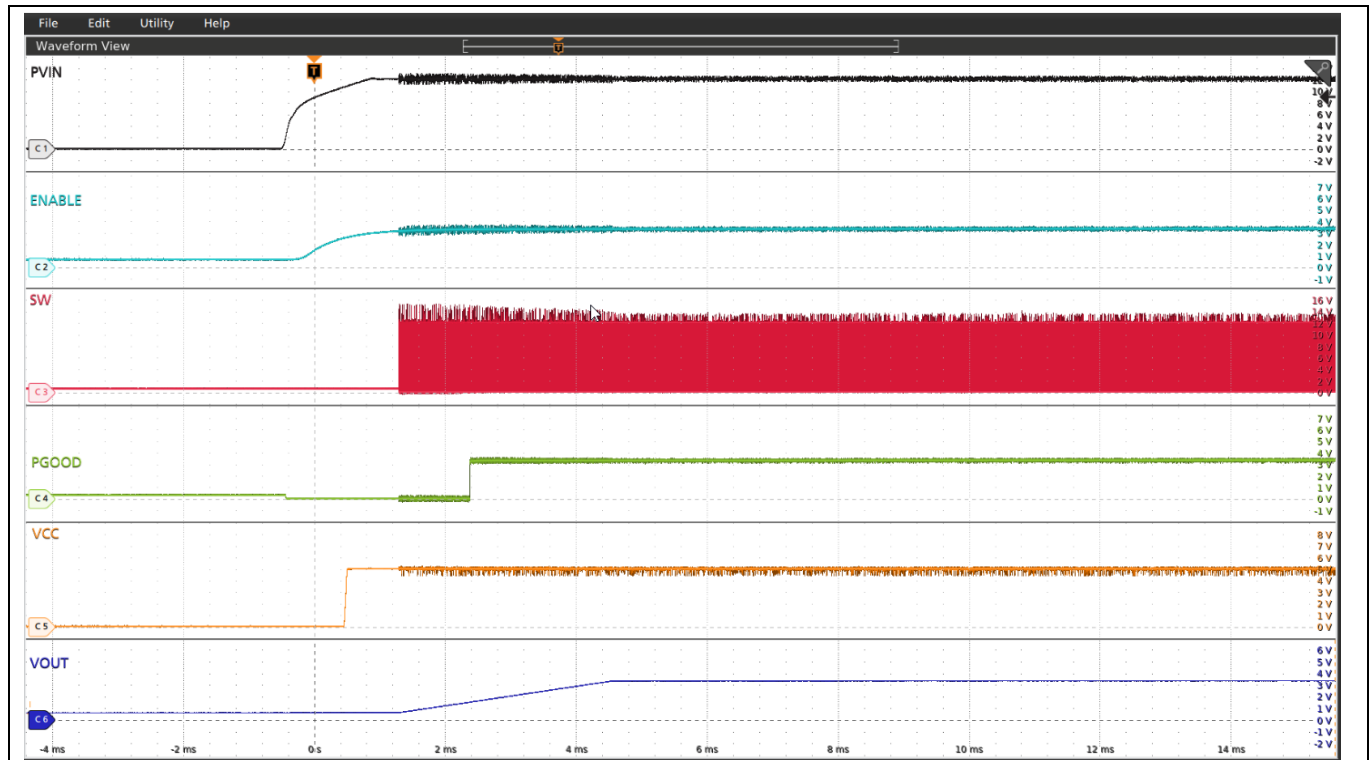


Figure 25 Start-up at 3.3 V V_{OUT} 0 A load (Ch₁: P_{VIN} , Ch₂: enable, Ch₃: switch node, Ch₄: P_{GOOD} , Ch₅: V_{DRV} , Ch₆: V_{OUT})

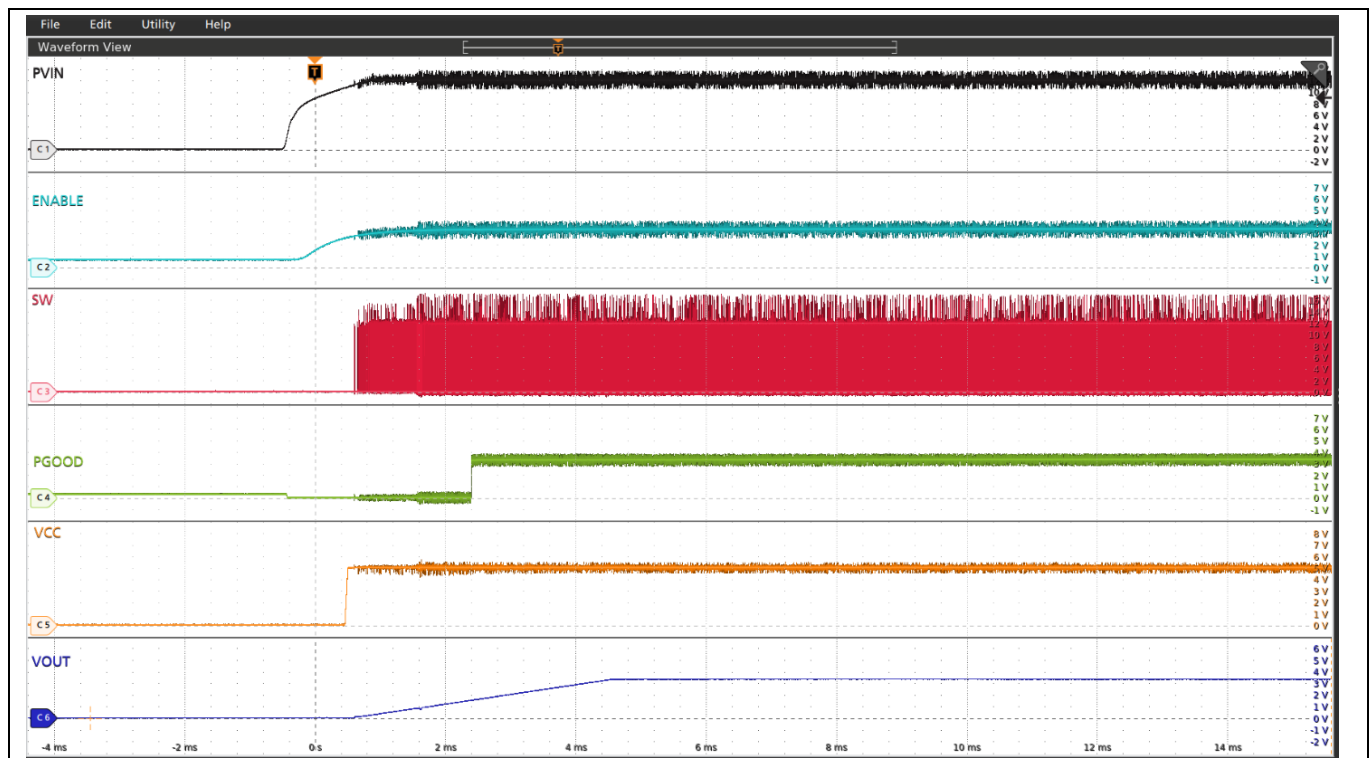


Figure 26 Start-up at 3.3 V V_{OUT} 20 A load (Ch₁: P_{VIN} , Ch₂: enable, Ch₃: switch node, Ch₄: P_{GOOD} , Ch₅: V_{DRV} , Ch₆: V_{OUT})

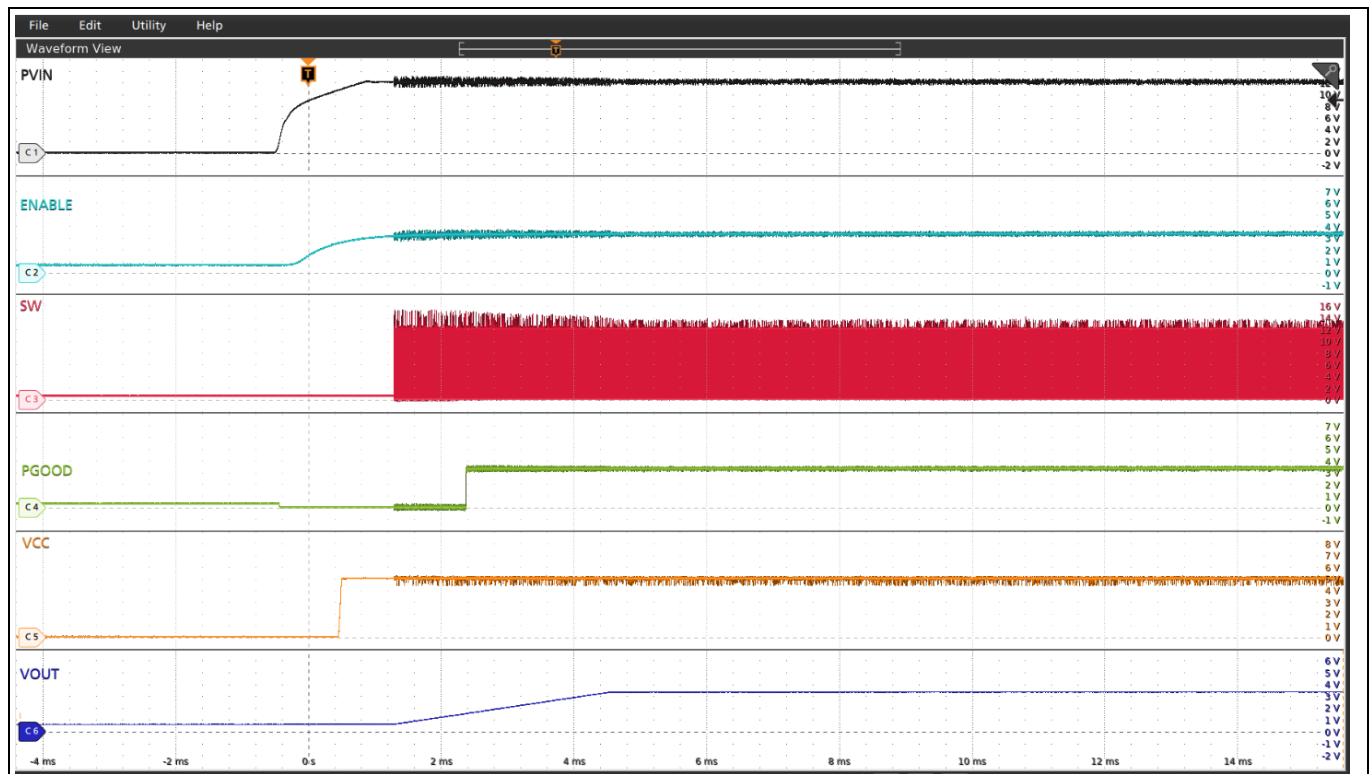


Figure 27 Pre-bias start-up at 3.3 V 0 A (Ch₁: P_{VIN}, Ch₂: enable, Ch₃: switch node, Ch₄: P_{GOOD}, Ch₅: V_{DRV}, Ch₆: V_{OUT})

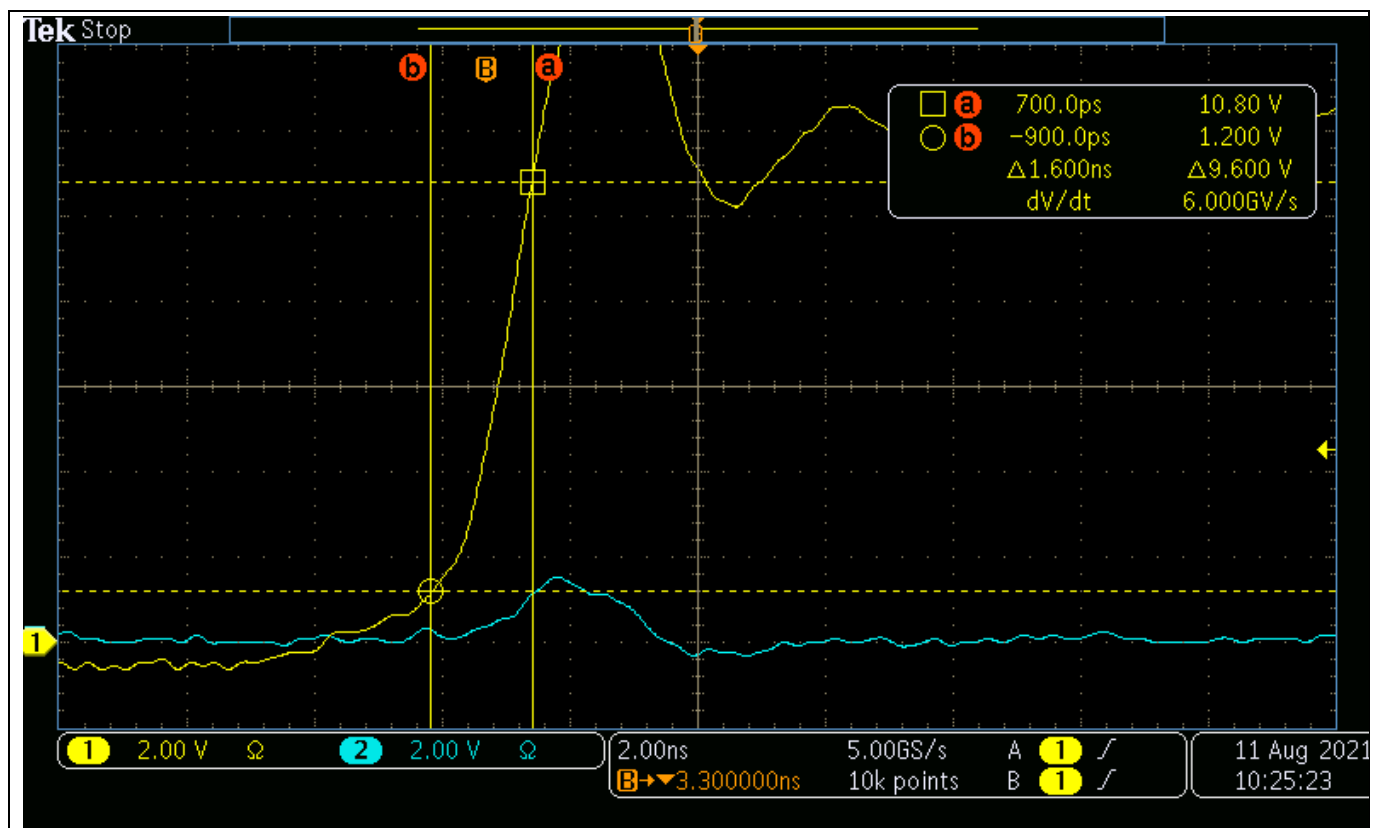


Figure 28 SW and GL, 30 A load, $f_{sw} = 800 \text{ kHz}$

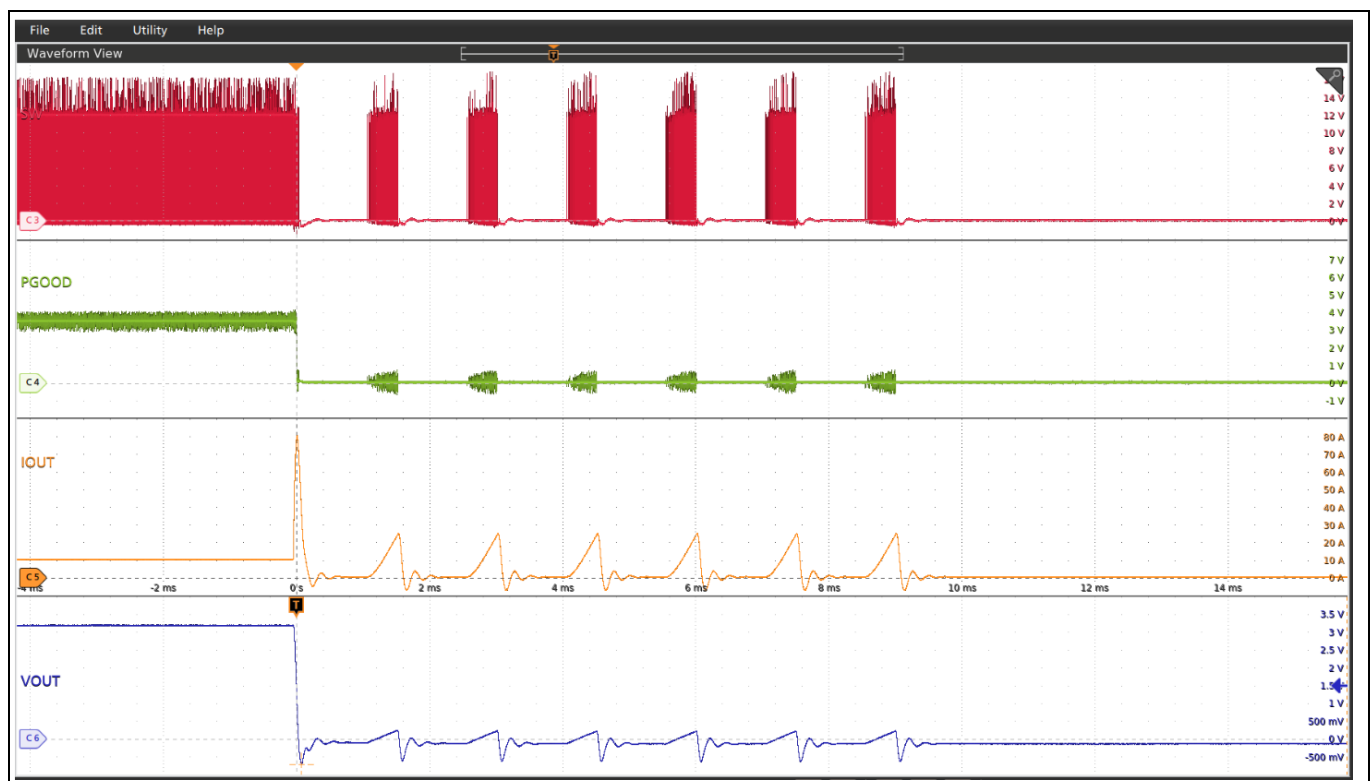


Figure 29 Short-circuit and retry six times and shut down (Ch₃: SW, Ch₄: I_{OUT}, Ch₅: P_{GOOD}, Ch₆: V_{OUT})

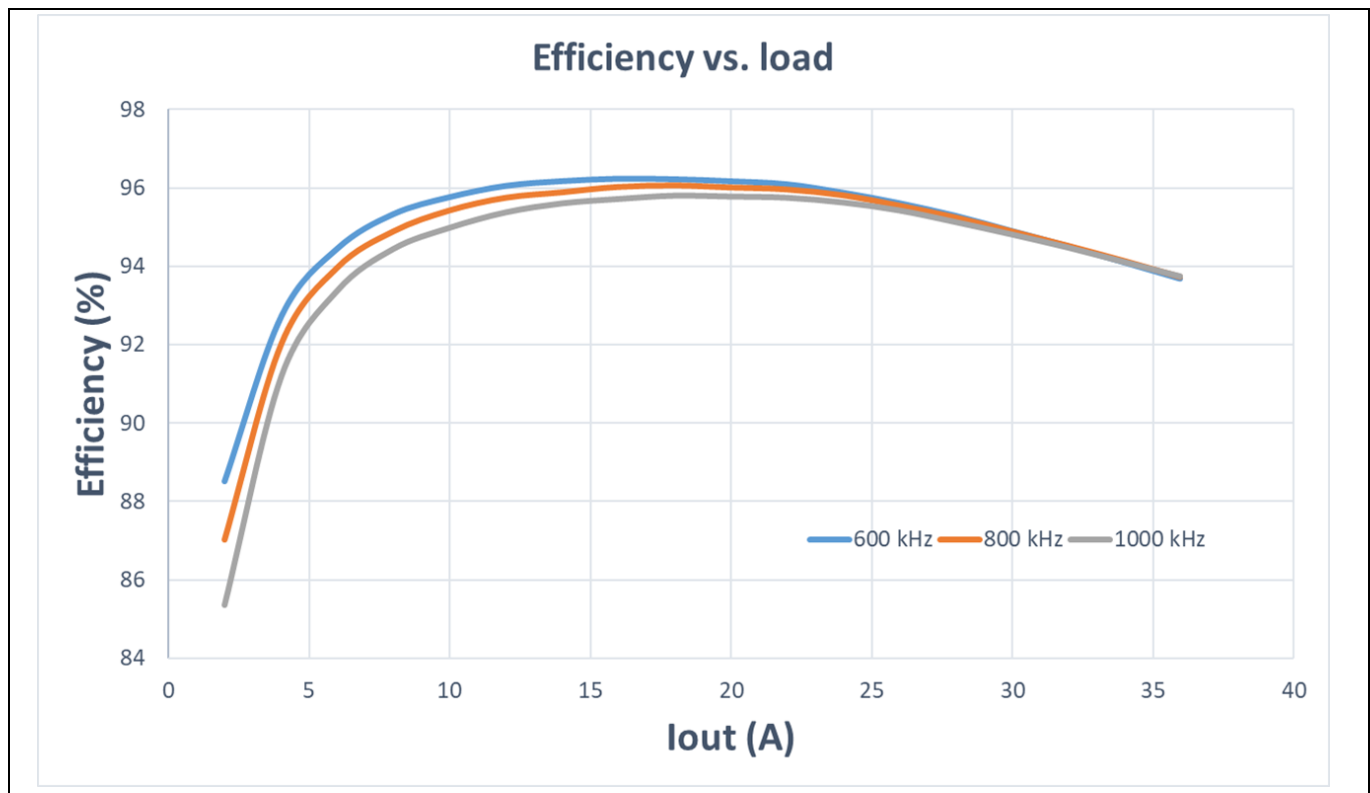


Figure 30 Efficiency vs. load current without airflow in FCCM with external V_{CC} (12 V P_{VIN}, V_{OUT} = 3.3 V, no airflow, 150 nH, 600 kHz/800 kHz/1000 kHz, T_a = 25°C)



Figure 31 Power loss vs. load current without airflow in FCCM with external V_{CC} (12 V P_{VIN} , 3.3 V V_{OUT} , no airflow, 150 nH, 600 kHz/800 kHz/1000 kHz, $T_a = 25^\circ\text{C}$)

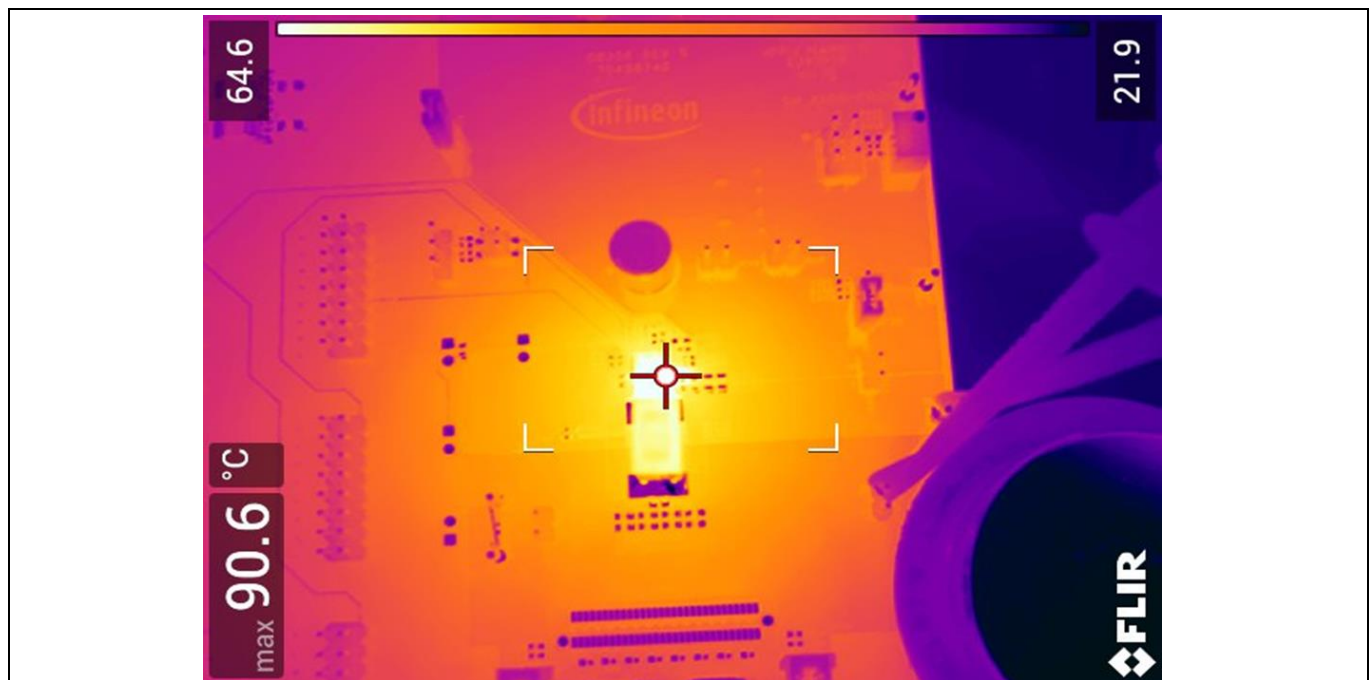


Figure 32 Thermal image of the board at 3.3 V 35 A load TDA38740 = 90.6°C, L = 61.3°C, $T_a = 22.3^\circ\text{C}$, natural convection, $f_{sw} = 1000 \text{ kHz}$

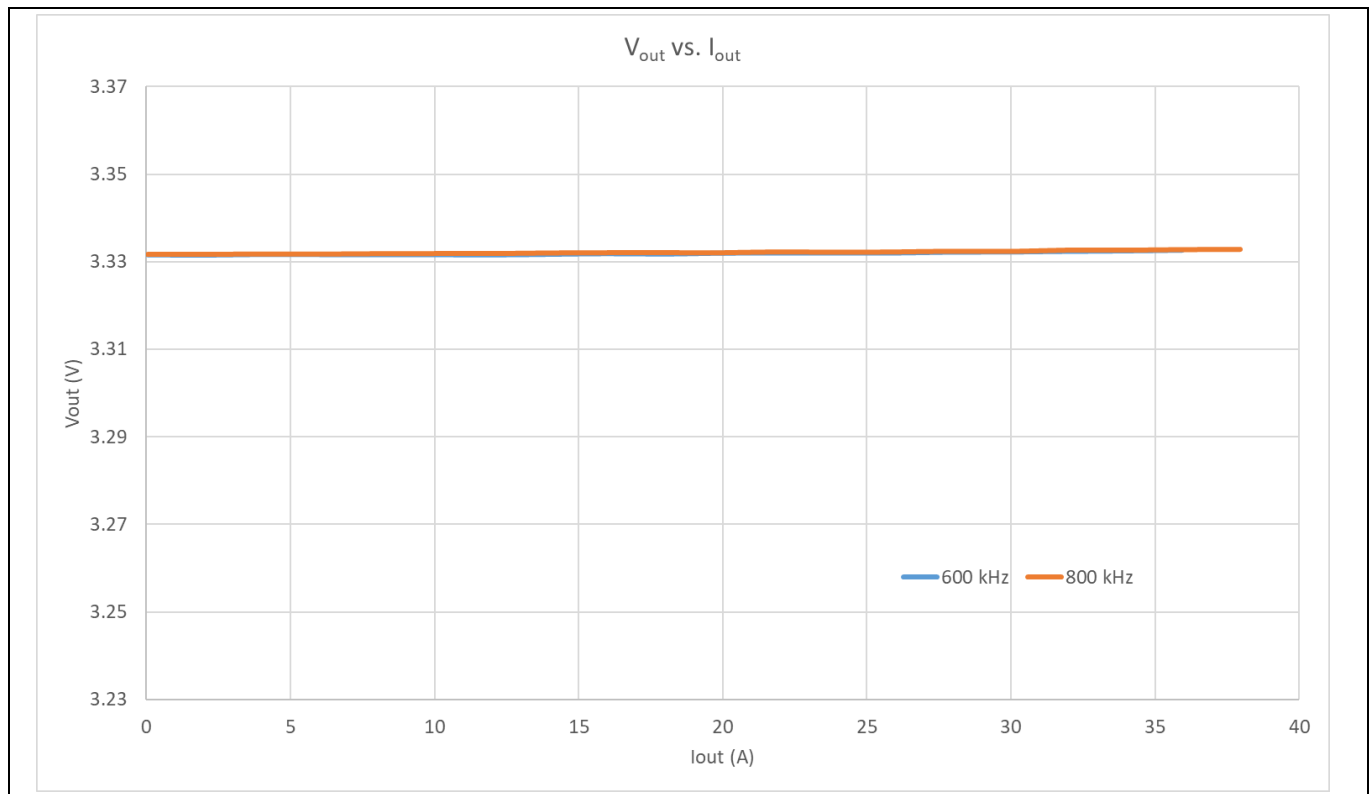


Figure 33 TDA38740 V_{OUT} regulation (12 V P_{VIN} , 3.3 V V_{OUT} , no airflow, 150 nH, 600/800 kHz, $T_a = 25^\circ\text{C}$)

Revision history

Document version	Date of release	Description of changes
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