IRPS5401 Errata Final Silicon

PSS DCDC Enterprise Power
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IRPS5401 Errata Final Si --Summary

- Last 24 bits not restored correctly from NVM during Power On Reset (POR)
- READ_IOUT PMBus command returns non-zero value when VOUT is off
- IOUT_OC_WARNING bit is set in STATUS_IOUT register at start up
- OCP shutdown causes VOUT_OV_WARNING bit to be set in STATUS_VOUT register
- Do not use +0, +1 and +2 offsets for applications that require cold temp operation (<0°C)
- I2C/PMBus is not tolerant of the Data changing between the Start Symbol and the first Data bit while the Clock is low.
- Scanning reserved I2C addresses, 04h to 07h (7bit), will cause the lsb of the de_off_time_adj register in each switcher loop to be set to 1. The off time of the LSFET in DE Mode will increase by 62nsec (if this bit was not already set to 1)
- PMBus commands VOUT_TRIM, MARGIN_HIGH, and MARGIN_LOW are not stored in OTP
- At starting temperatures of <0°C, extra time is required after 5V Vcc becomes available to ensure a reliable start-up.

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Item	Errata Description			
1	Errata	During Power On Reset (POR), the last 24 bits of data stored in NVM are not restored correctly to the working registers. These 24 bits affect PMBus commands related to the LDO output		
	Issue	**LDO PMBus command bits not restored correctly**	**Data Source in NVM**	**Acceptable Values in Source Registers**
		STATUS_INPUT mask [7:5]	VIN_UV_WARN_LIMIT; bits 6 to 8	**Set to 0.** Since VIN_UV_WARN_LIMIT bits 6 through 9 must be set to 0, the largest value that can be set without causing an issue is 0xC83F ➔ 0.49V.
		STATUS_TEMPERATURE mask[7:6]	POWER_GOOD_ON; bit 0	
			VIN_UV_WARN_LIMIT; bit 9	
		STATUS_CML mask [7:1]	POWER_GOOD_ON; bits 1 to 7	**Set bits 1, 5, 6, and 7 to 0.** Bits 2, 3 and 4 can be set to 1 because the corresponding CML mask bits are not supported. Bits 8 to 11 can be set to 1 if a PG delay is acceptable The table below shows allowable values
				VOUT_MODE = -8 / (recommended)VOUT_MODE = -9
		MFR_TPGDLY[3:0]	POWER_GOOD_ON; bits 8 to 11	0x001C➔ 0.1V, 0msec PG delay / 0x0100➔ 0.5V, 1msec PG delay
				0x0100➔ 1V, 1msec PG delay / 0x0200➔ 1V, 2msec PG delay
				0x0200➔ 2V, 2msec PG delay / 0x0300➔ 1.5V, 3msec PG delay
				0x0300➔ 3V, 3msec PG delay / 0x0400➔ 2V, 4msec PG delay
		MFR_LDO_MARGIN[7:0]	POWER_GOOD_OFF; bits 0 to 3	**Set to 0.** Any POWER_GOOD_OFF value that is smaller than the POWER_GOOD ON value and has bits 0 to 3 = 0 is acceptable
			POWER_GOOD_ON; bits 12 to 15	**Set to 0.** These bits will always = 0 as they would set a POWER_GOOD_ON threshold that would too large if set to 1
		NOTE** Affects Source Only mode; POWER_GOOD_ON and OFF commands are irrelevant in Tracking mode…see below		
	Workaround	Configure NVM bits (Source registers) so that the affected registers have acceptable data		
	Corrective Action	None		

In Tracking mode, set POWER_GOOD_ON & OFF commands to 0. They are fixed thresholds set by VIN

power_good_on: Non-tracking mode: this command sets the output voltage above which the Power Good indication is asserted. Tracking mode: the Power Good On threshold is fixed at 87.5% of (VIN/2). Resolution is specified by VOUT_MODE in non-tracking

power_good_off: Non-tracking mode: this command sets the output voltage below which the Power Good indication is de-asserted. Tracking mode: the Power Good Off threshold is fixed at 81.25% of (VIN/2). Resolution is specified by VOUT_MODE.

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Item	Errata Description	
2	Errata:	Internal Switcher outputs will report IOUT when the output has been shut off with EN pin, OPERATION command or VOUT_COMMAND to 0V (<250mV)
	Issue:	Sending a READ_IOUT command to an 'off' output results in non-0A IOUT being reported
	Workaround:	Do not sent READ_IOUT command to 'off' output
	Corrective Action:	none
3	Errata:	IOUT_OC_WARNING bit is set in STATUS_IOUT register during a start up into a 0A load
	Issue:	SM_ALERT asserts and IOUT_OC_WARNING bit is 'falsely' set at startup
	Workaround:	Send CLEAR_FAULTS command after start up
	Corrective Action:	none
4	Errata:	VOUT_OV_WARNING bit is set in STATUS_VOUT register when an OCP event occurs
	Issue:	VOUT_OV_WARNING bit is falsely set due to an OCP event
	Workaround:	None required. An enable pin cycle, OPERATION off/on cycle or CLEAR_FAULTS command is required to reset the ALERT# line, OC_WARN, and OC_FAULT STATUS bits after an OCP event. These same operations will clear the OV_WARNING STATUS bit at the same time
	Corrective Action:	None
5	Errata:	For applications where the ambient temperature is below 0°C, address offset and MTP offset values of +0, +1 and +2 are not available
	Issue:	There is a small risk that the LSADC will not correctly decode the voltage on the external resistor at temperatures below 0°C
	Workaround:	For applications with T_{amb} always > 0°C: none required For applications with T_{amb} may be < 0°C: for the ADDR_PROT pin and MTP pin, do not use resistor values that represent offsets +0, +1, and +2. When creating *.mic files, (MTP pin) load segments +0, +1 and +2 with 'filler' data. As an example, use the same file that will be programmed into the +3 location as the file that is programmed into the +0, +1 and +2 locations
	Corrective Action:	None

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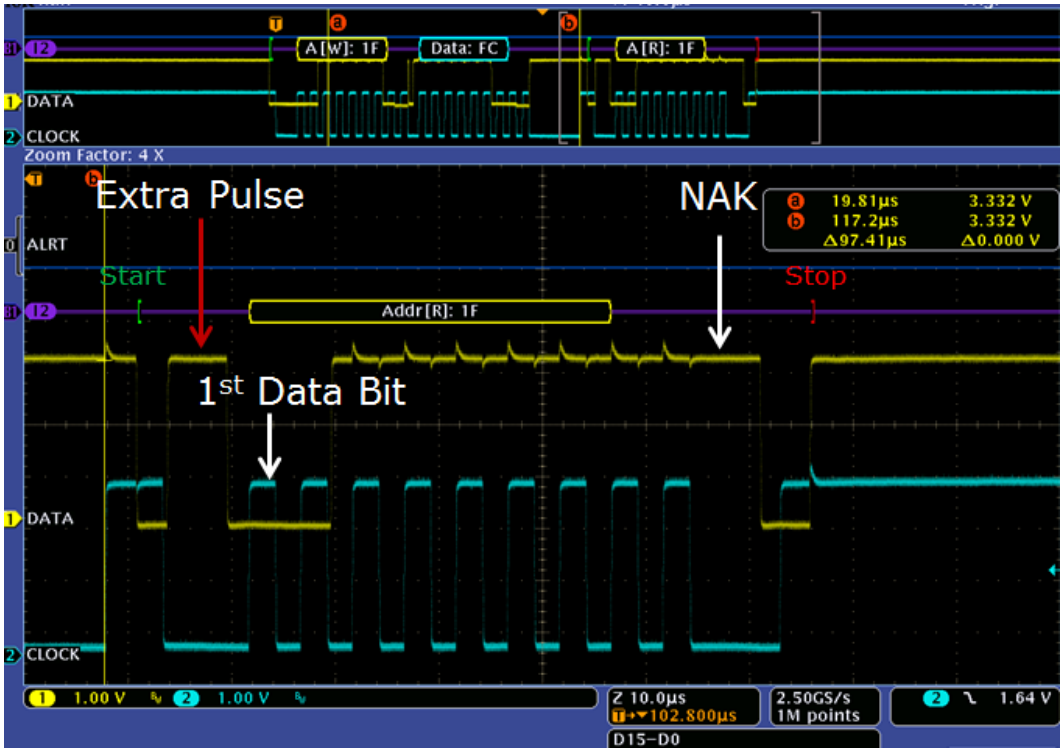
Item	Errata Description	
6	Errata:	I2C/PMBus is not tolerant of the Data changing between the Start Symbol and the first Data bit while the Clock is low.
	Issue:	If a low-high-low pulse on DATA occurs between a Start (or Repeated Start) symbol and the 1st data bit while clock is low, the device will NAK the transaction.
	Workaround:	The I2C/PMBus Master should avoid issuing an extra pulse following the Start Symbol while the clock is low
	Corrective Action:	Will not be fixed



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Item	Errata Description	
7	Errata:	Enabling I2C Hs-mode inadvertently causes the setting of bit 0 in register 28h for all four of the switching outputs
	Issue:	Enabling I2C HS-mode is supposed to set bit 0 in register 28h of the common area. An error in the logic causes the request to set bit 0 to be broad cast to all loop pages. Resulting in bit 0 being set in register 28h on pages 0 to 3 (all loop areas) instead of in the common area. Setting bit 0 of reg 28h will result in the adjusted off time during DE mode to be increased by 62nsec
	Workaround:	1. Do not scan the reserved addresses 04h to 07h (7bit). The 8b0000_1xxx seen by the controller in the address byte is the I2C HS-mode indicator 2. Ensure that bit 0 in Reg 0x0028 is set to 1 if operating the I2C bus at speeds above 400KHz is required
	Corrective Action:	Will not be fixed
8	**Errata:**	PMBUS commands VOUT_TRIM, MARGIN_HIGN and MARGIN_LOW are not backed up with an OTP location
	Issue:	It is not possible to store these commands in OTP. The value will not be restored after a 5V POR. A programmed value will be available as long as the 5V VCC is high
	Workaround:	Adjust the VOUT_COMMAND value by the amount that would have been written to VOUT_TRIM
	Corrective Action:	Will not be fixed
9	**Errata:**	**At starting temperatures of <0°C, extra time is required after 5V Vcc becomes available to ensure a reliable start-up.**
	Issue:	The OCP circuit does not start up correctly at lower temperatures. An OCP fault may be declared immediately at start up
	Workaround:	The start up must be delayed by 60ms after 5V VCC is applied. The delay can be done by delaying the EN pin or using the TON_DELAY command
	Corrective Action:	Will not be fixed

Revision History

VER	Description of Change	Date	Apps	Approved
1.0	Initial release	6/14/2016	D. Caron	
1.1	Add CLEAR_FAULTS to Item 4	6/20/2016	D. Caron	
1.2	Update Item 2 with additional Detail and correct VIN_UV_WARN_LIMIT bit error	7/16/2017	D. Caron	
1.3	Add item 5, address offset and MTP offset +0, +1 and +2 are not available	5/18/2017	D. Caron	
1.4	Add item 6…extra DIO pulse errata	4/9/2018	D. Caron	
1.5	Add item 7, HSMODE errata	1/23/2019	D. Caron	
1.6	Add item 8, no OTP for VOUT_TRIM	8/14/2020	D. Caron	
1.7	Add MARGIN_HIGH and LOW to item 8 Add cold temp start issue	1/11/2021	D. Caron	
1.8	Change wording for item 9	1/12/2021	D. Caron	