IRPS5401 Errata

About this document

Scope and purpose

Documentation of errata items for the PMIC IRPS5401.

Intended audience

Designers and FAEs working with the IRPS5401.

Table of contents

1 Errata overview

Table 1 Errata listing

Erratum no.	Type	Description
1	24-bit restoration	Last 24 bits not restored correctly from NVM (non-volatile memory) during Power-On-Reset (POR)
2	Non-zero READ_IOUT value	READ_IOUT PMBus command returns non-zero value when V_{OUT} is off
3	IOUT_OC_WARNING bit	IOUT_OC_WARNING bit is set in STATUS_IOUT register at start-up
4	VOUT_OV_WARNING bit	OCP (Over Curren Protection) shut-down causes VOUT_OV_WARNING bit to be set in STATUS_VOUT register
5	Cold temperature	Do not use +0, +1 and +2 offsets for applications that require cold-temperature operation (less than 0°C)
6	I^2C communication	I^2C/PMBus is not tolerant of the data changing between the start symbol and the first data bit while the clock is low
7	Diode emulation off-time	Scanning reserved I^2C addresses, 04 h to 07 h (7 bit), will cause the LSB (Least Significant Bit) of the de_off_time_adj register in each switcher loop to be set to 1. The off-time of the LSFET in DE mode will increase by 62 ns (if this bit was not already set to 1)

2 Detailed explanation of errata

2.1 Last 24-bit restoration

Erratum: When performing a POR data will be transferred from MTP (Multiple-times Programmable) to the working memory. During POR, the last 24 bits of data stored in NVM are not restored correctly to the working registers. These 24 bits affect PMBus commands related to the LDO output.

Issue:

LDO PMBus command bits not restored correctly	Data Source in NVM	Acceptable Values in Source Registers	
STATUS_INPUT mask [7:5]	VIN_UV_WARN_LIMIT; bits 6 to 8	**Set to 0.** Since VIN_UV_WARN_LIMIT bits 6 through 9 must be set to 0, the largest value that can be set without causing an issue is 0xC83F → 0.49V.	
STATUS_TEMPERATURE mask[7:6]	POWER_GOOD_ON; bit 0		
	VIN_UV_WARN_LIMIT; bit 9		
STATUS_CML mask [7:1]	POWER_GOOD_ON; bits 1 to 7	**Set bits 1, 5, 6, and 7 to 0.** Bits 2, 3 and 4 can be set to 1 because the corresponding CML mask bits are not supported. Bits 8 to 11 can be set to 1 if a PG delay is acceptable The table below shows allowable values	
		VOUT_MODE = -8	(recommended)VOUT_MODE = -9
MFR_TPGDLY[3:0]	POWER_GOOD_ON; bits 8 to 11	0x001C→ 0.1V, 0msec PG delay	0x0100→ 0.5V, 1msec PG delay
		0x0100→ 1V, 1msec PG delay	0x0200→ 1V, 2msec PG delay
		0x0200→ 2V, 2msec PG delay	0x0300→ 1.5V, 3msec PG delay
		0x0300→ 3V, 3msec PG delay	0x0400→ 2V, 4msec PG delay
MFR_LDO_MARGIN[7:0]	POWER_GOOD_OFF; bits 0 to 3	**Set to 0.** Any POWER_GOOD_OFF value that is smaller than the POWER_GOOD ON value and has bits 0 to 3 = 0 is acceptable	
	POWER_GOOD_ON; bits 12 to 15	**Set to 0.** These bits will always = 0 as they would set a POWER_GOOD_ON threshold that would too large if set to 1	

Figure 1 Bit restoration errors

POWER_GOOD_ON and POWER_GOOD_OFF commands are not affected in tracking mode.

In tracking mode, set POWER_GOOD_ON and POWER_GOOD_OFF command values to “0”. These thresholds are fixed values set by V_{IN}. The POWER_GOOD_ON threshold is then 87.5 percent of $V_{IN}/2$. The POWER_GOOD_OFF threshold is 81.25 percent of $V_{IN}/2$.

Workaround: Configure NVM bits (source registers) so that the affected registers have acceptable data.

Corrective action: None.

2.2 Non-zero READ_IOUT value

Erratum: Internal switcher outputs will report I_{OUT} when the output has been shut off with the EN pin, OPERATION command or VOUT_COMMAND to 0 V (less than 250 mV).

Issue: Sending a READ_IOUT command to an “off” output results in non-0 A I_{OUT} being reported.

Workaround: Do not sent READ_IOUT command to “off” output.

Corrective action: None.

2.3 IOUT_OC_WARNING bit

Erratum: IOUT_OC_WARNING bit is set in STATUS_IOUT register during a start-up into a 0 A load.

Issue: SM_ALERT asserts an IOUT_OC_WARNING bit is “falsely” set at start-up.

Workaround: Send CLEAR_FAULTS command after start-up.

Corrective action: None.

2.4 VOUT_OV_WARNING bit

Erratum: VOUT_OV_WARNING bit is set in STATUS_VOUT register when an OCP event occurs.

Issue: VOUT_OV_WARNING bit is falsely set due to an OCP event.

Workaround: None required. An enable pin cycle, OPERATION off/on cycle or CLEAR_FAULTS command is required to reset the ALERT# line, OC_WARN and OC_FAULT STATUS bits after an OCP event. These operations will clear the OV_WARNING STATUS bit at the same time.

Corrective action: None.

2.5 Cold temperature

Erratum: For applications where the ambient temperature is below 0°C, address offset and MTP offset values of +0, +1 and +2 are not available.

Issue: There is a small risk that the LSADC will not correctly decode the voltage on the external resistor at temperatures below 0°C.

Workaround: For applications with T_{amb} always more than 0°C: none required.
For applications with T_{amb} that may be less than 0°C: for the ADDR_PROT pin and MTP pin, do not use resistor values that represent offsets +0, +1 and +2. When creating *.mic files, (MTP pin) load segments +0, +1 and +2 with “filler” data. As an example, use the same file that will be programmed into the +3 location as the file that is programmed into the +0, +1 and +2 locations.

Corrective action: None.

2.6 I²C communication

Erratum: I²C/PMBus is not tolerant of the DATA changing between the start symbol and the first data bit while the clock is low.

Issue: If a low-high-low pulse on DATA occurs between a start (or repeated start) symbol and the first data bit while the clock is low, the device will NAK (Not acknowledge) the transaction.

Workaround: The I²C/PMBus master should avoid issuing an extra pulse following the start symbol while the clock is low.

Corrective action: None.

Detailed explanation of errata

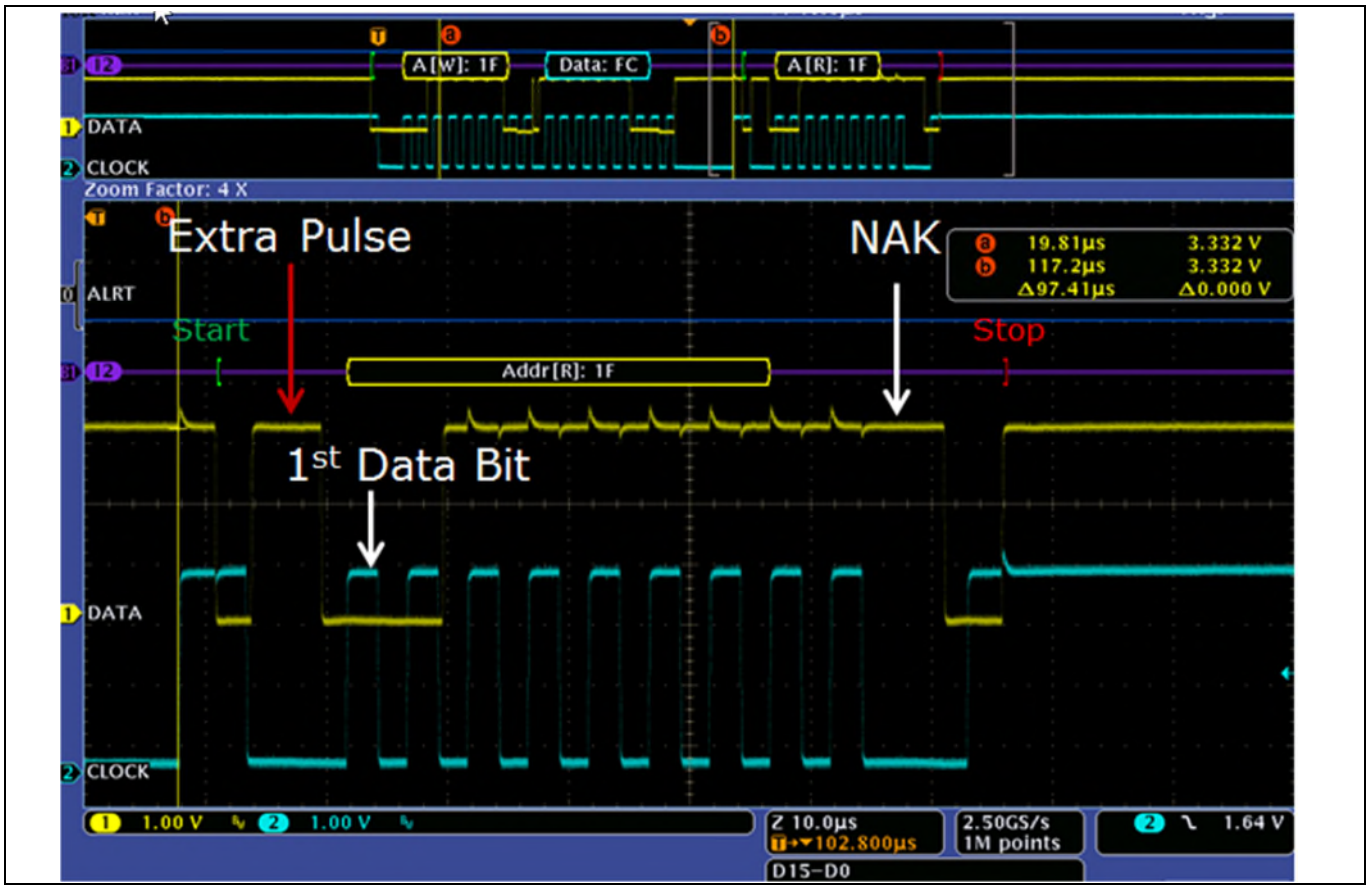

Figure 2 I²C extra pulse error

Proposed workaround:

The problem with having an extra pulse before the first clock pulse is not that an active pulsing of the data line is happening, rather than the idle state setting for the data line. If the default is low after the start condition was issued, there is no extra pulse. With a high as default and the first address bit (MSB) being “0”, an additional pulse has been created. To prevent this becoming a problem one can select addresses that begin with “1” in the MSB, i.e. 40 h or higher.

The USB005 dongle assumes that the PMBus address is bigger than the I²C address, or else it will not find the PMBus address during scanning.

Therefore, a recommended address setting for third-party interfaces is to set the I²C base address to 40 h and the PMBus base address to 50 h.

2.7 Diode emulation off-time

Erratum: Enabling I²C HS mode inadvertently causes the setting of bit 0 in register 28 h for all four of the switching outputs.

Issue: Enabling I²C HS mode is supposed to set bit 0 in register 28 h of the common area. An error in the logic causes the request to set bit 0 to be broadcast to all loop pages, resulting in bit 0 being set in register 28 h on pages 0 to 3 (all loop areas) instead of in the common area. Setting bit 0 of reg. 28 h will result in the adjusted off-time during DE mode being increased by 62 ns.

Workaround:

1. Do not scan the reserved addresses 04 h to 07 h (7 bit). The 8b0000_1xxx seen by the controller in the address byte is the I²C HS mode indicator.

2. Ensure that bit 0 in reg. 0 x 0028 is set to 1 if operating the I²C bus at speeds above 400 kHz is required.

Corrective action: None.

Revision history

Document version	Date of release	Description of changes
1.0	06/14/2016	Initial release
1.1	06/20/2016	Added CLEAR_FAULTS to item 4
1.2	07/06/2017	Updated item 2 with details and corrected VIN_UV_WARN_LIMIT bit error
1.3	05/18/2017	Added item 5, temperature sensitivity of MTP/ADDR offsets 0, 1 and 2
1.4	04/09/2018	Added item 6, extra pulse in I^2C communication
1.5	01/23/2019	Added item 7, I^2C HS mode affecting switches' off-time setting in DE mode

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Do you have a question about this document?

Email: erratum@infineon.com

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