FM4 Family

32-BIT Microcontroller
FM4
Peripheral Manual GDC Part

Errata Sheet

<table>
<tr><th>Page</th><th>Item</th><th>Description</th></tr>
<tr><td colspan="3">Original document code: MN709-00014-1v0-E</td></tr>
<tr><td colspan="3">Rev. 1.0 February 25, 2015</td></tr>
<tr><td>28</td><td>CHAPTER 2
4. Registers
4.5 GPCR4</td><td>“GPLLN: PLL feedback frequency division ratio setting bits” should be corrected as below.
(Error)
<table>
<tr><th>bit[6:0]</th><th>Description</th></tr>
<tr><td>000000</td><td>setting is prohibited</td></tr>
<tr><td>000001</td><td>setting is prohibited</td></tr>
<tr><td></td><td>setting is prohibited</td></tr>
<tr><td>0001011</td><td>setting is prohibited</td></tr>
<tr><td>0001100</td><td>1/13</td></tr>
<tr><td>0001101</td><td>1/14</td></tr>
<tr><td></td><td>1/(GPLLN[6:0] + 1)</td></tr>
<tr><td>0011111</td><td>1/32</td></tr>
<tr><td>010000</td><td>setting is prohibited</td></tr>
<tr><td></td><td>setting is prohibited</td></tr>
<tr><td>1111111</td><td>setting is prohibited</td></tr>
</table>
(Correct)
<table>
<tr><th>bit[6:0]</th><th>Description</th></tr>
<tr><td>000000
to
0001011</td><td>setting is prohibited</td></tr>
<tr><td>0001100</td><td>Division ratio: 1/13 (minimal value)</td></tr>
<tr><td>0001101</td><td>Division ratio: 1/14</td></tr>
<tr><td>(Continued)</td><td>Division ratio: 1/(GPLLN[6:0]+1)</td></tr>
<tr><td>1100011</td><td>Division ratio: 1/100 (maximum value)</td></tr>
<tr><td>1100100
to
1111111</td><td>setting is prohibited</td></tr>
</table></td></tr>
</table>

<table>
<tr><th>Page</th><th>Item</th><th>Description</th></tr>
<tr><td colspan="3">Rev. 2.0 September 04, 2015</td></tr>
<tr><td>6</td><td>The target products in this manual</td><td>“Table 4 TYPE4-M4 Product list” should be corrected as below.
(Error)
<table>
<tr><td rowspan="2">Description in this manual</td><td colspan="3">Flash memory size 384 Kbytes</td></tr>
<tr><td colspan="2">VRAM Size</td><td rowspan="2">VRAM 512 Kbytes
+
VFLASH 2 Mbytes</td></tr>
<tr><td>512 Kbytes</td><td>384 Kbytes</td></tr>
<tr><td rowspan="4">TYPE4-M4</td><td>S6E2D35G0AGB10
S6E2D35G0AGV20
S6E2D35G0AGZ20
S6E2D35J0AGV20
S6E2D35J0AGZ20</td><td>S6E2D35GAAGB10
S6E2D35GAAGV20
S6E2D35GAAGZ20
S6E2D35JAAGV20
S6E2D35JAAGZ20</td><td>S6E2D35GJAMV20</td></tr>
<tr><td>S6E2D55G0AGB10
S6E2D55G0AGV20
S6E2D55G0AGZ20
S6E2D55J0AGV20
S6E2D55J0AGZ20</td><td>S6E2D55GAAGB10
S6E2D55GAAGV20
S6E2D55GAAGZ20
S6E2D55JAAGV20
S6E2D55JAAGZ20</td><td>S6E2D55GJAMV20</td></tr>
<tr><td>S6E2DF5G0AGB10
S6E2DF5G0AGV20
S6E2DF5G0AGZ20
S6E2DF5J0AGV20
S6E2DF5J0AGZ20</td><td>S6E2DF5GAAG10
S6E2DF5GAAGV20
S6E2DF5GAAGZ20
S6E2DF5JAAGV20
S6E2DF5JAAGZ20</td><td>S6E2DF5GJAMV20</td></tr>
<tr><td>S6E2DH5G0AGB10
S6E2DH5G0AGV20
S6E2DH5G0AGZ20
S6E2DH5J0AGV20
S6E2DH5J0AGZ20</td><td>S6E2DH5GAAGB10
S6E2DH5GAAGV20
S6E2DH5GAAGZ20
S6E2DH5JAAGV20
S6E2DH5JAAGZ20</td><td>S6E2DH5GJAMV20</td></tr>
</table>
(Correct)
<table>
<tr><td rowspan="2">Description in this manual</td><td colspan="2">Flash memory size 384 Kbytes</td></tr>
<tr><td>VRAM 512 Kbytes</td><td>VRAM 512 Kbytes
+
VFLASH 2 Mbytes</td></tr>
<tr><td rowspan="4">TYPE4-M4</td><td>S6E2D35G0AGB30
S6E2D35G0AGV20
S6E2D35G0AGE20
S6E2D35J0AGV20</td><td>S6E2D35GJAMV20</td></tr>
<tr><td>S6E2D55G0AGB30
S6E2D55G0AGV20
S6E2D55G0AGE20
S6E2D55J0AGV20</td><td>S6E2D55GJAMV20</td></tr>
<tr><td>S6E2DF5G0AGB30
S6E2DF5G0AGV20
S6E2DF5G0AGE20
S6E2DF5J0AGV20</td><td>S6E2DF5GJAMV20</td></tr>
<tr><td>S6E2DH5G0AGB30
S6E2DH5G0AGV20
S6E2DH5G0AGE20
S6E2DH5J0AGV20</td><td>S6E2DH5GJAMV20</td></tr>
</table></td></tr>
</table>

<table>
<tr><th>Page</th><th>Item</th><th>Description</th></tr>
<tr><td>116</td><td>Appendixes
A.Register Map
1.Register Map
1.4 Clock/Reset</td><td>
The register of Clock/Reset should be corrected as indicated by shading bellow.

(Error)
<table>
<tr><td rowspan="2">Base_Address +
Address</td><td colspan="4">Register</td></tr>
<tr><td>+3</td><td>+2</td><td>+1</td><td>+0</td></tr>
<tr><td></td><td></td><td></td><td></td><td></td></tr>
<tr><td>0x068</td><td>-</td><td>-</td><td>-</td><td>INT_CLR[W]
-0-000</td></tr>
<tr><td>0x06C – 0xFFC</td><td>-</td><td>-</td><td>-</td><td>-</td></tr>
</table>
(Correct)
<table>
<tr><td rowspan="2">Base_Address +
Address</td><td colspan="4">Register</td></tr>
<tr><td>+3</td><td>+2</td><td>+1</td><td>+0</td></tr>
<tr><td></td><td></td><td></td><td></td><td></td></tr>
<tr><td>0x068</td><td>-</td><td>-</td><td>-</td><td>INT_CLR[W]
-0-000</td></tr>
<tr><td>0x06C – 0x070</td><td>-</td><td>-</td><td>-</td><td>-</td></tr>
<tr><td>0x074</td><td colspan="4">PLLCG_CTL[W]
-------- 11111111 00000000 00----00</td></tr>
<tr><td>0x078 – 0xFFC</td><td>-</td><td>-</td><td>-</td><td>-</td></tr>
</table>
</td></tr>
<tr><td>228</td><td>Appendixes
A.Register Map
1.Register Map
1.48 GDC Sub System SDRAM Controller</td><td>
Base_Address of GDC Sub system SDRAM controller should be corrected as indicated by the shading bellow.

(Error)
GDC Sub system SDRAM controller Base_Address : 0xD0A3_0000

(Correct)
GDC Sub System SDRAM Controller Base_Address : 0xD0A0_3000
</td></tr>
</table>

Page	Item	Description
Rev. 3.0 September 16, 2015		
12	1.Overview 1.1 Feature Summary 1.1.1 General features	Note should be added as indicated by the shading below. (Error) **1.1.1 General Features** ■ Controller for external graphics display. ■ Accelerator for 2D block image transfer (blit) operations. ■ Embedded SRAM video memory. ■ Multilayer GDC bus matrix with master and slave ports. ■ Signature computation for display content (use: data integrity/safety requirements) ■ Command Sequencer for graphic operations. ■ Quad SPI (Serial Peripheral Interface) for external memory extensions. ■ SDRAM interface for external memory extensions. ■ HBI (Hyper Bus Interface) interface for external memory extensions. ■ Two processing pipeline (blit / display). ■ Maximum core system clock frequency: Refer to the Data sheet. (Correct) **1.1.1 General Features** ■ Controller for external graphics display. ■ Accelerator for 2D block image transfer (blit) operations. ■ Embedded SRAM video memory. ■ Multilayer GDC bus matrix with master and slave ports. ■ Signature computation for display content (use: data integrity/safety requirements) ■ Command Sequencer for graphic operations. ■ Quad SPI (Serial Peripheral Interface) for external memory extensions. ■ SDRAM interface for external memory extensions. ■ HBI (Hyper Bus Interface) interface for external memory extensions. ■ Two processing pipeline (blit / display). ■ Maximum core system clock frequency: Refer to the Data sheet. ***Note:*** – *User can leverage internal VRAM and external HyperRAM as a graphics memory allowed to be written by GDC.*