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Errata

This errata sheet is for MB91265A Series Hardware Manual Rev.4 (CM44-10130-4E)

FR60Lite
32-BIT MICROCONTROLLER
MB91265A Series
HARDWARE MANUAL

2009.4.1

<table>
<tr><th>Date</th><th>Page</th><th>Item</th><th>Description</th></tr>
<tr><td>2009/
4/1</td><td>360</td><td>15.4.2.2</td><td>The following description of "[bit2] TxRqst/NewDat: Message transfer request bit" in "■ Function of Registers" was corrected as indicated by the shading below.

(Error)<table><tr><th>TxRqst/NewDat</th><th>Function</th></tr><tr><td>0</td><td>Indicates that "0" is set to the TxRqst bit of the message object * and CAN transmission request register. [Initial value]</td></tr><tr><td>1</td><td>"1" is set to the message object* and TxRqst bit of CAN transmission request register (transmission request).</td></tr></table>(Correct)<table><tr><th>TxRqst/NewDat</th><th>Function</th></tr><tr><td>0</td><td>Indicates that the TxRqst bit of CAN transmission request register and the message object * are not to be changed. [Initial value]</td></tr><tr><td>1</td><td>"1" is set to the message object* and TxRqst bit of CAN transmission request register (transmission request).</td></tr></table>[mcu_doc:08891]</td></tr>
<tr><td>2008/
6/13</td><td>381</td><td>15.4.4.3</td><td>"■ Function" of Registers was added as indicated by the shading below.

・Set condition
- When WR/RD of IFx command mask register is set to “1” and IntPnd of IFx message control register is set to “1”, IntPnd of specific object can be set
by writing to IFx command request register.</td></tr>
<tr><td>2008/
6/13</td><td>381</td><td>15.4.4.3</td><td>"■ Function" of Registers was corrected as indicated by the shading below.

・Reset condition

(Error)
When IFx command mask register sets WR/RD and ClrIntPnd to "1",

(Correct)
When IFx command mask register sets WR/RD and CIP to "1",</td></tr>
<tr><td>2008/
6/13</td><td>381</td><td>15.4.4.3</td><td>"■ Function" of Registers was added as indicated by the shading below.

・Reset condition

- When WR/RD of IFx command mask register is set to “1” and IntPnd of IFx messagecontrol register is set to “0”, IntPnd of specific object can be reset by
writing to IFx command request register.</td></tr>
</table>

Date	Page	Item	Description
2008/ 6/13	386	15.5.1	"■ Message Object" was corrected as indicated by the shading below. (Error) Message object setting of message RAM (except for MsgVal, NewDat, IntPnd and TxRqst bits) is not initialized by hardware reset. So, initialize the message object by CPU or set the MsgVal bit invalid (MsgVal=0). Set the CAN bit timing register also when Init bit of CAN control register is "0". (Correct) Message object setting of message RAM (except for MsgVal, NewDat, IntPnd and TxRqst bits) is not initialized by hardware reset. So, initialize the message object by CPU or set the MsgVal bit invalid (MsgVal=0). Set the CAN bit timing register(BTR) and CAN prescaler extension register (BRPER) also when Init bit of CAN control register is "1" and CCE bit is “1”. [mcu_doc:0735]

FUJITSU

Corrections of Hardware Manual

MB91265

hm91265-cm71-10130-4e-corr-x1-00

Addendum, MB91265 Hardware Manual (CM71-10130-4E)

This is the Addendum for the Hardware Manual CM71-10130-4E of the MB91265 microcontroller series. It describes all known discrepancies of the MB91265 microcontroller series Hardware Manual.

Ref. Number (Internal ref. number) (Text Link)	Date dd.mm.yy	Version No.	Chapter/Page	Description/Correction
HWM91265001	02.05.06	1.00	12.4.9/240	Typo in the table for input capture control register (ch2, ch3), lower byte (ICSL23)

There is a typo in the table for input capture control register (ch2, ch3), lower byte (ICSL23). The correction is marked grey in the following table.

The bit-name of bit 6 (ICSL23) is ICP2 instead of IP2.

■ Input Capture State Control Register (ch2, ch3), Lower Byte (ICSL23)

Input capture state control register (Lower)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ICP3	ICP2	ICE3	ICE2	EG31	EG30	EG21	EG20
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

ICSL23
Address : 0000B7$_H$
Initial value : 00000000$_B$

EG21	EG20	Edge selection bits (input capture 2)
0	0	No edge is detected (stop).
0	1	Rising edge is detected.
1	0	Falling edge is detected.
1	1	Both edges are detected.

EG31	EG30	Edge selection bits (input capture 3)
0	0	No edge is detected (stop).
0	1	Rising edge is detected.
1	0	Falling edge is detected.
1	1	Both edges are detected.

ICE2	Interrupt request enable bit (input capture 2)
0	Disable interrupt requests.
1	Enable interrupt requests.

ICE3	Interrupt request enable bit (input capture 3)
0	Disable interrupt requests.
1	Enable interrupt requests.

ICP2	Interrupt request flag bit (input capture 2)	
	Read	Write
0	No valid edge is detected.	This bit is cleared.
1	Valid edge is detected.	Not affect this bit.

ICP3	Interrupt request flag bit (input capture 3)	
	Read	Write
0	No valid edge is detected.	This bit is cleared.
1	Valid edge is detected.	Not affect this bit.

R/W : Readable/Writable
□ : Initial value