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Continuity of Specifications
There is no change to this document as a result of offering the device as a Cypress product. Any changes that have been made are the result of normal document improvements and are noted in the document history page, where supported. Future revisions will occur when appropriate, and changes will be noted in a document history page.

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About Cypress
Cypress (NASDAQ: CY) delivers high-performance, high-quality solutions at the heart of today's most advanced embedded systems, from automotive, industrial and networking platforms to highly interactive consumer and mobile devices. With a broad, differentiated product portfolio that includes NOR flash memories, F-RAM™ and SRAM, Traveo™ microcontrollers, the industry's only PSoC® programmable system-on-chip solutions, analog and PMIC Power Management ICs, CapSense® capacitive touch-sensing controllers, and Wireless BLE Bluetooth® Low-Energy and USB connectivity solutions, Cypress is committed to providing its customers worldwide with consistent innovation, best-in-class support and exceptional system value.

CM71-10127-2ET1

Errata

This errata sheet is for MB91260B Series Hardware Manual Rev.2 (CM71-10127-2E)

FR60Lite
32-BIT MICROCONTROLLER
MB91260B Series
HARDWARE MANUAL

2009.4.1

Date	Page	Item	Description
2009/ 4/1	24	2.1	The following description of "■ Handing Devices" was added as indicated by the shading below. ● Synchronous Mode Software Reset When using the synchronous mode software reset, the following two conditions must be satisfied before setting the SRST bit in the STCR (standby control register) to "0". ・Set interrupt enable flag (I-Flag) to interrupts disabled (I-Flag=0) ・NMI not used
2009/ 4/1	71	3.11.1	"● Setting of PLL multiplier" was deleted as indicated by the shading below. ● Setting of PLL multiplier To change the PLL multiplier setting from the initial value, start program operation and set the new value either before or at the same time as enabling the PLL for oscillation. After changing the multiplier, switch the source clock after the lock wait time has passed. For this PLL lock wait time, it is recommended to use a timebase timer interrupt. Before changing the PLL multiplier setting during operation, switch the source clock to any resource other than the PLL. After changing the multiplier, switch the source clock after the lock wait time has passed in the same way as above. The PLL multiplier setting can be changed while the PLL is being used. In this case, however, the device enters the oscillation stabilization wait state automatically after updating the PLL multiplier and stops program operation until the oscillation stabilization wait time has passed. When the clock source is switched to any resource other than the PLL, the device does not stop program operation. [mcu_doc:0849]
2009/ 4/1	78	3.11.6	The following description of "[bit11] SRST (Software ReSeT occurred)" in "■ RSRR: Reset Source Register/watchdog Timer Control Register" was added as indicated by the shading below. [bit11] SRST (Software ReSeT occurred) This bit indicates whether a reset (RST) by writing to the SRST bit (software reset) in the STCR register has occurred. Note the restrictions that apply to bit9:SYNCR in the TBCR (time-base counter control register) when using the synchronous mode software reset.
2009/ 4/1	82	3.11.6	The following description of "[bit9] SYNCR (SYNChronous Reset enable)" in "■ TBCR: Timebase Counter Control Register" was added as indicated by the shading below. Note: When using the synchronous mode software reset, the following two conditions must be satisfied before setting the SRST bit in the STCR (standby control register) to "0". ・Set interrupt enable flag (I-Flag) to interrupts disabled (I-Flag=0) ・NMI not used