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Continuity of Specifications

There is no change to this document as a result of offering the device as a Cypress product. Any changes that have been made are the result of normal document improvements and are noted in the document history page, where supported. Future revisions will occur when appropriate, and changes will be noted in a document history page.

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For More Information

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About Cypress

Cypress (NASDAQ: CY) delivers high-performance, high-quality solutions at the heart of today's most advanced embedded systems, from automotive, industrial and networking platforms to highly interactive consumer and mobile devices. With a broad, differentiated product portfolio that includes NOR flash memories, F-RAM™ and SRAM, Traveo™ microcontrollers, the industry's only PSoC® programmable system-on-chip solutions, analog and PMIC Power Management ICs, CapSense® capacitive touch-sensing controllers, and Wireless BLE Bluetooth® Low-Energy and USB connectivity solutions, Cypress is committed to providing its customers worldwide with consistent innovation, best-in-class support and exceptional system value.

Errata

This errata sheet is for MB91F127/128 Hardware Manual Rev.1 (CM71-10115-1E)

FR30
32-BIT MICROCONTROLLER
MB91F127/128
HARDWARE MANUAL

2008.12.24

Date	Page	Item	Description																																																												
2008/ 12/24	70	3.11.5	<p>The following description of " [Bit 08] CHC" in "■ GCR Configuration" was corrected as indicated by the shading below.</p> <p>(誤)</p> <table><tr><th>CHC</th><th>Clock selection</th></tr><tr><td>0</td><td>Uses half the clock cycle from the oscillation circuit as reference clock [default].</td></tr><tr><td>1</td><td>Uses the oscillation output from the PLL as reference clock.</td></tr></table> <p>(正)</p> <table><tr><th>CHC</th><th>Clock selection</th></tr><tr><td>0</td><td>Uses the oscillation output from the PLL as reference clock.</td></tr><tr><td>1</td><td>Uses half the clock cycle from the oscillation circuit as reference clock [default].</td></tr></table> <p>[mcu_doc0631]</p>	CHC	Clock selection	0	Uses half the clock cycle from the oscillation circuit as reference clock [default].	1	Uses the oscillation output from the PLL as reference clock.	CHC	Clock selection	0	Uses the oscillation output from the PLL as reference clock.	1	Uses half the clock cycle from the oscillation circuit as reference clock [default].																																																
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2004/ 4/21	273	13.2.3	<p>The figure 13.2-5 to be corrected as indicated by shading below:</p> <p>•Error</p> <table><tr><td>bit</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td><td>Initial value</td></tr><tr><td>Address 0000D5_H</td><td>A17</td><td>A16</td><td>A15</td><td>A14</td><td>A13</td><td>A12</td><td>A11</td><td>A10</td><td>11111111_B</td></tr><tr><td></td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td></td></tr></table> <p>•Correct</p> <table><tr><td>bit</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td><td>Initial value</td></tr><tr><td>Address 0000D5_H</td><td>A17</td><td>A16</td><td>A15</td><td>A14</td><td>A13</td><td>A12</td><td>A11</td><td>A10</td><td>11111111_B</td></tr><tr><td></td><td>W</td><td>W</td><td>W</td><td>W</td><td>W</td><td>W</td><td>W</td><td>W</td><td></td></tr></table>	bit	7	6	5	4	3	2	1	0	Initial value	Address 0000D5 _H	A17	A16	A15	A14	A13	A12	A11	A10	11111111 _B		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		bit	7	6	5	4	3	2	1	0	Initial value	Address 0000D5 _H	A17	A16	A15	A14	A13	A12	A11	A10	11111111 _B		W	W	W	W	W	W	W	W	
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2004/ 4/21	371	A	<p>The table A-1 to be corrected as indicated by shading below:</p> <p>•Error</p> <table><tr><th rowspan="2">Address</th><th colspan="4">Register</th><th rowspan="2">Internal resource</th></tr><tr><th>+0</th><th>+1</th><th>+2</th><th>+3</th></tr><tr><td>0000D4_H</td><td>-</td><td>AIC3 [R/W] 11111111</td><td>-</td><td>-</td><td>A/D converter</td></tr></table> <p>•Correct</p> <table><tr><th rowspan="2">Address</th><th colspan="4">Register</th><th rowspan="2">Internal resource</th></tr><tr><th>+0</th><th>+1</th><th>+2</th><th>+3</th></tr><tr><td>0000D4_H</td><td>-</td><td>AIC3 [W] 11111111</td><td>-</td><td>-</td><td>A/D converter</td></tr></table>	Address	Register				Internal resource	+0	+1	+2	+3	0000D4 _H	-	AIC3 [R/W] 11111111	-	-	A/D converter	Address	Register				Internal resource	+0	+1	+2	+3	0000D4 _H	-	AIC3 [W] 11111111	-	-	A/D converter																												
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