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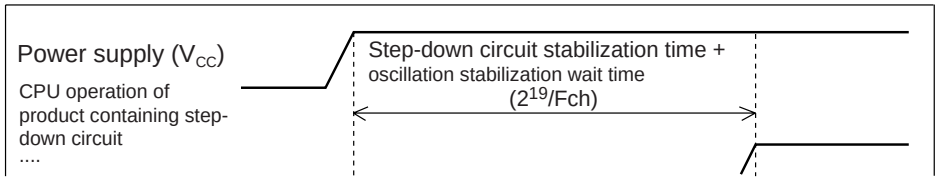
CM25-10135-5ET1

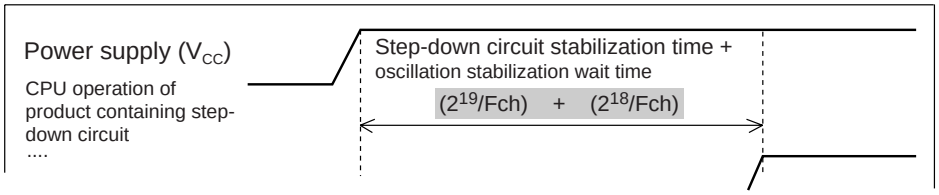
Errata

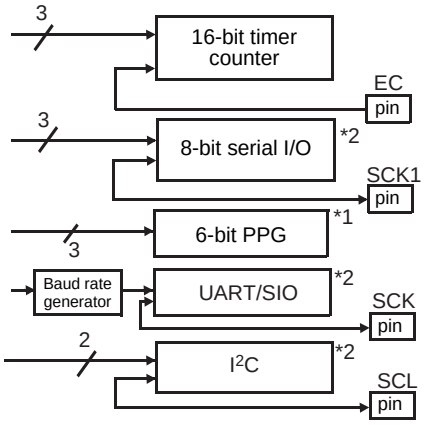
F²MC-8L
8-BIT MICROCONTROLLER
MB89530/530H/530A Series
HARDWARE MANUAL

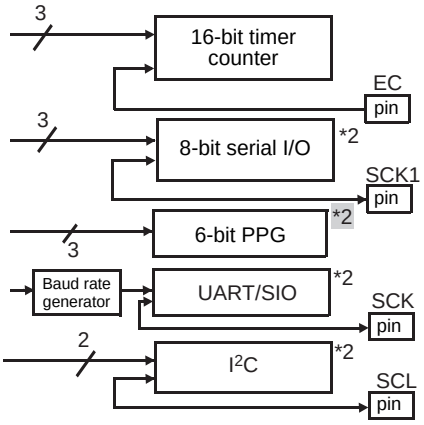
2004.4.21

<table>
<tr><th>Page</th><th>Item</th><th>Description</th></tr>
<tr><td>32</td><td>2.1</td><td>The description at the upper side of Figure 2.1-1 to be corrected as indicated by shading below.

•error
 

•correct
 
</td></tr>
<tr><td>64</td><td>3.6</td><td>The description at the center-right of Figure 3.6-1 to be corrected as indicated by shading below.

•error
 

•correct
 
</td></tr>
<tr><td>69</td><td>3.6-3</td><td>The description at the center-right of Figure 3.6-5 to be corrected as indicated by shading below.

•error
<table>
<tr><th rowspan="2">WT1</th><th rowspan="2">WT0</th><th>Oscillation stabilization wait time select bit</th></tr>
<tr><th>Main clock oscillation stabilization wait time by timebase timer output (for FCH = 12.5 MHz)</th></tr>
<tr><td>0</td><td>0</td><td>Setting prohibited</td></tr>
<tr><td>0</td><td>1</td><td>About 2^{12} / FCH (about 1.31 ms)</td></tr>
<tr><td>1</td><td>0</td><td>About 2^{16} / FCH (about 10.5 ms)</td></tr>
<tr><td>1</td><td>1</td><td>About 2^{18} / FCH (about 20.97 ms)</td></tr>
</table>
•correct
<table>
<tr><th rowspan="2">WT1</th><th rowspan="2">WT0</th><th>Oscillation stabilization wait time select bit</th></tr>
<tr><th>Main clock oscillation stabilization wait time by timebase timer output (for FCH = 12.5 MHz)</th></tr>
<tr><td>0</td><td>0</td><td>Setting prohibited</td></tr>
<tr><td>0</td><td>1</td><td>About 2^{14} / FCH (about 1.31 ms)</td></tr>
<tr><td>1</td><td>0</td><td>About 2^{17} / FCH (about 10.5 ms)</td></tr>
<tr><td>1</td><td>1</td><td>About 2^{18} / FCH (about 20.97 ms)</td></tr>
</table></td></tr>
</table>

<table>
<tr><th>Page</th><th>Item</th><th>Description</th></tr>
<tr><td>123</td><td>4.5</td><td>The following sentence to be corrected as indicated by shading below.

•error
Reference
……
Note that I²C can be used with the MB89PV530, MB89P538, MB89537C/538C, MB89537HC/538HC, and MB89537AC/538AC only.

•correct
Reference
……
Note that I²C can be used with the MB89PV530, MB89P538, MB89F538/F538L, MB89537C/538C, MB89537HC/538HC, and MB89537AC/538AC only.</td></tr>
<tr><td>125</td><td>4.5.1</td><td>The following sentence of “❍ Port 4 direction register (DDR4)”in” ■ Functions of the Port 4 registers” to be corrected as indicated by shading below.

•error
The DDR4 register sets the direction (I/O) of each pin by bit.
Specifying 1 to the bit of a pin sets it up for output, and specifying 0 sets it up for input.
(Note that the DDR4 register does not allow bit 2 and bit 3 to be used.)

•correct
The DDR4 register sets the direction (I/O) of each pin by bit.
Specifying 1 to the bit of a pin sets it up for output, and specifying 0 sets it up for input.
For the bit 3 and bit 2 of the DDR4, when the P43 and P42 are used as the resource input pin, set the bit corresponding PDR4 register to “1” because there is no DDR.</td></tr>
<tr><td>235</td><td>9.4.2</td><td>The description at the upper-right of Figure 9.4-3 to be corrected as indicated by shading below.

•error
<table>
<tr><th rowspan="2">W2</th><th rowspan="2">W1</th><th rowspan="2">W0</th><th>Measured pulse selection bits</th></tr>
<tr><th>Effective only when the pulse width measurement function is selected (Fc=1)</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>"H" level (rising edge - falling edge)</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>"L" (rising edge - falling edge)</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Rising edge - rising edge (one cycle)</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>Falling edge - falling edge (one cycle)</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>Detection of "H" level (rising edge - falling edge) and the rising edge - rising edge</td></tr>
</table>
•correct
<table>
<tr><th rowspan="2">W2</th><th rowspan="2">W1</th><th rowspan="2">W0</th><th>Measured pulse selection bits</th></tr>
<tr><th>Effective only when the pulse width measurement function is selected (Fc=1)</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>"H" level (rising edge - falling edge)</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>"L" (rising edge - falling edge)</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Rising edge - rising edge (one cycle)</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>Falling edge - falling edge (one cycle)</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>Both edge detection</td></tr>
</table></td></tr>
<tr><td>249</td><td>9.9</td><td>The following item to be added to “❍ Notes on setting the timer using a program” in ”■ Notes on Using the Pulse Width Count Timer”.

• When detecting both edges are set (PCR2: W2, W1, W0 = 001_B), first detection edge will be the rising edge after the operation is enabled (PCR1: EN = 1). The counter value set by detecting both edges is initialized by the rising edge but not initialized by the falling edge.</td></tr>
<tr><td>270</td><td>11.1</td><td>The following sentence of “■ 12-Bit PPG Timer Function” to be corrected as indicated by shading below.

•error
• Frequencies ranging from 2 to 2^{12-1} count clock cycles can be generated.

•correct
• Frequencies ranging from 2 to 2^{12}-1 count clock cycles can be generated.</td></tr>
</table>

<table>
<tr><th>Page</th><th>Item</th><th>Description</th></tr>
<tr><td>359</td><td>15.8</td><td>The following sentences of “❍ Coding example” in ”■ Program Example of the A/D Conversion Function” to be corrected as indicated by shading below.

•error
(1st line) DDR5 EQU 0012H ;Address of the Port 5 direction register
:
(17th line) SETB AN0 ;Specify the P00/AN0 pin as an analog input
:
(34th line) MOVW A,ADDL ;Read the A/D conversion data (lower 8 bits)
:

•correct
(1st line) PDR5 EQU 0012H ;Address of the Port 5 direction register
:
(17th line) SETB AN0 ;Specify the P50/AN0 pin as an analog input
:
(34th line) MOV A,ADDL ;Read the A/D conversion data (lower 8 bits)
:</td></tr>
<tr><td rowspan="2">371</td><td rowspan="2">16.4.2</td><td>The title of Table 16.4-2 to be corrected as indicated by shading below.

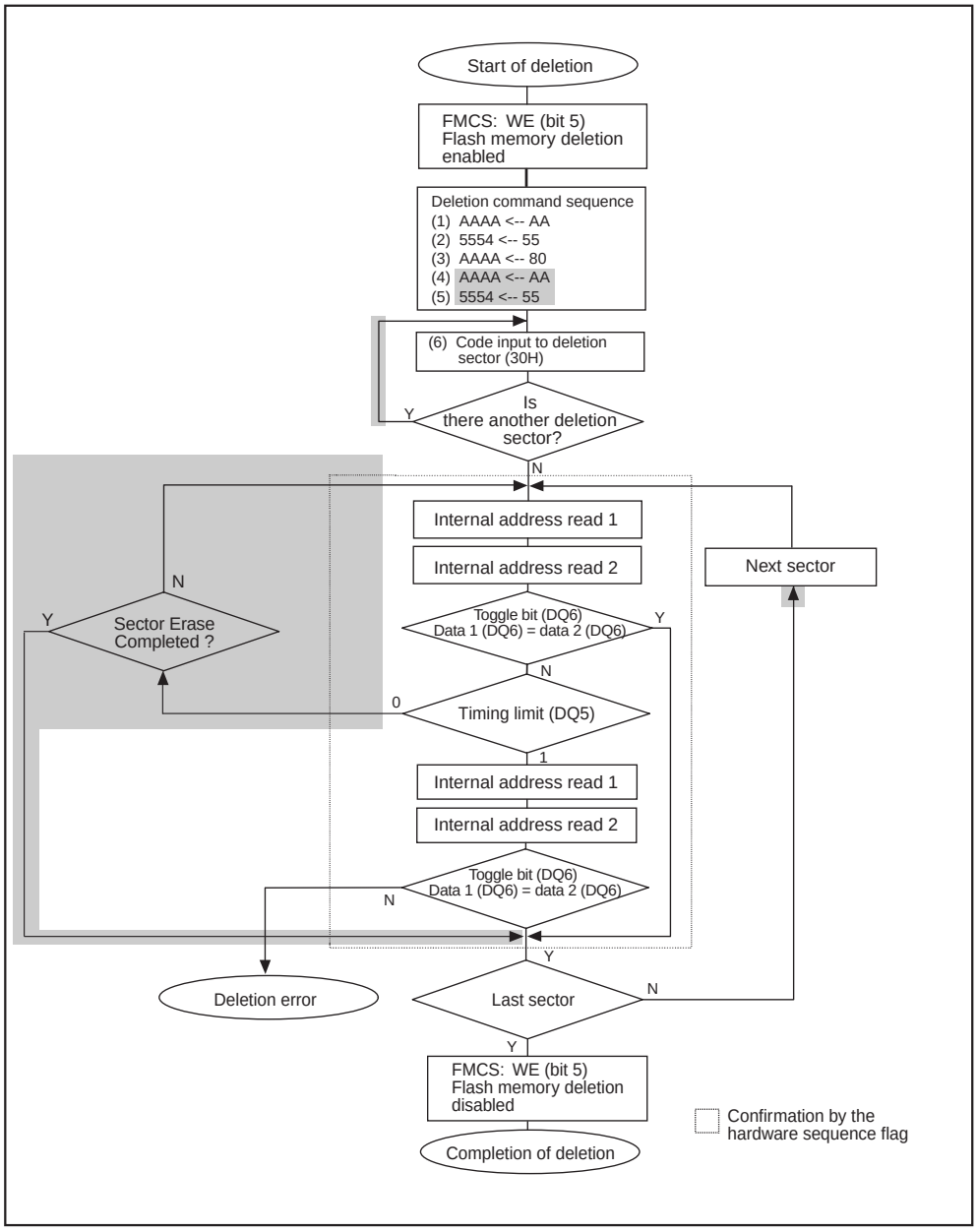
•error
Functions of Each Bit in Serial Mode Control Register 2 (SMC2)

•correct
Functions of Each Bit in Serial Mode Control Register 2 (SMC22)</td></tr>
<tr><td>The following Note to be added to ”16.4.2 Serial Mode Control Register 2 (SMC22)”.

Note:
The bit manipulation instructions (SETB, CLRB) cannot be used with the SMC22 register.
As the BRGE bit which value is undefined during a read operation is write-only, the BRGE bit value may be changed by using the bit manipulation instructions.</td></tr>
<tr><td>504</td><td>22.3</td><td>The description at the bottom side of Figure 22.3-1 to be corrected as indicated by shading below.

•error
<table><tr><th>INTE</th><th>Bit causing an interrupt to the CPU to be generated</th></tr><tr><td>0</td><td>Enables an interrupt when data writing/erasing is completed.</td></tr><tr><td>1</td><td>Disables an interrupt when data writing/erasing is completed.</td></tr></table>
•correct
<table><tr><th>INTE</th><th>Bit causing an interrupt to the CPU to be generated</th></tr><tr><td>0</td><td>Disables an interrupt when data writing/erasing is completed.</td></tr><tr><td>1</td><td>Enables an interrupt when data writing/erasing is completed.</td></tr></table></td></tr>
<tr><td>516</td><td>22.6.2</td><td>The following sentence of “■ Specifying addresses” to be deleted as indicated by shading below.

Only even addresses can be specified in bytes for the write addresses specified in a write data cycle.
Writing can be done in any order of addresses or even if the sector boundary is exceeded.
However, the Write command writes only data of one byte for each execution.</td></tr>
</table>

Page	Item	Description
520	22.6.4	Figure 22.6-2 to be corrected as indicated by shading below. 
523	22.7	The following sentence of "■ Input of a hardware reset ($\overline{RST}$)" to be deleted as indicated by shading below. To input a hardware reset when reading is in progress, i.e., when the automatic algorithm has not been started, secure a minimum low-level width of 500 ns. To input a hardware reset while a write or erase is in progress, i.e., while the automatic algorithm is being started, secure a minimum low-level width of 500 ns. In this case, 20 µs are required until the data becomes readable after the operation being performed terminates and the flash memory is fully initialized. Performing a hardware reset during a write operation makes the data being written undetermined. Also note that performing a hardware reset during an erase operation may make the sector from which data is being erased unusable.

Page	Item	Description
558	B.5	Table B.5-4 to be corrected as indicated by shading below.

No.	MNEMONIC	~	#	Operation	TL	TH	AH	N	Z	V	C	OP CODE
1	PUSHW A	4	1	((SP))←(A),(SP)←(SP)-2	-	-	-	-	-	-	-	40
2	POPW A	4	1	(A)←((SP)),(SP)←(SP)+2	-	-	dH	-	-	-	-	50
3	PUSHW IX	4	1	((SP))←(IX),(SP)←(SP)-2	-	-	-	-	-	-	-	41
4	POPW IX	4	1	(IX)←((SP)),(SP)←(SP)+2	-	-	-	-	-	-	-	51
5	NOP	1	1	No operation	-	-	-	-	-	-	-	00
6	CLRC	1	1	(C)←0	-	-	-	-	-	-	R	81
7	SETC	1	1	(C)←1	-	-	-	-	-	-	S	91
8	CLRI	1	1	(I)←0	-	-	-	-	-	-	-	80
9	SETI	1	1	(I)←1	-	-	-	-	-	-	-	90