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Continuity of Specifications

There is no change to this document as a result of offering the device as a Cypress product. Any changes that have been made are the result of normal document improvements and are noted in the document history page, where supported. Future revisions will occur when appropriate, and changes will be noted in a document history page.

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Cypress continues to support existing part numbers. To order these products, please use only the Ordering Part Numbers listed in this document.

For More Information

Please contact your local sales office for additional information about Cypress products and solutions.

About Cypress

Cypress (NASDAQ: CY) delivers high-performance, high-quality solutions at the heart of today's most advanced embedded systems, from automotive, industrial and networking platforms to highly interactive consumer and mobile devices. With a broad, differentiated product portfolio that includes NOR flash memories, F-RAM™ and SRAM, Traveo™ microcontrollers, the industry's only PSoC® programmable system-on-chip solutions, analog and PMIC Power Management ICs, CapSense® capacitive touch-sensing controllers, and Wireless BLE Bluetooth® Low-Energy and USB connectivity solutions, Cypress is committed to providing its customers worldwide with consistent innovation, best-in-class support and exceptional system value.

Errata

This errata sheet is for MB90895 Series Hardware Manual Rev. 3 (CM44-10127-3E).

F²MC-16LX
16-BIT MICROCONTROLLER
MB90895 Series
HARDWARE MANUAL

2009. 5. 12

Date	Page	Item	Description																																																						
2009/5/12	335	12.3.2	<p>“Figure 12.3-3 DTP/external interrupt enable register (ENIR)” was corrected as corrected by the shading below.</p> <p>(Error)</p> <table><tr><td>bit7</td><td>bit6</td><td>bit5</td><td>bit4</td><td>bit3</td><td>bit2</td><td>bit1</td><td>bit0</td><td>Reset value</td></tr><tr><td></td><td></td><td></td><td></td><td>Re-served</td><td>Re-served</td><td>Re-served</td><td></td><td>00000000_B</td></tr><tr><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W -</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td></td></tr></table> <p>(Correct)</p> <table><tr><td>bit7</td><td>bit6</td><td>bit5</td><td>bit4</td><td>bit3</td><td>bit2</td><td>bit1</td><td>bit0</td><td>Reset value</td></tr><tr><td>EN7</td><td>EN6</td><td>EN5</td><td>EN4</td><td>Re-served</td><td>Re-served</td><td>Re-served</td><td>EN0</td><td>00000000_B</td></tr><tr><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W -</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td></td></tr></table>	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reset value					Re-served	Re-served	Re-served		00000000 _B	R/W	R/W	R/W	R/W -	R/W	R/W	R/W	R/W		bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reset value	EN7	EN6	EN5	EN4	Re-served	Re-served	Re-served	EN0	00000000 _B	R/W	R/W	R/W	R/W -	R/W	R/W	R/W	R/W	
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2009/5/12	443	15.3.3	<p>“Table 15.3-4 Functions of Serial Status Register 1 (SSR1)” was corrected as corrected by the shading below.</p> <p>(Error)</p> <table><tr><th colspan="2">bit name</th><th>Function</th></tr><tr><td>bit8</td><td>TIE: Transmit interrupt request enable bit</td><td>Enable or disable send interrupt. When set to "1": A receive interrupt request is issued when data written to the serial output data register 1 (SODR1) is sent to the transmit shift register (bit 11: TDRE = 1).</td></tr></table> <p>(Correct)</p> <table><tr><th colspan="2">bit name</th><th>Function</th></tr><tr><td>bit8</td><td>TIE: Transmit interrupt request enable bit</td><td>Enable or disable send interrupt. When set to "1": A transmit interrupt request is issued when data written to the serial output data register 1 (SODR1) is sent to the transmit shift register (bit 11: TDRE = 1).</td></tr></table>	bit name		Function	bit8	TIE: Transmit interrupt request enable bit	Enable or disable send interrupt. When set to "1": A receive interrupt request is issued when data written to the serial output data register 1 (SODR1) is sent to the transmit shift register (bit 11: TDRE = 1).	bit name		Function	bit8	TIE: Transmit interrupt request enable bit	Enable or disable send interrupt. When set to "1": A transmit interrupt request is issued when data written to the serial output data register 1 (SODR1) is sent to the transmit shift register (bit 11: TDRE = 1).																																										
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