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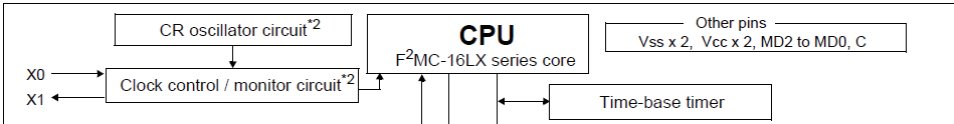
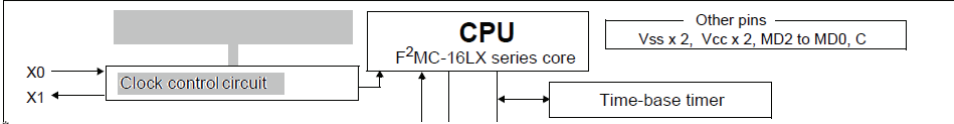
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## Errata

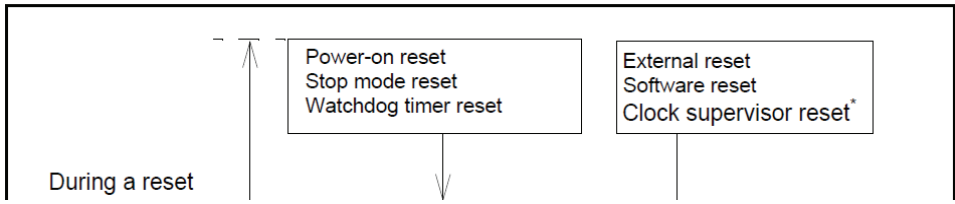
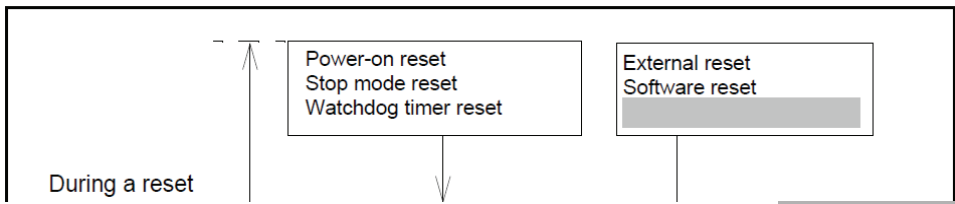
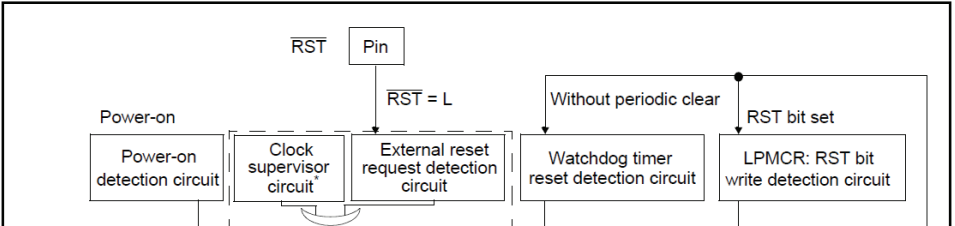
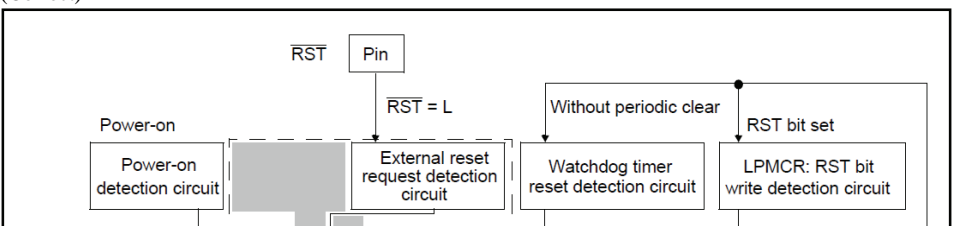
This errata sheet is for MB90820B Series Hardware Manual Rev. 2\_(CM44-10147-2E).


F<sup>2</sup>MC-16LX  
16-BIT MICROCONTROLLER  
MB90820B Series  
HARDWARE MANUAL

2012.12.7

Date	Page	Item	Description												
2012/12/7	4	1.1	"● Clock supervisor" of "■ Internal Peripheral Features" should be deleted. <span style="float: right;">[mcu_doc1192]</span>												
2012/12/7	5,6	1.2	"MB90F828B" row of "Table 1.2-1 MB90820B Series Product Line-up" should be deleted. <span style="float: right;">[mcu_doc1192]</span>												
2012/12/7	5	1.2	"Clock supervisor"Line of "Table 1.2-1 MB90820B Series Product Line-up" should be deleted. <span style="float: right;">[mcu_doc1192]</span>												
2012/12/7	7	1.3	<p>"Figure 1.3-1 MB90820B Series Overall Block Diagram" should be corrected as indicated by the shading below.</p> <p>(Error)</p>  <p>*1: High current drive pin. *2: MB90F828B</p> <p>(Correct)</p>  <p>*1: High current drive pin.</p> <p style="text-align: right;">[mcu_doc1192]</p>												
2012/12/7	29	2.3	<p>"Figure 2.3-1 Memory Maps" should be deleted as indicated by the shading below.</p> <table border="1" style="width: 100%; border-collapse: collapse; text-align: center;"> <thead> <tr> <th>Model</th><th>Address #1</th><th>Address #2</th><th>Address #3</th></tr> </thead> <tbody> <tr> <td>MB90V820B</td><td>(FE0000<sub>H</sub>)</td><td>008000<sub>H</sub></td><td>0040FF<sub>H</sub></td></tr> <tr> <td>MB90F828B</td><td>FE0000<sub>H</sub></td><td>008000<sub>H</sub></td><td>0020FF<sub>H</sub></td></tr> </tbody> </table> <p style="text-align: right;">[mcu_doc1192]</p>	Model	Address #1	Address #2	Address #3	MB90V820B	(FE0000 <sub>H</sub> )	008000 <sub>H</sub>	0040FF <sub>H</sub>	MB90F828B	FE0000 <sub>H</sub>	008000 <sub>H</sub>	0020FF <sub>H</sub>
Model	Address #1	Address #2	Address #3												
MB90V820B	(FE0000 <sub>H</sub> )	008000 <sub>H</sub>	0040FF <sub>H</sub>												
MB90F828B	FE0000 <sub>H</sub>	008000 <sub>H</sub>	0020FF <sub>H</sub>												

Date	Page	Item	Description															
2012/12/7	64	3.1	<p>"3.1 Reset" should be corrected as indicated by the shading below.</p> <p>(Error) There are five causes of a reset:</p> <ul style="list-style-type: none"><li>• Power-on reset</li><li>• Watchdog timer overflow</li><li>• External reset request via the RST pin</li><li>• Software reset request</li><li>• Clock supervisor reset request (MB90F828B only)</li></ul> <p>(Correct) There are <b>four</b> causes of a reset:</p> <ul style="list-style-type: none"><li>• Power-on reset</li><li>• Watchdog timer overflow</li><li>• External reset request via the RST pin</li><li>• Software reset request</li></ul> <div></div> <div>[mcu_doc1192]</div>															
2012/12/7	64	3.1	<p>"Table 3.1-1 Reset causes" should be deleted as indicated by the shading below.</p> <table><tr><th>Type of reset</th><th>Cause</th><th>Machine clock</th><th>Watchdog timer</th><th>Oscillation stabilization wait</th></tr><tr><td>Power-on</td><td>When the power is turned on</td><td>MCLK</td><td>Stop count</td><td>Yes</td></tr><tr><td>Clock Supervisor reset*</td><td>Main clock failure detected</td><td>Internal CR oscillator clock</td><td>Stop</td><td>No</td></tr></table> <p>MCLK: Main clock frequency (oscillation clock frequency divided by 2) *:MB90F828B only</p> <div>[mcu_doc1192]</div>	Type of reset	Cause	Machine clock	Watchdog timer	Oscillation stabilization wait	Power-on	When the power is turned on	MCLK	Stop count	Yes	Clock Supervisor reset*	Main clock failure detected	Internal CR oscillator clock	Stop	No
Type of reset	Cause	Machine clock	Watchdog timer	Oscillation stabilization wait														
Power-on	When the power is turned on	MCLK	Stop count	Yes														
Clock Supervisor reset*	Main clock failure detected	Internal CR oscillator clock	Stop	No														
2012/12/7	65	3.1	<p>" Clock supervisor reset" of " Reset Causes" should be deleted as indicated.</p> <div>[mcu_doc1192]</div>															
2012/12/7	66	3.2	<p>"Table 3.2-1 Reset causes and oscillation stabilization wait intervals" should be deleted as indicated by the shading below.</p> <table><tr><th>Reset cause</th><th>Oscillation stabilization wait interval The corresponding time interval for an oscillation clock frequency of 4 MHz is given in parentheses.</th></tr><tr><td>Software reset</td><td>None. (However the WS1 &amp; WS0 bits are initialized to “11”.)</td></tr><tr><td>Clock supervisor reset*</td><td>None. (However the WS1 &amp; WS0 bits are initialized to “11”.)</td></tr></table> <p>HCLK:Oscillation clock frequency *: MB90F828B only</p> <div>[mcu_doc1192]</div>	Reset cause	Oscillation stabilization wait interval The corresponding time interval for an oscillation clock frequency of 4 MHz is given in parentheses.	Software reset	None. (However the WS1 & WS0 bits are initialized to “11”.)	Clock supervisor reset*	None. (However the WS1 & WS0 bits are initialized to “11”.)									
Reset cause	Oscillation stabilization wait interval The corresponding time interval for an oscillation clock frequency of 4 MHz is given in parentheses.																	
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Clock supervisor reset*	None. (However the WS1 & WS0 bits are initialized to “11”.)																	

Date	Page	Item	Description																				
2012/12/7	69	3.4	<p>"Figure 3.4-1 Reset operation flow" should be corrected as indicated by the shading below.</p> <p>(Error)</p> <div></div> <p style="text-align: right;">*: MB90F828B only</p> <p>(Correct)</p> <div></div> <p style="text-align: right;">[mcu_doc1192]</p>																				
2012/12/7	71	3.5	<p>"Figure 3.5-1 Block diagram of reset cause bits" should be corrected as indicated by the shading below.</p> <p>(Error)</p> <div></div> <p style="text-align: right;">*: MB90F828B only</p> <p>(Correct)</p> <div></div> <p style="text-align: right;">[mcu_doc1192]</p>																				
2012/12/7	72	3.5	<p>"Table 3.5-1 Correspondence between reset cause flag bits and reset causes" should be deleted as indicated by the shading below.</p> <table><tr><th>Reset cause</th><th>PONR</th><th>WRST</th><th>ERST</th><th>SRST</th></tr><tr><td>External reset request via RST pin</td><td></td><td></td><td></td><td></td></tr><tr><td>Clock supervisor reset (MB90F828B only)</td><td>*</td><td>*</td><td>1</td><td>*</td></tr><tr><td>Software reset request</td><td>*</td><td>*</td><td>*</td><td>1</td></tr></table> <p style="text-align: right;">[mcu_doc1192]</p>	Reset cause	PONR	WRST	ERST	SRST	External reset request via RST pin					Clock supervisor reset (MB90F828B only)	*	*	1	*	Software reset request	*	*	*	1
Reset cause	PONR	WRST	ERST	SRST																			
External reset request via RST pin																							
Clock supervisor reset (MB90F828B only)	*	*	1	*																			
Software reset request	*	*	*	1																			

Date	Page	Item	Description																					
2012/12/7	89 to 100	5.	"CHAPTER 5 CLOCK SUPERVISOR" should be deleted as indicated. <div>[mcu_doc1192]</div>																					
2009/8/21	505	20.4.2	Figure 20.4-3 Serial mode register (SMR0/SMR1) was corrected as indicated by the shading below.  (Error) <table><tr><td>CS2 to CS0</td><td>Clock selection bit</td></tr><tr><td>"000<sub>B</sub>" to "100<sub>B</sub>"</td><td>Baud rate by dedicated baud rate generator</td></tr><tr><td>"101<sub>B</sub>"</td><td>Disables setting</td></tr><tr><td>"110<sub>B</sub>"</td><td>Baud rate by internal timer (16-bit reload timer)</td></tr><tr><td>"111<sub>B</sub>"</td><td>Baud rate by external clock</td></tr></table> (Correct) <table><tr><td>CS2 to CS0</td><td>Clock selection bit</td></tr><tr><td>"000<sub>B</sub>" to "101<sub>B</sub>"</td><td>Baud rate by dedicated baud rate generator</td></tr><tr><td>"110<sub>B</sub>"</td><td>Baud rate by internal timer (16-bit reload timer)</td></tr><tr><td>"111<sub>B</sub>"</td><td>Baud rate by external clock</td></tr></table>	CS2 to CS0	Clock selection bit	"000 <sub>B</sub> " to "100 <sub>B</sub> "	Baud rate by dedicated baud rate generator	"101 <sub>B</sub> "	Disables setting	"110 <sub>B</sub> "	Baud rate by internal timer (16-bit reload timer)	"111 <sub>B</sub> "	Baud rate by external clock	CS2 to CS0	Clock selection bit	"000 <sub>B</sub> " to "101 <sub>B</sub> "	Baud rate by dedicated baud rate generator	"110 <sub>B</sub> "	Baud rate by internal timer (16-bit reload timer)	"111 <sub>B</sub> "	Baud rate by external clock			
CS2 to CS0	Clock selection bit																							
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CS2 to CS0	Clock selection bit																							
"000 <sub>B</sub> " to "101 <sub>B</sub> "	Baud rate by dedicated baud rate generator																							
"110 <sub>B</sub> "	Baud rate by internal timer (16-bit reload timer)																							
"111 <sub>B</sub> "	Baud rate by external clock																							
2012/12/7	548	21.4	"Notes:" should be deleted as indicated by the shading below. <div>• The program address detection register exists at 001FF0H to 001FF5H that overlaps with the RAM area of MB90F828B, preventing RAM access when using this feature on MB90F828B.</div> <div>[mcu_doc1192]</div>																					
2012/12/7	556	22.2	"  ROM Mirroring Function Selection Register (ROMM)" should be deleted as indicated by the shading below. <table><tr><td></td><td>MB90822B</td><td>MB90823B</td><td>MB90F822B</td><td>MB90F823B</td><td>MB90F828B</td><td>MB90V820B</td></tr><tr><td>Address 1</td><td>FF0000<sub>H</sub></td><td>FE0000<sub>H</sub></td><td>FF0000<sub>H</sub></td><td>FE0000<sub>H</sub></td><td>FE0000<sub>H</sub></td><td>FE0000<sub>H</sub></td></tr><tr><td>Address 2</td><td>0010FF<sub>H</sub></td><td>0010FF<sub>H</sub></td><td>0010FF<sub>H</sub></td><td>0010FF<sub>H</sub></td><td>0020FF<sub>H</sub></td><td>0040FF<sub>H</sub></td></tr></table> <div>[mcu_doc1192]</div>		MB90822B	MB90823B	MB90F822B	MB90F823B	MB90F828B	MB90V820B	Address 1	FF0000 <sub>H</sub>	FE0000 <sub>H</sub>	FF0000 <sub>H</sub>	FE0000 <sub>H</sub>	FE0000 <sub>H</sub>	FE0000 <sub>H</sub>	Address 2	0010FF <sub>H</sub>	0010FF <sub>H</sub>	0010FF <sub>H</sub>	0010FF <sub>H</sub>	0020FF <sub>H</sub>	0040FF <sub>H</sub>
	MB90822B	MB90823B	MB90F822B	MB90F823B	MB90F828B	MB90V820B																		
Address 1	FF0000 <sub>H</sub>	FE0000 <sub>H</sub>	FF0000 <sub>H</sub>	FE0000 <sub>H</sub>	FE0000 <sub>H</sub>	FE0000 <sub>H</sub>																		
Address 2	0010FF <sub>H</sub>	0010FF <sub>H</sub>	0010FF <sub>H</sub>	0010FF <sub>H</sub>	0020FF <sub>H</sub>	0040FF <sub>H</sub>																		

Date	Page	Item	Description																														
2012/12/7	587,589	APPENDIX A	" Table A-1 I/O map" should be corrected as indicated by the shading below.																														
			(Error)																														
			<table><tr><th>Address</th><th>Abbreviation</th><th>Register</th><th>Byte access</th><th>Word access</th><th>Resource name</th><th>Initial value</th></tr><tr><td>000088H</td><td rowspan="2">TMR1 / TMRD1</td><td rowspan="2">16 bit timer register 1 / 16-bit reload register 1</td><td rowspan="2">-</td><td rowspan="2">R/W</td><td rowspan="2">16-bit reload timer 1</td><td>XXXXXXXX<sub>B</sub></td></tr><tr><td>000089H</td><td>XXXXXXXX<sub>B</sub></td></tr><tr><td>00008AH</td><td>CSVCR</td><td>Clock supervisor control register *</td><td>R, R/W</td><td>-</td><td>Clock supervisor</td><td>00011100<sub>B</sub></td></tr><tr><td>00008BH</td><td colspan="6">Prohibited area</td></tr></table>	Address	Abbreviation	Register	Byte access	Word access	Resource name	Initial value	000088H	TMR1 / TMRD1	16 bit timer register 1 / 16-bit reload register 1	-	R/W	16-bit reload timer 1	XXXXXXXX <sub>B</sub>	000089H	XXXXXXXX <sub>B</sub>	00008AH	CSVCR	Clock supervisor control register *	R, R/W	-	Clock supervisor	00011100 <sub>B</sub>	00008BH	Prohibited area					
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			00008BH	Prohibited area																													
			*: MB90F828B only. Prohibited for the other product types.																														
			(Correct)																														
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			Address	Abbreviation	Register	Byte access	Word access	Resource name	Initial value																								
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