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Cypress (NASDAQ: CY) delivers high-performance, high-quality solutions at the heart of today's most advanced embedded systems, from automotive, industrial and networking platforms to highly interactive consumer and mobile devices. With a broad, differentiated product portfolio that includes NOR flash memories, F-RAM™ and SRAM, Traveo™ microcontrollers, the industry's only PSoC® programmable system-on-chip solutions, analog and PMIC Power Management ICs, CapSense® capacitive touch-sensing controllers, and Wireless BLE Bluetooth® Low-Energy and USB connectivity solutions, Cypress is committed to providing its customers worldwide with consistent innovation, best-in-class support and exceptional system value.

Errata

This errata sheet is for MB90580C Series Hardware Manual Rev.3 (CM44-10111-3E)

F^{2}MC-16LX
16-BIT MICROCONTROLLER
MB90580C Series
HARDWARE MANUAL

2009.4.2
: Corrected part

Date	Page	Item	Description
2008/ 8/18	-	-	See the following page for details.
2009/ 4/2	337	20.4.2	The following description of "■ Transmitter Operation" was corrected as indicated by the shading below. (Error) When the data set in the SODR register is loaded into the transmitter shift register and begins to be transmitted, the TDRE flag is set again and the next transmitter data can be set. If the TIE bit (bit 8) of the SSR register is set to 1 at this time, a transmitter interrupt occurs to the CPU to request the SODR register to set transmitter data. (Correct) When the data set in the SODR register is loaded into the transmitter shift register and begins to be transmitted, the TDRE flag is set again and the next transmitter data can be set. If the TIE bit (bit 8) of the SCR register is set to 1 at this time, a transmitter interrupt occurs to the CPU to request the SODR register to set transmitter data. [mcu_doc0621]
2009/ 1/6	539	APPENDIX B	■Table B.9-20 XCH Ri, ea Instruction (First Byte = 7E$_H$) is changed. ・Error Item "A" Line of +A "W2+d16,A" ・Correct Item "A0" Line of +A "@RW2+d16"

FUJITSU

Corrections of Hardware Manual

MB90580C series

hm90580c-cm44-10111-3e-corr-x1-00

Addendum, MB90580C Hardware Manual (CM44-10111-3E)

This is the Addendum for the Hardware Manual CM44-10111-3E of the MB90580C Microcontroller series. It describes all known discrepancies of the MB90580C Microcontroller series Hardware Manual.

Ref. Number (Text Link)	Date dd.mm.yy	Version No.	Chapter/Page	Description/Correction
HWM90580001	09.07.01	1.00	Chapter 17	A/D Converter: AVcc value must be same as Vcc
HWM90580002	09.07.01	1.00	Chapter 5	Release from Watch Mode
HWM90580003	09.07.01	1.00	Chapter 1.6	Voltage drop down

HWM90580001

Chapter 17: A/D Conveter

If the A/D converter is used AVcc must have the same value as Vcc.
Otherwise a Latchup could happen.

HWM90580002

Chapter 1.8 Precautions on Handling of Device

Watchmode

Condition: Watch Mode Subclock connected(normal operation) or Watchmode, No subclock connected

Description: If MCU has entered the Watch Mode and only the RST Reset signal is asserted, it could happen, that the CPU does not restart correctly.

Workaround: RST and HST reset must be asserted simultaneously.
Also a power-on reset will restart the CPU correctly again.

HWM90580003

Chapter 1.8: Precautions on Handling of Device

Voltage Drop down

Condition: Voltage Drop on Vcc, No Subclock connected

Description: If no subclock is connected, it possibly may happen, that after a voltage drop on Vcc, the MCU does not restart correctly, even if RST and HST is asserted simultaneously.

Details: If a voltage drop on Vcc occurs, there is no power-on reset executed, if the voltage Vcc does not drop below under 0.2V for a certain time (toff), which is specified in the DS. See details on Vcc in the corresponding Datasheet. Normally, if HST & RST is asserted afterwards, the MCU would restart correctly. If no subclock is connected, it possibly may happen, that the CPU does not start/work correctly even after RST & HST reset.

Workaround:
a) The usage of a Subclock is highly recommended. If a Subclock is connected and a RST & HST Reset is asserted (RST = HST, reset simultaneously) the CPU will restart correctly.
b) Perform a correct power-on Reset (corresponding to Vcc timing specified in Datasheet)