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CM44-10102-8ET2

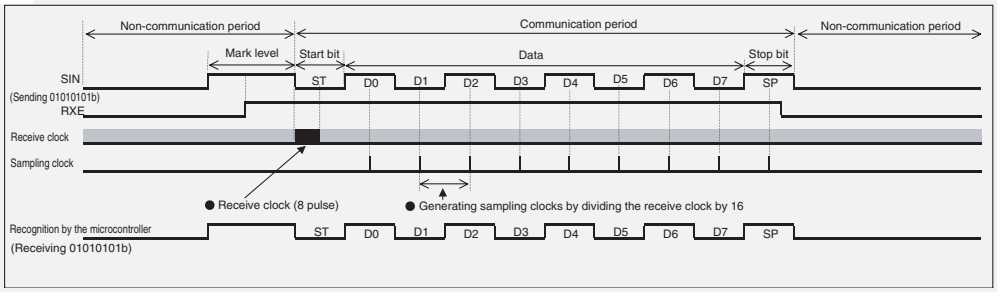
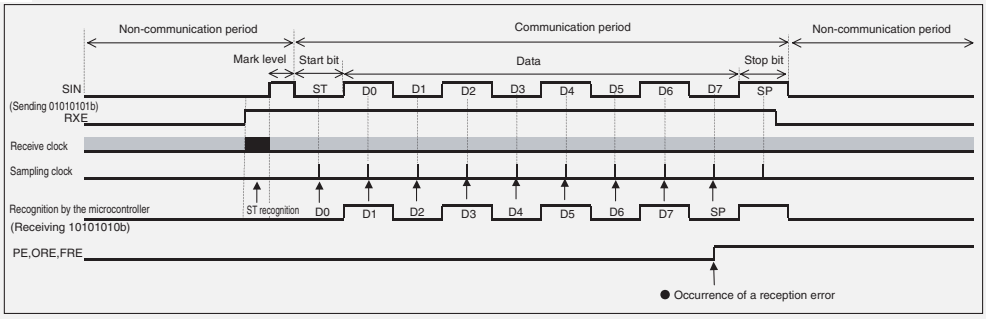
Errata

F²MC-16LX
16-BIT MICROCONTROLLER
MB90570 Series
HARDWARE MANUAL
[This Errata covers error corrections included in the previous version of the Errata.]

2009.1.16

Page	Item	Description
11	Table 1.6-1	The shading in the table below indicates changes made to Table 1.6-1. Pin No. | | Explanation of function 92/93 | | Pins for high-speed oscillation 74/73 | | Pin for low-speed oscillation
17	Table 1.7-1	The Remarks of the Circuit type " B" in the table was corrected as indicated by the shading below. • Low-speed oscillation feedback resistor = approx. 10 MΩ
22	Section 1.8	The following description was added at the end of the page: ❍ Notes on during operation of PLL clock mode If the PLL clock mode is selected, the microcontroller attempt to be working with the self-oscillating circuit even when there is no external oscillator or external clock input is stopped. Performance of this operation, however, cannot be guaranteed.
92	Section 5.1	The shaded sentence below was added at the end of the note: Note: When tune on the power or hardware standby mode or stop mode is released, the sub clock oscillation stabilization time (about 2 seconds) is generated. In the meantime, when switching from the main clock mode to the subclock mode, the oscillation stabilization time is generated. In attempting to switch the clock mode, do not attempt to switch to another clock mode or low-power consumption mode until the first switching is completed. The MCM and SCM bits of the clock selection register (CKSCR) indicate that switching is completed.
97	Section 5.3.2	The sentence on lines 3 of the description of "[Bit 15] SCM" was changed as follows: Old: When SCS is 1 and SCM is 1, the main clock is in the oscillation stabilization wait state. New: When SCS is 0 and SCM is 1, this is an indication that the machine clock is being switched from the main clock to the subclock. When SCS is 1 and SCM is 0, this is an indication that the machine clock is being switched from the subclock to the main clock.
101	Section 5.4	The following note was added at the end of the page: Note: In attempting to switch the clock mode, do not attempt to switch to another clock mode or low-power consumption mode until the first switching is completed. The MCM and SCM bits of the clock selection register (CKSCR) indicate that switching is completed.

Page	Item	Description
105	Section 6.1	The following note was added at the end of "■ low-power consumption mode". Note: In attempting to switch the clock mode, do not attempt to switch to another clock mode or low-power consumption mode until the first switching is completed. The MCM bit of the clock selection register (CKSCR) indicates that switching is completed.
123	Section 6.3	The following note was added at the end of the page: Note: In attempting to switch the clock mode, do not attempt to switch to another clock mode or low-power consumption mode until the first switching is completed. The MCM bit of the clock selection register (CKSCR) indicates that switching is completed.
261	Section 15.2.2	The following note was added at the end of the page: Note: If more than one external interrupt request output is enabled (EN7 to EN0 of ENIR are set to 1), clear to 0 only the bit for which the CPU accepted an interrupt (any of bits ER7 to ER0 that are set to 1). Do not clear the other bits without a valid reason.
308	Table 19.3-2	The shading in the table below indicates changes made to the table. Internal timer (8-bit PPG timer ch1 or 16-bit PPG timer)
319	Section 19.4	The following sentence of "■ internal timer" were corrected as indicated by the shading below. (The line 2) …, 8-bit PPG timer ch1 or 16-bit PPG timer can be used as a baud rate clock source. To obtain… (The line 4) Asynchronous (start-stop synchronous): (ϕ / N) / (16 × 2 × (n + 1)) (The line 7) N: Divide factor value of count clock source of the PPG timer (The line 8) n: Reload value of the PPG timer (The line 9) Table 19.4-4 "Baud Rates and Reload Values (Asynchronous) of PPG Timer" shows baud rates and reload values (in decimal) of the PPG timer when… (The title of the table 19.4-4) Baud Rates and Reload Values (Asynchronous) of PPG Timer (The header of the table 19.4-4) Reload value of the PPG timer (Under the table 19.4-4) When the internal timer (8-bit PPG timer ch1 or 16-bit PPG timer) is selected as a baud rate clock source, the output (PPG1) of the 8-bit PPG timer ch1 or 16-bit PPG timer is already connected in this controller. Therefore, the external pin (PPG1) of the 8-bit PPG timer ch1 or 16-bit PPG timer and the external clock input pin SCK0 do not require external connection. Also, the output pin of the 8-bit PPG timer ch1 or 16-bit PPG timer can be used as an I/O port pin if not used otherwise.
320		The following sentence of " ■ External clock" was corrected as indicated by the shading below. (The line 4) CLK synchronous: f (up to 1 MHz) --> CLK synchronous: f (The line 5) Note that the maximum value for f is 1MHz. --> Note that the maximum value for f is 2MHz.

Page	Item	Description
322	Section 19.5.1	The following description was added below the "■ Receiving Operation". ■ Detecting the start bit Implement the following settings to detect the start bit: • Set the communication line level to H (attach the mark level) before the communication period. • Specify reception permission (RXE = H) while the communication line level is H (mark level). • Do not specify reception permission (RXE = H) for periods other than the communication period (without mark level). Otherwise, data is not received correctly. • After the stop bit is detected (the RDRF flag is set to 1), specify reception inhibition (RXE = L) while the communication line level is H (mark level).  Note that specifying reception permission at the timing shown below obstructs the correct recognition of the input data (SIN) by the microcontroller. • Example of operation if reception permission (RXE = H) is specified while the communication line level is L. 
341	Section 20.3.1	The lines 3 and 4 of "■ External Shift Clock Mode" were corrected as indicated by the shading below. A transfer rate with a frequency from DC to 1 divided by eight machine cycles is available. For example, when one machine cycle is 62.5 ns, a transfer rate of up to 2 MHz is available.
393	Section 25.2	The note of "[Bit 8] MI" was corrected as indicated by the shading below: Because addresses FF4000 to FFFFFF is mirrored at addresses 004000 to 00FFFF of the 00 bank in operating the ROM mirror function, less than addresses FF3FFF are not mirrored at the 00 bank regardless of the setting of the mirror function.

Page	Item	Description
502	APPENDIX B	■Table B.9-20 XCH Ri, ea Instruction (First Byte = $7E_H$) is changed. ・Error Item "A" Line of +A "W2+d16,A" ・Correct Item "A0" Line of +A "@RW2+d16"

FUJITSU

Corrections of Hardware Manual

MB90570

hm90570-cm44-10102-8e-corr-x1-04

Addendum, MB90570 Hardware Manual (CM44-10102-8E)

This is the Addendum for the Hardware Manual CM44-10102-8E of the MB90570 microcontroller series. It describes all known discrepancies of the MB90570 microcontroller series Hardware Manual.

Ref. Number (Text Link)	Date dd.mm.yy	Version No.	Chapter/Page	Description/Correction
HWM90570001	20.04.01	1.00		Differences between MB90570 and MB90574A series
HWM90570002	20.04.01		Chapter 14.1	Up/Down Counter, incorrect count clock time
HWM90570003	20.04.01		Chapter 1.2	Product Lineup, wrong RAM size of MB90573 mentioned
HWM90570004	20.04.01		Chapter 10	Conditions when release from Watchmode
HWM90570005	20.04.01		Chapter 1	Condition when Voltage drop down
HWM90570006	20.04.01		Chapter 1	Information about Pinstate behaviour during Power-on
HWM90570007	20.04.01		Chapter 19	UART, SCR Register bit definition of PEN-bit exchanged
HWM90570022	26.04.04	1.04	21	I2C INTERFACE, Note added

HWM90570001

Differences between MB90570 and MB90574A/C series:

Request of return from Stop mode:

MB90F574, MB90573,MB90574, MB90V570:
The request of return from STOP mode is High level.
MB90F574A/C, MB90574A/C, MB90V570A/C:
Edge detection (high/low) for return from STOP mode.

Leakage current of DAC:

To avoid a high leakage current of DAC on MASK devices,
DVcc should be >= 3.3V

Affected devices:
MB90573, MB90574: (other O.K.)

Series	Affected	solved
MB90573, MB90574	Yes	--
MB90574A/C	--	Yes

HWM90570002

Chapter 14.1 Functions of 8/16-Bit Up/Down Counter/Timer

Count clock (for 16-MHz operation)

Old:
1.0us (2MHz: divided by 8)
Correct:
0.5us (2MHz: divided by 8)

HWM90570003

Chapter 1.2 Product Line-up

Typo in the table, incorrect RAM size mentioned. See correction below.

Table 1.2-1

	MB90573
ROM size	128Kbyte
RAM size	5 Kbyte
Others	MASK products

HWM90570004

Chapter 10: Watchdog Timer, Time base timer an Watch timer

Watchmode Problem

Condition: Watch Mode Subclock connected(normal operation) or Watchmode, No subclock connected

Description:
If MCU has entered the Watch Mode and only the RST Reset signal is asserted, it could happen, that the CPU does not restart correctly.

Workaround:
RST and HST reset must be asserted simultaneously. Also a power-on reset will restart the CPU correctly again.

HWM90570005

Voltage Drop down Problem

Condition: Voltage Drop on Vcc, No Subclock connected

Description:
If no subclock is connected, it possibly may happen, that after a voltage drop on Vcc, the MCU does not restart correctly, even if RST and HST is asserted simultaneously.

Details:
If a voltage drop on Vcc occurs, there is no power-on reset executed, if the voltage Vcc does not drop below under 0.2V for a certain time (toff), which is specified in the DS. See details on Vcc in the corresponding Datasheet.
Normally, if HST & RST is asserted afterwards, the MCU would restart correctly.
If no subclock is connected, it possibly may happen, that the CPU does not start/work correctly even after RST & HST reset.

Workaround:
a) The usage of a Subclock is highly recommended. If a Subclock is connected and a RST & HST Reset is asserted (RST = HST, reset simultaneously) the CPU will restart correctly.
b) Perform a correct power-on Reset (corresponding to Vcc timing specified in Datasheet)

Power-On Reset

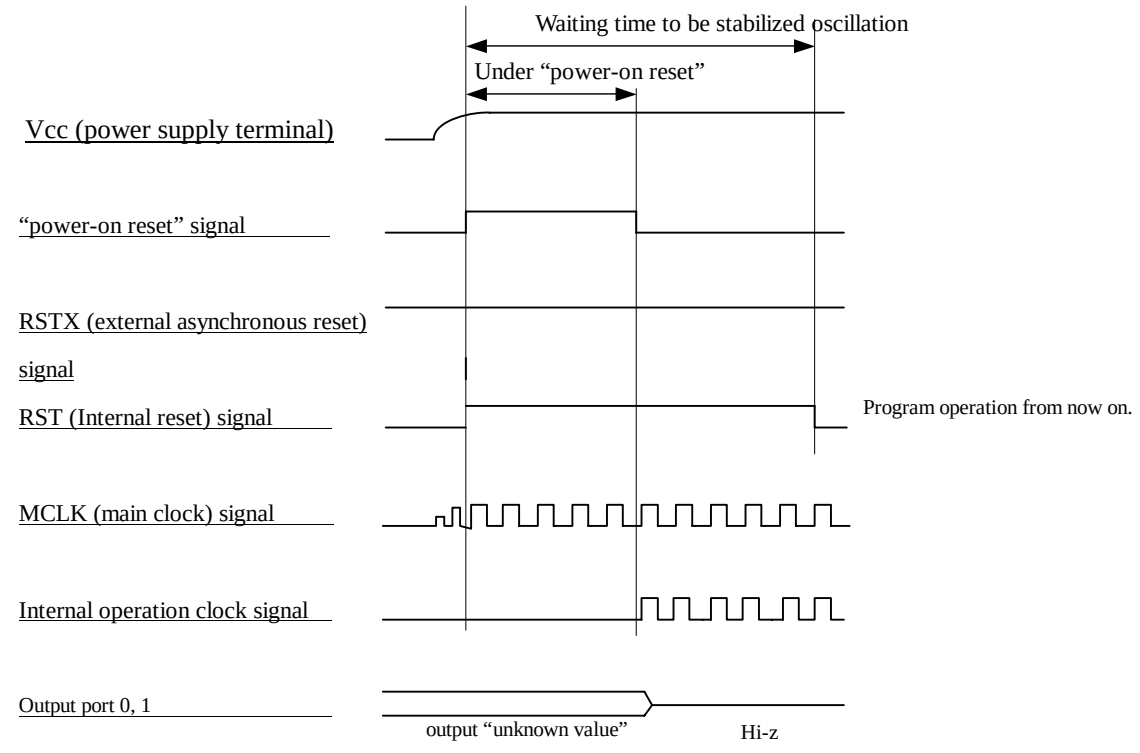
Output “unknown value” , when the power supply Is turned on If F^{2}MC-16LX is used. (Note)

1.Device covered

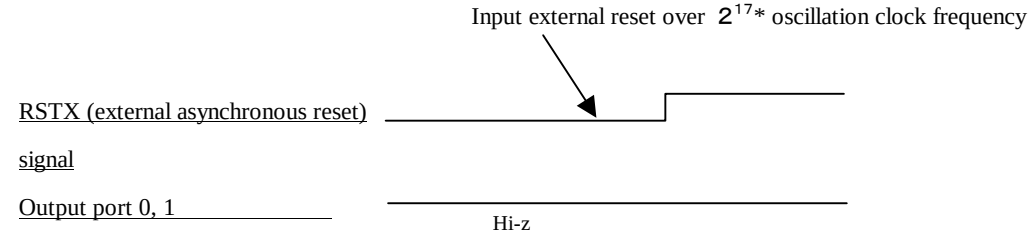
MB90574

2. Note:
Output “unknown value” of pin 00 to pin 7 and pin 10 to pin 17 terminal, when the power supply Is turned on.

Pin 00 to pin 07 and pin 10 to pin 17 terminal become “unknown value” (output “H”, “L” level or output “Hi-z”) under “power-on reset” (stabilized times (2^{17} * oscillation clock frequency) of clamping circuit for internal power supply), when the power supply is turned on, and when “power-on reset” function operates and RSTX terminal is “H” level.
If you want to output “Hi-z” under “power-on reset”, it is applied reset input “ “L” level “ from external and so pin 00 to pin 07 and pin 10 to pin 17 terminal become “Hi-z” condition during the time.
It shows timing chart in detail the next page.
Note:
This workaround will work for Mode pin setting 011 (Single chip, Internal ROM external bus), 110 (Burn_In ROM), 111 (EPROM mode)



How to output “Hi-z” under “power-on reset”



Timing chart

Under “power-on reset” 2^{17} * oscillation clock frequency
(8.192ms in case of oscillation clock frequency = 16MHz)

Waiting time to be stabilized oscillation 2^{18} * oscillation clock frequency
(16.384ms in case of oscillation clock frequency = 16MHz)

HWM90570007

Chapter 19 UART

Chapter 19.3 Serial Control Register (SCR)

[bit 15] PEN (Parity Enable)

Bit definition exchanged

See correction below:

0	Parity not added
1	Parity added

HWM90570022

Chapter 21 I2C INTERFACE

Restriction of specification at sending General Call Address for MCU with I2C

When using Multi-Master mode for I2C and another Master is sending a General Code Address at same time as Fujitsu MCU, an arbitration lost* occurs after 2nd byte.
Under following conditions the restriction do not exist:
- no usage of I2C peripheral
- usage of I2C with Single Master system
- usage of I2C with Multi Master system, no General Call Address used
- usage of I2C with Multi Master system, General Call Address used by Fujitsu MCU, only

*: If the value of data is smaller than another transfer, the arbitration lost does not occur.
Arbitration lost occurs when the transmitting data of the other Master is larger than Fujitsu MCU transmission data.