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Errata

This errata sheet is for MB90560/565 Series Hardware Manual Rev.5 (CM44-10107-5E)

F^{2}MC-16LX
16-BIT MICROCONTROLLER
MB90560/565 Series
HARDWARE MANUAL

2009.4. 2

<table>
<tr><th>Date</th><th>Page</th><th>Item</th><th>Description</th></tr>
<tr><td>-</td><td>5</td><td>Table 1.2-1</td><td>The caption was corrected as follows:

Table 1.2-1 Product Lineup of the MB90560 Series</td></tr>
<tr><td>-</td><td>6</td><td>Table 1.2-1</td><td>The shading in the table below indicates changes made to Table 1.2-1.

<table>
<tr><td>Model</td><td>MB90V560</td><td>MB90F562/B</td><td>MB90562/A</td><td>MB90561/A</td></tr>
<tr><td>Package</td><td>PGA-256</td><td colspan="3">QFP-64 (FPT-64P-M09: 0.65 mm pin pitch)
QFP-64 (FPT-64P-M06: 1.00 mm pin pitch)
SH-DIP-64 (DIP-64P-M01: 1.778 mm pin pitch)</td></tr>
</table></td></tr>
<tr><td>2009/
4/2</td><td>7</td><td>Section 1.2</td><td>Table 1.2-2 was corrected as indicated by the shading below.

• Error

<table>
<tr><td>Model</td><td>MB90F568</td><td>MB90568</td><td>MB90567</td></tr>
<tr><td>Operating voltage</td><td colspan="3">3V+10% to 3V-10% (on maximum machine clock of 8 MHz)</td></tr>
</table>
• Correct

<table>
<tr><td>Model</td><td>MB90F568</td><td>MB90568</td><td>MB90567</td></tr>
<tr><td>Operating voltage</td><td colspan="3">3.3V+0.3V to 3.3V-0.3V (on maximum machine clock of 8 MHz)</td></tr>
</table>
[mcu_doc0338]</td></tr>
<tr><td>-</td><td>11</td><td>Figure 1.4-3</td><td>The following description was added at the under-left of Figure 1.4-3:

*1: Neither MB90568, MB90567 nor MB90F568 are supported.</td></tr>
<tr><td>-</td><td>20</td><td>Table 1.7-1</td><td>The shading in the table below indicates changes made to Table 1.7-1.

<table>
<tr><td>Classification</td><td></td><td>Remarks</td></tr>
<tr><td>A</td><td></td><td>● Oscillation circuit
Oscillation feedback resistor: 1 MΩ approx.</td></tr>
</table></td></tr>
</table>

<table>
<tr><th>Date</th><th>Page</th><th>Item</th><th>Description</th></tr>
<tr><td>-</td><td>21</td><td>Table 1.7-1</td><td>The shading in the table below indicates changes made to Table 1.7-1.

<table>
<tr><th>Classification</th><th>Remarks</th></tr>
<tr><td>E</td><td>● CMOS I/O pin
:
:
● I_{OL} = 12mA</td></tr>
</table>
</td></tr>
<tr><td>-</td><td>25</td><td>Section 1.8</td><td>The following description was added at the end of the page:

❍ Notes on during operation of PLL clock mode
If the PLL clock mode is selected, the microcontroller attempt to be working with the self-oscillating circuit even when there is no external oscillator or external clock input is stopped. Performance of this operation, however, cannot be guaranteed.

❍ N.C. Pin
The N.C. (internally connected) pin must be opened for use.</td></tr>
<tr><td>-</td><td>33</td><td>Figure 2.3-1</td><td>The description in Figure 2.3-1 was corrected as indicated by the shading below:

<table>
<tr><th>Model</th><th>Address #1</th></tr>
<tr><td>MB90V560</td><td>$FE0000_H$ *</td></tr>
</table>
</td></tr>
</table>

<table>
<tr><th>Date</th><th>Page</th><th>Item</th><th>Description</th></tr>
<tr><td>-</td><td>87</td><td>Table 4.3-1</td><td>The shading in the table below indicates changes made to Table 4.3-1.

<table>
<tr><th>Bit name</th><th>Function</th></tr>
<tr><td>bit13
bit12</td><td>WS1, WS0:
Oscillation stabilization wait interval selection bita</td><td>● These bits select the oscillation stabilization wait interval for the oscillation clock after the stop mode has been cleared due to an external interrupt. When PLL stop mode is returned to PLL clock mode, the oscillation stabilization wait interval requires 2^{14}/HCLK or more. When changing to PLL clock mode, these bits are set to "10_B" or "11_B".
::</td></tr>
<tr><td>bit10</td><td>MCS:
Machine clock selection bit</td><td>:
:
● When the main clock mode is switched to PLL clock mode, the oscillation stabilization wait interval is fixed to 2^{14}/HCLK. The oscillation stabilization wait interval is about 4.1 ms if the oscillation clock frequency is 4 MHz.)
● When the main clock has been selected, the oscillation clock divided by 2 is used as the machine clock.
::</td></tr>
</table></td></tr>
<tr><td>-</td><td>88</td><td>Section 4.4</td><td>The shaded portion below was added to the Note for "■ Clock Mode Transition".

In attempting to switch the clock mode, do not attempt to switch to another clock mode or low-power consumption mode until the first switching is completed. The MCM bit of the clock selection register (CKSCR) indicates that switching is completed.</td></tr>
<tr><td>-</td><td>88</td><td>Section 4.4</td><td>The following description of "❍ Switching from PLL clock mode to main clock mode " in "■ Clock Mode Transition " were added as indicated by shading below.

Note:
Before setting the peripheral functions (resources) after the machine clock switching, makesure that the machine clock has been switched by referring to the MCM bit of the CKSCR.
If the mode is switched to another clock mode or low-power-consumption mode before completion of switching, the mode may not be switched.</td></tr>
<tr><td>-</td><td>90</td><td>Section 4.5</td><td>The last line of " Oscillation Stabilization Wait Interval" was corrected as indicated by the shading below.

during an oscillation stabilization wait interval. After the oscillation stabilization wait interval has elapsed, the CPU changes to PLL clock mode.</td></tr>
<tr><td>-</td><td>95</td><td>Section 5.1</td><td>The Note for " Standby Mode" was corrected as indicated by the shading below.

Note:
Because stop mode and hardware standby mode turn the oscillation clock off, these modes save the most power while data is being retained. In attempting to switch the clock mode, do not attempt to switch to another clock mode or low-power consumption mode until the first switching is completed. The MCM bit of the clock selection register (CKSCR) indicates that switching is completed.
If the mode is switched to another clock mode or low-power-consumption mode before completion of switching, the mode may not be switched.</td></tr>
</table>

<table>
<tr><th>Date</th><th>Page</th><th>Item</th><th>Description</th></tr>
<tr><td>-</td><td>99</td><td>Section 5.3</td><td>The following note was added at the end of the page:

Note:
To set a pin to high impedance when the pin is shared by a peripheral function and a port in stop mode or time-base timer mode, disable the output of peripheral functions, and set the STP bit of the low-power consumption mode control register (LPMCR) to 1 or set the TMD bit to 0.
This applies to the following pins:
P21/TO0, P23/TO1, P30/RTO0, P31/RTO1, P32/RTO2, P33/RTO3, P34/RTO4, P35/RTO5, P37/SOT0</td></tr>
<tr><td>-</td><td>100</td><td>Section 5.3</td><td>Table5.3-2 was corrected as indicated by shading below.

• Error
<table>
<tr><td>MOV</td><td>io,#imm8</td><td>MOV</td><td>dir,#imm8</td><td>MOV</td><td>eam,#imm8</td><td>MOV</td><td>eam, Ri</td></tr>
<tr><td>MOV</td><td>io,A</td><td>MOV</td><td>dir,A</td><td>MOV</td><td>addr16,A</td><td>MOV</td><td>eam,A</td></tr>
<tr><td>MOV</td><td>@RLi+disp8,A</td><td>MOVP</td><td>addr24,A</td><td></td><td></td><td></td><td></td></tr>
<tr><td>MOVW</td><td>io,#imm16</td><td>MOVW</td><td>dir,#imm16</td><td>MOVW</td><td>eam,#imm16</td><td>MOVW</td><td>eam,RWi</td></tr>
<tr><td>MOVW</td><td>io,A</td><td>MOVW</td><td>dir,A</td><td>MOVW</td><td>addr16</td><td>MOVW</td><td>eam,A</td></tr>
<tr><td>MOVW</td><td>@RLi+disp8,A</td><td>MOVPW</td><td>addr24,A</td><td></td><td></td><td></td><td></td></tr>
</table>

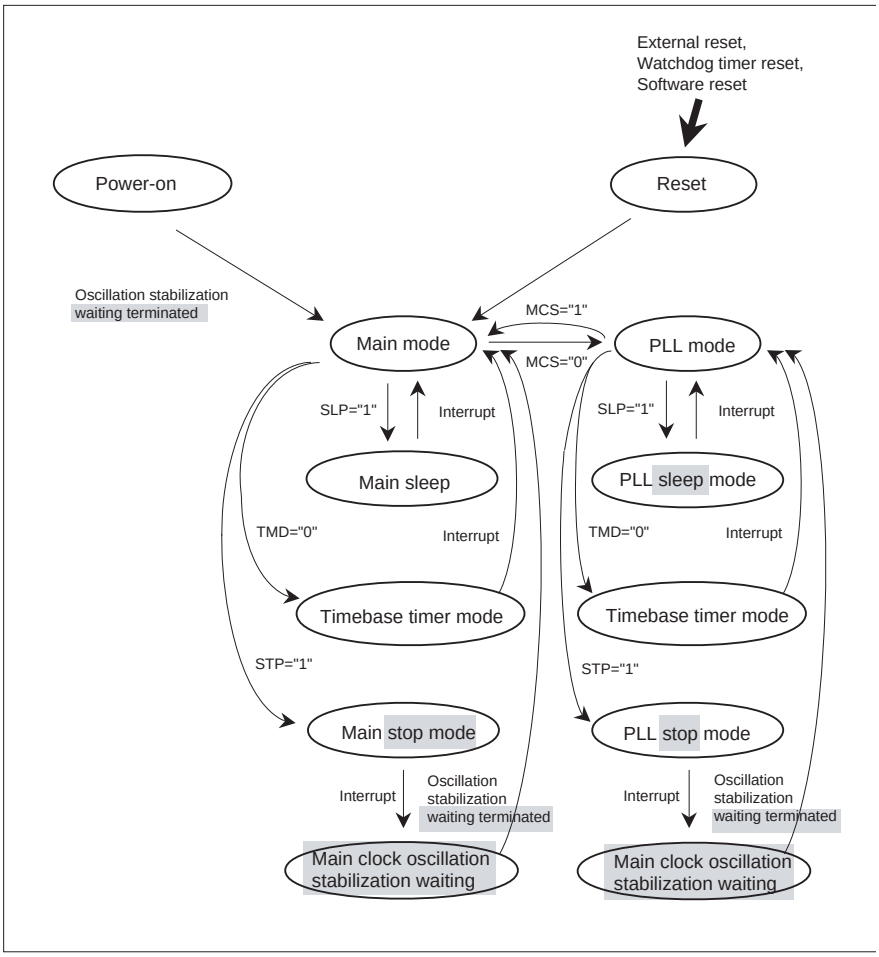
• Correct
<table>
<tr><td>MOV</td><td>io,#imm8</td><td>MOV</td><td>dir,#imm8</td><td>MOV</td><td>eam,#imm8</td><td>MOV</td><td>eam,Ri</td></tr>
<tr><td>MOV</td><td>io,A</td><td>MOV</td><td>dir,A</td><td>MOV</td><td>addr16,A</td><td>MOV</td><td>eam,A</td></tr>
<tr><td>MOV</td><td>@RLi+disp8,A</td><td></td><td></td><td></td><td></td><td></td><td></td></tr>
<tr><td>MOVW</td><td>io,#imm16</td><td>MOVW</td><td>dir,#imm16</td><td>MOVW</td><td>eam,#imm16</td><td>MOVW</td><td>eam,RWi</td></tr>
<tr><td>MOVW</td><td>io,A</td><td>MOVW</td><td>dir,A</td><td>MOVW</td><td>addr16,A</td><td>MOVW</td><td>eam,A</td></tr>
<tr><td>MOVW</td><td>@RLi+disp8,A</td><td></td><td></td><td></td><td></td><td></td><td></td></tr>
<tr><td>SETB</td><td>io:bp</td><td>SETB</td><td>dir:bp</td><td>SETB</td><td>addr16:bp</td><td></td><td></td></tr>
<tr><td>CLRB</td><td>io:bp</td><td>CLRB</td><td>dir:bp</td><td>CLRB</td><td>addr16:bp</td><td></td><td></td></tr>
</table>
</td></tr>
<tr><td>-</td><td>102</td><td>Table 5.5-1</td><td>The shading in the table below indicates changes made to Table 5.5-1.

<table>
<tr><td>Standby mode</td><td>Condition for switch</td><td>Oscillation</td><td>Machine clock</td></tr>
<tr><td></td><td></td><td></td><td></td></tr>
</table>
</td></tr>
<tr><td>-</td><td>102</td><td>Section 5.5</td><td>The following note was added to "■ Operating Status during Standby Mode":

Note:
To set a pin to high impedance when the pin is shared by a peripheral function and a port in stop mode or time-base timer mode, disable the output of peripheral functions, and set the STP bit of the low-power consumption mode control register (LPMCR) to 1 or set the TMD bit to 0.
This applies to the following pins:
P21/TO0, P23/TO1, P30/RTO0, P31/RTO1, P32/RTO2, P33/RTO3, P34/RTO4, P35/RTO5, P37/SOT0</td></tr>
<tr><td>-</td><td>103</td><td>Section 5.5.1</td><td>The following description was deleted:

❍ Hold function
In sleep mode, the hold function is enabled. A hold request sets the hold status.</td></tr>
</table>

Date	Page	Item	Description
-	105	Section 5.5.2	The following note was added to "■ Switching to Timebase Timer Mode": Note: To set a pin to high impedance when the pin is shared by a peripheral function and a port in time-base timer mode, disable the output of peripheral functions, and set the TMD bit of the low-power consumption mode control register (LPMCR) to 0. This applies to the following pins: P21/TO0, P23/TO1, P30/RTO0, P31/RTO1, P32/RTO2, P33/RTO3, P34/RTO4, P35/RTO5, P37/SOT0
-	107	Section 5.5.3	The following note was added to "■ Switching to Stop Mode": Note: To set a pin to high impedance when the pin is shared by a peripheral function and a port in stop mode, disable the output of peripheral functions, and set the STP bit of the low-power consumption mode control register (LPMCR) to 1. This applies to the following pins: P21/TO0, P23/TO1, P30/RTO0, P31/RTO1, P32/RTO2, P33/RTO3, P34/RTO4, P35/RTO5, P37/SOT0
-	107	Section 5.5.3	The following sentence was added at the second line of "■ Release of Stop Mode": At return from stop mode, since the oscillation clock (HCLK) has stopped, the stop mode is released after the oscillation stabilization wait interval of the main clock.
-	108	Section 5.5.3	The following note was added at the end of the page: Note: In PLL stop mode, the main clock and PLL multiplication circuit stop. At return from PLL stop mode, it is necessary to allot the main clock oscillation stabilization wait interval and PLL clock oscillation stabilization wait interval. The oscillation stabilization wait intervals for the main clock and PLL clock are counted simultaneously according to the value specified in the oscillation stabilization wait interval selection bits (CKSCR: WS1, WS0) in the clock selection register. The oscillation stabilization wait interval selection bits (CKSCR: WS1, WS0) in the clock selection register must be selected accordingly to account for the longer of main clock and PLL clock oscillation stabilization wait interval. The PLL clock oscillation stabilization wait interval, however, requires 2^{14}/HCLK or more. Set the oscillation stabilization wait interval selection bits (CKSCR: WS1, WS0) in the clock selection register to "10_B" or "11_B".

Date	Page	Item	Description
-	109	Figure 5.6-1	The shading in the figure below indicates changes made to Figure 5.6-1. 
-	110	Section 5.7	The following note was added to "■ Status of Pins in Single-Chip Mode": Note: To set a pin to high impedance when the pin is shared by a peripheral function and a port in stop mode or time-base timer mode, disable the output of peripheral functions, and set the STP bit of the low-power consumption mode control register (LPMCR) to 1 or set the TMD bit to 0. This applies to the following pins: P21/TO0, P23/TO1, P30/RTO0, P31/RTO1, P32/RTO2, P33/RTO3, P34/RTO4, P35/RTO5, P37/SOT0
-	110	Table 5.7-1	The shading in the table below indicates changes made to Table 5.7-1.

Pin name	Standby mode			Hold
	Sleep mode	Stop mode / Timebase timer mode		
		SPL=0	SPL=1	

Date	Page	Item	Description
-	111	Section 5.8	The following description was added below the "■ Switching to Standby Mode and Interrupts": ■ Notes on the transition to standby mode To set a pin to high impedance when the pin is shared by a peripheral function and a port in stop mode or time-base timer mode, use the following procedure: 1. Disable the output of peripheral functions. 2. Set the SPL bit of the low-power consumption mode control register (LPMCR) to 1, and set the STP bit to 1 or set the TMD bit to 0.
-	112	Section 5.8	The description of "❍ PLL clock oscillation stabilization wait interval" was corrected as follows: In main clock mode, the PLL multiplication circuit stops. When changing to PLL clock mode, it is necessary to reserve the PLL clock oscillation stabilization wait interval. While waiting for PLL clock oscillation stabilization, the CPU operates on the main clock. The PLL clock oscillation stabilization wait interval is fixed at 2^{14}/HCLK (HCLK: clock oscillation frequency). In PLL stop mode, the main clock and PLL multiplication circuit stop. At return from PLL stop mode, it is necessary to allot the main clock oscillation stabilization wait interval and PLL clock oscillation stabilization wait interval. The oscillation stabilization wait intervals for the main clock and PLL clock are counted simultaneously according to the value specified in the oscillation stabilization wait interval selection bits (CKSCR: WS1, WS0) in the clock selection register. The oscillation stabilization wait interval selection bits (CKSCR: WS1, WS0) in the clock selection register must be selected accordingly to account for the longer of main clock and PLL clock oscillation stabilization wait interval. The PLL clock oscillation stabilization wait interval, however, requires 2^{14}/HCLK or more. Set the oscillation stabilization wait interval selection bits (CKSCR: WS1, WS0) in the clock selection register to "10_B" or "11_B".
-	112	Section 5.8	The following description was added at the end of the page: ■ Switching the clock mode In attempting to switch the clock mode, do not attempt to switch to another clock mode or low-power consumption mode until the first switching is completed. The MCM bit of the clock selection register (CKSCR) indicates that switching is completed. If the mode is switched to another clock mode or low-power-consumption mode before completion of switching, the mode may not be switched.
-	184	Section 8.5.2	The following note was added to "❍ Port operation in stop or time-base timer mode": Note: To set a pin to high impedance when the pin is shared by a peripheral function and a port in stop mode or time-base timer mode, disable the output of peripheral functions, and set the STP bit of the low-power consumption mode control register (LPMCR) to 1 or set the TMD bit to 0. This applies to the following pins: P21/TO0, P23/TO1
-	189	Section 8.6.2	The following note was added to "❍ Port operation in stop or time-base timer mode": Note: To set a pin to high impedance when the pin is shared by a peripheral function and a port in stop mode or time-base timer mode, disable the output of peripheral functions, and set the STP bit of the low-power consumption mode control register (LPMCR) to 1 or set the TMD bit to 0. This applies to the following pins: P30/RTO0, P31/RTO1, P32/RTO2, P33/RTO3, P34/RTO4, P35/RTO5, P37/SOT0

<table>
<tr><th>Date</th><th>Page</th><th>Item</th><th>Description</th></tr>
<tr><td>-</td><td>215</td><td>Table 9.3-1</td><td>The shading in the table below indicates changes made to Table 9.3-1.

<table>
<tr><th colspan="2">Bit name</th><th>Function</th></tr>
<tr><td colspan="3"></td></tr>
<tr><td>bit11</td><td></td><td>:
:
● When this bit is set to "1", there is no effect on operation.
● Reading by read - modify - write type instructions always returns "1".
Note:
:
:
● This bit is cleared to "0" when writing "0", a transition to stop mode occurs, a transition from main clock mode to PLL clock mode, the timebase timer is cleared due to the timebase timer initialization bit (TBR), or a reset occurs.</td></tr>
<tr><td colspan="3"></td></tr>
</table></td></tr>
<tr><td>-</td><td>217</td><td>Section 9.5</td><td>The first line of "■ Oscillation Stabilization Wait Interval Timer Function" was corrected as follows:

The timebase timer is also used as the oscillation stabilization wait interval timer for the main clock and the PLL clocks.</td></tr>
<tr><td>-</td><td>218</td><td>Table 9.5-1</td><td>The shading in the table below indicates changes made to Table 9.5-1.

<table>
<tr><th>Operation</th><th>Counter clear</th><th>TBOF clear</th><th>Oscillation Stabilization Wait Interval</th></tr>
<tr><td>TBTC: Writing of 0 to TBR</td><td>❍</td><td>❍</td><td></td></tr>
<tr><td>Power - on reset</td><td>❍</td><td>❍</td><td rowspan="2">Main clock oscillation stabilization wait Interval</td></tr>
<tr><td>Watchdog reset</td><td>X</td><td>❍</td></tr>
<tr><td>Releasing of stop mode</td><td>❍</td><td>❍</td><td>Main clock oscillation stabilization wait Interval</td></tr>
<tr><td>Transition from main clock mode to PLL clock mode (MCS = 1 to 0)</td><td>❍</td><td>❍</td><td>PLL clock oscillation stabilization wait Interval</td></tr>
<tr><td>Releasing of timebase timer mode</td><td>X</td><td>X</td><td>Not provided</td></tr>
<tr><td>Releasing of sleep mode</td><td>X</td><td>X</td><td>Not provided</td></tr>
</table></td></tr>
<tr><td>-</td><td>276</td><td>Section 12.3.2</td><td>The following note was added at the end of the page:

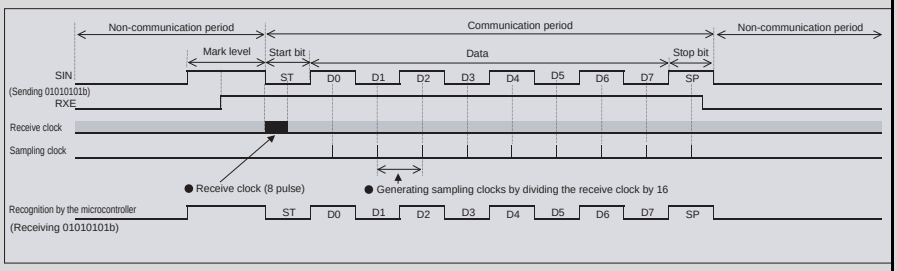
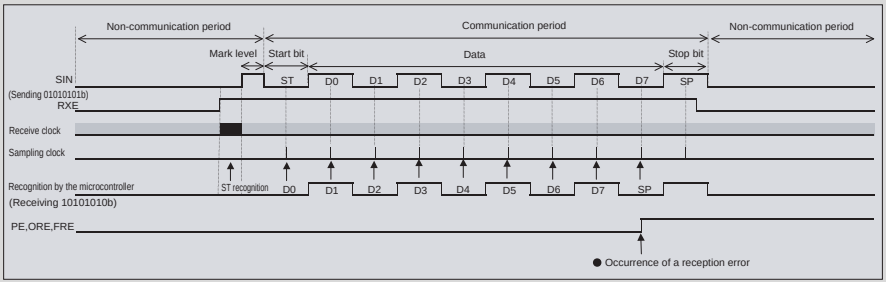
Note:
To rewriting the compare register, within the compare interrupt routine or compare operation is disabled.
Be sure not to occur simultaneously a compare match and writing the compare register.</td></tr>
<tr><td>-</td><td>302</td><td>Section 12.4.2</td><td>The following sentence was deleted from the "■ Output Compare Timing":

No compare operation with the counter value is performed when setting the compare register.</td></tr>
<tr><td>-</td><td>302</td><td>Section 12.4.2</td><td>The Figure 12.4-7 was deleted.</td></tr>
<tr><td>-</td><td>303</td><td>Section 12.4.2</td><td>The following note was added at the end of the page:

Note:
To rewriting the compare register, within the compare interrupt routine or compare operation is disabled.
Be sure not to occur simultaneously a compare match and writing the compare register.</td></tr>
</table>

Date	Page	Item	Description
-	324	Table 13.1-1	The shading in the table below indicates changes made to Table 13.1-1. Baud rate: ● Up to 2MHz (when the machine clock is operated at 16MHz) ● A dedicated baud rate generator is provided. ● Baud rate by an external clock (clock input through the SCK0/SCK1 pins) ● Internal clock (internal clocks supplied from 16-bit reload timer 0 and 1 can be used.) ● The baud rate can be selected from a total of eight types
-	327	Figure 13.2-1	In the description upper-left the figure, the following terms was changed as indicated by the shading below: 16-bit reload timer --> 16-bit reload timer 0, 1
-	327	Section 13.2	The last line of "❍ Clock Selector" was corrected as follows: supplied from the 16-bit reload timer). --> supplied from the 16-bit reload timer 0 and 1).
-	335	Figure 13.4-3	The description in Figure 13.4-3 was corrected as indicated by the shading below: "110_B" | Baud rate by internal timer (16-bit reload timer 0, 1)
-	336	Table 13.4-2	The shading in the table below indicates changes made to Table 13.4-2. bit 5, bit 4, bit 3 | CS2 to CS0: Clock selection bits | ● This bit selects a baud rate clock source. When the dedicated baud rate : : ● Clock input can be selected from external clocks (SCK0/SCK1 pin input), the internal clock (16-bit reload timer 0 and 1), and the dedicated baud rate generator.
-	349	Section 13.6	The third line of the summary was corrected as follows: ● Internal clock (16-bit reload timer 0) --> ● Internal clock (16-bit reload timer 0 and 1).
-	349	Section 13.6	The following description was corrected: ❍ Baud Rates Determined Using the Internal Clock The internal clock supplied from 16-bit reload timer 0 and 1 is used as is (synchronous) or by dividing it by 16 (asynchronous) for the baud rate. Any baud rate can be set by the reload timer 0 and 1 value.
-	350	Figure 13.6-1	In the description left the figure, the following terms was changed as indicated by the shading below: 16-bit reload timer 0 --> 16-bit reload timer 0, 1

Date	Page	Item	Description
-	353	Section 13.6.2	The section title was corrected as follows: 13.6.2 Baud Rates Determined Using the Internal Timer (16-bit Reload Timer 0 and 1)
-	353	Section 13.6.2	The summary was corrected as follows: This section describes the settings used when the internal clock supplied from 16-bit reload timer 0 and 1 is selected as the UART transfer clock. It also shows the baud rate calculation formulas.
-	353	Section 13.6.2	The following description was corrected: ■ Baud Rates Determined Using the Internal Timer (16-bit Reload Timer 0 and 1) If the clock setting bits (CS2 to CS0) of the mode register (SMR0/SMR1) are set to "110_B", the baud rate is set by the internal clock. The baud rate can be set by specifying the prescaler division ratio and reload value of the 16-bit reload timer 0 and 1.
-	353	Figure 13.6-2	The caption was corrected as follows: Figure 13.6-2 Baud Rate Selection Circuit for the Internal Timer (16-Bit Reload Timer 0, 1)
-	353	Figure 13.6-2	In the description left the figure, the following terms was changed as indicated by the shading below: 16-bit reload timer output --> 16-bit reload timer 0, 1 output
-	353	Section 13.6.2	The sentences of "❍ Baud Rate Calculation Formulas" were corrected as indicated by the shading below. N: Division ratio for the prescaler of 16-bit reload timer 0, 1 (2^1, 2^3, or 2^5) n: Reload value for 16-bit reload timer 0, 1 (0 to 65535)
-	354	Table 13.6-4	The footer of the Table 13.6-4 was corrected as follows: N: Division ratio for the prescaler of 16-bit reload timer 0, 1

Date	Page	Item	Description
-	359	13.7.1	The following description was added below the "❍ Receiving Operation": ❍ Detecting the start bit Implement the following settings to detect the start bit: ● Set the communication line level to H (attach the mark level) before the communication period. ● Specify reception permission (RXE = H) while the communication line level is H (mark level). ● Do not specify reception permission (RXE = H) for periods other than the communication period (without mark level). Otherwise, data is not received correctly. ● After the stop bit is detected (the RDRF flag is set to 1), specify reception inhibition (RXE = L) while the communication line level is H (mark level).  Note that specifying reception permission at the timing shown below obstructs the correct recognition of the input data (SIN) by the microcontroller. ● Example of operation if reception permission (RXE = H) is specified while the communication line level is L. 
-	381	Section 14.4.1	The Note was corrected as follows: Note: A read-modify-write instruction always reads "1" from the DTP/interrupt cause register (EIRR). If more than one external interrupt request output is enabled (EN7 to EN0 of ENIR are set to 1), clear to 0 only the bit for which the CPU accepted an interrupt (any of bits ER7 to ER0 that are set to 1). Do not clear the other bits without a valid reason.

<table>
<tr><th>Date</th><th>Page</th><th>Item</th><th>Description</th></tr>
<tr><td>-</td><td>416</td><td>Section 16.4.1</td><td>Table 16.4-1 was added as indicated by shading below.

<table>
<tr><th>Bit name</th><th></th><th>Function</th></tr>
<tr><td>bit 9</td><td>STRT:
A/D
conversion
activation bit</td><td>l This bit allows software to start A/D conversion.
● When this bit is set to "0", operation is not affected.
● Writing 1 to this bit activates A/D conversion.
● In stop conversion mode, conversion cannot be reactivated with this bit.
● The value read from this bit is "1".
● The read-modify-write series commands read "0".
Note:
Never perform the forced stop and activation (BUSY="0", STRT="1") of the A/D conversion simultaneously.</td></tr>
</table></td></tr>
<tr><td>-</td><td>418</td><td>Section 16.4.2</td><td>Table 16.4-2 was corrected as indicated by shading below.

• Error

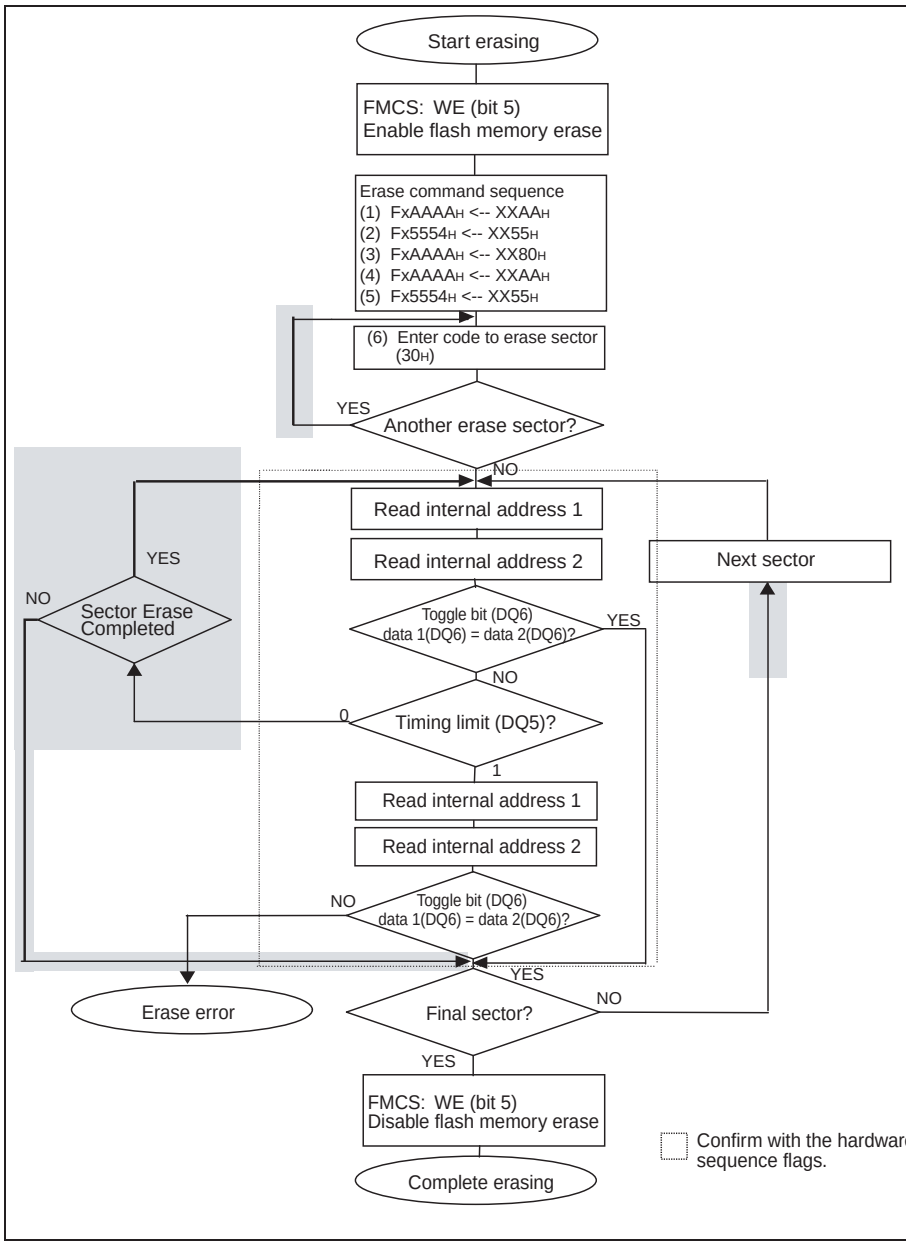
<table>
<tr><th>Bit name</th><th></th><th>Function</th></tr>
<tr><td>bit5
bit4
bit3</td><td>ANS2, ANS1,
ANS0:
A/D conversion
start channel
setting bit</td><td>● These bits are used to set the A/D conversion start channel and check the channel number being converted.
● When the A/D conversion is activated, it is started from the channel specified by the A/D conversion start channel setting bits (ANS2 to ANS0).
● During A/D conversion, the channel number being converted is read out.
During a pause in stop conversion mode, the channel number converted just before is read out.</td></tr>
</table>
・Correct

<table>
<tr><th>Bit name</th><th></th><th>Function</th></tr>
<tr><td>bit5
bit4
bit3</td><td>ANS2, ANS1,
ANS0:
A/D conversion
start channel
setting bit</td><td>● These bits are used to set the A/D conversion start channel and check the channel number being converted.
● When the A/D conversion is activated, it is started from the channel specified by the A/D conversion start channel setting bits (ANS2 to ANS0).
● During A/D conversion, the channel number being converted is read out.
And before A/D conversion starts, the previous conversion channel will be read even if these bits have already been set to the new value.
● These bits are initialized to "000_B" at reset.</td></tr>
</table></td></tr>
<tr><td>-</td><td>456</td><td>Section 19.1</td><td>The eighth line of "■ Characteristics of the 512K-Bit Flash Memory" was corrected as follows:

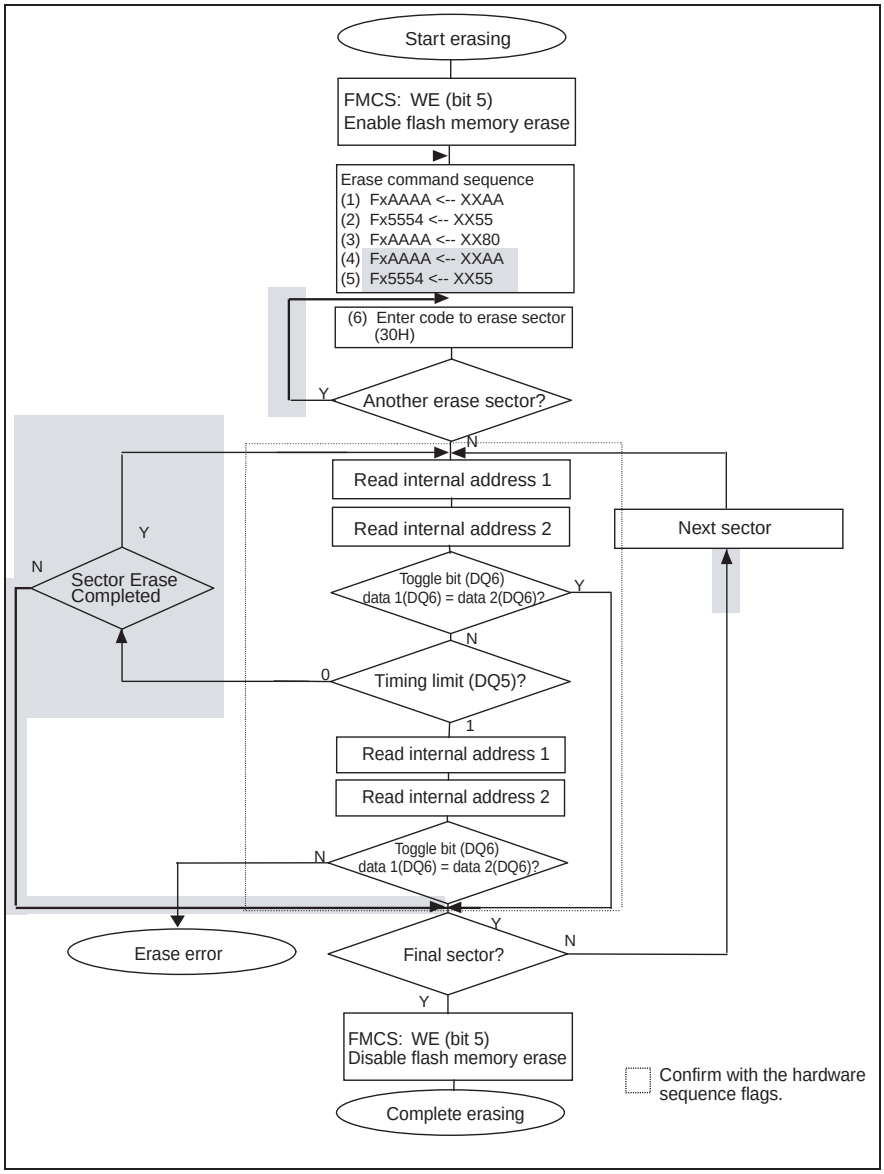
● Minimum of 10,000 write/erase operations</td></tr>
<tr><td>-</td><td>460</td><td>Table 19.3-1</td><td>The shading in the table below indicates changes made to Table 19.3-1.

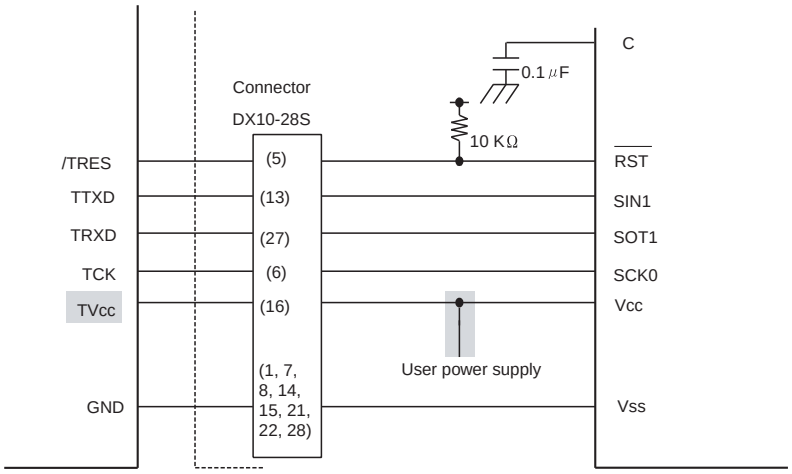
<table>
<tr><td>bit 3
bit 1</td><td>Reserved:
Reserved bit</td><td>● Always set this bit to "0".</td></tr>
</table></td></tr>
</table>

Date	Page	Item	Description
2009/ 4/2	476	Section 19.6.4	Figure 19.6-2 was corrected as indicated by the shading below.



Date	Page	Item	Description
2009/ 4/2	505	Section 20.6.4	Figure 20.6-2 was corrected as indicated by the shading below.



<table>
<tr><th>Date</th><th>Page</th><th>Item</th><th>Description</th></tr>
<tr><td>2009/
4/2</td><td>513</td><td>Section 21.1</td><td>Table 21.1-3 was deleted as indicated by the shading below.
<table><tr><th>Model</th><th>Function</th></tr><tr><td>AZ264</td><td>Power regulator (MB90F568: Required when power is supplied from the flash microcomputer programmer to the 3V products)</td></tr></table></td></tr>
<tr><td>2009/
4/2</td><td>517
518</td><td>Section 21.3</td><td>The description of section 21.3.2 was deleted.</td></tr>
<tr><td>-</td><td>519</td><td>Figure 21.4-1</td><td>The description in Figure 21.4-1 was corrected as indicated by the shading below:
 
</td></tr>
<tr><td>2009/
4/2</td><td>521</td><td>Section 21.5</td><td>The description of section 21.5.2 was deleted.</td></tr>
<tr><td>2009/
1/16</td><td>592</td><td>APPENDIX
B</td><td>■Table B.9-20 XCH Ri, ea Instruction (First Byte = 7E_H) is changed.
・Error
Item "A"
Line of +A "W2+d16,A"
・Correct
Item "A0"
Line of +A "@RW2+d16"</td></tr>
</table>

FUJITSU

Corrections of Hardware Manual

MB90560/5 -

hm90560-cm44-10107-5e-corr-x1-05

Addendum, MB90560/5 Hardware Manual (CM42-10107-5E)

This is the Addendum for the Hardware Manual CM42-10107-5E of the MB90560/5 microcontroller series. It describes all known discrepancies of the MB90560/5 microcontroller series Hardware Manual.

Ref. Number (Internal ref. number) (Text Link)	**Date** dd.mm.yy	**Version No.**	**Chapter/Page**	**Description/Correction**
HWM90560001	11.06.01	1.00	6.4.5	Interrupt Processing time
HWM90560002	11.06.01	1.00	1.8	Power On Reset
HWM90560003	20.08.01	1.02	19	Flash Security Feature, Description updated
HWM90560004	11.06.01	1.00	1.8	Handling the Device, Information about reserved memory area
HWM90560005	28.06.01	1.01	1.8	RTO Port behaviour during Reset

HWM90560001

Chapter 6.4.5 Interrupt processing Time

The correct interrupt processing time is calculated with:
When returning from an interrupt : o = 15 + 6 * z machine cycles

HWM90560002

Power-On Reset
==========

Output “unknown value” , when the power supply Is turned on If F^{2}MC-16LX is used. (Note)

1.Device covered

MB90V560, MB90F562, MB90F568,
MB90561, MB90562, MB90567, MB90568

2. Note:

During testing it has been found that some port pins may enter an undefined state during power on. By asserting RSTx during the power on reset (2^{17} cycles of main clock) port pins can be forced to high impedance.

The following Ports will output a High Impedance (Hi-z) at the terminal when the power supply is turned on when PONR and RSTX = 1:

P40 – P67

The following ports will output High Impedance (High-Z) on RSTX or with the End of PONR and Start of internal clocks:

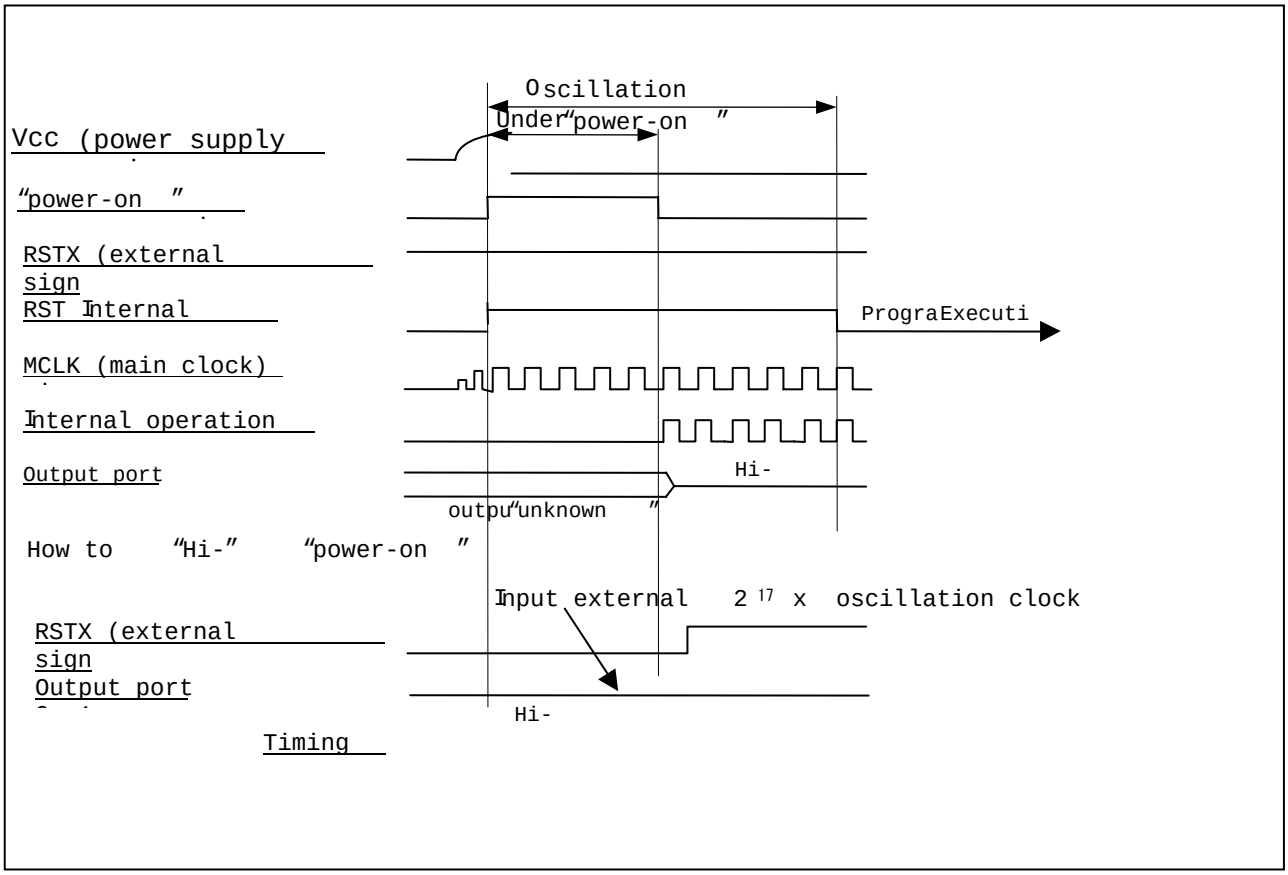
P00 – P17

The following Ports will output High Impedance (high-Z) with the End of PONR and Start of the internal Clock. RSTX does not force the pins to high-Z during power on.

P20 – P37

Note:
This workaround will work for Mode pin setting 011 (Single chip, Internal ROM external bus), 110 (Burn_In ROM), 111 (EPROM mode)

The following diagram shows the timing chart in detail.



Under “power-on reset” 2^{17} x oscillation clock frequency
(8.192ms in case of oscillation clock frequency = 16MHz)

Waiting time to be stabilized oscillation 2^{18} x oscillation clock frequency
(16.384ms in case of oscillation clock frequency = 16MHz).

CHAPTER 19 512K-BIT (64 KB) FLASH MEMORY

Flash Security Feature
==========

Correction:

The Flash Security Feature is not inside MB90F562 Series, these Feature is **only** inside **MB90F562B** Series!

Chapter 19.8 Flash Security Feature

The Flash security Controller provides possibilities to protect the content of the flash memory from being read from external pins.

- **Flash Security Feature**

One predefined address of the flash memory is assigned to the Flash Security Controller (512K-bit flash memory: FF0001). If the protection code of "01H" is written is this address, access to the flash memory is restricted. Once the flash memory is protected, performing the chip erase operation only can unlock the function otherwise read/write access to the flash memory from any external pins is not generally possible.
This function is suitable for applications requiring security of self-containing and data stored in the flash memory. If the target application requires any part of program to locate outside the microcontroller, the Flash Security Controller can not offer the intended features. For this reason, the External Vector Fetch mode should not be used when the protection code is set.
Programming of the flash microcontroller by standard parallel programmer may require unique set-up. For example, with the programmer from Minato Electronics the device checking should be turned off. Writing the protection code is generally recommended to take place at the end of the flash programming. This is to avoid unnecessary protection during the programming.
In order to re-program the once protected flash memory, the chip erase operation should be performed.

For further information, please contact Fujitsu.

HWM90560004

Chapter 1.8 Handling the Device

Reserved Area
==========
Last Word of Memory (FFFFFE – FFFFFF) is reserved AREA. Do not use this last WORD

Chapter 1.8 Handling the device

RTO Port pin (P30-P35) behaviour during Reset

When using RTO port Function or the port pins P30-P35, the following behaviour occurs if the external RST Reset pin is asserted:

When asserting RST low, the RTO Ports (P30-P35) will drive active ‘High’ Level about 400 ns, starting with the falling edge of the RST signal. This might cause problems in some kind of applications.

Especially in case of IGBT drivers, a workaround could be used to disable the output drivers during reset. This could be done e.g by using an additional I/O port, which is tristate during RST. With a corresponding pull-up/down resistance at this port, the level on this pin can be hold high/low during reset in order to keep the driver disabled. After the reset the drivers could be enabled by initialising the port pin correspondingly by software.