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Errata

This errata sheet is for MB90550A/B Series Hardware Manual Rev.6 (CM44-10103-6E)

F^{2}MC-16LX
16-BIT MICROCONTROLLER
MB90550A/B Series
HARDWARE MANUAL

2009.4.2
: Corrected part

<table>
<tr><th>Date</th><th>Page</th><th>Item</th><th>Description</th></tr>
<tr><td>2008/
8/14</td><td>-</td><td>-</td><td>See the following page for details.</td></tr>
<tr><td>2009/
4/2</td><td>106</td><td>5.4.5</td><td>The following two columns were added to the right side of "Table 5.4-3 Status of Each Pin in the External Bus 16-Bit Data Bus Mode".
<table>
<tr><th>Pin Name</th><th>Internal ROM access immediately after reset cancellation</th><th>Internal ROM access after external ROM access</th></tr>
<tr><td>P07 to P00
(AD07 to AD00) ,
P17 to P10
(AD15 to AD08)</td><td>Output Hi-Z/Input enabled</td><td>Output Hi-Z/Input enabled</td></tr>
<tr><td>P27 to P20
(A23 to A16)</td><td>Output state (*1)</td><td>Maintains the previous address</td></tr>
<tr><td>P37(CLK)</td><td>CLK output</td><td>CLK output</td></tr>
<tr><td>P36(RDY)</td><td rowspan="3">Output Hi-Z/Input enabled</td><td rowspan="3">Output Hi-Z/Input enabled</td></tr>
<tr><td>P35 (HAKY)</td></tr>
<tr><td>P34(HRQ)</td></tr>
<tr><td>P33($\overline{\text{WRH}}$)</td><td rowspan="3">"H" output</td><td rowspan="3">"H" output</td></tr>
<tr><td>P32($\overline{\text{WRL}}$)</td></tr>
<tr><td>P31($\overline{\text{RD}}$)</td></tr>
<tr><td>P30(ALE)</td><td>"L" output</td><td>"L" output</td></tr>
<tr><td>P47 to P40,
P55 to P50,
P67 to P60,
P87 to P80,
P97 to P90,
PA4 to PA0</td><td rowspan="2">Output Hi-Z/Input enabled</td><td rowspan="2">Output Hi-Z/Input enabled</td></tr>
<tr><td>P77 to p70</td></tr>
</table>
[mcu_doc0318]</td></tr>
</table>

<table>
<tr><th>Date</th><th>Page</th><th>Item</th><th>Description</th></tr>
<tr><td>2009/
4/2</td><td>107</td><td>5.4.5</td><td>The following two columns were added to the right side of "Table 5.4-4 Status of Each Pin in the External Bus 8-Bit Data Bus Mode".
<table>
<tr><th>Pin Name</th><th>Internal ROM access immediately after reset cancellation</th><th>Internal ROM access after external ROM access</th></tr>
<tr><td>P07 to P00
(AD07 to AD00)</td><td>Output Hi-Z/Input enabled</td><td>Output Hi-Z/Input enabled</td></tr>
<tr><td>P17 to P10
(AD15 to AD08) ,
P23 to P20
(A23 to A16)</td><td>Output state</td><td>Maintains the previous address</td></tr>
<tr><td>P37(CLK)</td><td>CLK output</td><td>CLK output</td></tr>
<tr><td>P36(RDY)</td><td rowspan="4">Output Hi-Z/Input enabled</td><td rowspan="4">Output Hi-Z/Input enabled</td></tr>
<tr><td>P35($\overline{\text{HAK}}$)</td></tr>
<tr><td>P34(HRQ)</td></tr>
<tr><td>P33</td></tr>
<tr><td>P32($\overline{\text{WR}}$)</td><td rowspan="2">"H" output</td><td rowspan="2">"H" output</td></tr>
<tr><td>P31($\overline{\text{RD}}$)</td></tr>
<tr><td>P30(ALE)</td><td>"L" output</td><td>"L" output</td></tr>
<tr><td>P27 to P24,
P47 to P40,
P55 to P50,
P67 to P60,
P87 to P80,
P97 to P90,
PA4 to PA0</td><td rowspan="2">Output Hi-Z/Input enabled</td><td rowspan="2">Output Hi-Z/Input enabled</td></tr>
<tr><td>P77 to p70</td></tr>
</table>
[mcu_doc0318]</td></tr>
<tr><td>2009/
1/6</td><td>467</td><td>APPEN
DIX
B</td><td>■Table B.9-20 XCH Ri, ea Instruction (First Byte = $7E_H$) is changed.

・Error

Item "A"

Line of +A "W2+d16,A"

・Correct

Item "A0"

Line of +A "@RW2+d16"</td></tr>
</table>

FUJITSU

Corrections of Hardware Manual

MB90550

hm90550a-cm44-10103-6e-corr-x1-00

Addendum, MB90550 Hardware Manual (CM44-10103-6E)

This is the Addendum for the Hardware Manual CM44-10103-6E of the MB90550 microcontroller series. It describes all known discrepancies of the MB90550 microcontroller series Hardware Manual.

Ref. Number (Internal ref. number) (Text Link)	**Date** dd.mm.yy	**Version No.**	**Chapter/Page**	**Description/Correction**
HWM90550001	12.05.04	1.00	19	I²C Interface, Note added
HWM90550002	26.09.05	1.01		Short Name of register is ECSR

HWM90550001 TOP

CHAPTER 19 I^2C INTERFACE

Restriction of specification at sending General Call Address for MCU with I2C

When using Multi-Master mode for I2C and another Master is sending a General Code Address at same time as Fujitsu MCU, an arbitration lost* occurs after 2nd byte.
Under following conditions the restriction do not exist:
- No usage of I2C peripheral
- Usage of I2C with Single Master system
- Usage of I2C with Multi Master system, no General Call Address used
- Usage of I2C with Multi Master system, General Call Address used by Fujitsu MCU, only
- Usage of I2C with Multi Master system, General Call Address used. If the value of data, send by Fujitsu MCU, is smaller than another transfer data, the arbitration lost does not occur.

*: If the data value is smaller than another one, oneself never has "Arbitration lost" because one with large transmission data value will have "Arbitration lost".

HWM90550002 TOP

The short name of the bus control signal selection register is ECSR. The hardware manual uses sometimes EPCR instead of ECSR.