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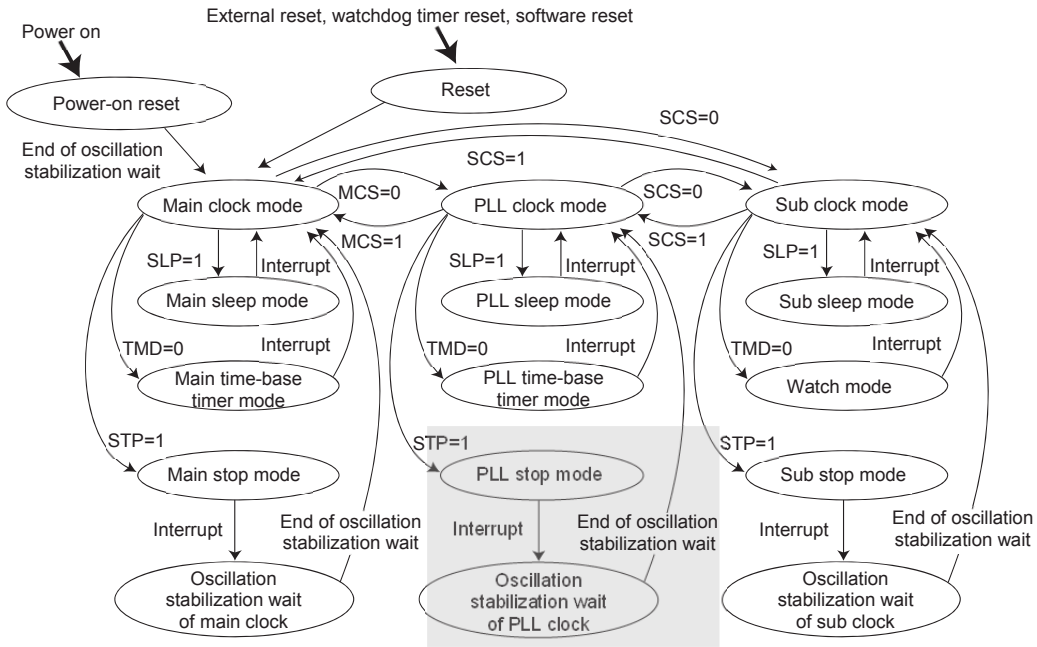
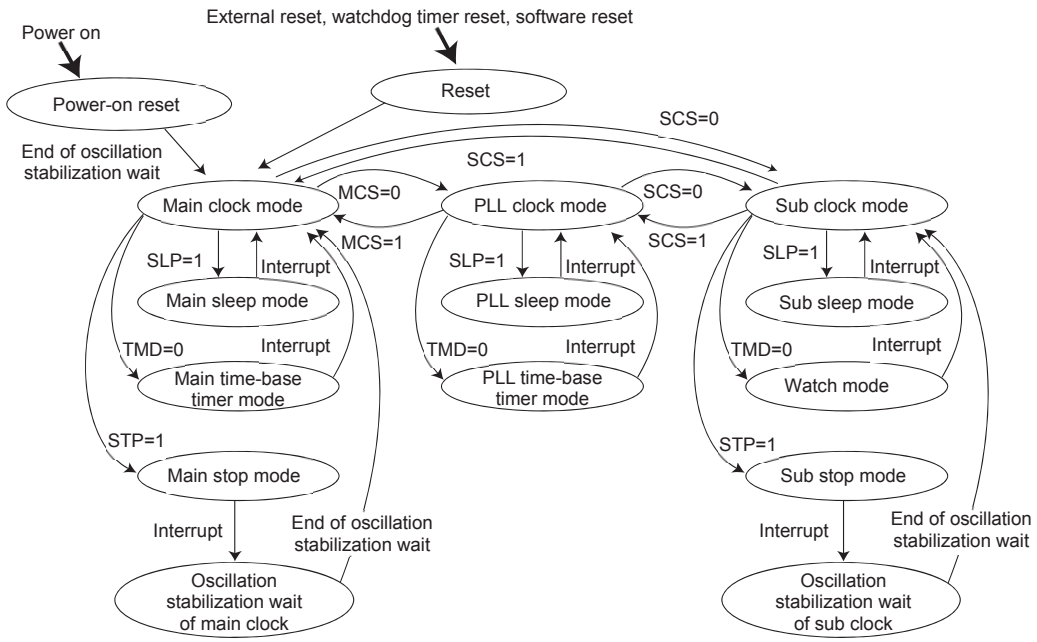
MB90880 Series

16-BIT Microcontroller
F^2MC-16LX
Hardware Manual

Errata Sheet

Page	Section	Description
Original document code: CM44-10139-6E		
Revision 1.0 February 2, 2015		
111	5.3	Table 5.3-1 Functions of Bits in Clock Selection Register (CKSCR) (1 / 2) of WS1 and WS0 bits were corrected to delete the description concerned with PLL stop mode as shown the shading below. (Error) When the main clock mode is switched to PLL clock mode, the oscillation stabilization wait time is fixed at 2^{14}/HCLK. When the mode is switched to the sub clock mode or when PLL stop mode is returned to PLL clock mode, the oscillation stabilization wait time uses the specified values in the WS1 and WS0 bits. For PLL clock oscillation stabilization wait time, at least 2^{14} /HCLK is required. Accordingly, when sub clock mode is switched to PLL clock mode, or when the transition to the PLL stop mode occurs, set WS1 and WS0 bits to "10_B" or "11_B". (Correct) When the main clock mode is switched to PLL clock mode, the oscillation stabilization wait time is fixed at 2^{14}/HCLK. When the mode is switched to the sub clock mode, the oscillation stabilization wait time uses the specified values in the WS1 and WS0 bits. For PLL clock oscillation stabilization wait time, at least 2^{14} /HCLK is required. Accordingly, when sub clock mode is switched to PLL clock mode occurs, set WS1 and WS0 bits to "10_B" or "11_B".
141	6.5.4	The Note was added for the change to the stop mode as follows. • The transition to the stop mode must be set at Main clock and Sub clock mode.
141	6.5.4	The Note was corrected to delete the description concerned with PLL stop mode as shown the shading below. • In PLL stop mode, the main clock and PLL multiplication circuit stop. During recovery from PLL stop mode, it is necessary to allot the main clock oscillation stabilization wait time and PLL clock oscillation stabilization wait time. The oscillation stabilization wait times for the main clock and PLL clock are counted simultaneously according to the value specified in the oscillation stabilization wait time selection bits in the clock selection register (CKSCR: WS1, WS0). The oscillation stabilization wait time selection bits in the clock selection register (CKSCR: WS1, WS0) must be selected accordingly to account for the longer of main clock and PLL clock oscillation stabilization wait time. The PLL clock oscillation stabilization wait time, however, requires 2^{14}/HCLK or more. Set the oscillation stabilization wait time selection bits in the clock selection register (CKSCR: WS1, WS0) to "10_B" or "11_B".

Page	Section	Description
142	6.6	Figure 6.6-1 State Transition and Transition Conditions was corrected to delete the description concerned with PLL stop mode and PLL clock oscillation stabilization wait as shown below figure. (Error)  (Correct) 

<table>
<tr><th>Page</th><th>Section</th><th>Description</th></tr>
<tr><td>143</td><td>6.6</td><td>Table 6.6-1 Operational States in Low-Power Consumption Mode was corrected the description concerned with PLL stop mode as shown the shading below table.

(Error)
<table>
<tr><th>Operation state</th><th>Main clock</th><th>Sub clock</th><th>PLL clock</th><th>CPU</th><th>Peripheral</th><th>Watch</th><th>Time-base timer</th><th>Clock source</th></tr>
<tr><td>PLL clock mode</td><td rowspan="3">Operating</td><td rowspan="3">Operating</td><td rowspan="3">Operating</td><td>Operating</td><td>Operating</td><td rowspan="3">Operating</td><td rowspan="3">Operating</td><td rowspan="4">PLL clock</td></tr>
<tr><td>PLL sleep mode</td><td rowspan="3">Not operating</td><td rowspan="3">Not operating</td></tr>
<tr><td>PLL time-base timer mode</td></tr>
<tr><td>PLL stop mode</td><td>Not operating</td><td>Not operating</td><td>Not operating</td><td>Not operating</td><td>Not operating</td><td>Not operating</td></tr>
<tr><td>Oscillation stabilization wait of PLL clock mode</td><td>Operating</td><td>Operating</td><td>Operating</td><td></td><td></td><td>Operating</td><td>Operating</td></tr>
</table>
(Correct)
<table>
<tr><th>Operation state</th><th>Main clock</th><th>Sub clock</th><th>PLL clock</th><th>CPU</th><th>Peripheral</th><th>Watch</th><th>Time-base timer</th><th>Clock source</th></tr>
<tr><td>PLL clock mode</td><td rowspan="3">Operating</td><td rowspan="3">Operating</td><td rowspan="3">Operating</td><td>Operating</td><td>Operating</td><td rowspan="3">Operating</td><td rowspan="3">Operating</td><td rowspan="4">PLL clock</td></tr>
<tr><td>PLL sleep mode</td><td rowspan="3">Not operating</td><td rowspan="3">Not operating</td></tr>
<tr><td>PLL time-base timer mode</td></tr>
<tr><td>Oscillation stabilization wait of PLL clock mode</td><td>Operating</td><td>Operating</td><td>Operating</td><td></td><td></td><td>Operating</td><td>Operating</td></tr>
</table></td></tr>
<tr><td>149</td><td>6.8</td><td>6.8 Caution on Using Low-Power Consumption Mode was corrected to add the description concerned with transiting stop mode as shown the shading below.

When operating in the low-power consumption mode, exercise reasonable care concerning the following:
• Change to the standby mode and interrupts
• Cancellation of standby mode by interrupt
• At transiting the stop mode
• Cancellation of stop mode
• Oscillation stabilization wait time
• Notes on accessing the low-power consumption mode control register (LPMCR) to enter the standby mode

■ At Transiting the Stop Mode
The transition to the stop mode must be set at Main clock and Sub clock mode.
If the mode is transited to the stop mode during PLL clock mode,set the stop mode after transiting Main clock mode once.</td></tr>
<tr><td>150</td><td>6.8</td><td>6.8 Caution on Using Low-Power Consumption Mode was corrected to delete the description concerned with PLL stop mode as shown the shading below.

■ Oscillation Stabilization Wait Time
❍ Oscillation stabilization wait time of PLL clock
In PLL stop mode, the main clock and PLL multiplication circuit stop. During recovery from PLL stop mode, it is necessary to allot the main clock oscillation stabilization wait time and PLL clock oscillation stabilization wait time. The oscillation stabilization wait times for the main clock and PLL clock are counted simultaneously according to the value specified in the oscillation stabilization wait time selection bits (CKSCR: WS1, WS0) in the clock selection register. The oscillation stabilization wait time selection bits (CKSCR: WS1, WS0) in the clock selection register must be selected accordingly to account for the longer of main clock and PLL clock oscillation stabilization wait time. The PLL clock oscillation stabilization wait time, however, requires 2^{14}/HCLK or more. Set the oscillation stabilization wait time selection bits in the clock selection register (CKSCR: WS1, WS0) to "10_B" or "11_B".</td></tr>
</table>

Page	Section	Description
190	9.2	9.2 Configuration of Time-base Timer of Block Diagram of Counter clear circuit was corrected to delete the description concerned with PLL stop mode as shown the shading below. (Error) ■ Block Diagram of Time-base Timer ❍ Counter clear circuit This circuit clears the counter at the time of writing of "0" to the time-base timer initializing bit (TBR) in the time-base timer control register (TBTC), a power-on reset, a transition to the main stop mode, a transition to the PLL stop mode, switching from the main clock mode to the PLL clock mode, switching from sub clock mode to the PLL clock mode, and switching from the sub clock mode to main clock mode. (Correct) ■ Block Diagram of Time-base Timer ❍ Counter clear circuit This circuit clears the counter at the time of writing of "0" to the time-base timer initializing bit (TBR) in the time-base timer control register (TBTC), a power-on reset, a transition to the main stop mode, switching from the main clock mode to the PLL clock mode, switching from sub clock mode to the PLL clock mode, and switching from the sub clock mode to main clock mode.
193	9.3	Table 9.3-1 Functions of Bits in Time-base Timer Control Register (TBTC) of TBOF bit was corrected to delete the description concerned with PLL stop mode as shown the shading below. (Error) • This bit is cleared to "0" by writing "0", a transition to the main stop mode, a transition to the PLL stop mode, a transition from the sub clock mode to the main clock mode, a transition from the sub clock mode to the PLL clock mode, a transition from the main clock mode to the PLL clock mode, writing "0" to the time-base timer initializing bit (TBR) or a reset. (Correct) • This bit is cleared to "0" by writing "0", a transition to the main stop mode, a transition from the sub clock mode to the main clock mode, a transition from the sub clock mode to the PLL clock mode, a transition from the main clock mode to the PLL clock mode, writing "0" to the time-base timer initializing bit (TBR) or a reset.

<table>
<tr><th>Page</th><th>Section</th><th>Description</th></tr>
<tr><td>196</td><td>9.5</td><td>
Table 9.5-1 Time-base Timer Counter Clear Operation and Oscillation Stabilization Wait Time was corrected the description concerned with PLL stop mode as shown the shading below table.

(Error)
<table>
<tr><th>Operation</th><th>Timebase timer counter</th><th>TBOF bit</th><th>Oscillation stabilization wait time</th></tr>
<tr><td>Writing "0" to time-base timer initializing bit (TBR) for timebase timer control register (TBTC)</td><td>○</td><td>○</td><td>None</td></tr>
<tr><td>Power-on reset</td><td>○</td><td>○</td><td rowspan="4">Oscillation stabilization wait time of main clock</td></tr>
<tr><td>Watchdog reset</td><td>×</td><td>○</td></tr>
<tr><td>Release of the main stop mode</td><td>○</td><td>○</td></tr>
<tr><td>Release of the PLL stop mode</td><td>○</td><td>○</td></tr>
<tr><td>Release of the sub stop mode</td><td>×</td><td>×</td><td>Oscillation stabilization wait time of sub clock</td></tr>
</table>

(Correct)
<table>
<tr><th>Operation</th><th>Timebase timer counter</th><th>TBOF bit</th><th>Oscillation stabilization wait time</th></tr>
<tr><td>Writing "0" to time-base timer initializing bit (TBR) for timebase timer control register (TBTC)</td><td>○</td><td>○</td><td>None</td></tr>
<tr><td>Power-on reset</td><td>○</td><td>○</td><td rowspan="3">Oscillation stabilization wait time of main clock</td></tr>
<tr><td>Watchdog reset</td><td>×</td><td>○</td></tr>
<tr><td>Release of the main stop mode</td><td>○</td><td>○</td></tr>
<tr><td>Release of the sub stop mode</td><td>×</td><td>×</td><td>Oscillation stabilization wait time of sub clock</td></tr>
</table>
</td></tr>
</table>