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MB90990 Series

16-BIT Microcontroller
F^2MC-16LX
Hardware Manual

Errata Sheet

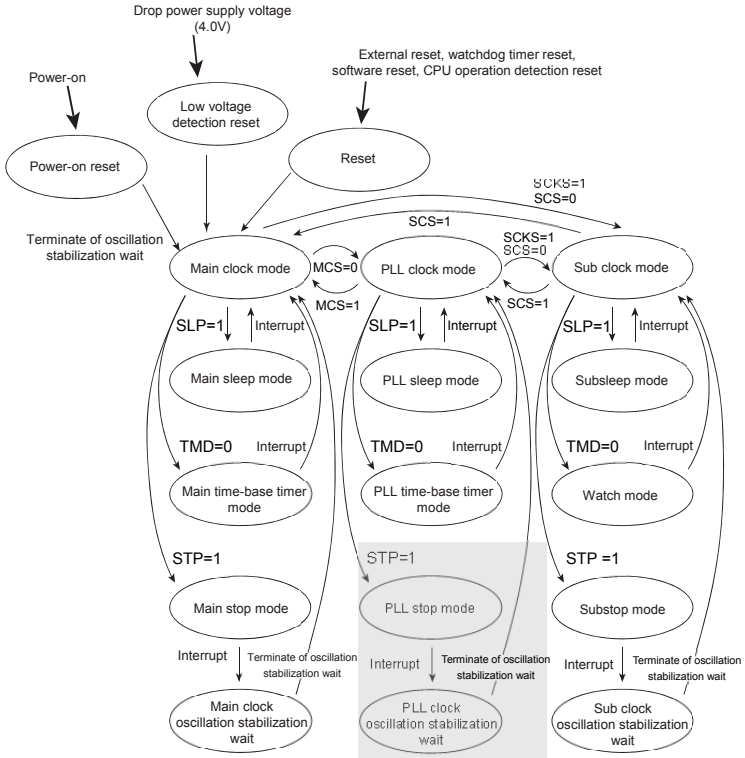
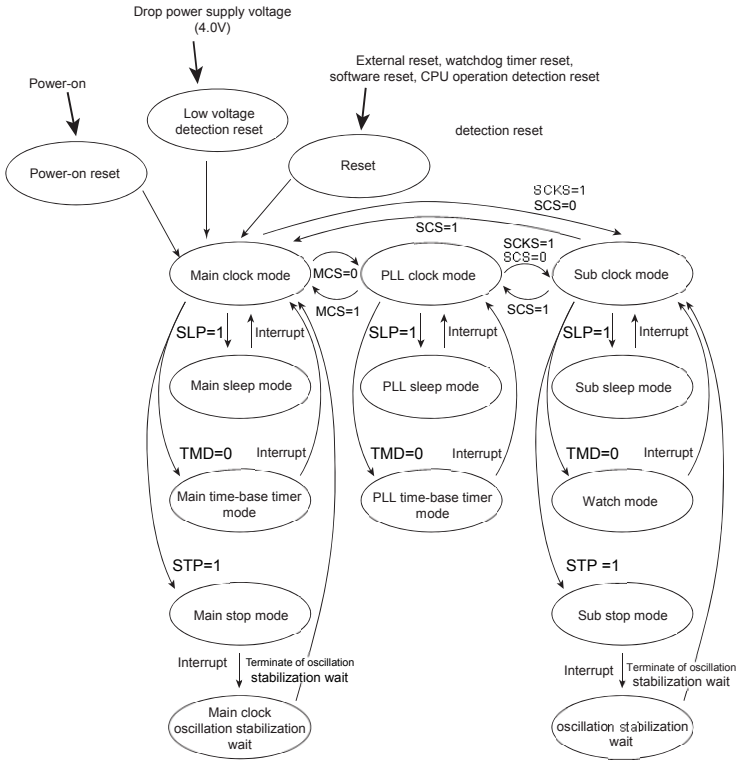
Page	Section	Description
Original document code: CM44-10149-4E		
Revision 1.0 February 2, 2015		
94	5.3	Table 5.3-1 Functions of Clock Selection Register (CKSCR) (1 / 2) of WS1 and WS0 bits were corrected to delete the description concerned with PLL stop mode as shown the shading below. (Error) The oscillation stabilization wait time taken when the clock mode is switched from main clock to PLL clock is fixed at 2^{14}/HCLK (about 4.1 ms during operation at an oscillation clock frequency of 4 MHz). When the CPU switches from sub clock mode to PLL clock mode or when it returns from PLL stop mode to PLL clock mode, the oscillation stabilization wait time follows the values specified in these bits. The PLL clock requires an oscillation stabilization wait time of at least 2^{14}/HCLK. For switching from sub clock mode to PLL clock mode and transiting to the PLL stop mode, therefore, set these bits to "10_B" or "11_B". (Correct) The oscillation stabilization wait time taken when the clock mode is switched from main clock to PLL clock is fixed at 2^{14}/HCLK (about 4.1 ms during operation at an oscillation clock frequency of 4 MHz). When the CPU switches from sub clock mode to PLL clock mode, the oscillation stabilization wait time follows the values specified in these bits. The PLL clock requires an oscillation stabilization wait time of at least 2^{14}/HCLK. For switching from sub clock mode to PLL clock mode, therefore, set these bits to "10_B" or "11_B".
150	8.5.4	8.5.4 Stop Mode was corrected to change the description concerned with PLL stop mode as shown the shading below. (Error) ■ Stop Mode When "1" is written to the STP bit of the low-power consumption mode control register (LPMCR) during operation in the PLL clock mode (CKSCR: MCS=1, SCS=0), the mode transits to the stop mode according to the settings of the MCS bit and SCS bit in the clock selection register (CKSCR). (Correct) ■ Stop Mode When "1" is written to the STP bit of the low-power consumption mode control register (LPMCR) during operation in each clock mode , the mode transits to the stop mode according to the settings of the MCS bit and SCS bit in the clock selection register (CKSCR).

<table>
<tr><th>Page</th><th>Section</th><th>Description</th></tr>
<tr><td>150</td><td>8.5.4</td><td>Table 8.5-3 Clock Selection Register (CKSCR) Settings and Stop Modes was corrected to change the description concerned with PLL stop mode as shown the shading below.

(Error)
<table>
<tr><td colspan="2">Clock selection register (CKSCR)</td><td rowspan="2">Stop Mode to be Transited</td></tr>
<tr><td>MCS</td><td>SCS</td></tr>
<tr><td>1</td><td>1</td><td>Main stop mode</td></tr>
<tr><td>0</td><td>1</td><td>PLL stop mode</td></tr>
<tr><td>1</td><td>0</td><td rowspan="2">Sub-stop mode</td></tr>
<tr><td>0</td><td>0</td></tr>
</table>
(Correct)
<table>
<tr><td colspan="2">Clock selection register (CKSCR)</td><td rowspan="2">Stop Mode to be Transited</td></tr>
<tr><td>MCS</td><td>SCS</td></tr>
<tr><td>1</td><td>1</td><td>Main stop mode</td></tr>
<tr><td>0</td><td>1</td><td>Setting disabled</td></tr>
<tr><td>1</td><td>0</td><td rowspan="2">Sub-stop mode</td></tr>
<tr><td>0</td><td>0</td></tr>
</table></td></tr>
<tr><td>150</td><td>8.5.4</td><td>The Note was added for the transition to the stop mode as follows.

・The transition to the stop mode must be set at Main clock and Sub clock mode.</td></tr>
<tr><td>152</td><td>8.5.4</td><td>The Note was corrected to delete the description concerned with PLL stop mode as shown the shading below.

When transiting to the PLL stop mode, set the oscillation stabilization wait time selection bits in the clock selection register (CKSCR: WS1, WS0) to "10_B" or "11_B".
・In PLL stop mode, the main clock and PLL multiplication circuit stop. During recovery from PLL stop mode, it is necessary to allot the main clock oscillation stabilization wait time and PLL clock oscillation stabilization wait time. The oscillation stabilization wait times for the main clock and PLL clock are counted simultaneously according to the value specified in the oscillation stabilization wait time selection bits in the clock selection register (CKSCR: WS1, WS0). The oscillation stabilization wait time selection bits in the clock selection register (CKSCR: WS1, WS0) must be selected accordingly to account for the longer of main clock and PLL clock oscillation stabilization wait time. The PLL clock oscillation stabilization wait time, however, requires 2^{14}/HCLK or more. Set the oscillation stabilization wait time selection bits in the clock selection register (CKSCR: WS1, WS0) to "10_B" or "11_B".</td></tr>
</table>

Page	Section	Description
153	8.6	Figure 8.6-1 Status Change Diagram was corrected to delete the description concerned with PLL stop mode and PLL clock oscillation stabilization wait as shown below figure. (Error)  (Correct) 

Page	Section	Description
155	8.8	8.8 Notes on Using the Low-power Consumption Mode was corrected to add the description concerned with transiting stop mode as shown the shading below. ■ At Transiting the Stop Mode The transition to the stop mode must be set at Main clock and Sub clock mode. If the mode is transited to the stop mode during PLL clock mode,set the stop mode after transiting Main clock mode once.
156	8.8	8.8 Notes on Using the Low-power Consumption Mode was corrected to delete the description concerned with PLL stop mode as shown the shading below. ■ Oscillation Stabilization Wait Time ● PLL clock oscillation stabilization wait time In PLL stop mode, the main clock and PLL multiplication circuit stop. During recovery from PLL stop mode, it is necessary to allot the main clock oscillation stabilization wait time and PLL clock oscillation stabilization wait time. The oscillation stabilization wait time for the main clock and PLL clock are counted simultaneously according to the value specified in the oscillation stabilization wait time selection bits in the clock selection register (CKSCR: WS1, WS0). The oscillation stabilization wait time selection bits in the clock selection register (CKSCR: WS1, WS0) must be selected accordingly to account for the longer of main clock and PLL clock oscillation stabilization wait time. The PLL clock oscillation stabilization wait time, however, requires 2^{14}/HCLK or more. Set the oscillation stabilization wait time selection bits in the clock selection register (CKSCR: WS1, WS0) to "10_B" or "11_B".
181	11.2	11.2 Block Diagram of the Time-base Timer was corrected to change the description concerned with PLL stop mode as shown the shading below. (Error) ■ Block Diagram of the Time-base Timer ● Counter clear circuit The counter clear circuit clears the value of the time-base timer counter by the following sources: • Time-base timer counter clear bit in the time-base timer control register (TBTC: TBR=0) • Power-on reset • Transition to main stop mode or PLL stop mode (CKSCR:SCS=1, LPMCR: STP=1) (Correct) ■ Block Diagram of the Time-base Timer ● Counter clear circuit The counter clear circuit clears the value of the time-base timer counter by the following sources: • Time-base timer counter clear bit in the time-base timer control register (TBTC: TBR=0) • Power-on reset • Transition to main stop mode (CKSCR: MCS=1,SCS=1, LPMCR: STP=1)

<table>
<tr><th>Page</th><th>Section</th><th>Description</th></tr>
<tr><td>184</td><td>11.3.1</td><td>Table 11.3-1 Functions of the Time-base Timer Control Register (TBTC) of TOBF bit was corrected to delete the description concerned with PLL stop mode as shown the shading below.

(Error)
・The TBOF bit is cleared at a write of "0", transition to main stop mode or to PLL stop mode, transition from sub clock mode to main clock mode or to PLL clock mode, transition from main clock mode to PLL clock mode, at a write of "0" to the time-base timer counter clear bit (TBR), or at reset.

(Correct)
・The TBOF bit is cleared at a write of "0", transition to main stop mode, transition from sub clock mode to main clock mode or to PLL clock mode, transition from main clock mode to PLL clock mode, at a write of "0" to the time-base timer counter clear bit (TBR), or at reset.</td></tr>
<tr><td>189</td><td>11.5</td><td>Table 11.5-1 Clearing Conditions and Oscillation Stabilization Wait Time of Time-base Timer (2/2) was corrected to delete the description concerned with PLL stop mode as shown the shading below table.

(Error)
<table>
<tr><th>Operation</th><th>Counter clear</th><th>TBOF clear</th><th>Oscillation stabilization wait time</th></tr>
<tr><td colspan="4">Cancellation of stop modes</td></tr>
<tr><td>Cancellation of main stop mode</td><td>○</td><td>○</td><td>Transition to PLL clock mode after oscillation stabilization wait time of main clock completed</td></tr>
<tr><td>Cancellation of PLL stop mode</td><td>○</td><td>○</td><td>Transition to PLL clock mode after oscillation stabilization wait time of main clock completed</td></tr>
<tr><td>Cancellation of sub-stop mode</td><td>×</td><td>×</td><td>Transition to sub clock mode after oscillation stabilization wait time of sub clock completed</td></tr>
</table>
(Correct)
<table>
<tr><th>Operation</th><th>Counter clear</th><th>TBOF clear</th><th>Oscillation stabilization wait time</th></tr>
<tr><td colspan="4">Cancellation of stop modes</td></tr>
<tr><td>Cancellation of main stop mode</td><td>○</td><td>○</td><td>Transition to PLL clock mode after oscillation stabilization wait time of main clock completed</td></tr>
<tr><td>Cancellation of sub-stop mode</td><td>×</td><td>×</td><td>Transition to sub clock mode after oscillation stabilization wait time of sub clock completed</td></tr>
</table></td></tr>
<tr><td>190</td><td>11.6</td><td>11.6 Notes on Using the Time-base Timer was corrected to delete the description concerned with PLL stop mode as shown the shading below.

(Error)
● Using time-base timer as oscillation stabilization wait time timer
After power on or in the main stop mode, PLL stop mode, and sub clock mode, the oscillation clock stops.

(Correct)
● Using time-base timer as oscillation stabilization wait time timer
After power on or in the main stop mode, and sub clock mode, the oscillation clock stops.</td></tr>
</table>

Page	Section	Description
190	11.6	11.6 Notes on Using the Time-base Timer was corrected to delete the description concerned with PLL stop mode as shown the shading below. (Error) ● Resources to which time-base timer supplies clock • At transition to operation modes (PLL stop mode, sub clock mode, and main stop mode) in which the oscillation clock stops, the time-base timer counter is cleared and the time-base timer stops. (Correct) ● Resources to which time-base timer supplies clock • At transition to operation modes (sub clock mode, and main stop mode) in which the oscillation clock stops, the time-base timer counter is cleared and the time-base timer stops.