60 W 12 V 5 V SMPS demo board with ICE5ASAG and IPA80R600P7

ER_DEMO_5ASAG_60W1

About this document

Feedback

Scope and purpose

This document is an engineering report that describes a universal-input 60 W 12 V 5 V off-line isolated Flyback converter using the latest fifth-generation Infineon fixed-frequency controller (FFC) ICE5ASAG and CoolMOS™ IPA80R600P7, which offers high-efficiency, low standby power with selectable entry and exit standby power options, wide V_{CC} operating range with fast start-up, robust line protection with input overvoltage protection (OVP) and various protection modes for a highly reliable system. This demo board is designed for users who wish to evaluate the performance of ICE5ASAG and IPA80R600P7 in terms of optimized efficiency, thermal performance and EMI.

Intended audience

This document is intended for power supply design/application engineers, students, etc. who wish to design low-cost and highly reliable systems for off-line SMPS; either auxiliary power supplies for white goods, PCs, servers and TVs, or enclosed adapters for Blu-ray players, set-top boxes, games consoles, etc.

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1 Abstract

This document is an engineering report for a 60 W 12 V 5 V demo board designed in an FF isolated Flyback converter topology using the fifth-generation FFC ICE5ASAG and a P7 series of HV CoolMOS™ IPA80R600P7. The demo board is operated in Discontinuous Conduction Mode (DCM) and is running at 100 kHz fixed switching frequency. The frequency reduction with soft gate driving and frequency jittering offers lower EMI and better efficiency between light load and 50% load. The selectable Active Burst Mode (ABM) power enables ultra-low power consumption. In addition, numerous adjustable protection functions have been implemented in ICE5ASAG to protect the system and customize the IC for the chosen application. In case of failures like line overvoltage (OV), V_{CC} OV/undervoltage (UV), open control-loop or over-load, overtemperature, V_{CC} short-to-GND and CS short-to-GND, the device enters protection mode. By means of the cycle-by-cycle Peak Current Limitation (PCL), the dimensions of the transformer and current rating of the secondary diode can both be optimized. In this way, a cost-effective solution can easily be achieved. The target applications of ICE5ASAG are either auxiliary power supplies for white goods, PCs, servers and TVs, or enclosed adapters for Blu-ray players, set-top boxes, games consoles, etc.

2 Demo board

This document contains the list of features, power supply specifications, schematics, bill of materials (BOM) and transformer construction documentation. Typical operating characteristics such as performance curve and scope waveforms are shown at the end of the report.

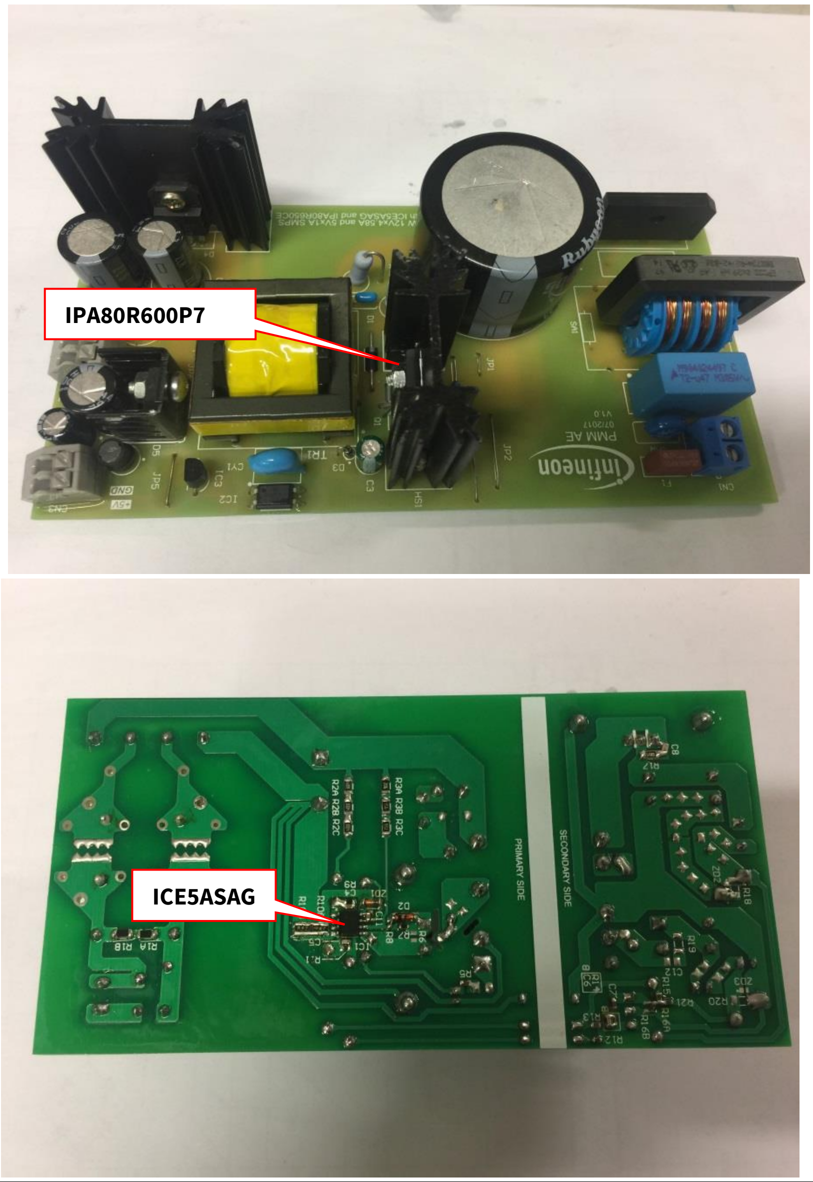


Figure 1 DEMO_5ASAG_60W1

3 Specifications of the demo board

Table 1 Specifications of DEMO_5ASAG_60W1

Input voltage and frequency	85 V AC (60 Hz) ~ 300 V AC (50 Hz)
Output voltage, current and power	(12 V × 4.58 A) + (5 V × 1 A) = 60 W
Regulation	+5 V: less than ±5% +12 V: less than ±5%
Output ripple voltage (full load, 85 V AC ~ 300 V AC)	5 $V_{ripple\_p\_p}$ < 100 mV 12 $V_{ripple\_p\_p}$ < 200 mV
Active mode four-point average efficiency (25%, 50%, 75%, 100% load)	> 83% at 115 V AC and 230 V AC
Standby power consumption	No load: P_{in} < 100 mW at 230 V AC 60 mW load: P_{in} < 170 mW at 230 V AC
Conducted emissions (EN 55022 class B)	Pass with 6 dB margin for 115 V AC and 6 dB margin for 230 V AC
ESD immunity (EN 61000-4-2)	Level 4 for contact discharge and level 3 for air discharge (±8 kV for both contact and air discharge)
Surge immunity (EN 61000-4-5)	Installation class 4 (±2 kV for line-to-line and ±4 kV for line-to-earth)
Form factor case size (L × W × H)	(144 × 73 × 43) mm

Note: *"The demo board is designed for dual-output with cross-regulated loop feedback (FB). It may not regulate properly if loading is applied only to single-output. If the user wants to evaluate for single-output (12 V only) conditions, the following changes are necessary on the board.*

1. Remove D5, L3, C13A, C13B, R21 (to disable 5 V output).
2. Change R16A to 10 kΩ and R15 to 38 kΩ (to disable 5 V FB and enable 100% weighted factor on 12 V output).

Since the board (especially the transformer) is designed for dual-output with optimized cross-regulation, single-output efficiency might not be optimized. It is only for IC functional evaluation under single-output conditions."

4 Circuit description

4.1 Line input

The AC-line input side comprises the input fuse F1 as overcurrent (OC) protection. The choke L1, X-capacitor CX1 and Y-capacitor CY1 act as EMI suppressors. Optional spark-gap devices SA1, SA2 and varistor VAR can absorb HV stress during a lightning surge test. A rectified DC voltage (120 ~ 424 V DC) is obtained through the bridge rectifier BR1 together with bulk capacitor C1.

4.2 Start-up

To achieve fast and safe start-up, ICE5ASAG is implemented with start-up resistor and V_{CC} short-to-GND protection. When V_{VCC} reaches the turn-on voltage threshold 16 V, the IC begins with a soft-start. The soft-start implemented in ICE5ASAG is a digital time-based function. The preset soft-start time is 12 ms with four steps. If not limited by other functions, the peak voltage on the CS pin will increase incrementally from 0.3 V to 0.8 V. After IC turn-on, the V_{CC} voltage is supplied by auxiliary windings of the transformer. V_{CC} short-to-GND protection is implemented during the start-up time.

4.3 PWM control with frequency reduction and switching MOSFET

The PWM pulse is generated by the fifth-generation FF current-mode controller ICE5ASAG. The new controller can be operated in either DCM or Continuous Conduction Mode (CCM) with frequency-reduction mode to achieve the overall average efficiency. This demo board is designed to operate in DCM. When the system is operating at the maximum power, the controller will switch at the FF of 100 kHz. In order to achieve a better efficiency between light-load and medium-load conditions, frequency reduction is implemented, and this reduction curve is shown in Figure 2. The V_{CS} is clamped by the current limitation threshold or by the PWM op-amp while the switching frequency is reduced. After the maximum frequency reduction, the minimum switching frequency is f_{OSC4_MIN} (43 kHz).

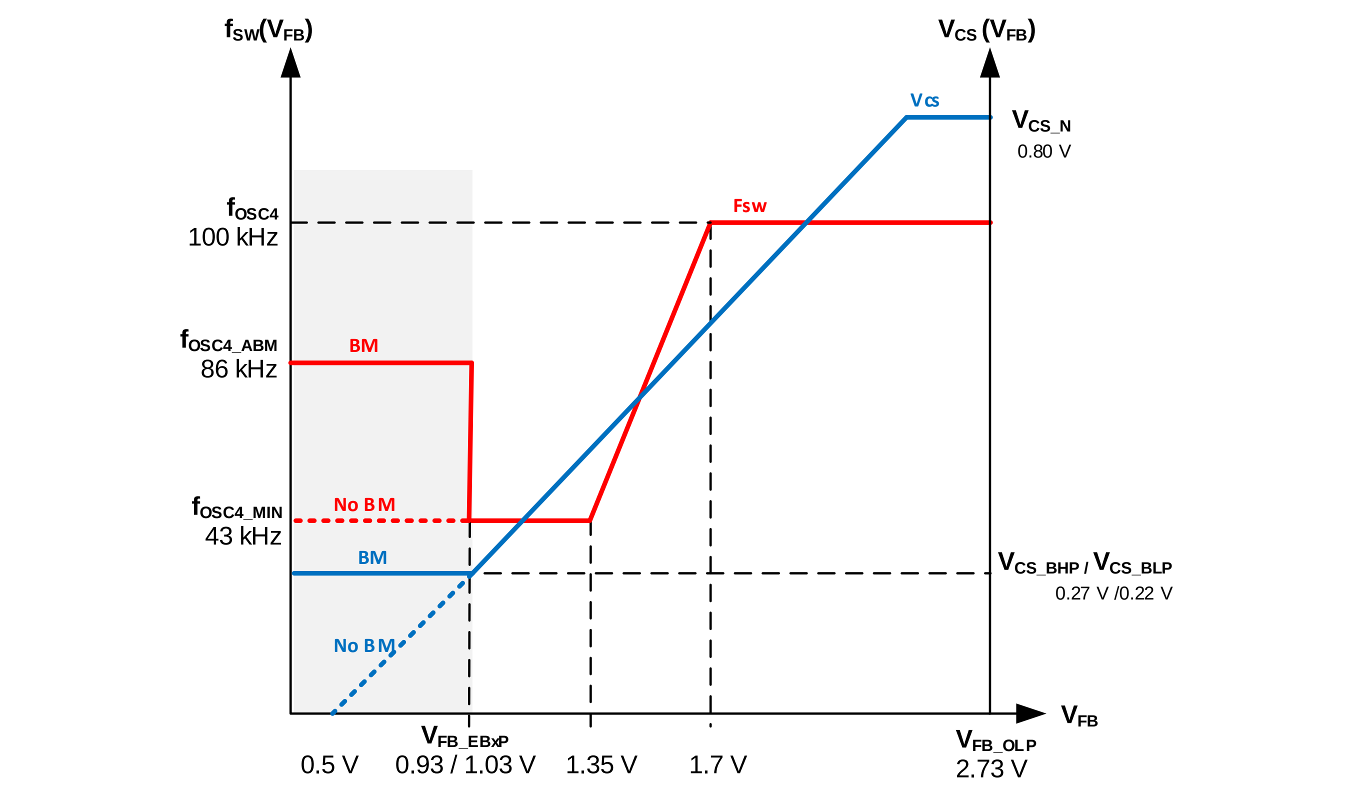


Figure 2 Frequency reduction curve

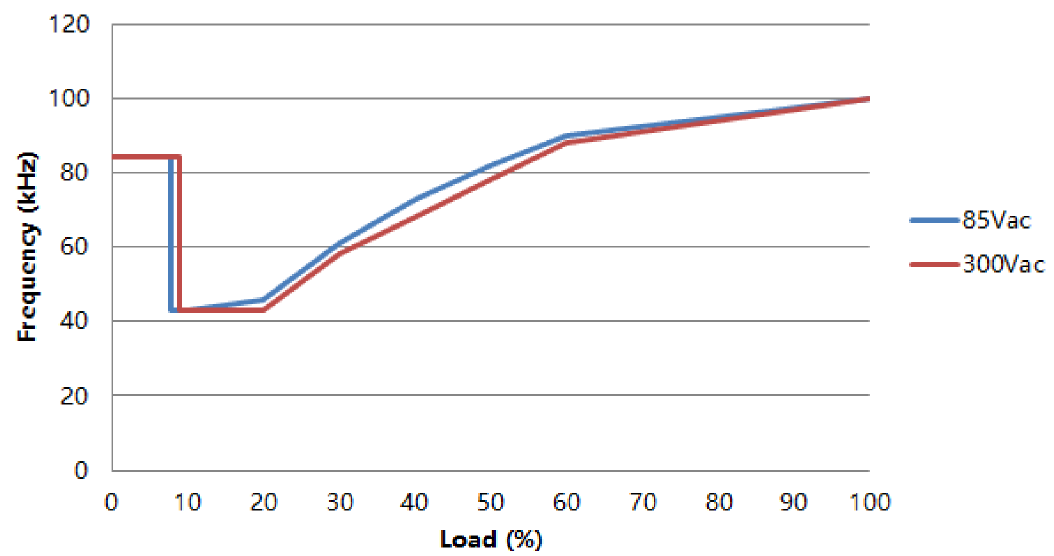


Figure 3 Frequency reduction curve of DEMO_5ASAG_60W1

The measured frequency reduction curve of DEMO_5ASAG_60W1 is shown in Figure 3.

4.4 Frequency jittering

The ICE5ASAG has a frequency jittering feature to reduce the EMI noise. The jitter frequency is internally set at 100 kHz (±4 kHz) and the jitter period is 4 ms.

4.5 RCD clamper circuit

A clamper network (R4A, R4B, C2 and D1) dissipates the energy of the leakage inductance and suppresses ringing on the SMPS transformer.

4.6 Output stage

There are two outputs on the secondary side, 12 V and 5 V. The power is coupled out via Schottky diodes D4 and D5. The capacitors C9A, C9B and C13A provide energy buffering followed by the L-C filters L2-C10 and L3-C13B to reduce the output ripple and reduce interference between SMPS switching frequency and line frequency. Storage capacitors C9A, C9B and C13A are selected to have a very small ESR to minimize the output voltage ripple.

4.7 FB loop

For FB, the output is sensed by the voltage divider of R15, R21, R16A and compared to IC3 (TL431) internal reference voltage. C6, C7 and R14 comprise the compensation network. The output voltage of IC3 (TL431) is converted to the current signal via optocoupler IC2 and two resistors R12 and R13 for regulation control.

4.8 ABM

ABM entry and exit power (three levels) can be selected in ICE5ASAG. Details are illustrated in the product datasheet. Under light-load conditions, the SMPS enters ABM. At this stage, the controller is always active but

the V_{VCC} must be kept above the switch-off threshold. During ABM, the efficiency increases significantly and at the same time it supports low ripple on V_{out} and fast response on load-jump.

In order to enter ABM operation, two conditions must apply:

1. The FB voltage must be lower than the threshold of V_{FB_EBXP}.
2. There must be a certain blanking time (t_{FB_BEB} = 36 ms).

Once both of these conditions are fulfilled, the ABM flip-flop is set and the controller enters ABM operation. This dual-condition determination for entering ABM operation prevents mis-triggering of ABM, so that the controller enters ABM operation only when the output power is really low during the preset blanking time.

During ABM, the maximum Current Sense (CS) voltage is reduced from V_{CS_N} to V_{CS_BXP} to reduce the conduction loss and the audible noise. In ABM, the FB voltage is changing like a sawtooth between $V_{FB\_Bon\_ISO}$ and $V_{FB\_Boff\_ISO}$.

The FB voltage immediately increases if there is a high load-jump. This is observed by one comparator. As the current limit is 27/33% during ABM a certain load is needed so that FB voltage can exceed V_{FB_LB} (2.73 V). After leaving ABM, maximum current can then be provided to stabilize V_{out}.

5 Protection features

Protection is one of the major factors in determining whether the system is safe and robust. Therefore, sufficient protection is necessary. ICE5ASAG provides comprehensive protections to ensure the system is operating safely. These include line OV, V_{CC} OV and UV, over-load, overtemperature (controller junction), CS short-to-GND and V_{CC} short-to-GND. When those faults are found, the system will enter protection mode until the fault is removed, when the system will resume normal operation. A list of protection functions and failure conditions are shown in the table below.

Table 2 Protection functions of ICE5ASAG

Protection function	Failure condition	Protection mode
Line OV	V_{VIN} > 2.85 V	Non-switch auto restart
V_{CC} OV	V_{VCC} > 25.5 V	Odd-skip auto restart
V_{CC} UV	V_{VCC} < 10 V	Auto restart
Over-load	V_{FB} > 2.73 V and lasts for 54 ms	Odd-skip auto restart
Overtemperature (junction temperature of controller chip only)	T_J > 140°C	Non-switch auto restart
CS short-to-GND	V_{CS} < 0.1 V, lasts for 0.4 µs and three consecutive pulses	Odd-skip auto restart
V_{CC} short-to-GND (V_{VCC} = 0 V, $R_{Start\text{-}up}$ = 50 MΩ and V_{DRAIN} = 90 V)	V_{VCC} < 1.2 V, $I_{VCC\_Charge1}$ ≈ -0.27 mA	Cannot start up

6 Circuit diagram

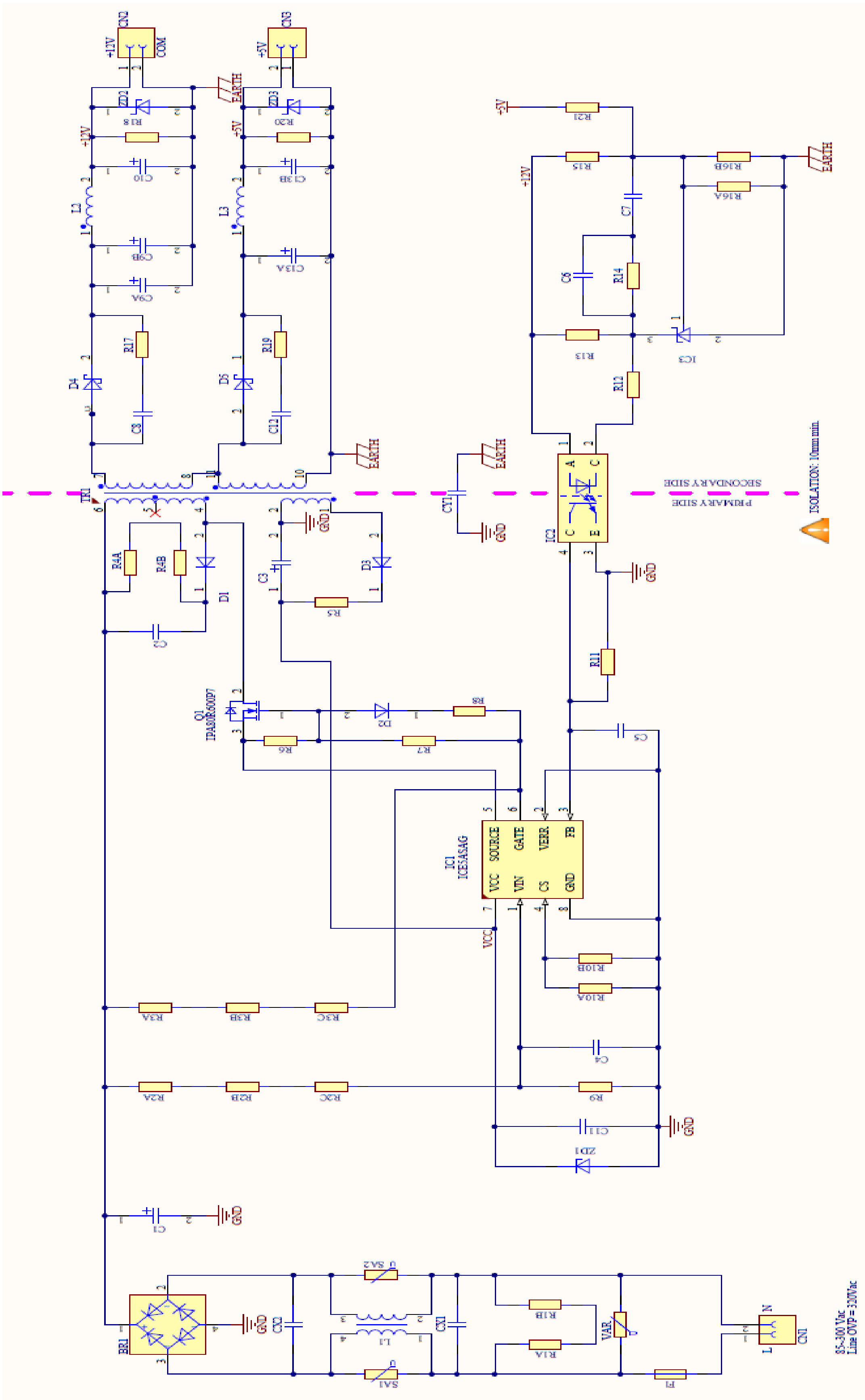


Figure 4 Schematic of DEMO_5ASAG_60W1

7 PCB layout

7.1 Top side

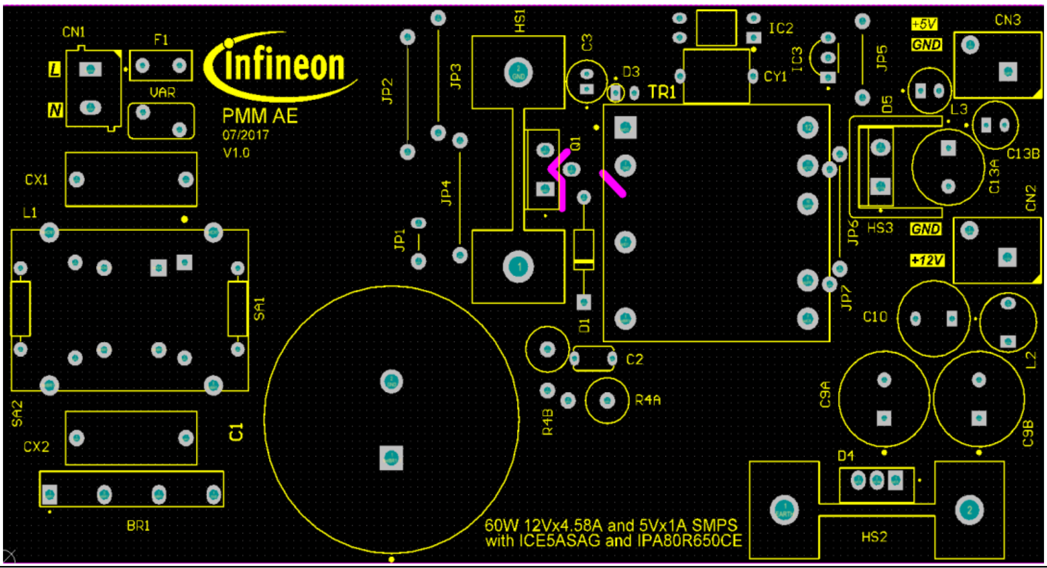


Figure 5 Top side component legend

7.2 Bottom side

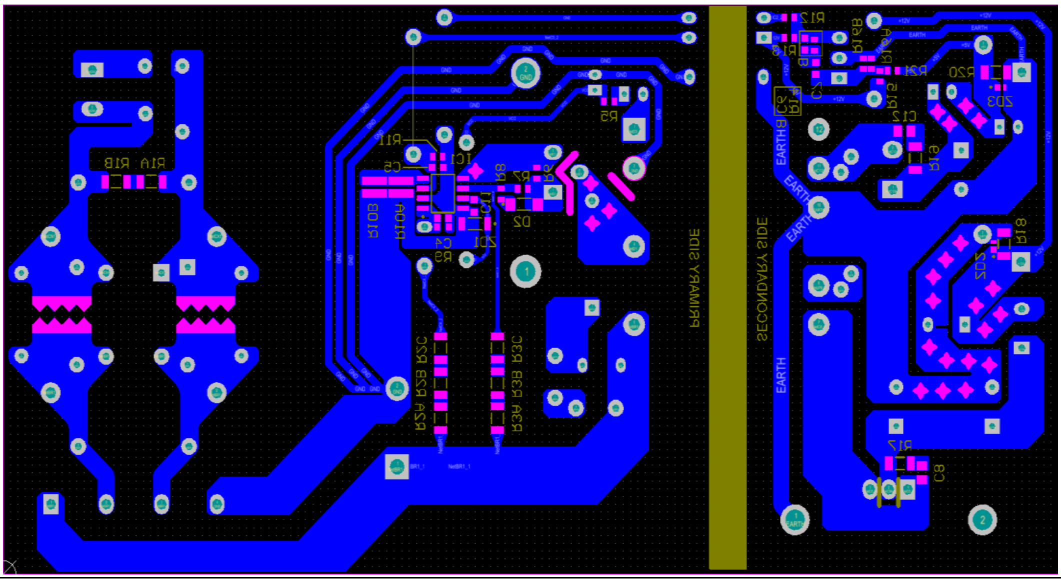


Figure 6 Bottom side copper and component legend

8 Bill of materials

Table 3 BOM

No.	Designator	Description	Part number	Manufacturer	Quantity
1	BR1	600 V/4 A	D4SB60L	Shindengen	1
2	CX1	0.47 µF, X-cap	B32922C3474	EPCOS/TDK	1
3	CY1	2.2 nF/500 V	DE1E3RA222MA4BQ	Murata	1
4	C1	180 uF/500 V	500VXG180MEFCSN35X30	Rubycon	1
5	C2	1 nF/1000 V	RDE7U3A102J2M1H03A	Murata	1
6	C3	22 uF/50 V	50PX22MEFC5X11	Rubycon	1
7	C11	100 nF/50 V	GRM188R71H104KA93D	Murata	1
8	C8	1 nF/100 V (0805)	GRM2162C2A102JA01#	Murata	1
9	C9A, C9B	1500 uF/16 V	16ZLH1500MEFC10X20	Rubycon	2
10	C10	100 uF/16 V	16ZLH100MEFC5X11	Rubycon	1
11	C7	220 nF/50 V (0603)	GRM188R71H224KAC4D	Murata	1
12	C4, C5, C6	1 nF/50 V (0603)	GRM1885C1H102GA01D	Murata	3
13	C13A	1500 uF/10 V	10ZLH1500MEFC10X16	Rubycon	1
14	C13B	330 uF/10 V	10ZLH330MEFC6.3X11	Rubycon	1
15	D1	800 V/1A	UF4006-E3/54	VISHAY	1
16	D2	0.2 A/100 V (SOD-80)	FDLL4148	Fairchild	1
17	D3	0.2 A/200 V (DO-35)	1N485B	Fairchild	1
18	D4	30 A/200 V	VF30200C		1
19	D5	10 A/45 V	VFT1045BP-M2/4W		1
20	F1	3.15 A/300 V	36913150000	Littlefuse	1
21	IC1	ICE5ASAG (DSO-8)	ICE5ASAG	Infineoon	1
22	Q1	800 V, 0.6 Ω, TO-220	IPA80R600P7	Infineoon	1
23	IC2	Optocoupler	SFH617A-3		1
24	IC3	Shunt regulator	TL431BVLPG		1
25	JP1–JP3, JP5–JP7	Jumper			6
26	JP4	Resistor, 27 Ω			1
27	L1	39 mH/1.4 A	B82734R2142B030	Epcos	1
28	L2	2.2 uH,6 A	744772022	Wurth Electronics	1
29	L3	4.7 uH,4.2 A	7447462047	Wurth Electronics	1
30	R4A, R4B	15 kR/2 W/350 V	ERG-2SJ153		2
31	R5, R7	15 R (0603)			2
32	R8	0 Ω (0603)			1
33	R10A, R10B	0.47 R/0.33 W	ERJB2BFR47V		2
34	R3A, R3B, R3C	15 MΩ/0.25 W/5%/1206	RC1206JR-0715ML	Yageo	3
35	R2A, R2B, R2C	3 M Ω/0.25 W/5%/1206	RESISTOR		3
36	R9	58.3 k (0603)	RT0603DRE0758K3L		1
37	R12	820 R (0603)			1
38	R13	1.2 k (0603)			1
39	R14	4.3 k (0603)			1
40	R15	16 k (0603)			1
41	R21	6.2 k/(0603)			1
42	R16A	2.49 k (0603)			1

43	R17	51 R (1206)			1
44	R1A, R1B	1 M/200 V (1206)			2
45	TR1	ER28/14, 170 uH	750343710 (Rev 00)	Wurth Electronics	1
46	ZD1	22 V/500 mW (1206)	BZS55B22 RXG	Taiwan Semiconductor	1
47	VAR	Metal Oxide Varistor (MOV), 32 J	B72207S2321K101	Epcos	1
48	CN1	Connector_ Con (L N)	691102710002	Wurth Electronics	1
49	CN2, CN33	Connector_Con (+12 V com), con(+5 V com)	691 412 120 002B	Wurth Electronics	2
50	HS3	Heatsink	577202B00000G	AAVID	1
51	HS1, HS2	Heatsink	513002B02500G	AAVID	2

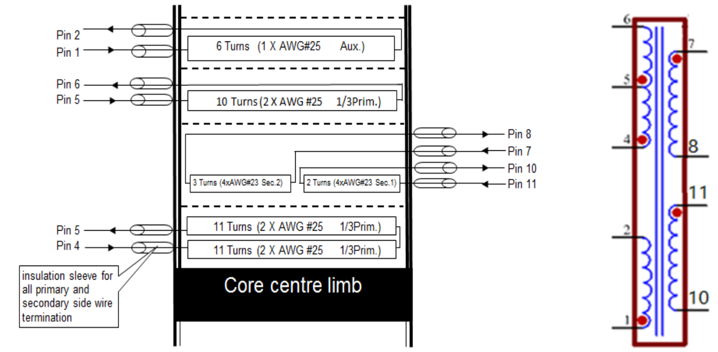
9 Transformer construction

Core and materials: ER28/14, TP4A (TDG)

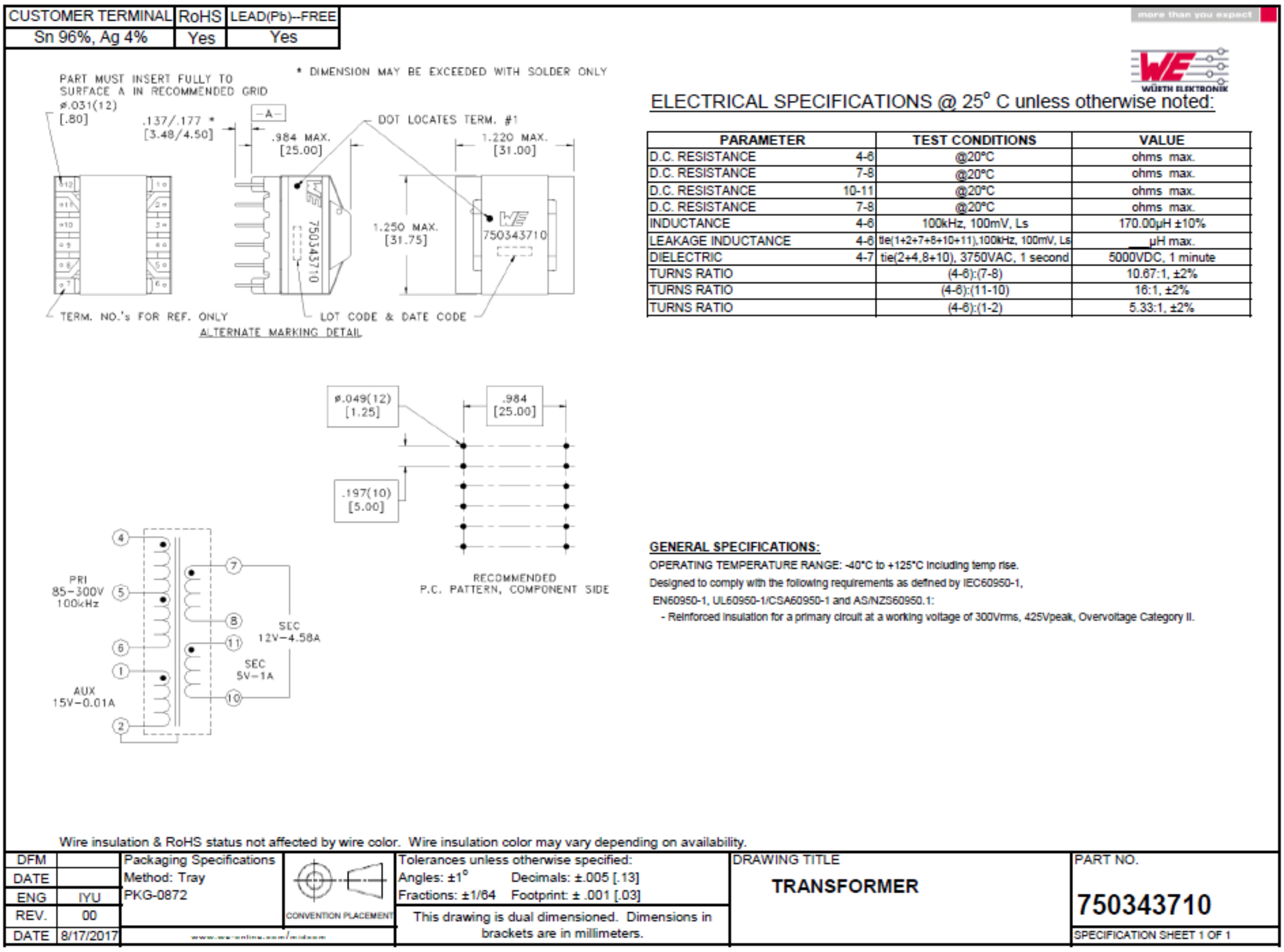
Bobbin: 070-4869 (9-pin EXT, THT, horizontal version)

Primary inductance: Lp = 170 µH (±10%), measured between pin 4 and pin 6

Manufacturer and part number: Wurth Electronics Midcom (750343710 Rev 00)



Start	Stop	No. of turns	Wire size	Layer
4	-	11	2XAWG# 25	1/3 Primary
-	5	11	2XAWG# 25	1/3 Primary
11	10	2	4XAWG#23	SEC - 5V
7	8	3	4XAWG#23	SEC - 12V (part)
5	6	10	2XAWG#25	1/3 Primary
1	2	6	1XAWG#30	Auxiliary



CUSTOMER TERMINAL	RoHS	LEAD(Pb)--FREE
Sn 96%, Ag 4%	Yes	Yes

ELECTRICAL SPECIFICATIONS @ 25° C unless otherwise noted:

PARAMETER		TEST CONDITIONS	VALUE
D.C. RESISTANCE	4-6	@20°C	ohms max.
D.C. RESISTANCE	7-8	@20°C	ohms max.
D.C. RESISTANCE	10-11	@20°C	ohms max.
D.C. RESISTANCE	7-8	@20°C	ohms max.
INDUCTANCE	4-6	100kHz, 100mV, Ls	170.00µH ±10%
LEAKAGE INDUCTANCE	4-6	tie(1+2+7+8+10+11),100kHz, 100mV, Ls	__µH max.
DIELECTRIC	4-7	tie(2+4,8+10), 3750VAC, 1 second	5000VDC, 1 minute
TURNS RATIO		(4-6):(7-8)	10.67:1, ±2%
TURNS RATIO		(4-6):(11-10)	16:1, ±2%
TURNS RATIO		(4-6):(1-2)	5.33:1, ±2%

GENERAL SPECIFICATIONS:
OPERATING TEMPERATURE RANGE: -40°C to +125°C including temp rise.
Designed to comply with the following requirements as defined by IEC60950-1, EN60950-1, UL60950-1/CSA60950-1 and AS/NZS60950.1:
- Reinforced insulation for a primary circuit at a working voltage of 300Vrms, 425Vpeak, Overvoltage Category II.

Wire insulation & RoHS status not affected by wire color. Wire insulation color may vary depending on availability.

DFM		Packaging Specifications		Tolerances unless otherwise specified:	DRAWING TITLE	PART NO.
DATE		Method: Tray		Angles: ±1° Decimals: ±.005 [.13]	TRANSFORMER	750343710
ENG	IYU	PKG-0872		Fractions: ±1/64 Footprint: ± .001 [.03]		
REV.	00		CONVENTION PLACEMENT	This drawing is dual dimensioned. Dimensions in brackets are in millimeters.		SPECIFICATION SHEET 1 OF 1
DATE	8/17/2017					

Figure 7 Transformer structure

10 Test results

10.1 Efficiency, regulation and output ripple

Table 4 Efficiency, regulation and output ripple

Input (V AC/Hz)	P_{in} (W)	12 V (V)	I_{out_12V} (mA)	5 V (V)	I_{out_5V} (mA)	12 V_{RPP} (mV)	5 V_{RPP} (mV)	P_{out} (W)	Efficiency (η) (%)	Average η (%)	OLP pin (W)	OLP I_{out12V} (fixed 5 V at 1 A) (A)
85 V AC/ 60 Hz	0.049	12.46	0	4.82	0	66	27				116	7.18
	0.120	12.38	5	4.85	0	80	20	0.06				
	18.61	12.43	1145	4.83	250	66	30	15.44	82.97	81.35		
	37.64	12.43	2290	4.83	500	76	33	30.88	82.04			
	57.17	12.43	3435	4.82	750	80	37	46.31	81.01			
	77.80	12.43	4580	4.82	1000	93	43	61.75	79.37			
115 V AC/ 60 Hz	0.054	12.46	0	4.83	0	70	28				115	7.5
	0.125	12.38	5	4.86	0	80	22	0.06				
	18.19	12.44	1145	4.83	250	66	30	15.45	84.94	83.25		
	37.00	12.43	2290	4.82	500	73	35	30.87	83.45			
	56.00	12.43	3435	4.82	750	80	37	46.31	82.70			
	75.37	12.43	4580	4.82	1000	86	40	61.75	81.93			
230 V AC/ 50 Hz	0.088	12.45	0	4.83	0	73	30				120	7.9
	0.159	12.38	5	4.86	0	83	22	0.06				
	18.48	12.44	1145	4.83	250	70	28	15.45	83.61	83.85		
	36.78	12.43	2290	4.83	500	76	33	30.88	83.96			
	55.20	12.43	3435	4.83	750	83	37	46.32	83.91			
	73.58	12.43	4580	4.82	1000	90	40	61.75	83.92			
265 V AC/ 50 Hz	0.103	12.45	0	4.83	0	73	30				122	8.08
	0.176	12.38	5	4.86	0	83	23	0.06				
	18.57	12.44	1145	4.83	250	70	28	15.45	83.21	83.72		
	36.88	12.44	2290	4.83	500	76	33	30.90	83.79			
	55.26	12.44	3435	4.84	750	83	37	46.36	83.90			
	73.53	12.43	4580	4.82	1000	86	38	61.75	83.98			
300 V AC/ 50 Hz	0.124	12.43	0	4.83	0	76	30				125	8.18
	0.196	12.34	5	4.87	0	86	25	0.06				
	18.66	12.43	1145	4.83	250	73	28	15.44	82.74	83.47		
	36.97	12.44	2290	4.82	500	76	32	30.90	83.57			
	55.32	12.43	3435	4.82	750	83	35	46.31	83.72			
	73.64	12.43	4580	4.82	1000	93	40	61.75	83.85			

60 mW load condition: 12 V @ 5 mA and 5 V @ 0 mA

Maximum load condition: 5 V @ 1000 mA and 12 V @ 4580 mA

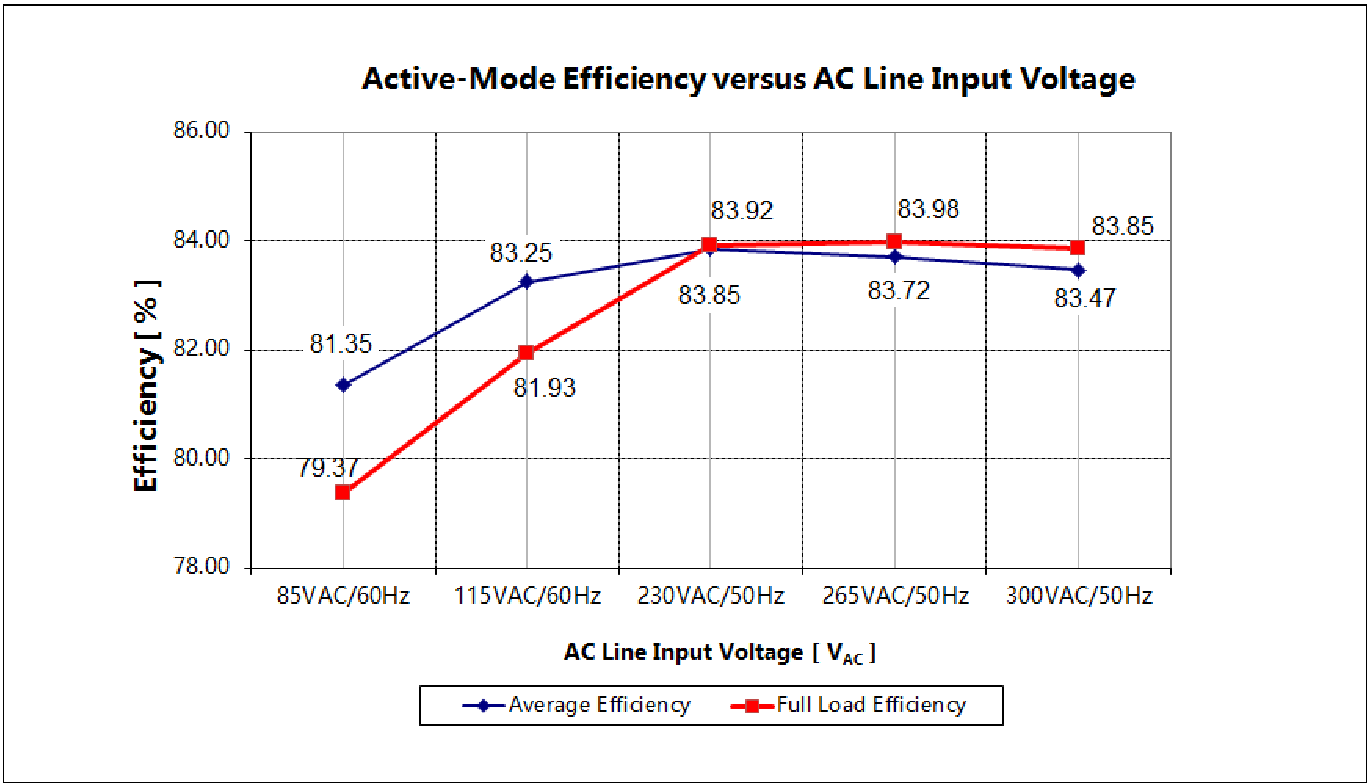


Figure 8 Efficiency vs AC-line input voltage

10.2 Standby power

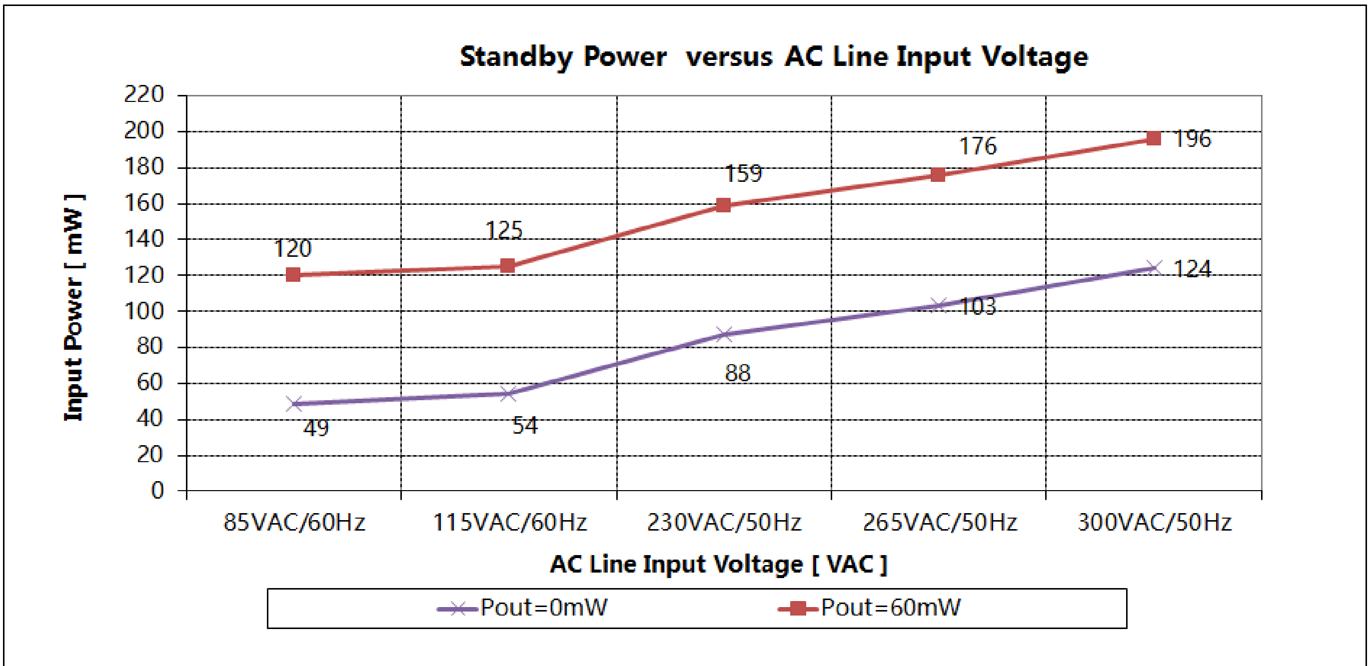


Figure 9 Standby power at no load and 60 mW load vs AC-line input voltage (measured by Yokogawa WT210 power meter – integration mode)

10.3 Line regulation

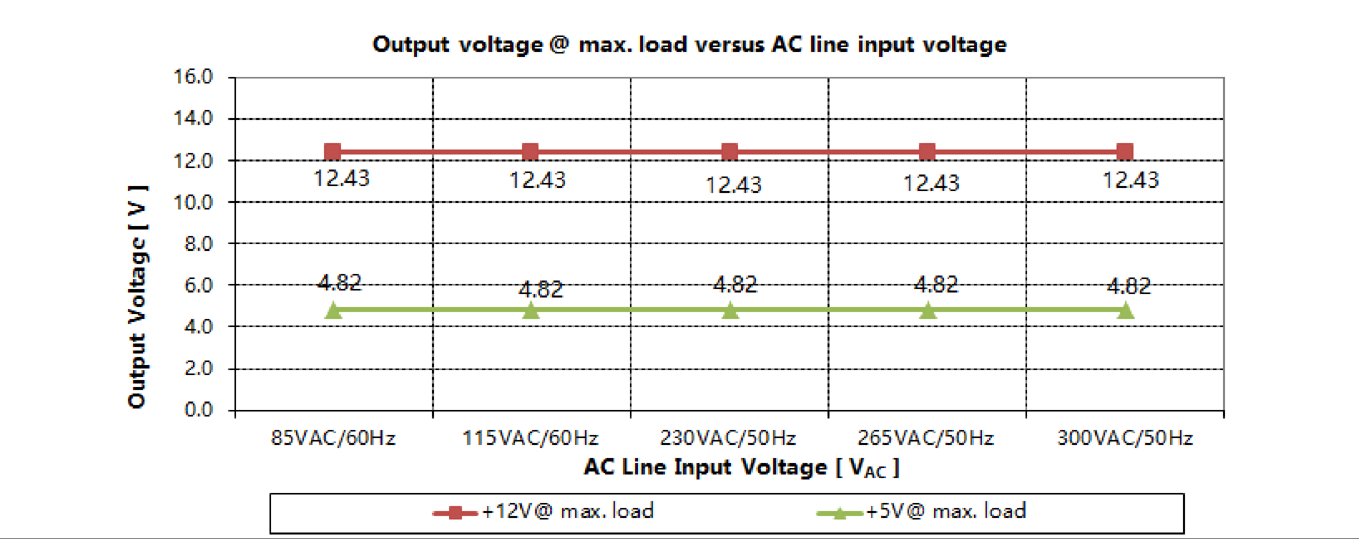


Figure 10 Line regulation V_{Out} at full load vs AC-line input voltage

10.4 Load regulation

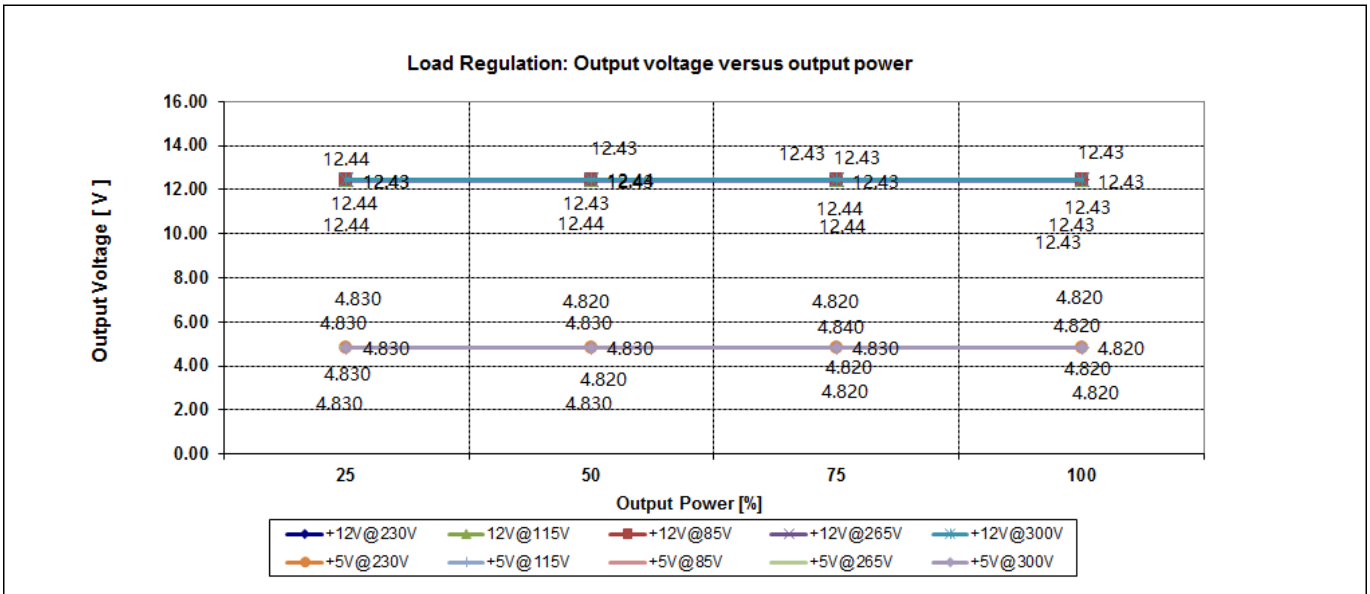


Figure 11 Load regulation V_{Out} vs output power

10.5 Maximum input power

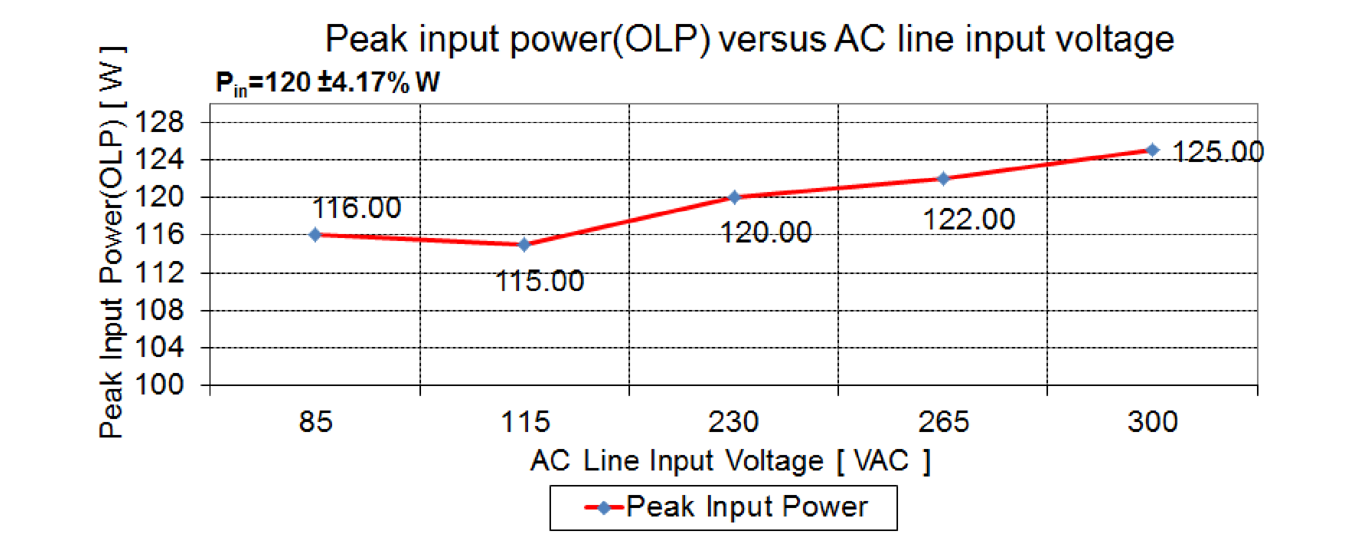


Figure 12 Maximum input power (before over-load protection) vs AC-line input voltage

10.6 ESD immunity (EN 61000-4-2)

Pass EN 61000-4-2 level 4 for contact discharge and level 3 for air discharge (±8 kV for both contact and air discharge).

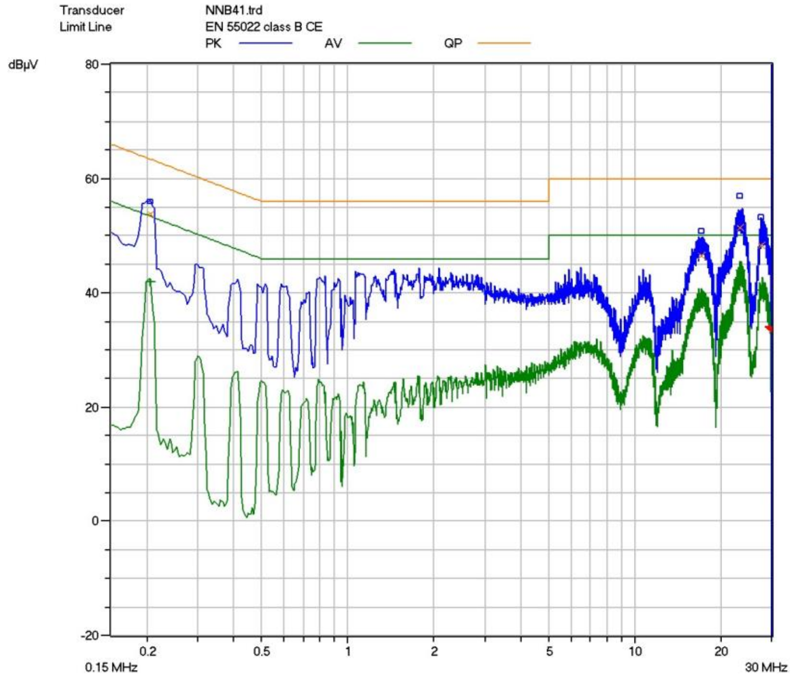
10.7 Surge immunity (EN 61000-4-5)

Pass EN 61000-4-5 installation class 4 (±2 kV for line-to-line and ±4 kV for line-to-earth).

10.8 Conducted emissions (EN 55022 class B)

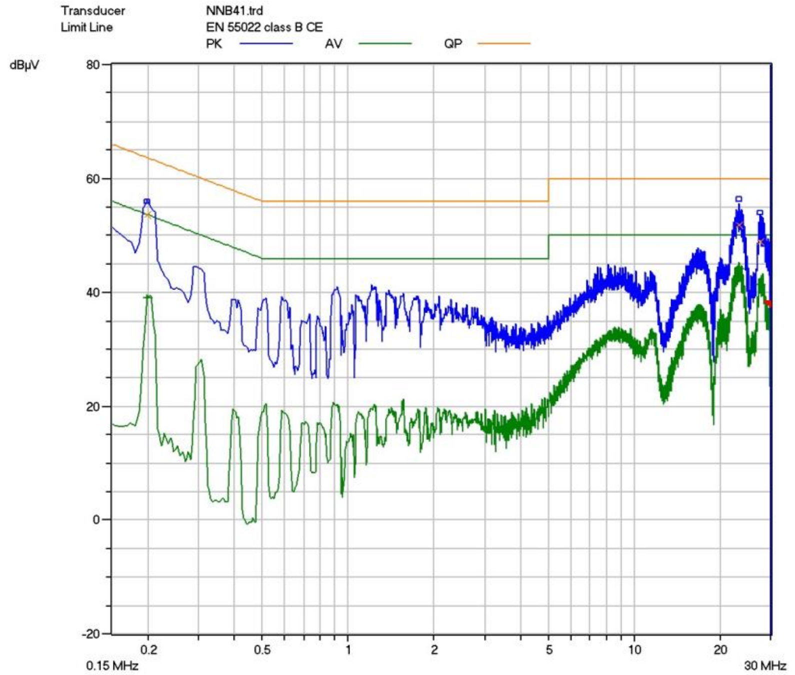
The conducted EMI was measured by Schaffner (SMR4503) and followed the test standard of EN 55022 (CISPR 22) class B. The demo board was set up at full load (60 W) with input voltage of 115 V AC and 230 V AC.

Pass conducted emissions EN 55022 (CISPR 22) class B with 6 dB margin at low-line (115 V AC) and with 6 dB margin for high-line (230 V AC).



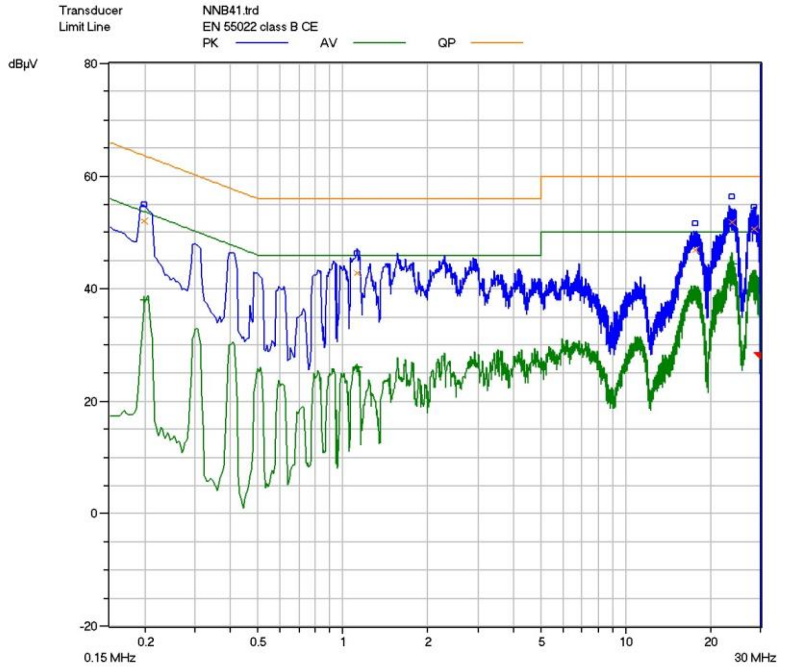
Frequency		Level Pk		Level AV		Level QP	Limit AV	Limit QP	Margin
0.2040	L	56.0	L	42.0	L	53.9	53.4	63.4	
17.1600	L	50.9	L	39.0	L	46.4	50.0	60.0	
23.2160	L	56.9	L	44.0	L	51.4	50.0	60.0	-6dB
27.6880	L	53.2	L	40.5	L	48.4	50.0	60.0	

Figure 13 Conducted emissions (line) at 115 V AC and maximum load



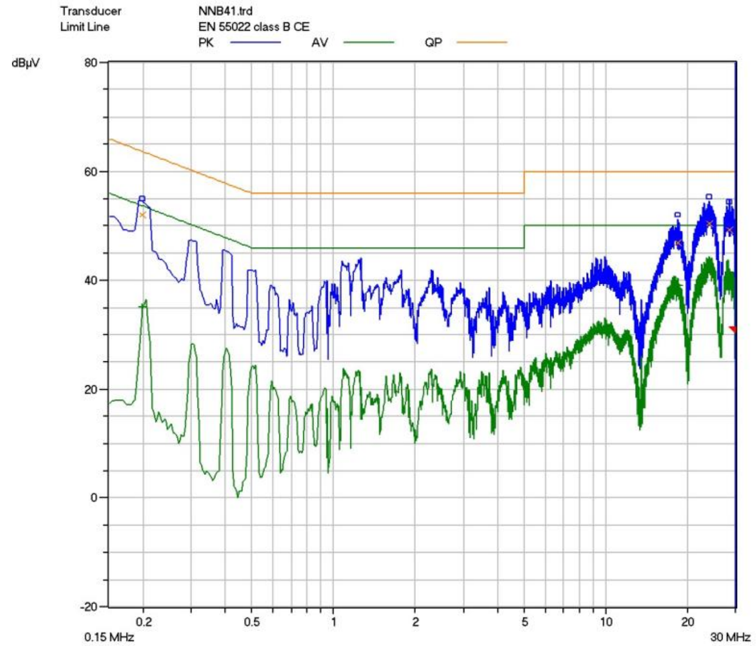
Frequency		Level Pk		Level AV		Level QP	Limit AV	Limit QP	Margin
0.1980	L	56.0	L	39.0	L	53.6	53.7	63.7	
23.3040	L	56.4	L	44.0	L	51.8	50.0	60.0	-6.0dB
27.5600	L	53.9	L	41.5	L	48.9	50.0	60.0	

Figure 14 Conducted emissions (neutral) at 115 V AC and maximum load



Frequency		Level Pk		Level AV		Level QP	Limit AV	Limit QP	Margin
0.1980	L	55.0	L	38.1	L	52.0	53.7	63.7	
1.1220	L	46.3	L	26.0	L	42.9	46.0	56.0	
17.5840	L	51.6	L	39.6	L	47.0	50.0	60.0	
23.6160	L	56.3	L	44.0	L	51.9	50.0	60.0	-6dB
28.4080	L	54.7	L	41.9	L	50.6	50.0	60.0	

Figure 15 Conducted emissions (line) at 230 V AC and maximum load



Frequency		Level Pk		Level AV		Level QP	Limit AV	Limit QP	Margin
0.1980	N	54.9	N	35.1	N	52.0	53.7	63.7	
18.3280	N	52.0	N	39.1	N	46.9	50.0	60.0	
24.0320	N	55.3	N	42.6	N	50.4	50.0	60.0	-7.4dB
28.3040	N	54.3	N	40.4	N	49.2	50.0	60.0	

Figure 16 Conducted emissions (neutral) at 230 V AC and maximum load

10.9 Thermal measurements

The thermal testing of the open-frame demo board was done using an infrared thermography camera (FLIR-T62101) at an ambient temperature of 25°C. The measurements were taken after one hour running at full load.

Table 5 Hottest temperature of demo board

No.	Major component	85 V AC (°C)	300 V AC (°C)
1	IC1 (ICE5ASAG)	81.9	55.4
2	Q1 (IPA80R600P7)	43.2	38.4
3	TR1 (transformer)	72.5	71.9
4	D4 (12 V diode)	84.8	80.0

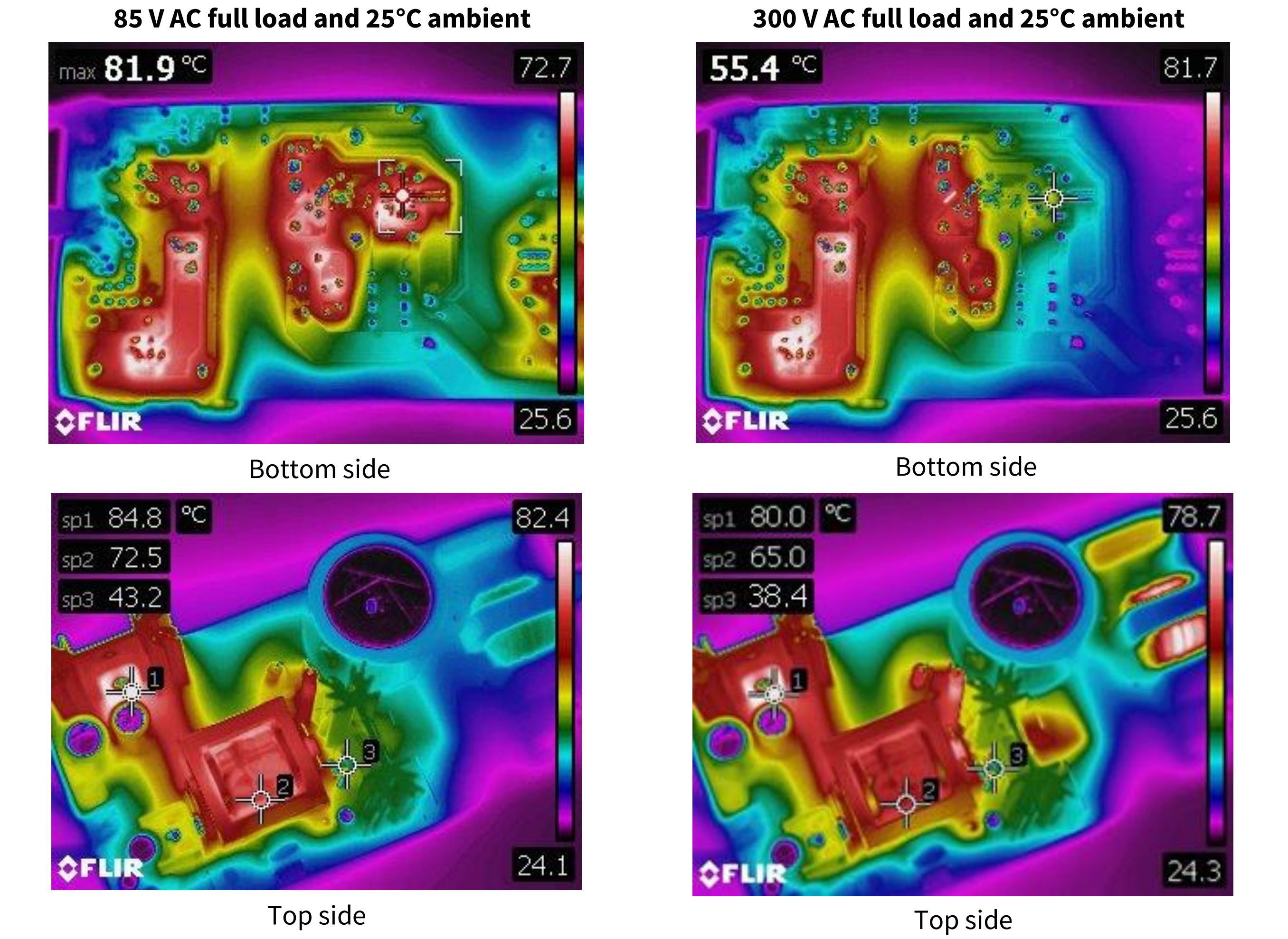


Figure 17 Infrared thermal image of DEMO_5ASAG_60W1

11 Waveforms and scope plots

All waveforms and scope plots were recorded with a Teledyne LeCroy 606Zi oscilloscope.

11.1 Start-up at low/high AC-line input voltage with maximum load

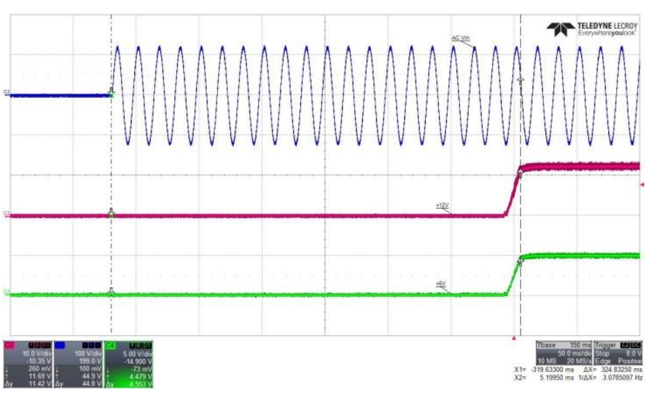
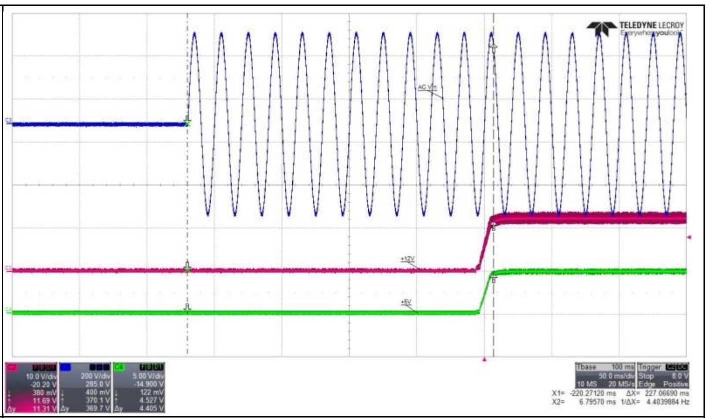
	
C2 (purple) : 12 V output voltage (V_{Out12}) C3 (blue) : AC-line voltage (V AC) C4 (green) : 5 V output voltage (V_{Out5})	C2 (purple) : 12 V output voltage (V_{Out12}) C3 (blue) : AC-line voltage (V AC) C4 (green) : 5 V output voltage (V_{Out5})
Start-up time at 85 V AC and maximum load ≈ 324 ms	Start-up time at 300 V AC and maximum load ≈ 227 ms

Figure 18 Start-up

11.2 Soft-start

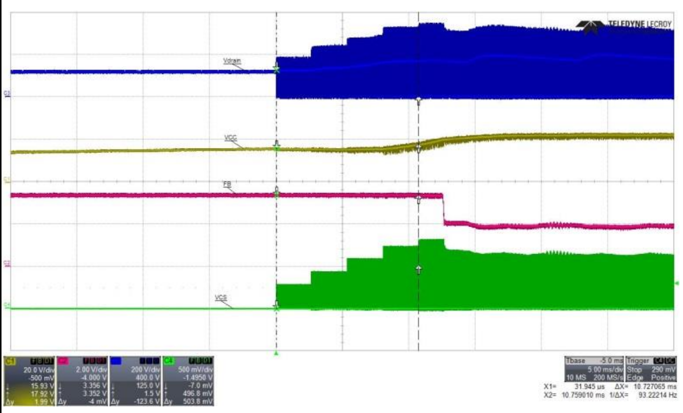
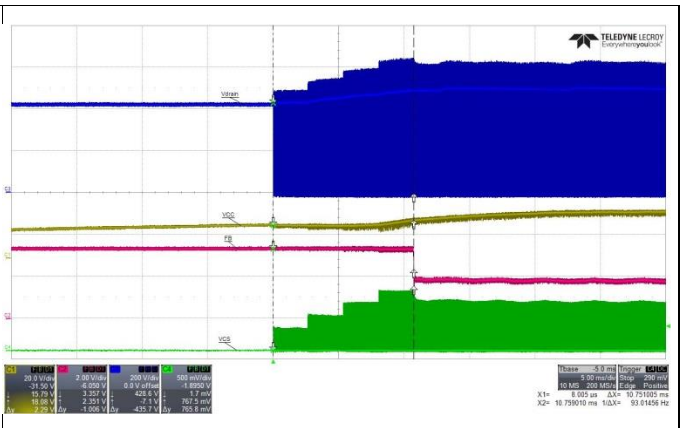
	
C1 (yellow) : Supply voltage (V_{VCC}) C2 (purple) : FB voltage (V_{FB}) C3 (blue) : Drain voltage (V_D) C4 (green) : CS voltage (V_{CS})	C1 (yellow) : Supply voltage (V_{VCC}) C2 (purple) : FB voltage (V_{FB}) C3 (blue) : Drain voltage (V_D) C4 (green) : CS voltage (V_{CS})
Soft-start time at 85 V AC and maximum load ≈ 10.1 ms	Soft-start time at 300 V AC and maximum load ≈ 10 ms

Figure 19 Soft-start

11.3 Drain and CS voltage at maximum load

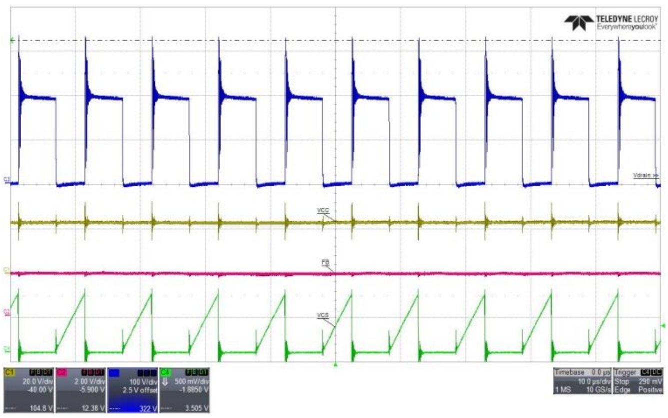
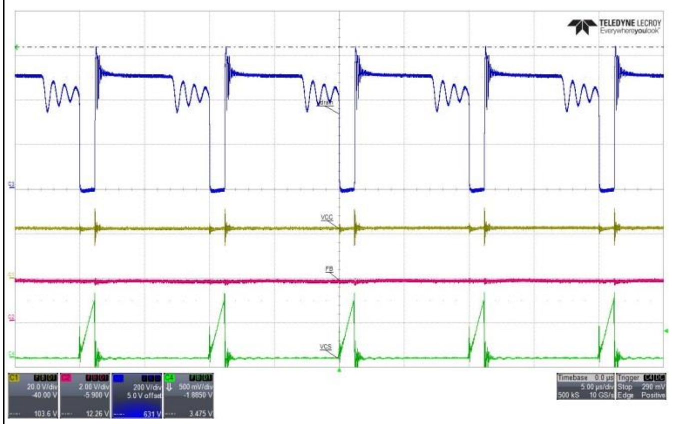
	
C1 (yellow) : Supply voltage (V_{VCC}) C2 (purple) : FB voltage (V_{FB}) C3 (blue) : Drain voltage (V_D) C4 (green) : CS voltage (V_{CS})	C1 (yellow) : Supply voltage (V_{VCC}) C2 (purple) : FB voltage (V_{FB}) C3 (blue) : Drain voltage (V_D) C4 (green) : CS voltage (V_{CS})
V_{Drain_peak} at 85 V AC ≈ 322 V	V_{Drain_peak} at 300 V AC ≈ 631 V

Figure 20 Drain and CS voltage at maximum load

11.4 Frequency jittering

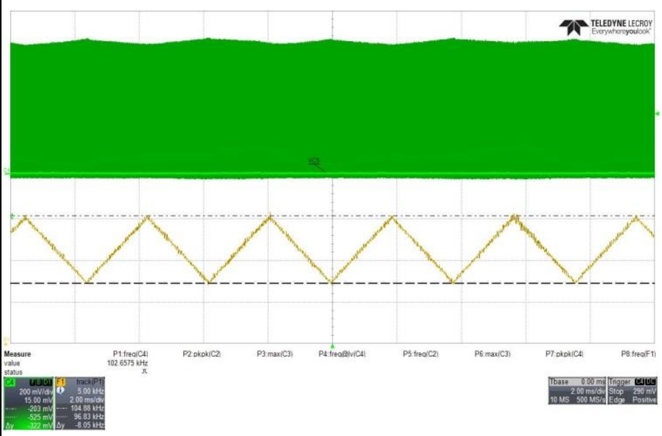
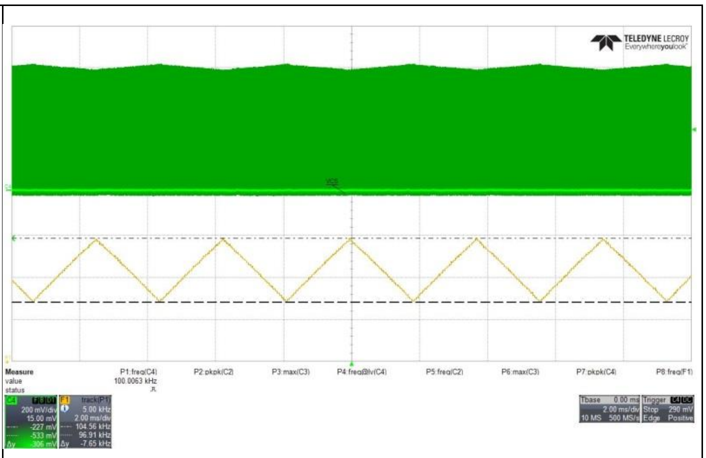
	
C4 (green) : CS voltage (V_{CS}) F1 (yellow) : Frequency track of gate (V_{CS})	C4 (green) : CS voltage (V_{CS}) F1 (yellow) : Frequency track of Gate (V_{CS})
Frequency jittering at 85 V AC and maximum load ≈ 96 kHz ~ 104 kHz, jitter period ≈ 3.5 ms	Frequency jittering at 300 V AC and maximum load ≈ 96 kHz ~ 104 kHz, jitter period ≈ 3.5 ms

Figure 21 Frequency jittering

11.5 Load transient response (dynamic load from 10% to 100%)

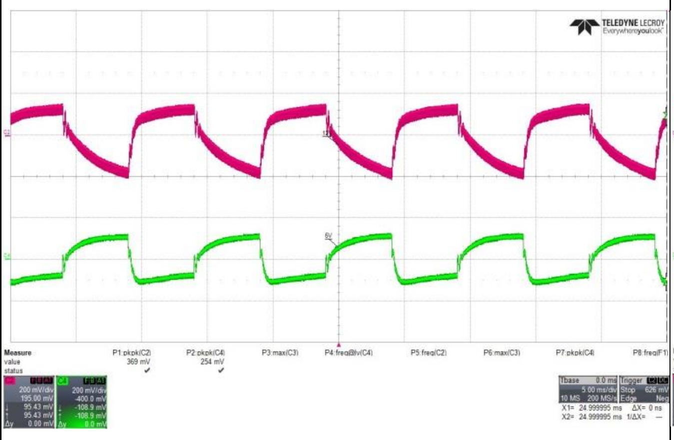
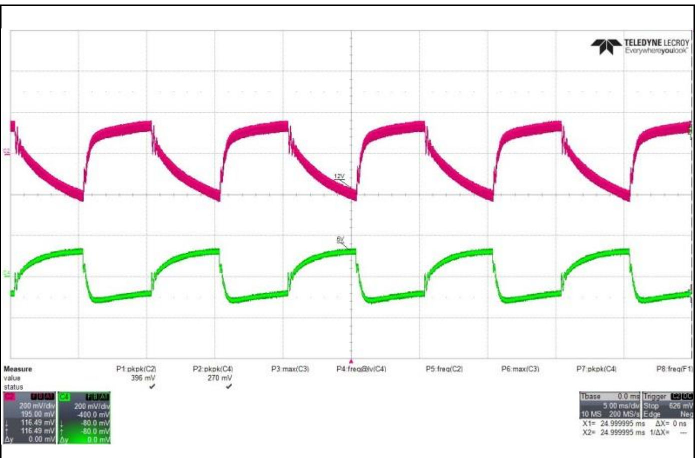
	
C2 (purple) : 12 V output ripple voltage (V_{Out12}) C4 (green) : 5 V output ripple voltage (V_{Out5})	C2 (purple) : 12 V output ripple voltage (V_{Out12}) C4 (green) : 5 V output ripple voltage (V_{Out5})
12 $V_{ripple\_pk\_pk}$ at 85 V AC ≈ 369 mV 5 $V_{ripple\_pk\_pk}$ at 85 V AC ≈ 254 mV (12 V load change from 10% to 100% and 5 V at 1 A load at 85 V AC, 100 Hz, 0.4 A/µs slew rate) Probe terminal end with decoupling capacitor of 0.1 µF (ceramic) and 1 µF (electrolytic), 20 MHz filter	12 $V_{ripple\_pk\_pk}$ at 300 V AC ≈ 396 mV 5 $V_{ripple\_pk\_pk}$ at 300 V AC ≈ 270 mV (12 V load change from 10% to 100% and 5 V at 1 A load at 300 V AC , 100 Hz, 0.4 A/µs slew rate) Probe terminal end with decoupling capacitor of 0.1 µF (ceramic) and 1 µF (electrolytic), 20 MHz filter

Figure 22 Load transient response

11.6 Output ripple voltage at maximum load

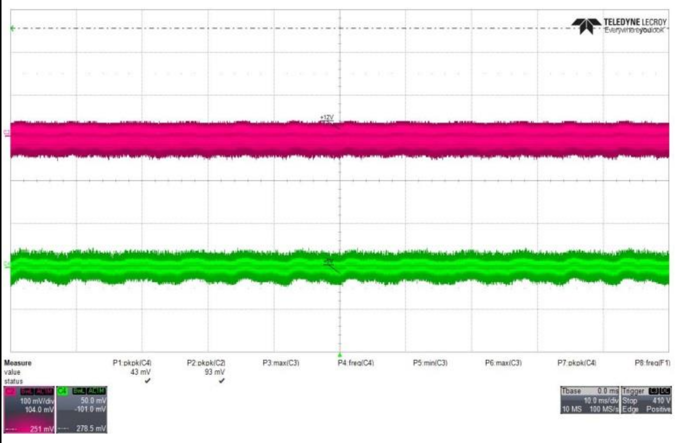
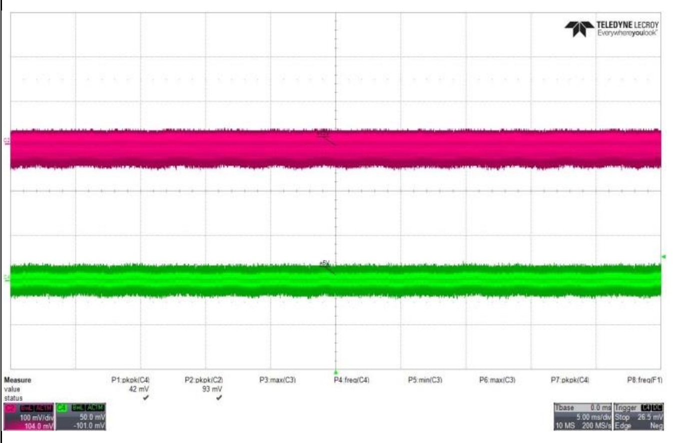
	
C2 (purple) : 12 V output ripple voltage (V_{Out12}) C4 (green) : 5 V output ripple voltage (V_{Out5})	C1 (yellow) : 12 V output ripple voltage (V_{Out12}) C3 (blue) : 5 V output ripple voltage (V_{Out5})
12 $V_{ripple\_pk\_pk}$ at 85 V AC ≈ 93 mV 5 $V_{ripple\_pk\_pk}$ at 85 V AC ≈ 43 mV Probe terminal end with decoupling capacitor of 0.1 µF (ceramic) and 1 µF (electrolytic), 20 MHz filter	12 $V_{ripple\_pk\_pk}$ at 300 V AC ≈ 93 mV 5 $V_{ripple\_pk\_pk}$ at 300 V AC ≈ 42 mV Probe terminal end with decoupling capacitor of 0.1 µF (ceramic) and 1 µF (electrolytic), 20 MHz filter

Figure 23 Output ripple voltage at maximum load

11.7 Output ripple voltage at ABM 1 W load

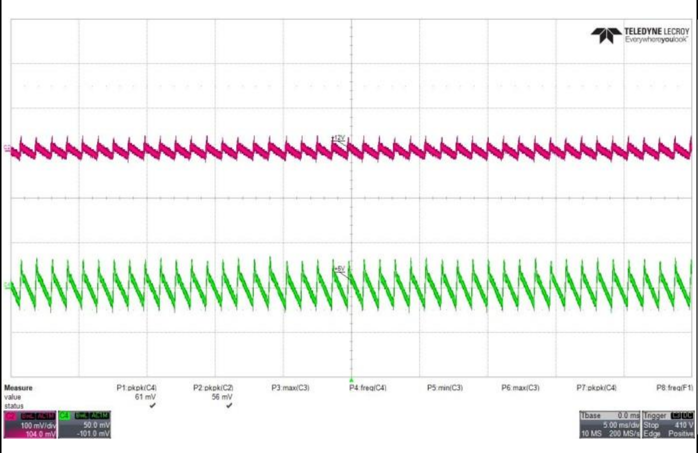
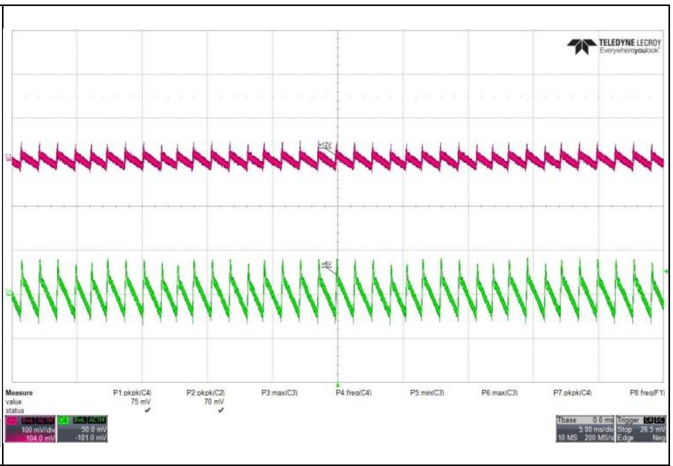
	
C2 (purple) : 12 V output ripple voltage (V_{Out12}) C4 (green) : 5 V output ripple voltage (V_{Out5})	C2 (purple) : 12 V output ripple voltage (V_{Out12}) C4 (green) : 5 V output ripple voltage (V_{Out5})
12 $V_{ripple\_pk\_pk}$ at 85 V AC ≈ 61 mV 5 $V_{ripple\_pk\_pk}$ at 85 V AC ≈ 56 mV Probe terminal end with decoupling capacitor of 0.1 µF (ceramic) and 1 µF (electrolytic), 20 MHz filter	12 $V_{ripple\_pk\_pk}$ at 300 V AC ≈ 75 mV 5 $V_{ripple\_pk\_pk}$ at 300 V AC ≈ 70 mV Probe terminal end with decoupling capacitor of 0.1 µF (ceramic) and 1 µF (electrolytic), 20 MHz filter

Figure 24 Output ripple voltage at ABM 1 W load

11.8 Entering ABM

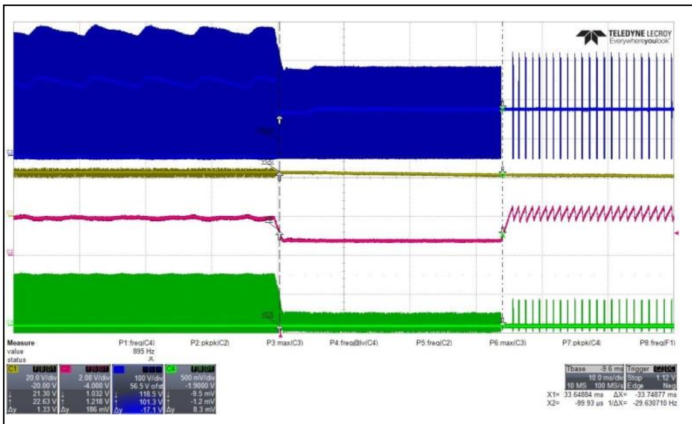
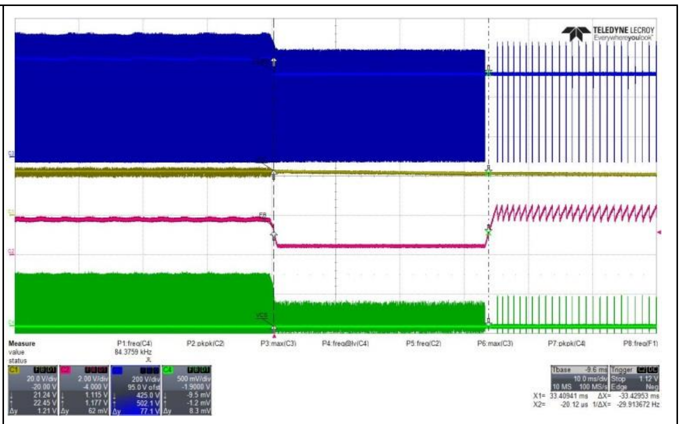
	
C1 (yellow) : Supply voltage (V_{VCC}) C2 (purple) : FB voltage (V_{FB}) C3 (blue) : Drain voltage (V_D) C4 (green) : CS voltage (V_{CS})	C1 (yellow) : Supply voltage (V_{VCC}) C2 (purple) : FB voltage (V_{FB}) C3 (blue) : Drain voltage (V_D) C4 (green) : CS voltage (V_{CS})
Condition to enter ABM level 3: V_{FB} < 1.03 V and $t_{blanking}$ = 36 ms (load change from full load to 1 W load at 85 V AC)	Condition to enter ABM level 3: V_{FB} < 1.03 V and $t_{blanking}$ = 36 ms (load change from full load to 1 W load at 300 V AC)

Figure 25 Entering ABM

11.9 During ABM

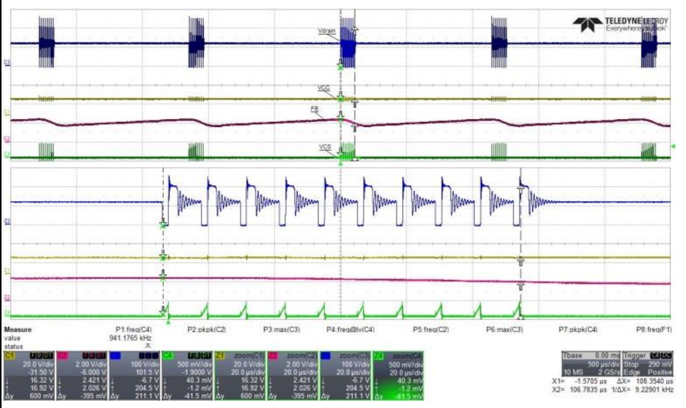
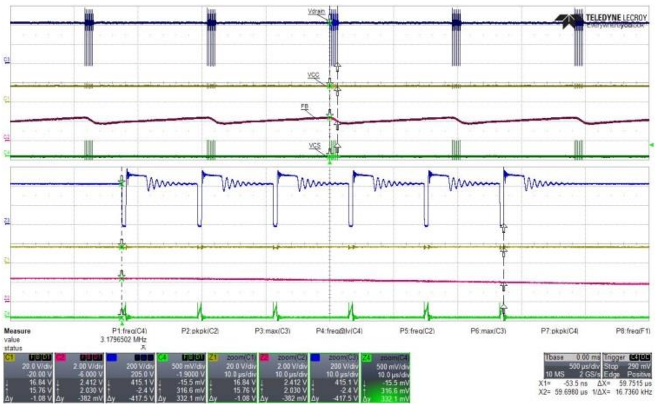
	
C1 (yellow) : Supply voltage (V_{VCC}) C2 (purple) : FB voltage (V_{FB}) C3 (blue) : Drain voltage (V_D) C4 (green) : CS voltage (V_{CS})	C1 (yellow) : Supply voltage (V_{VCC}) C2 (purple) : FB voltage (V_{FB}) C3 (blue) : Drain voltage (V_D) C4 (green) : CS voltage (V_{CS})
During ABM level 3: $V_{FB\_Bon\_ISO}$ = 2.35 V, $V_{FB\_Boff\_NISO}$ = 2.00 V, V_{CS_BHP} = 0.27 V (1 W load at 85 V AC)	During ABM level 3: $V_{FB\_Bon\_ISO}$ = 2.35 V, $V_{FB\_Boff\_NISO}$ = 2.00 V, V_{CS_BHP} = 0.27 V (1 W load at 300 V AC)

Figure 26 During ABM

11.10 Leaving ABM

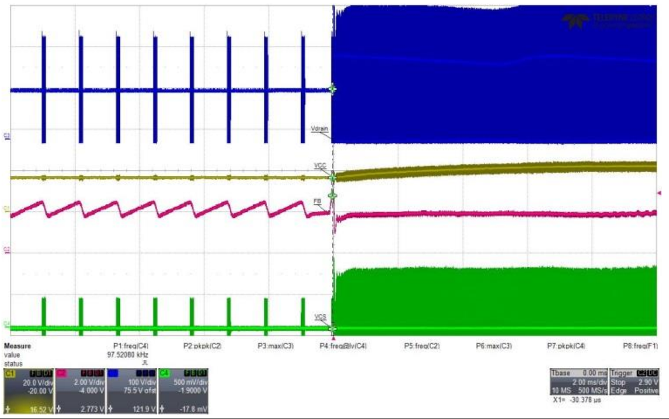
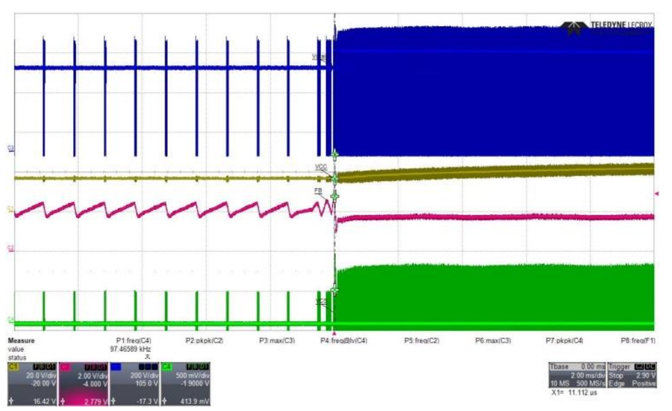
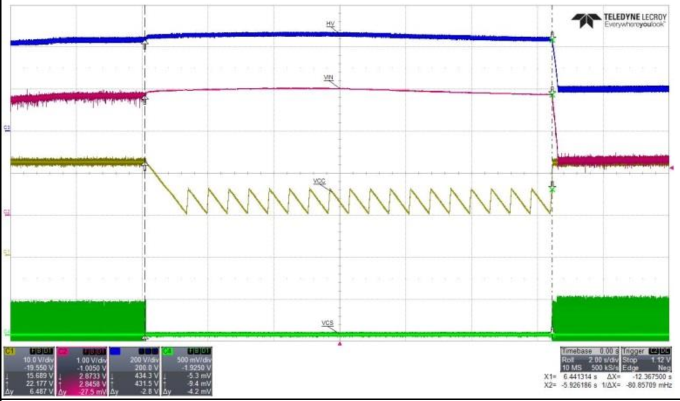
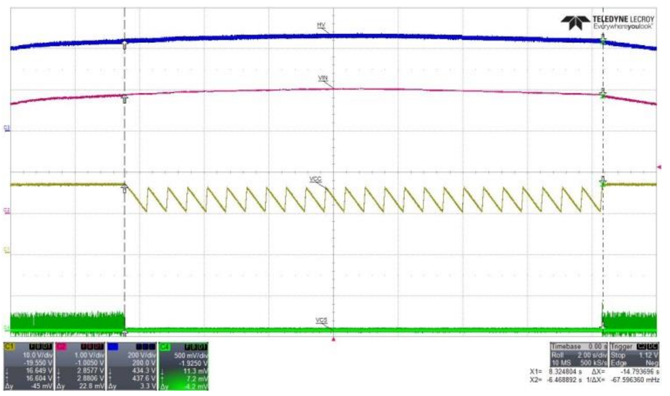
	
C1 (yellow) : Supply voltage (V_{VCC}) C2 (purple) : FB voltage (V_{FB}) C3 (blue) : Drain voltage (V_D) C4 (green) : CS voltage (V_{CS})	C1 (yellow) : Supply voltage (V_{VCC}) C2 (purple) : FB voltage (V_{FB}) C3 (blue) : Drain voltage (V_D) C4 (green) : CS voltage (V_{CS})
Condition to leave ABM level 3: V_{FB} > 2.73 V (load change from 1 W to full load at 85 V AC)	Condition to leave ABM level 3: V_{FB} >2.73 V (load change from 1 W to full load at 300 V AC)

Figure 27 Leaving ABM

11.11 Line OVP (non-switch auto restart)



C1 (yellow) : Supply voltage (V_{VCC})
C2 (purple) : VIN voltage (V_{VIN})
C3 (blue) : Bus voltage (V_{Bus})
C4 (green) : CS voltage (V_{CS})



C1 (yellow) : Supply voltage (V_{VCC})
C2 (purple) : VIN voltage (V_{VIN})
C3 (blue) : Bus voltage (V_{Bus})
C4 (green) : CS voltage (V_{CS})

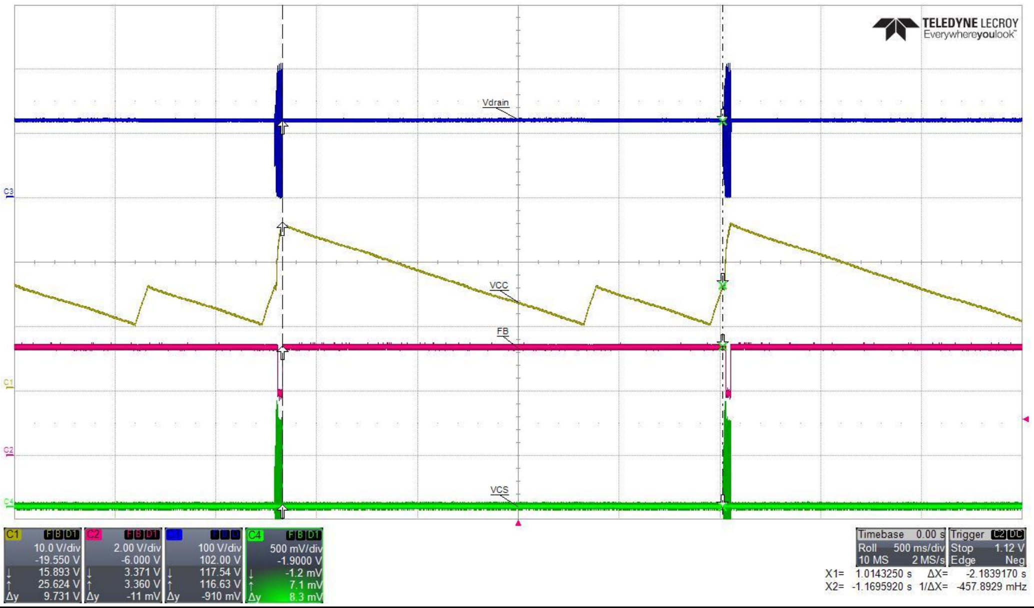
Condition to detect line OVP: V_{VIN} > 2.85 V (V_{BULK} > 447 V DC [≈ 320 V AC])
Condition to reset line OVP: V_{VIN} < 2.85 V (V_{BULK} < 447 V)

(Gradually increase AC-line voltage at full load until line OVP detect and decrease AC-line until line OVP reset)

(Gradually increase AC-line voltage at 1 W load until line OVP detect and decrease AC-line until line OVP reset)

Figure 28 Line OVP

11.12 V_{CC} OVP (odd-skip auto restart)

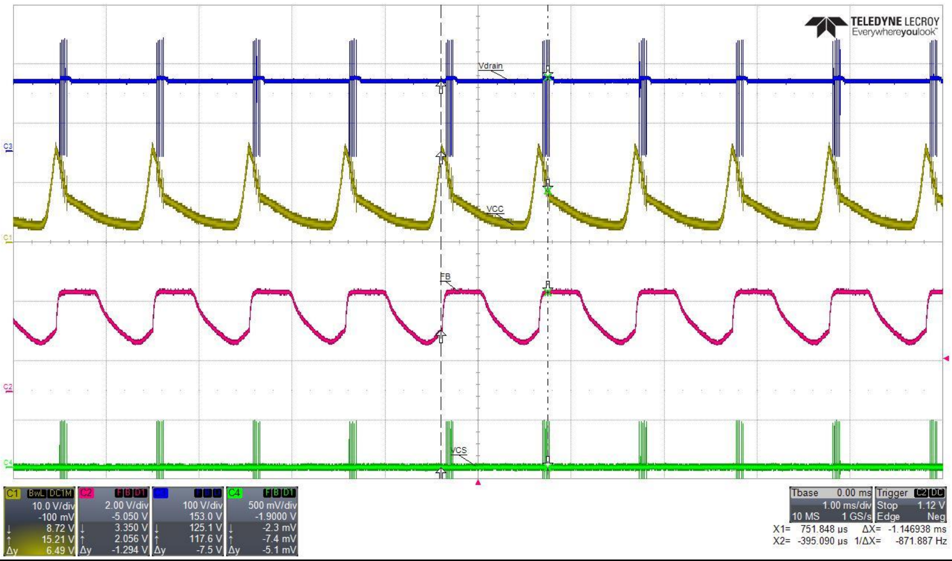


C1 (yellow) : Supply voltage (V_{VCC})
C2 (purple) : FB voltage (V_{FB})
C3 (blue) : Drain voltage (V_D)
C4 (green) : CS voltage (V_{CS})

Condition to enter V_{CC} OVP: V_{VCC} > 25.5 V
(remove ZD1 while system operating at 85 V AC and full load)

Figure 29 V_{CC} OVP

11.13 V_{CC} UV protection (auto restart)



C1 (yellow)	: Supply voltage (V_{VCC})
C2 (purple)	: FB voltage (V_{FB})
C3 (blue)	: Drain voltage (V_D)
C4 (green)	: CS voltage (V_{CS})

Condition to enter V_{CC} UV protection: V_{CC} < 10 V
(Remove R5 and C3 then power on the system with full load at 85 V AC)

Figure 30 V_{CC} UV protection

11.14 Over-load protection (odd-skip auto restart)

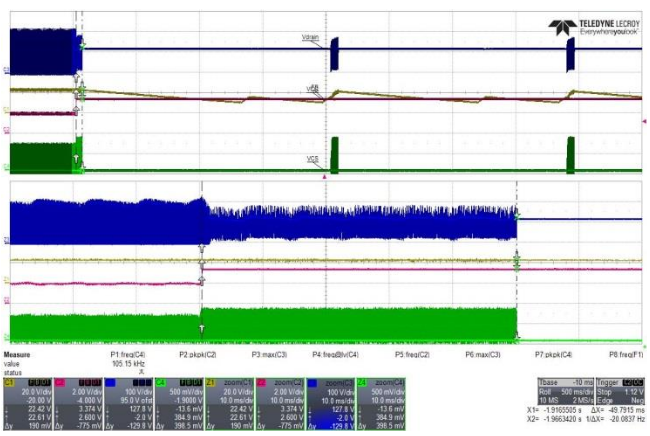
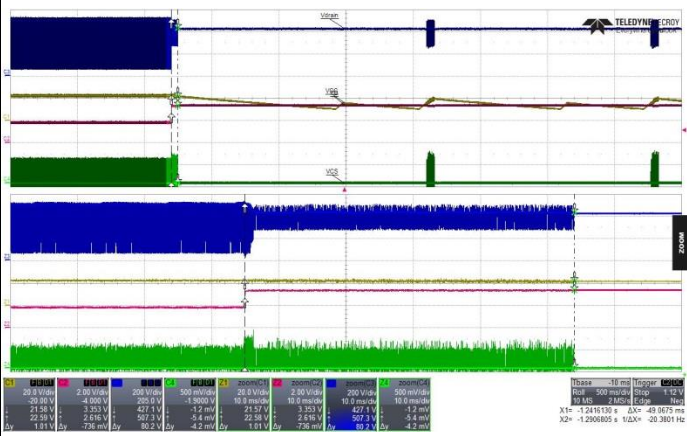
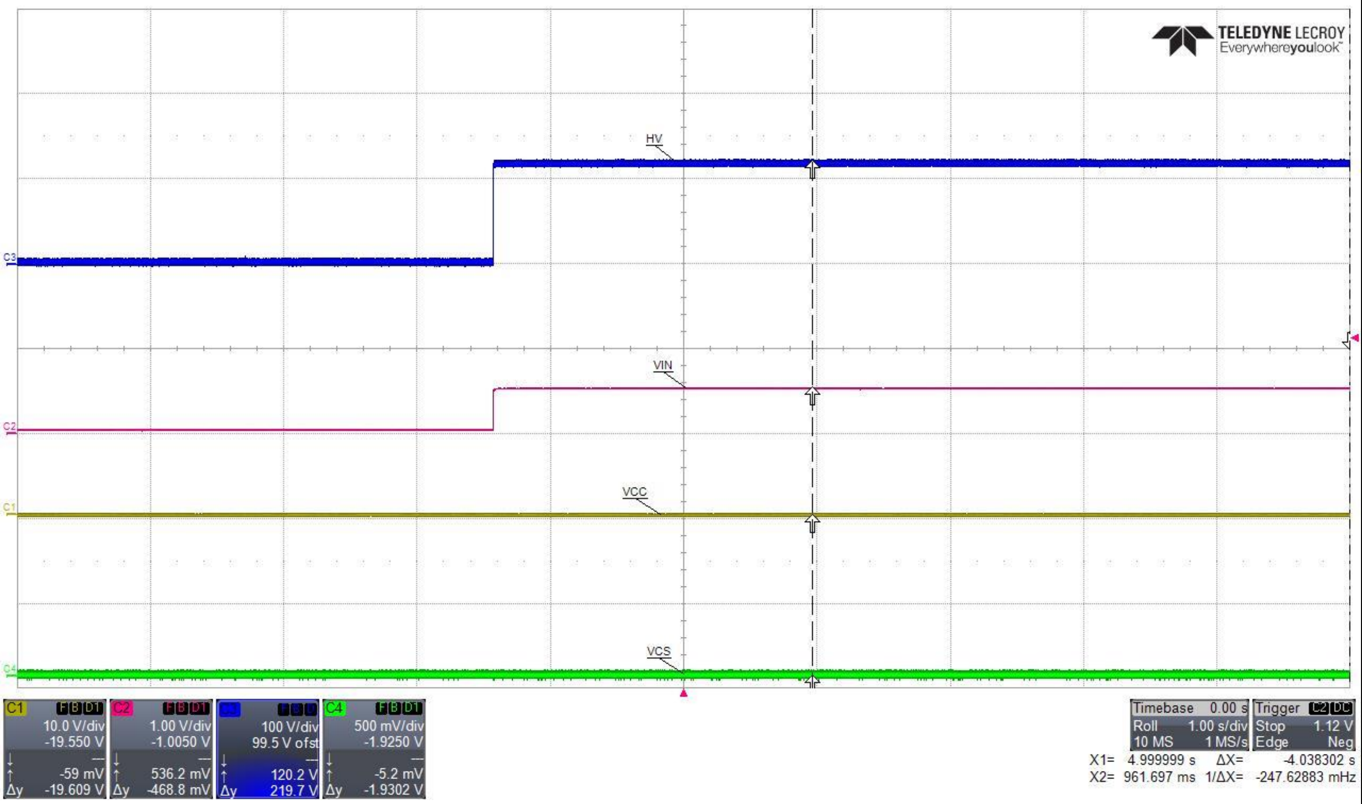
	
C1 (yellow) : Supply voltage (V_{VCC}) C2 (purple) : FB voltage (V_{FB}) C3 (blue) : Drain voltage (V_D) C4 (green) : CS voltage (V_{CS})	C1 (yellow) : Supply voltage (V_{VCC}) C2 (purple) : FB voltage (V_{FB}) C3 (blue) : Drain voltage (V_D) C4 (green) : CS voltage (V_{CS})
Condition to enter over-load protection: V_{FB} > 2.73 V and lasts for 54 ms blanking time (12 V output load change from full to short at 85 V AC)	Condition to enter over-load protection: V_{FB} > 2.73 V and lasts for 54 ms blanking time (12 V output load change from full to short at 300 V AC)

Figure 31 Over-load protection

11.15 V_{CC} short-to-GND protection



C1 (yellow) : Supply voltage (V_{VCC})
C2 (purple) : VIN voltage (V_{VIN})
C3 (blue) : Bus voltage (V_{Bus})
C4 (green) : CS voltage (V_{CS})

Condition to enter V_{CC} short-to-GND: if $V_{CC} < V_{VCC\_SCP}$ → $I_{VCC} = I_{VCC\_Charge1}$
(short V_{CC} pin-to-GND and measure the current with multimeter before system start-up, $I_{VCC} \approx 277$ µA at 85 V AC)

Figure 32 V_{CC} short-to-GND protection

12 References

[1] **ICE5xSAG datasheet, Infineon Technologies AG**

[2] **5th Generation fixed-frequency Design Guide**

[3] **Calculation Tool fixed-frequency CoolSET™ Generation 5**

Revision history

Major changes since the last revision

Page or reference	Description of change
–	First release
Page 12	Add C10 in BOM and change R14 from 12 kΩ to 4.3 kΩ
Page 24, Figure 22	Correct the load condition setting
Page 30	Reference [1] change to ICE5xSAG

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