EiceDRIVER™

Gate resistor for power devices

About this document

Scope and purpose

This application note explains the role of the gate resistor, and it points out what are the most important issues that should be considered when selecting the gate resistors of power devices.

Intended audience

Power electronics engineers who want to design reliable and efficient gate driving circuits

Table of Contents

1 Scope

This application note explains the most common related issues for the identification of suitable gate resistors for power electronic devices. It will depict the physical effects of the gate circuits and clarify the related equations. Please note, that this application note cannot give recommendations for each and every power transistor or power module. However, it will highlight which considerations are important and the effect they can have on the selection of the gate resistors for discrete power transistors as well as for power modules.

2 Gate resistor basics

- The gate resistor is located between the output of the driver and the input of the power device. It is commonly labelled R_G as depicted in Figure 1.

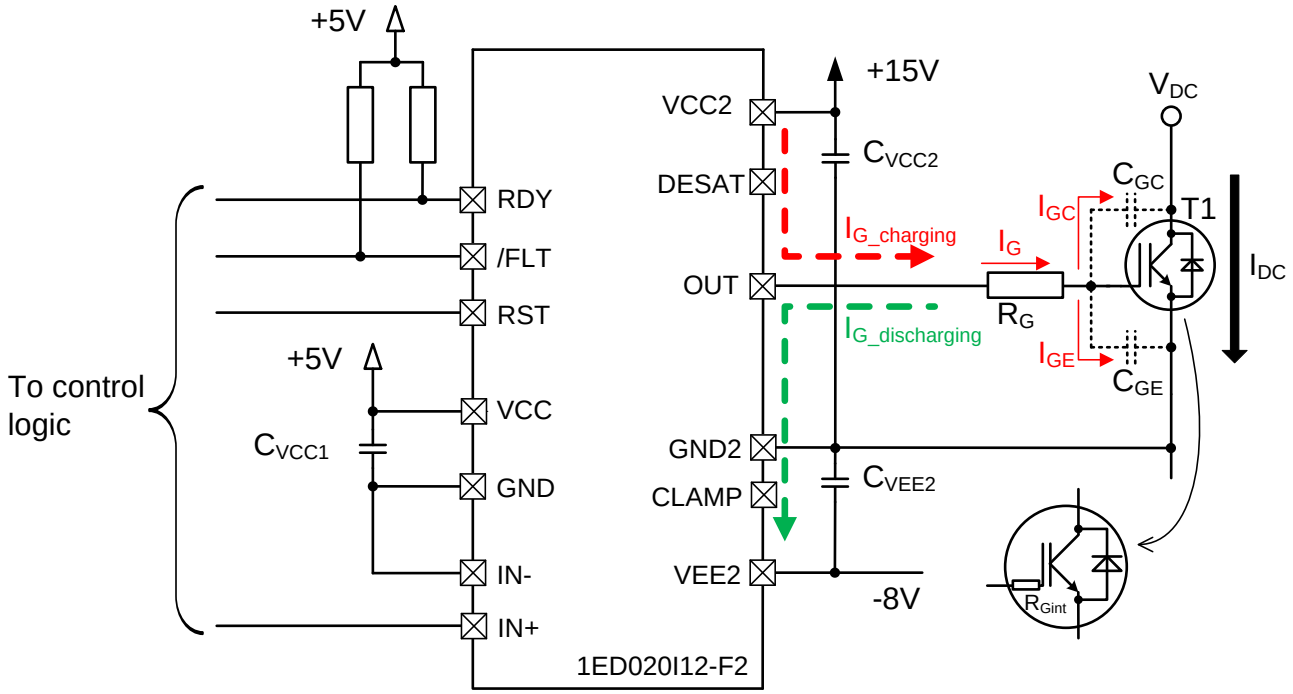

Figure 1 Basic gate driver circuit

The on/off status of the gate controlled power devices, for instance IGBT or power MOSFET, is defined by the gate voltage. The change of this gate voltage influences the charging and discharging of the power device's gate capacitor, which consist of the gate-collector capacitor C_{GC} and the gate-emitter capacitor C_{GE} when an IGBT is taken as example for this application note. The charging of the gate capacitor by $I_{G\_charging}$ will turn the power device on and the discharging of the gate capacitor by $I_{G\_discharging}$ of the gate capacitor will turn it off.

The current, charging and discharging the gate, is limited by the gate resistor R_G. This will influence the switching speed of the power device. Besides this, there are also several other influences from the gate resistor:

- Limit peak gate current to protect the driver output stage
- Dissipate power in the gate loop
- Electromagnetic interference
- Prevent gate ringing
- Avoid parasitic turn-on by carefully choosing gate resistance

3 What should be considered for gate resistance when design a gate driver circuit

The gate resistor as a physical entity has to be sufficient for its purpose in a multitude of aspects. This section focuses on the gate resistors abilities to define the peak current, its influence to the power dissipation, switching speed and the correlated switching losses. Furthermore Electromagnetic Compatibility, gate ringing and parasitic turn-on which are also affected by gate resistance are also explained. Finally a typical gate circuit is introduced.

3.1 Gate charging/discharging peak current

The gate driver IC's output stage has the maximum allowed peak current values I_{OH_PEAK} for turn-on and I_{OL_PEAK} for turn-off which are often specified within the driver IC's datasheet. When the output current of the driver IC is higher than this peak current value, the output stage could be damaged. Thus it is important to limit the output current for safety reason. Figure 2 depicts an example and helps to understand it in detail.

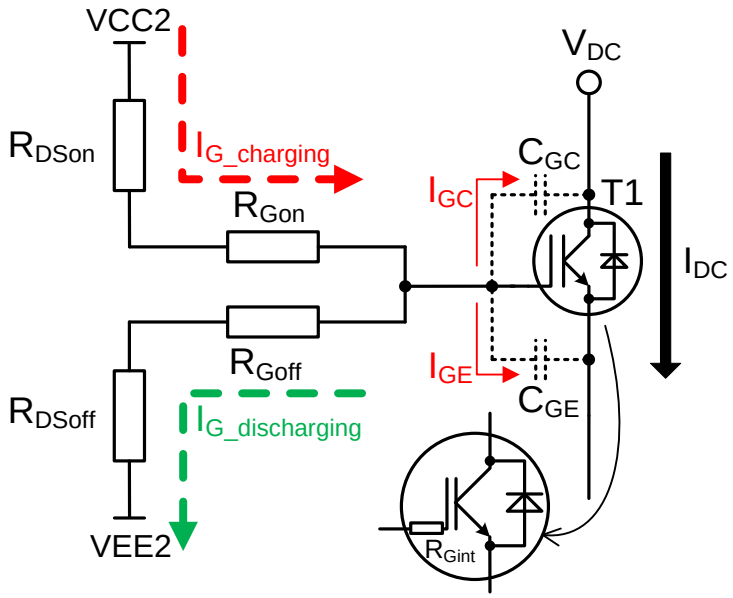

Figure 2 Gate charging/discharging diagram

Here the R_{DSon} depicts the resistance of the driver IC's output stage during turn-on and R_{DSoff} depicts the resistance during turn-off respectively, both are driver IC internal parameters. The resistor R_{Gon} represents the turn-on gate resistance and R_{Goff} represents the turn-off gate resistance. During IGBT T1 turn-on, the gate charging current $I_{G\_charging}$ is driven by the driver IC's supply VCC2 through R_{DSon} and R_{Gon} to the gate of the IGBT. During IGBT turn-off, the gate discharging current $I_{G\_discharging}$ flows from the IGBT's gate through R_{Goff} and R_{DSoff} to the power ground of the driver IC. Following this charging/discharging path, the peak current value can be derived by equations (1) and (2)

$$I_{\mathrm{G\_charging\_peak}} = \frac{VCC2 - VEE2}{R_{\mathrm{DSon}} + R_{\mathrm{Gon}}} \quad (1)$$

$$and\ I_{\mathrm{G\_discharging\_peak}} = \frac{VCC2 - VEE2}{R_{\mathrm{DSoff}} + R_{\mathrm{Goff}}}. \quad (2)$$

This charging/discharging current must be lower than the peak current allowed for the driver IC's output stage to guarantee the safe operation.

$$I_{\mathrm{G\_charging\_peak}} < I_{\mathrm{OH\_PEAK}} \quad (3)$$

$$I_{\mathrm{G\_discharging\_peak}} < I_{\mathrm{OL\_PEAK}} \quad (4)$$

3.2 Power dissipation

The gate resistor has a very important function – help to limit the power dissipation in the driver IC's output stage. A higher resistance reduces the current, thus reducing the power to be dissipated in the driver IC. According to Figure 2, during turn-on the power dissipation at the internal resistance R_{DSon} can be calculated as

$$P_{\mathrm{G\_charging}} = \frac{1}{2} Q_{\mathrm{G}} \cdot (VCC2 - VEE2) \cdot f_{\mathrm{SW}} \cdot \frac{R_{\mathrm{DSon}}}{R_{\mathrm{DSon}} + R_{\mathrm{Gon}}}. \quad (5)$$

During turn-off, the power dissipation at the internal resistance R_{DSoff} can be calculated as

$$P_{\mathrm{G\_discharging}} = \frac{1}{2} Q_{\mathrm{G}} \cdot (VCC2 - VEE2) \cdot f_{\mathrm{SW}} \cdot \frac{R_{\mathrm{DSoff}}}{R_{\mathrm{DSoff}} + R_{\mathrm{Goff}}}. \quad (6)$$

Here, f_{SW} is the switching frequency and $VCC2 - VEE2$ is the gate voltage step between charging and discharging of the gate capacitance. The value of the charge Q_G to be considered depends on the gate-emitter voltage V_{GE} and an accurate approximation can be done using the gate charge curve [1] as given in Figure 3.

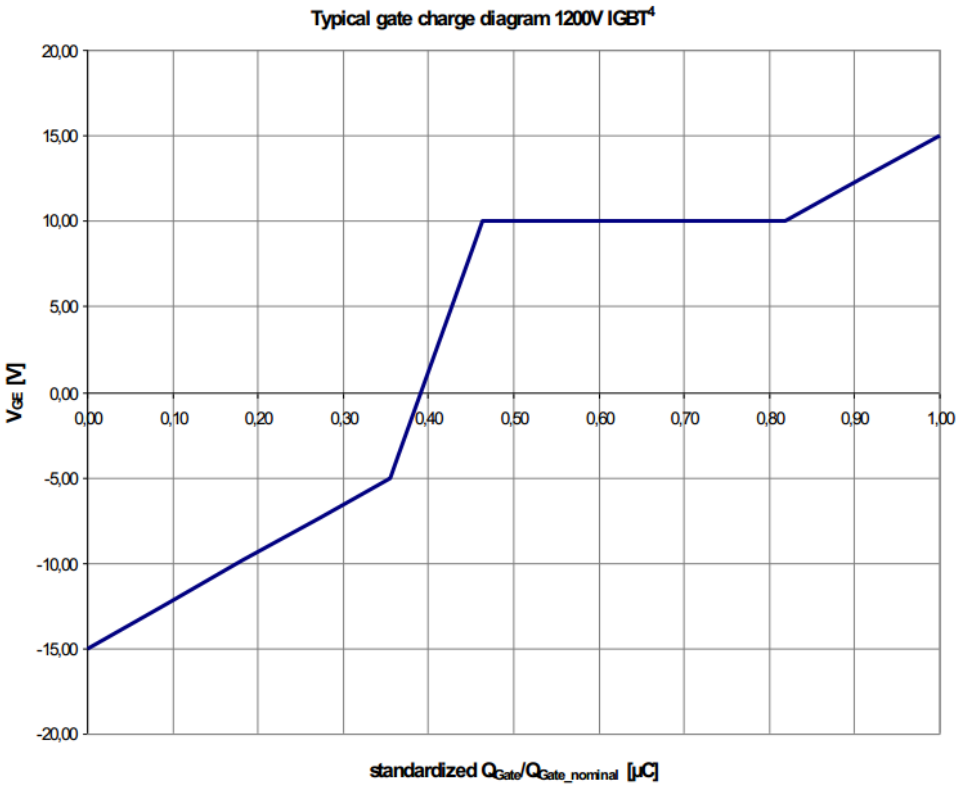

Figure 3 Gate charge diagram

In order to conduct quick calculation, some datasheets [2] directly specify the gate charge Q_G under the condition V_{GE} = -15V…+15V. In this case, when the turn-on voltage from the driver IC is +15V and turn-off voltage is -15V, this value can be directly used in equation (5) and (6). In case the turn-off voltage V_{GE} = 0V or V_{GE} = -8V, the respective value Q_G' can be approximateed as given in equations (7) and (8),

$$\mathrm{Q_G}'|_{\mathrm{V_{GE}=0..15V}} = 0.62 \cdot \mathrm{Q_G} \quad (7)$$

$$Q_G'|_{V_{GE}=-8..15V} = 0.75 \cdot Q_G. \quad (8)$$

The overall power dissipation of the driver IC must remain below the maximum allowed power dissipation value P_{D_max}, leading to the damand

$$P_{G\_charging} + P_{G\_discharging} + P_Q < P_{D\_max}. \quad (9)$$

In this equation, P_Q depicts the quiescent power of the driver IC. Combining equation (5), (6) and (9), it can be easily seen that higher values for the gate resistances R_{Gon} and R_{Goff} will reduce the power dissipation at the driver IC's output stage, so that it will help to guarantee a safe operation of the component.

3.3 Switching speed and electromagnetic compatibility

As described in section 3.2, higher gate resistance values can be beneficial from the driver IC's loss-situation and thermal point of view. Furthermore, the changing of the gate resistance will influence the switching speed of the power device, which will have an impact in two directions: efficiency and noise.

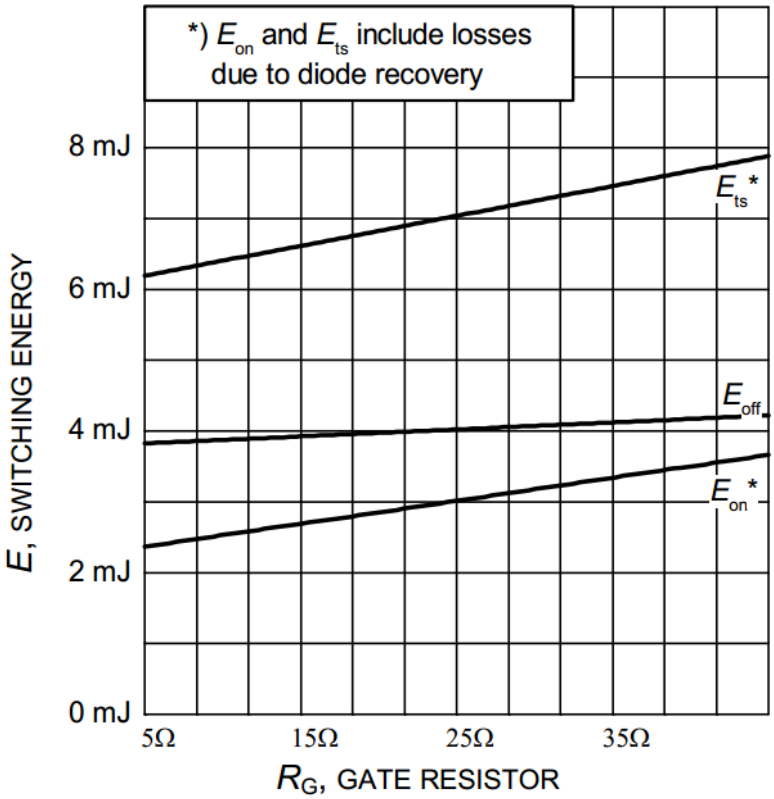

Figure 4 Typical switching losses as function of gate resistor for Infineon IKW25T120 [3]

Generally speaking, with higher gate resistance value, the switching speed of the power device will decrease. This means the switching loss will be increased as illustrated in Figure 4 as an example. This in turn will finally influence the efficiency. In contrast, when a lower gate resistance is applied, the switching will become faster which can reduce the switching loss. Meanwhile, the noise induced by di/dt and dv/dt will increase with higher switching speed. Since the electromagnetic compatibility (EMC) regulation must be fulfilled, the gate resistance value needs to be chosen carefully.

To get more information about this topic, please refer to the Infineon paper: Balancing losses and noise - considerations for choosing the gate resistor [4].

3.4 Gate ringing

In power electronic applications, gate ringing is an often observed phenomenon due to parasitics along the gate loop. As described in Figure 5, OUT is the output of the driver IC, which is used to drive a power device. I_G is the gate current along the gate loop. L_P and C_{GE} are the parasitics along the gate loop which form the resonant tank. With excitation, oscillation could appear.

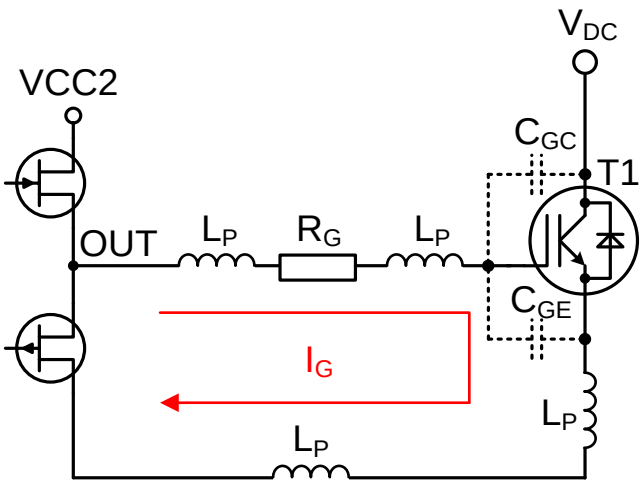

Figure 5 Gate loop with parasitics

For the applications which use power MOSFETs, this gate ringing effect normally becomes more severe, especially for parallel driving since more resonance tanks are formed. To avoid the ringing effect, one important measure is to limit the parasitic inductance L_P by layout optimization:

- Shorten the trace length to physically keep the gate loop as small as possible which can normally reduce the parasitic inductance by 1nH/mm.
- Connect Kelvin emitter/source when it is available on power device

In some designs, this cannot be achieved due to the geometry. In this case, use of a larger gate resistance value could be a workaround, which will increase the damping effect and finally suppress the ringing effect. Designers should be aware that, as already mentioned in section 3.3, increasing the gate resistance value will decrease the efficiency. Also, considering signal integrity, too high gate resistance value will decouple the gate signal which comes from the output stage of the driver. This will lead to longer delay times or even operation failure. Therefore, the value of the gate resistor should be chosen carefully.

Besides the value choosing, the layout of the gate resistor is also important. If it is physically possible, the gate resistor should be put as close as possible to the gate of the power device.

3.5 Parasitic turn-on

Parasitic turn-on is a common phenomenon in many situations. This is a physical effect due to the high dv/dt combined with the parasitic Miller capacitance.

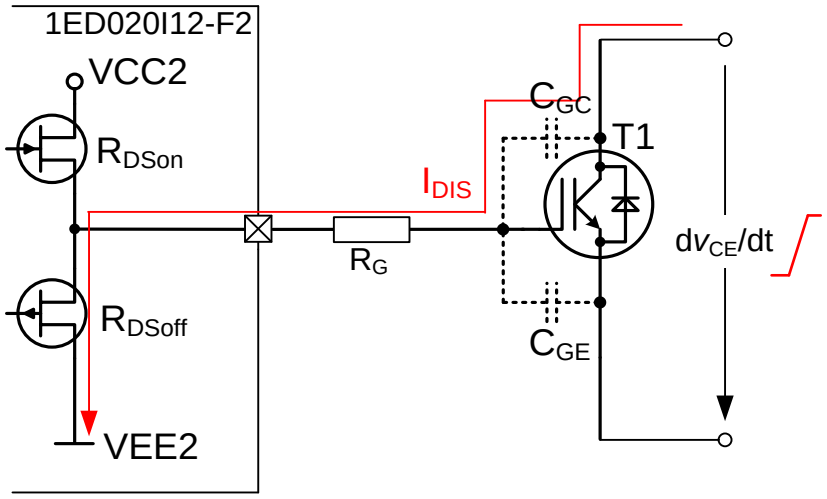

Figure 6 Parasitic tun-on

As sketched in Figure 6, high dv_{CE}/dt across the power device T1 will generate a displacement current I_{DIS} through the Miller capacitor C_{GC}. This is often triggered by turning on the paired device in a half bridge topology. Through the gate resistor R_G, this displacement current I_{DIS} will generate a voltage drop across the gate resistor and will lift up the gate voltage of the power device. This can be calculated according to equation (10) and (11)

$$I_{DIS} = C_{GC} \cdot \frac{dv_{CE}}{dt} \tag{10}$$

$$V_G = I_{DIS} \cdot (R_G + R_{DSoff}). \tag{11}$$

RDSoff depicts the resistance of the driver IC's pulling down device. Here, the pulling down device is on when the power device T1 is off. V_G is the voltage which appears at the gate of the power device. When V_G is higher than the threshold voltage of the power device T1, the parasitic turn-on happens. This will influence the safety of the system as bridge shoot-through could appear.

This parasitic turn-on effect could become more severe when the temperature increases, since the gate threshold voltage of the power device is normally negatively proportional to temperature. Figure 7 gives an example based on the datasheet of Infineon's IGBT IKW25T120 [3].

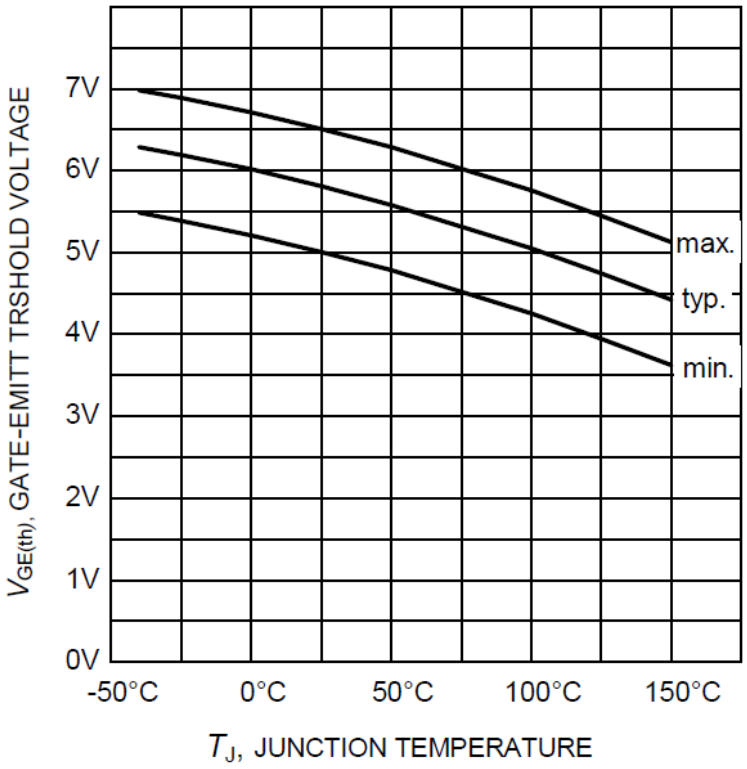

Figure 7 Gate-emitter threshold voltage as function of junction temperature [3]

One measure to limit this parasitic turn-on effect is to reduce the gate resistance value according to equation (11).

3.6 Typical gate circuit

In many applications, separated turn-on and turn-off gate resistors are used as seen in Figure 8. The series connected fast recovery diode D_{Goff} is used to keep the gate resistance during turn-off lower than the gate resistance during turn-on. This is done because the turn-off delay time is often longer than the turn-on delay time for some of the power devices. It can also help to prevent a capacitive turn-on via the Miller capacitance as explained in section 3.5. On the other hand, if the value chosen for R_{Goff} is too low, it could lead to large voltage overshoot across power devices due to too high di/dt during turn-off. So it is always a trade-off between switching speed and robustness. As a rule of thumb it can be assumed that $R_{Gon}=2 \cdot R_{Goff}$.

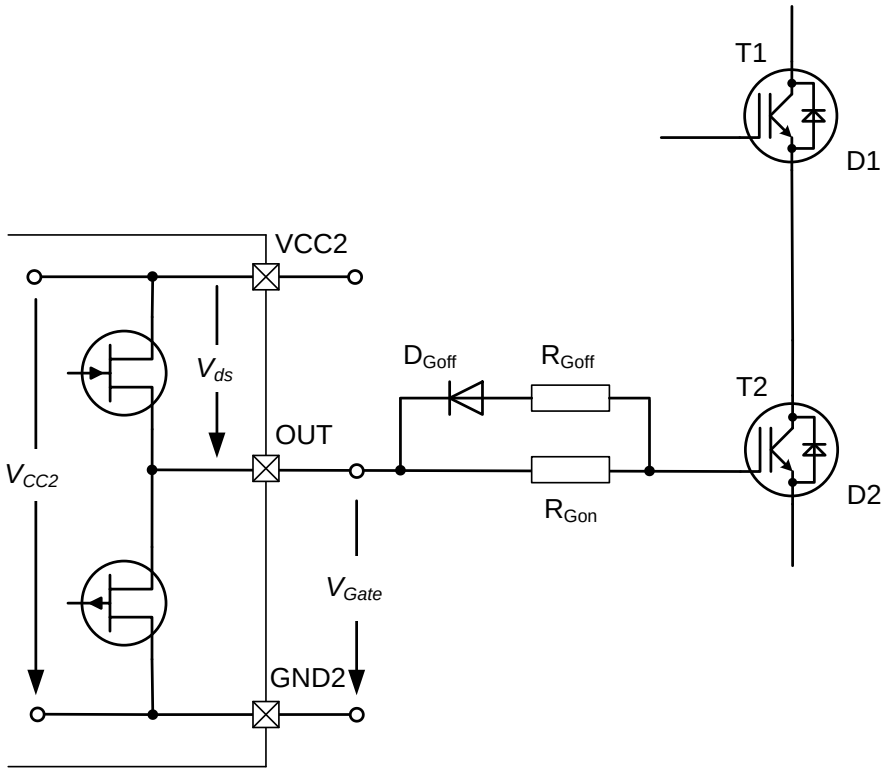

Figure 8 Basic gate circuit

4 The tricks to quickly select a proper gate resistor

Despite the various influences that are found in choosing a proper gate resistor, considering some basic hints can help the designer to get a quick start. This section focuses on the power rating of gate resistors and a thumb rule for quick selection.

4.1 Power rating of gate resistors

Driving the gate is the typical pulse operation. The gate resistor needs to sustain the gate charging and discharging pulse current repetitively. To select a proper gate resistor, the pulse power capability needs to be checked. As describe in section 3.1, the peak pulse current during gate charging/discharging can be calculated according to equation (1) and (2). Then, the pulse power can be derived from equations (12) and (13)

$$P_{\mathrm{G\_charing\_peak}} = I^2{}_{\mathrm{G\_charging\_peak}} \cdot R_{\mathrm{G}} \tag{12}$$

$$P_{\mathrm{G\_discharing\_peak}} = I^2{}_{\mathrm{G\_discharging\_peak}} \cdot R_{\mathrm{G}}. \tag{13}$$

This calculated pulse power must be in the range of the maximum allowed continuous pulse load, as displayed in Figure 9 as an example, to guarantee a safe and reliable operation.

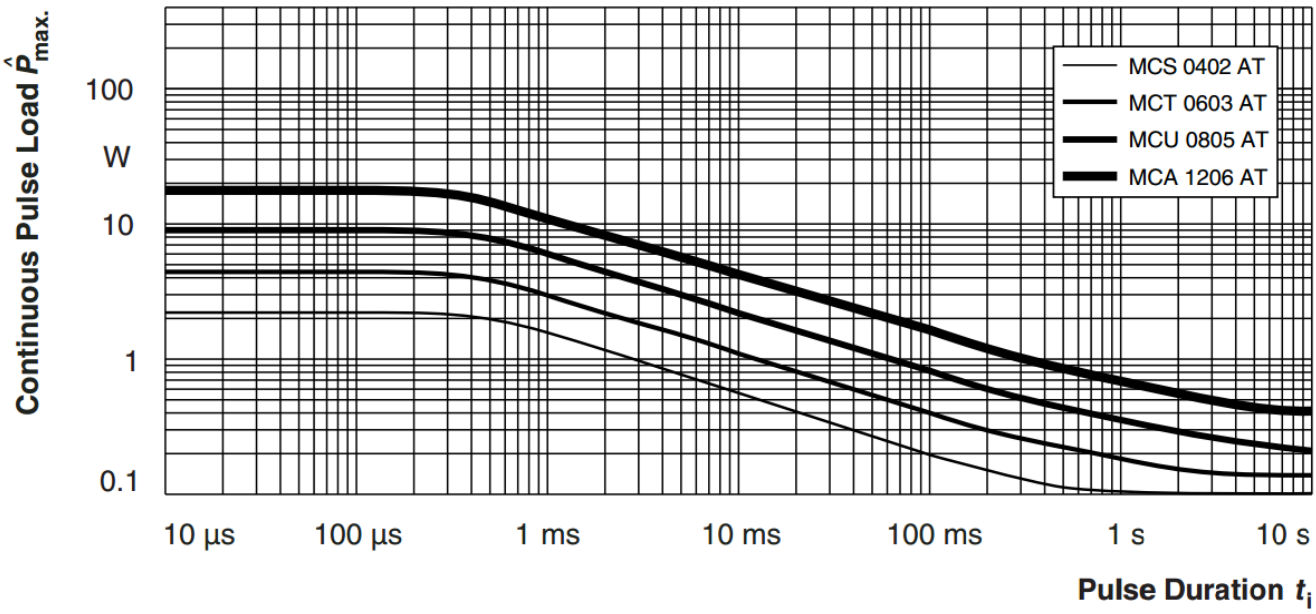

Figure 9 Maximum pulse load, continuous pules, Vishay thin film resistor [5]

4.2 Rule of Thumb

To quickly find a balance point between stability and efficiency, the gate resistance value between nominal value specified in the datasheet and twice of this nominal value can be considered as a point to start from. This is only in the case if there is no time to check through all related issues which are explained in the above chapters. To be sure the gate resistor really fits into the specified application, individual test must be applied based on the real system.

5 References

[1] Infineon Technologies: Application Note; Industrial IGBT Modules Explanation of Technical Information; Infineon Technologies, Germany

[2] Infineon Technologies: Datasheet; DF200R12W1H3_B27; Infineon Technologies, Germany

[3] Infineon Technologies: Datasheet; IKW25T120; Infineon Technologies, Germany

[4] Infineon Technologies: Paper; Balancing losses and noise - considerations for choosing the gate resistor; Infineon Technologies, Germany

[5] Vishay: Datasheet; MCA1206AT; Vishay, USA

Revision History

Major changes since the last revision

Page or Reference	Description of change

Edition 2015-12-17

Published by

Infineon Technologies AG

81726 Munich, Germany

Do you have a question about this document?

Email: erratum@infineon.com

Application Note AN2015-06

IMPORTANT NOTICE

The information contained in this application note is given as a hint for the implementation of the product only and shall in no event be regarded as a description or warranty of a certain functionality, condition or quality of the product. Before implementation of the product, the recipient of this application note must verify any function and other technical information given herein in the real application. Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind (including without limitation warranties of non-infringement of intellectual property rights of any third party) with respect to any and all information given in this application note.

The data contained in this document is exclusively intended for technically trained staff. It is the responsibility of customer's technical departments to evaluate the suitability of the product for the intended application and the completeness of the product information given in this document with respect to such application.

For further information on the product, technology, delivery terms and conditions and prices please contact your nearest Infineon Technologies office (**www.infineon.com**).

WARNINGS

Due to technical requirements products may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies office.

Except as otherwise explicitly approved by Infineon Technologies in a written document signed by authorized representatives of Infineon Technologies, Infineon Technologies' products may not be used in any applications where a failure of the product or any consequences of the use thereof can reasonably be expected to result in personal injury.