# Application Note

## EiceDRIVER 1EDI302xAS/1EDI303xAS

## About this document

### Scope and purpose

This is an application note for the EiceDRIVER™ 1EDI302xAS and 1EDI303xAS. This application note is intended to give users of the product hints for the application. For more details please refer to the datasheet.

It is the responsibility of the integrator to ensure that the EiceDRIVER™ 1EDI302xAS and 1EDI303xAS variants are suitable for the chosen application and comply with the appropriate application standards.

### Intended audience

This application note is intended for engineers who wants to use the 1EDI30xxAS in their application.

### Device variants in this document

**Table 1 Overview of device variants of EiceDRIVER 1EDI30xxAS**

| Name | Description and Features | Package |
|---|---|---|
| 1EDI3020AS | High voltage gate driver for IGBT with integrated ADC for temperature | PG-DSO-20 |
| 1EDI3021AS | High voltage gate driver for IGBT with integrated ASC | |
| 1EDI3023AS | High voltage gate driver for IGBT with integrated ADC for NTC and DC-link | |
| 1EDI3030AS | High voltage gate driver for SiC with integrated ADC for temperature | |
| 1EDI3031AS | High voltage gate driver for SiC with integrated ASC | |
| 1EDI3033AS | High voltage gate driver for SiC with integrated ADC for NTC and DC-link | |

# Table of content

## Table of content

# 1 Introduction

There are six different variants of the product as shown in Table 1. All variants are represented and their features are described within this application note. Devices including the Analog-Digital-Converter (ADC) function are referred to as 1EDI30x0AS. Devices which include the ASC function are referred to as 1EDI30x1AS. Any differences taken into account between the IGBT and SiC variants are described in the next chapter.

The variants can be categorized by functionality and power switch technology. Each variant offers a different feature set with optimized timings like:

- ADC for diode temperature measurement with an active accurate current source of 200 µA
- ADC for NTC temperature/DC-link voltage measurement with a deactivated internal current source
- Secondary side Active Short Circuit (ASC) are optimized for IGBT and SiC power switches.

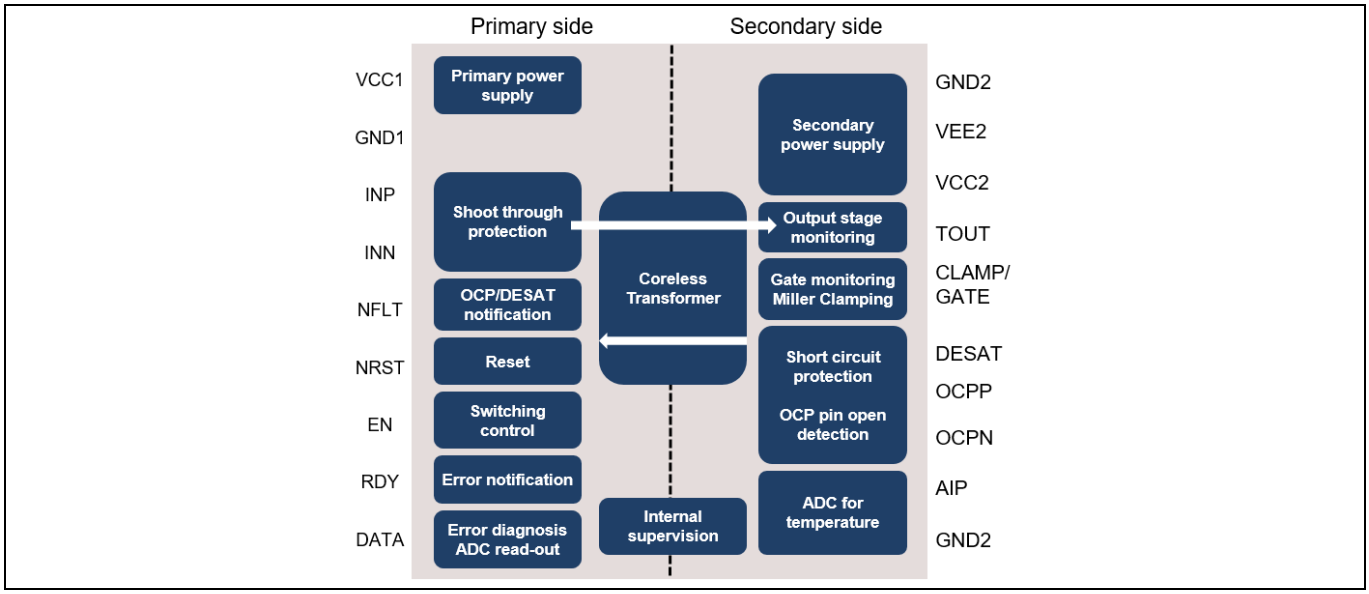



**Figure 1 Block diagram of EiceDRIVER™ 1EDI30x0AS and 1EDI30x3AS with ADC for temperature or DC-link measurement**

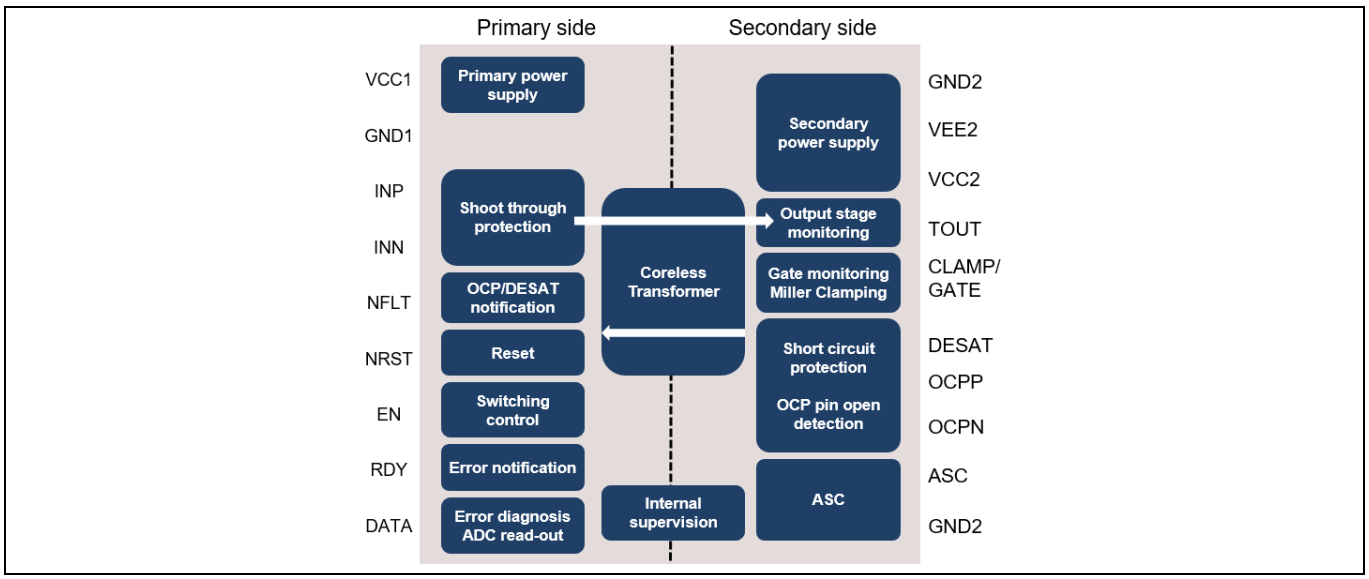
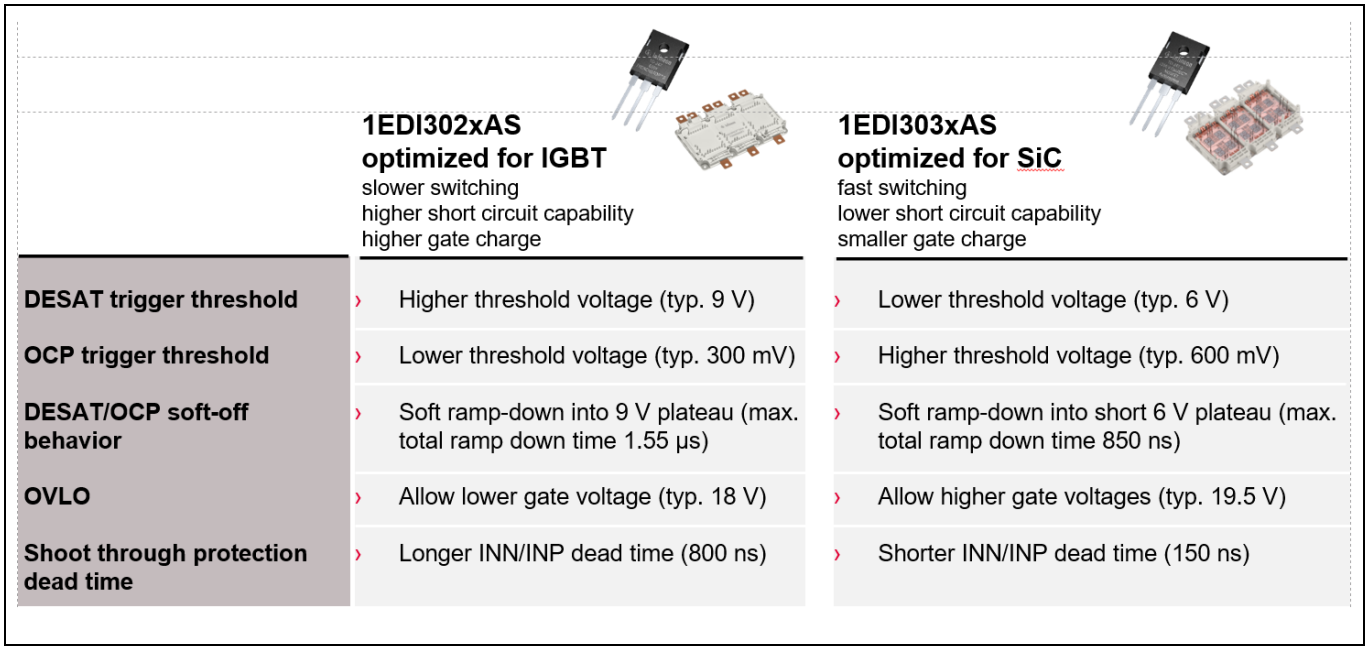



**Figure 2 Block diagram of EiceDRIVER™ 1EDI30x1AS with ASC on secondary side**

# 2 Differences in driving IGBT and SiC MOSFETs in main inverter

The EiceDRIVER™ 1EDI30xxAS is Infineon's first automotive gate driver family which is developed specifically to the needs of a SiC MOSFET and an IGBT. This chapter shows and explains the top level differences of driving an IGBT in comparison to a SiC MOSFET. In addition, it explains how the unique feature sets in six different variants cover these differences.

## 2.1 Summary of differences reflected in variants



| | 1EDI302xAS optimized for IGBT<br>slower switching<br>higher short circuit capability<br>higher gate charge | 1EDI303xAS optimized for SiC<br>fast switching<br>lower short circuit capability<br>smaller gate charge |
|---|---|---|
| **DESAT trigger threshold** | › Higher threshold voltage (typ. 9 V) | › Lower threshold voltage (typ. 6 V) |
| **OCP trigger threshold** | › Lower threshold voltage (typ. 300 mV) | › Higher threshold voltage (typ. 600 mV) |
| **DESAT/OCP soft-off behavior** | › Soft ramp-down into 9 V plateau (max. total ramp down time 1.55 µs) | › Soft ramp-down into short 6 V plateau (max. total ramp down time 850 ns) |
| **OVLO** | › Allow lower gate voltage (typ. 18 V) | › Allow higher gate voltages (typ. 19.5 V) |
| **Shoot through protection dead time** | › Longer INN/INP dead time (800 ns) | › Shorter INN/INP dead time (150 ns) |

**Figure 3 Parameter differences for IGBT and SiC variants**

### Advantage of the series

Infineon offers variants which are preconfigured to the needs of optimized SiC and IGBT usage. Apart from the differences of the functionalities and timings shown, all other functionalities are identical, meaning that the devices can be easily used in a platform approach for SiC and IGBT. Additional detailed information regarding the technologies itself can be found in the following dedicated application notes:

- IGBT
- CoolSiC MOSFET 1200V
- SicMOSFets_using EiceDRIVER

## 2.2 Calculation of maximum switching frequency

The EiceDRIVER™ 1EDI302xAS and 1EDI303xAS family offers a broad range of possible target applications. For main inverter and all auxiliary drive applications with IGBTs and SiC MOSFETs the switching frequency is typically between 10 and 25 kHz in order to keep the switching losses inside of the inverter at a controllable level. In peak conditions like the hill-hold scenario the switching frequencies are decreased further. For on board charger and DC/DC applications the application switching frequency of the resonant tank is above 100 kHz.

Wide-bandgap technologies like SiC enable higher switching frequencies due to lower switching losses.

The EiceDRIVER™ 1EDI302xAS and 1EDI303xAS family offers an optimized solution for each technology and application.

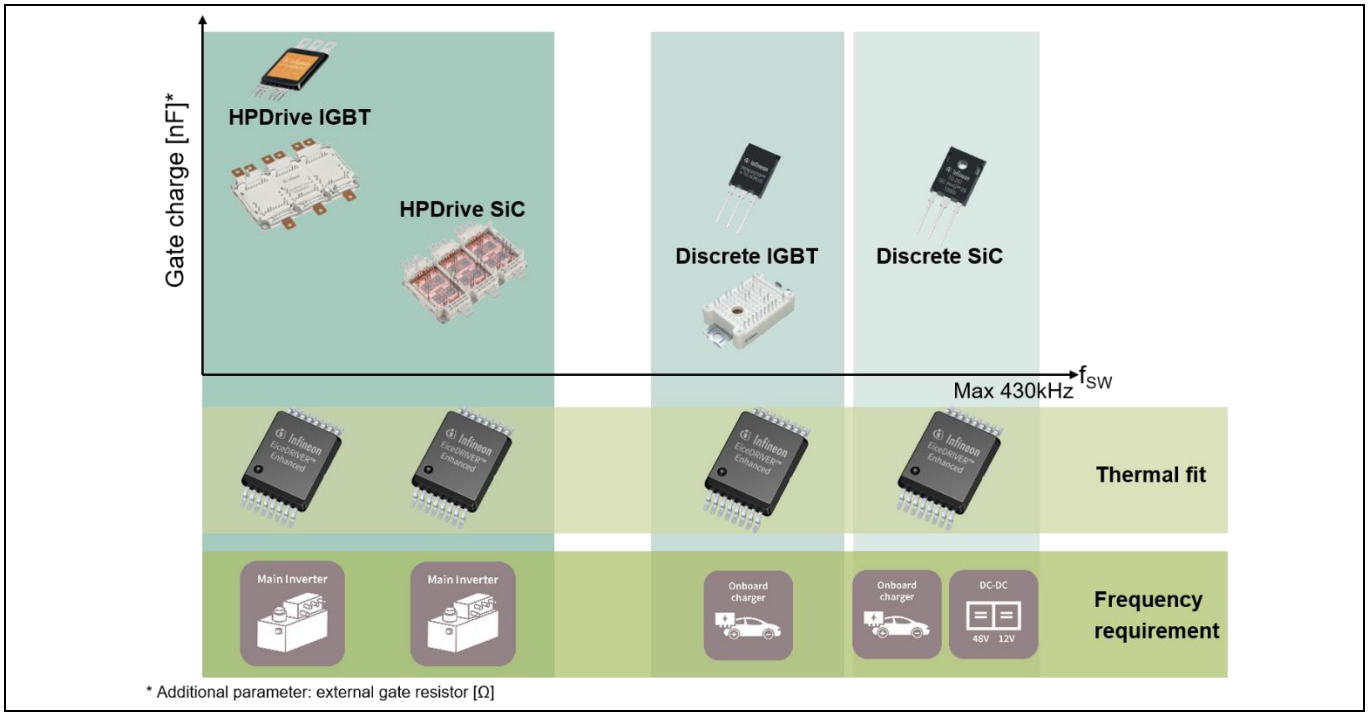



**Figure 4 Overview of the EiceDRIVER application possibilities**

*Note: Use the Calculator_EiceDRIVER for the estimation of the maximum switching frequency.*

With a low propagation delay of only 120 ns the EiceDRIVER™ offers a good fit for all HV applications in the car. For main inverter applications several additional diagnostic and functional features were integrated into this product.

When using the product the maximum thermal losses need to be calculated according to the application conditions. For calculating the maximum allowed switching frequency to stay below the specified junction temperature of 150°C, the formulas stated below can be used:

$$f_{SW} = \frac{P_{SW} \cdot (R_{DSON-OSLN} + R_{GATE})}{(V_{VCC2} - V_{VEE2})^2 \cdot C_{Gate} \cdot R_{DSON-OSLN}}$$

Max switching frequency

$$P_{SW} = \sum P_{dissipation} - P_{IDLE\_PRIM} - P_{IDLE\_SEC}$$

Switching losses

$$\sum P_{\text{dissipation}} = \frac{T_{\text{junction-max}} - T_{\text{ambient}}}{R_{\text{thjxx}}}$$

Power dissipation

$$P_{\text{IDLE\_PRIM}} = I_{\text{Qprim}} \cdot V_{\text{VCC1}},$$

Power dissipation @idle current

$$P_{\text{IDLE\_SEC}} = I_{\text{IdleVcc2}} \cdot V_{\text{VCC2}} + I_{\text{IdleVEE2}} \cdot V_{\text{VEE2}}$$

For these formulas a calculator is available; this can be downloaded in the given MYICP under the following link: Calculator_EiceDRIVER

## 2.3 Rise and fall time with 300 nF load

The key differentiators for a driver IC are the rise and fall time and the current capability of the output stage. In the following measurements and additional curves it can be concluded that:

- The rise time of the driver IC is fast and stable over the complete temperature range.
- The current capability enables a charging of a 300 nF capacitance without any additional booster stage in less than 3 µs up to 18 V.

This feature enables the customer to shrink the space of the gate driver IC to a small area on the PCB of the system because no additional booster stage with external components is needed.

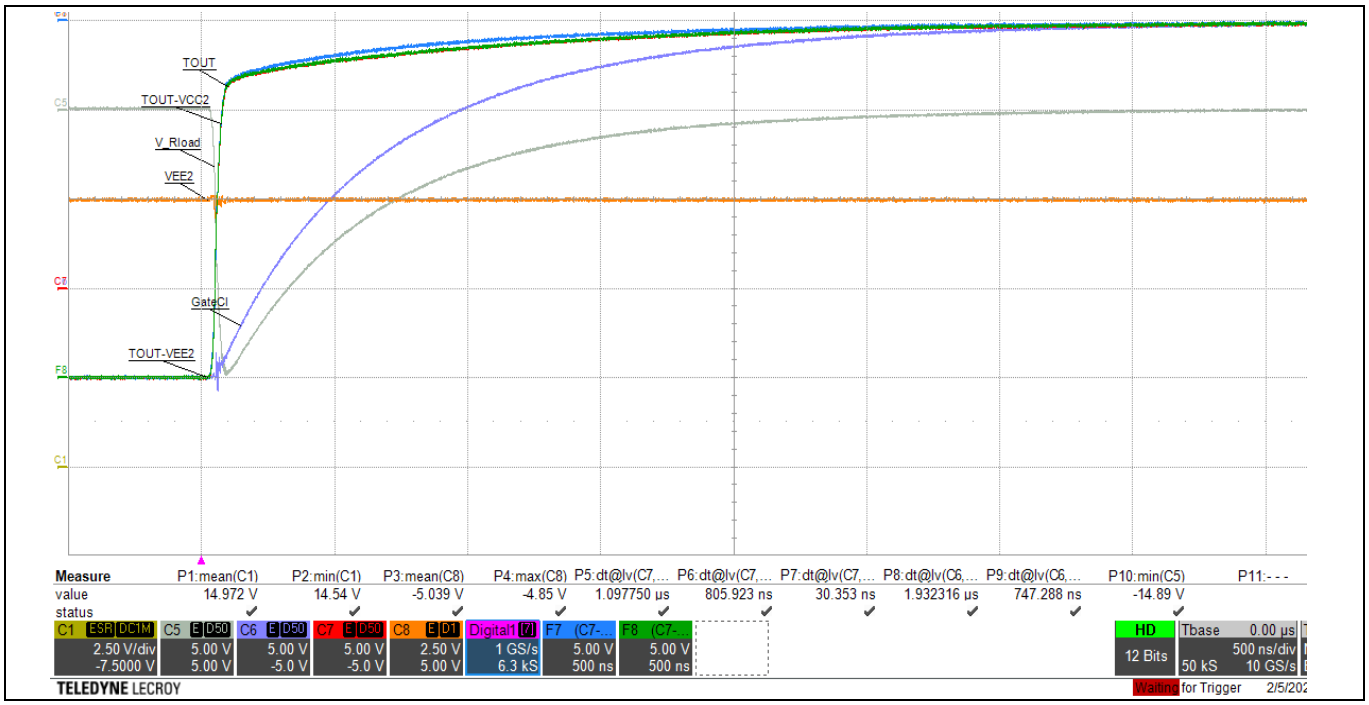



**Figure 5 Rise time with 300 nF load condition**

The same applies when sinking the charge of a 300 nF fully charged capacitor into the driver IC via the very low ohmic internal structure which is defined in the datasheet.

Furthermore it hast to be pointed out that at 2300 ns the active Miller clamping functionality is activated. This functionality is described in detail in Chapter 3.5.

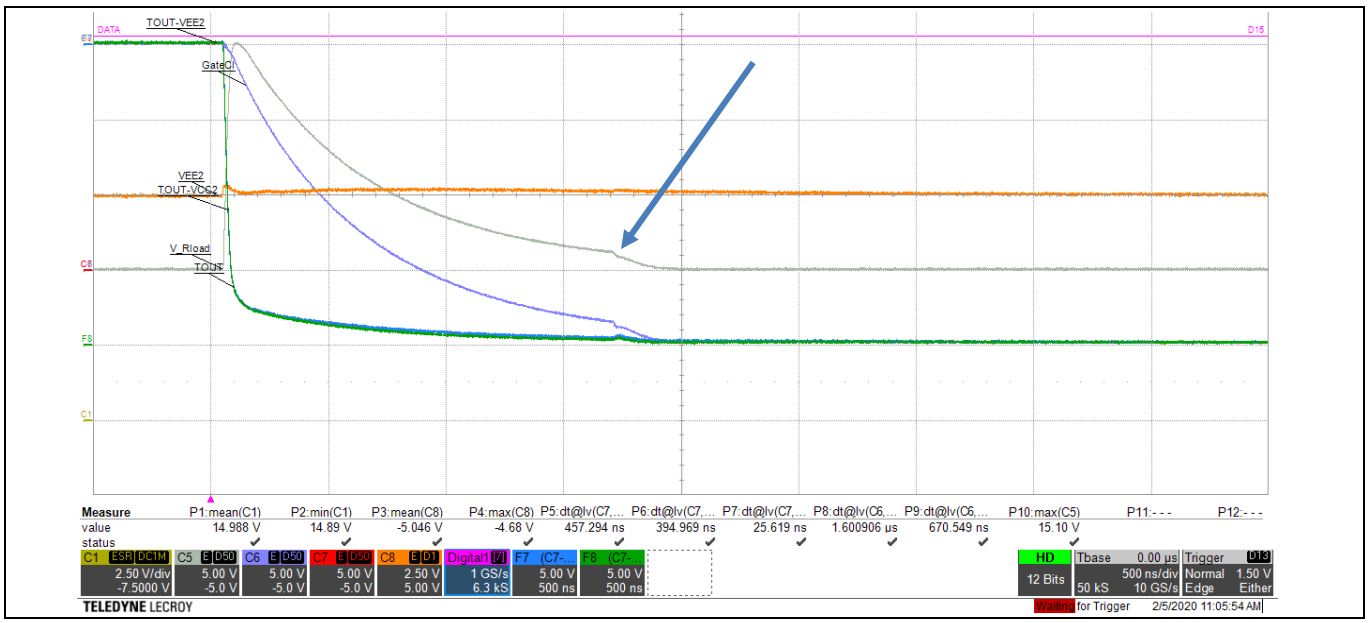



**Figure 6 Fall time with 300 nF load condition**

Combining this information into a detailed simulation of the output stage, the typical switching timing of the output stage in the complete specified temperature range can be extracted.

This is shown in Figure 7.

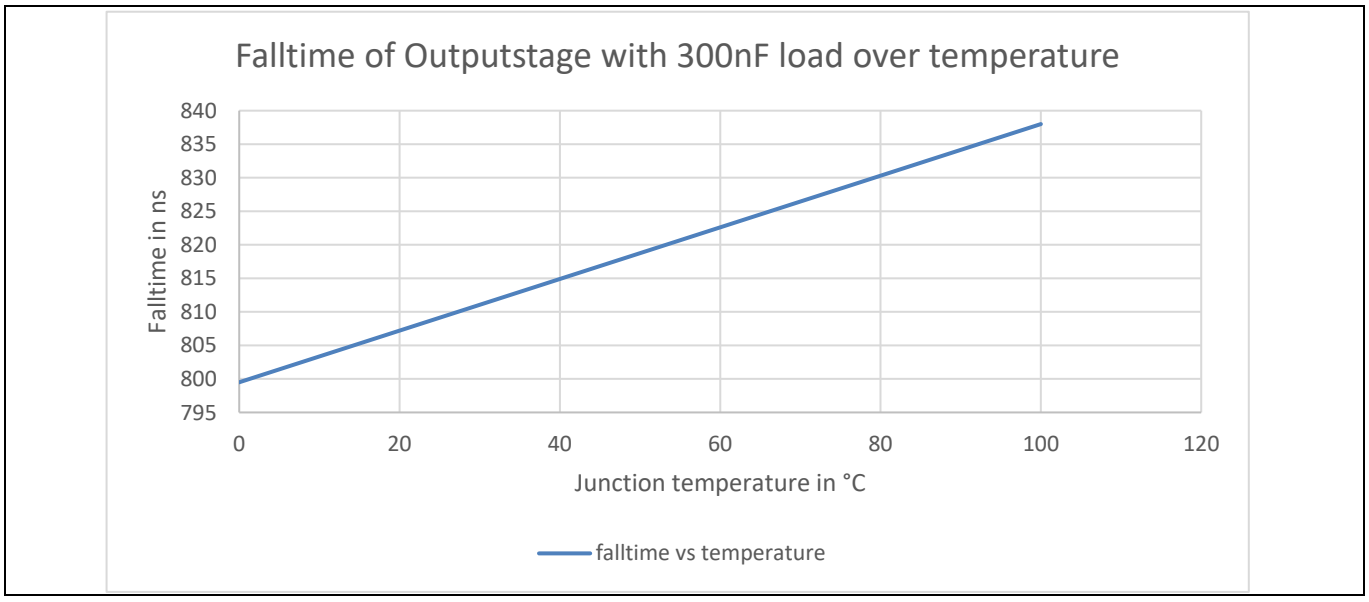



**Figure 7 Simulated fall time vs. temperature**

## 2.4 CMTI robustness increase

Through the benefits of using SiC MOSFETS in main inverter applications the switching frequency and the switching timings can be increased.

Therefore the common mode transient Immunity of all the driver ICs needs to be increased to make the system more robust in very fast switching applications.

### Definition of the CMTI

The CMTI is the maximum tolerable rate of rise and fall of the common mode voltage stated in V/ns. In addition, it can be distinguished between static and dynamic CMTI. The measurement principle of the CMTI test is shown in the following picture:

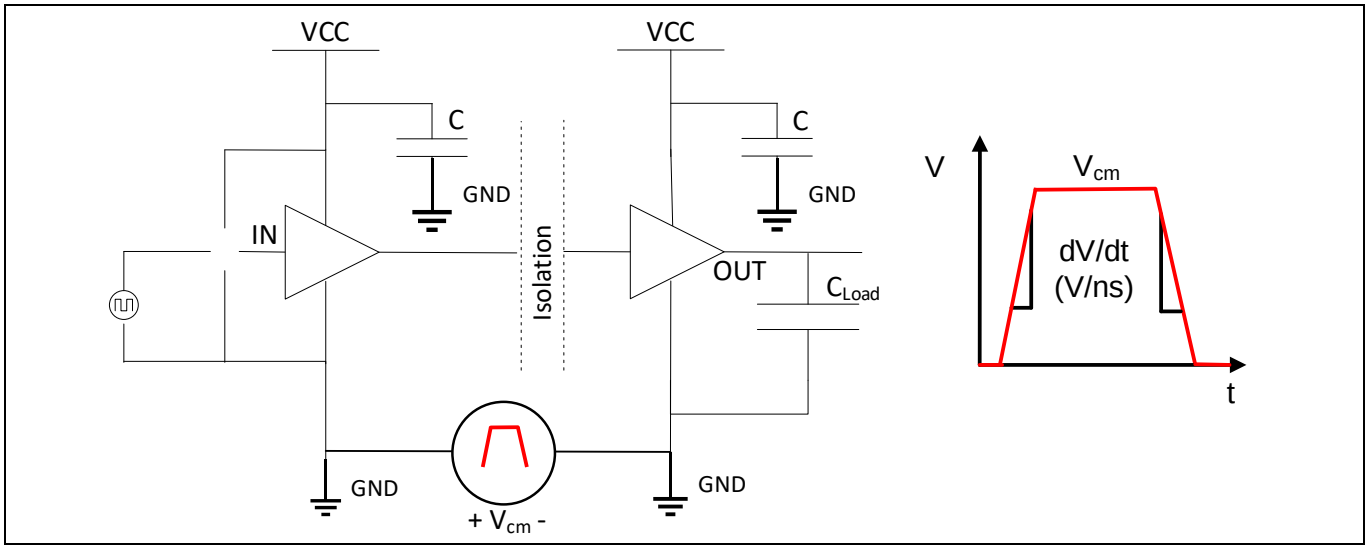



**Figure 8 Verification setup of the CMTI measurement**

### 1. Static CMTI

The static CMTI describes that in a static condition of the driver IC the output signals follows the input signal and is not disrupted due the fast voltages transients between primary and secondary GND.

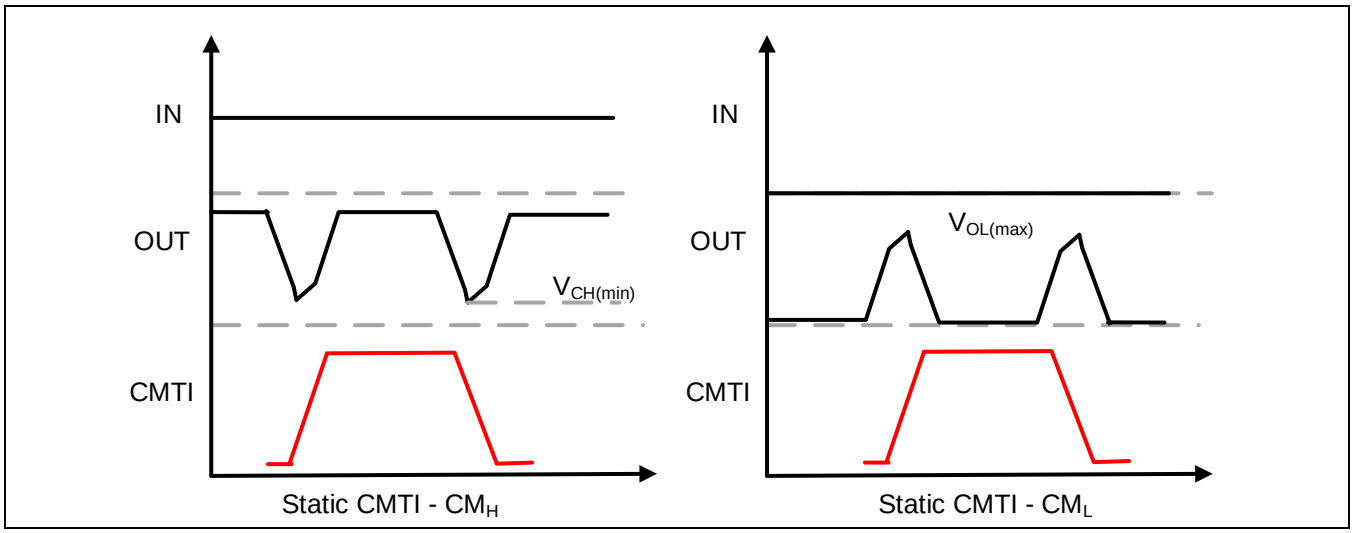



**Figure 9 Static CMTI**

## 2. Dynamic CMTI

The dynamic CMTI describes that in a switching condition of the gate driver IC the environment voltage transients between the primary and the secondary die do not lead to a disruption in communication such as a missing pulse, an upcoming undefined delay, a low or high error or a missing edge which causes the output signal to latch.

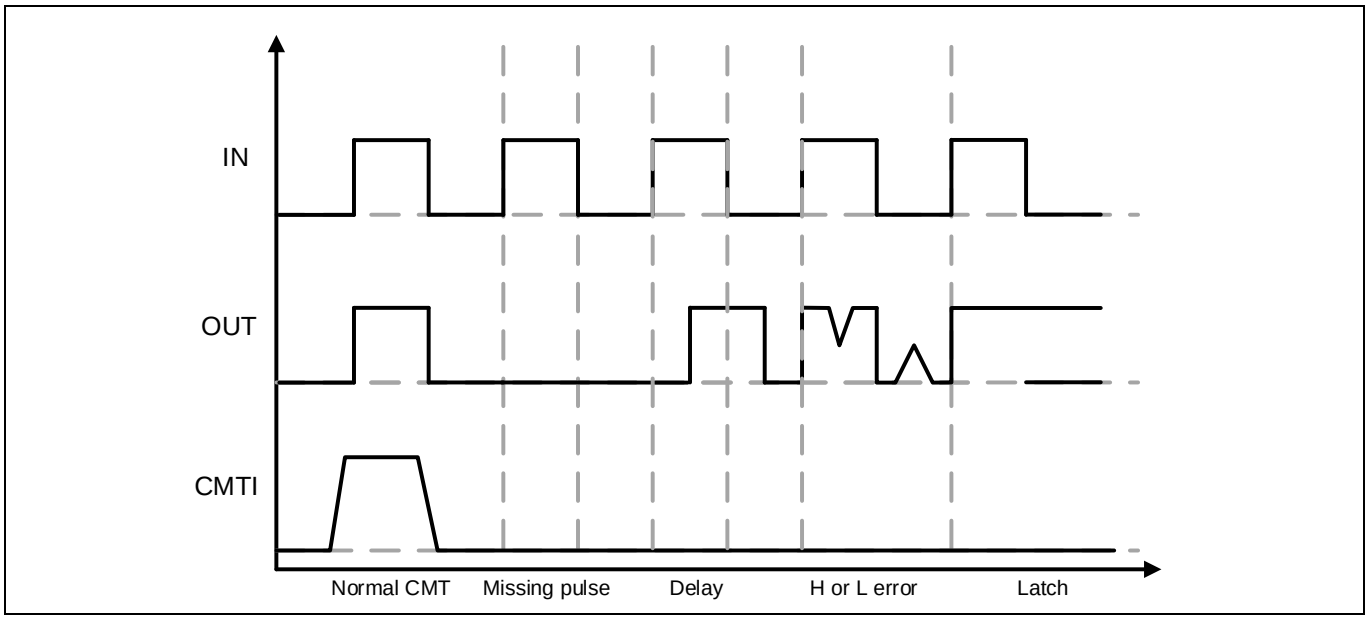



**Figure 10 Dynamic CMTI**

With the EiceDRIVER™ 1EDI302xAS and 1EDI303xAS family the CMTI robustness is increased to 150 V/ns from 100 V/ns in the 2nd Generation EiceDRIVER™ ICs. This allows to drive fast switching SiC MOSFETs.

Since CMTI is defined as a voltage slope, this immunity is independent of the DC-link voltage.

Figure 11 shows the robustness over the different applied voltages.

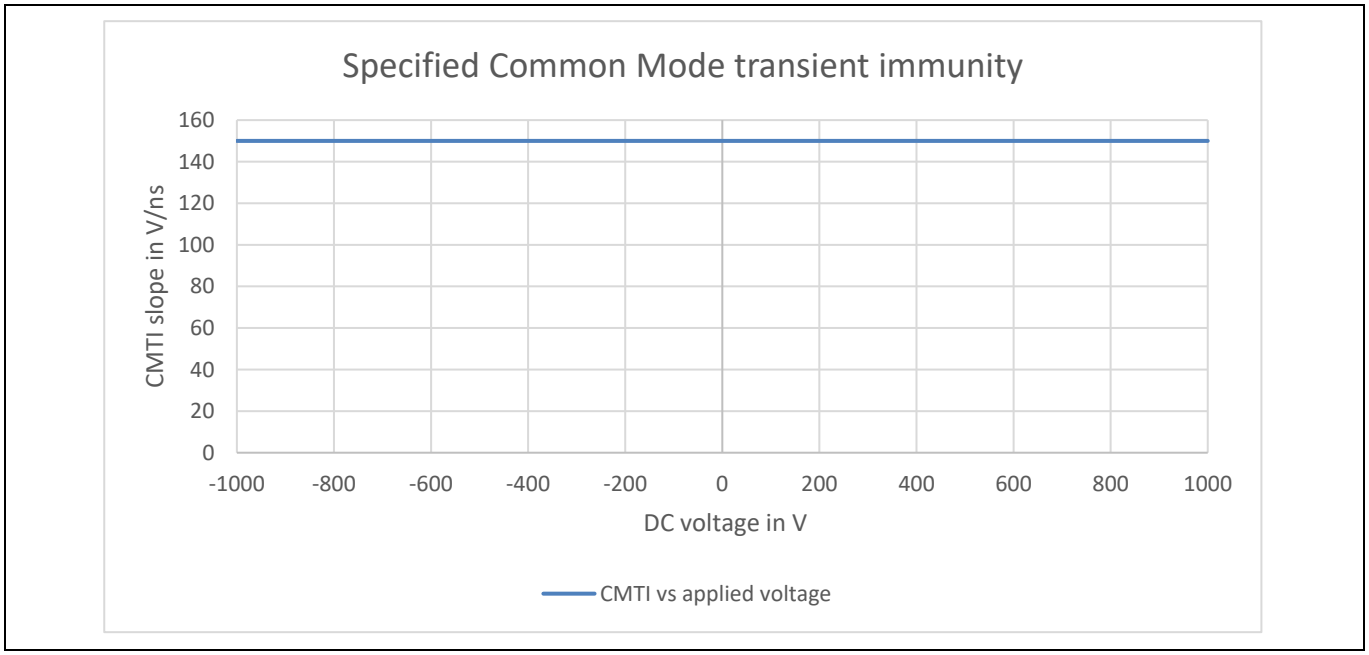



**Figure 11 CMTI robustness over different voltages**

# 3 Safety diagnosis and detection

In this chapter the safety features of the EiceDRIVER™ are stated and described in detail for the usage of this device in a main inverter application.

## 3.1 Desaturation detection of Silicon IGBTs

Desaturation is referred to the operating condition where the current conducted by the IGBT is controlled by the applied gate voltage. This causes a drastic increase in IGBT losses and can lead to the destruction of the IGBT. The EiceDRIVER™ implements a protection feature to prevent IGBT destruction in case of a desaturation event. According to the transfer characteristics, the bipolar transistor of the IGBT will desaturate at a defined current level which is dependent on the applied gate emitter voltage as shown in Figure 12. This desaturation characteristic of the IGBT leads to an increase of the voltage drop over collector/emitter channel as shown in the IGBT transfer characteristics. The increased collector/emitter voltage drop during a desaturation event up to the applied max voltage can be detected via the EiceDRIVER™'s DESAT pin:

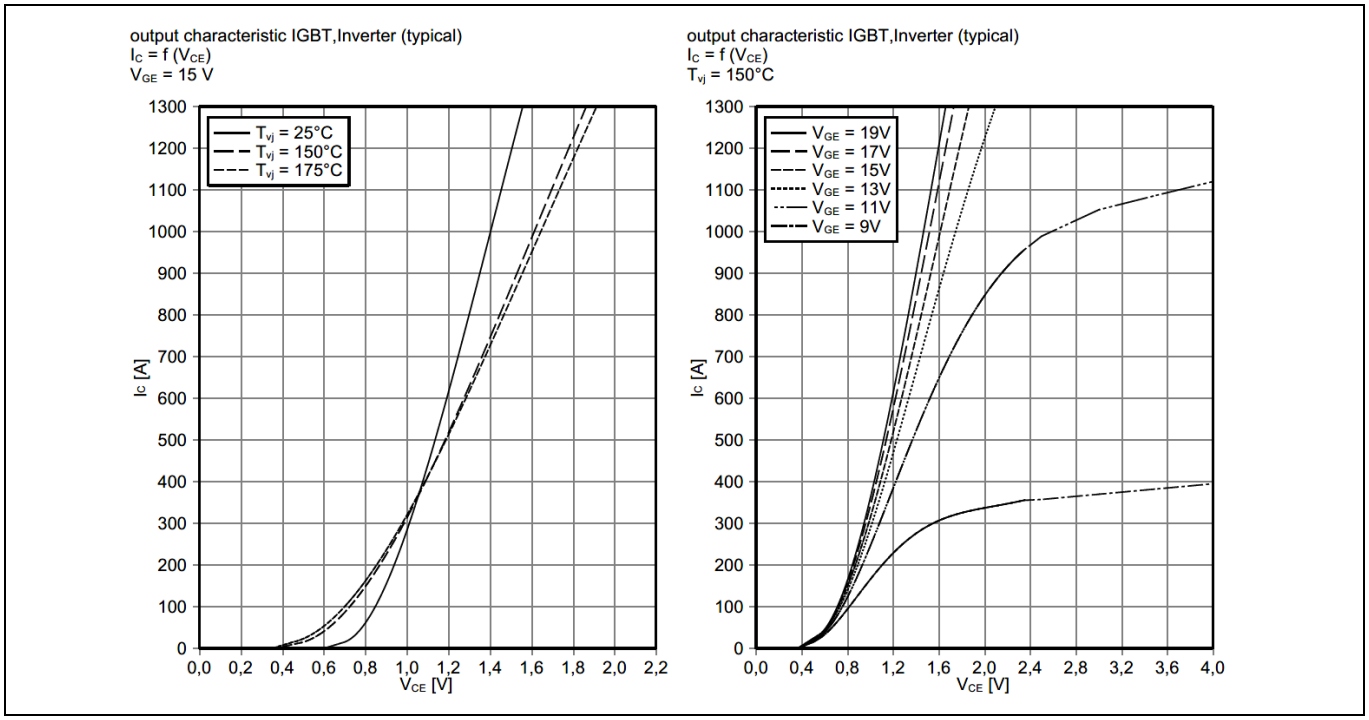



**Figure 12 Transfer characteristics of silicon IGBTs**

The detailed calculation procedure on how to configure the desaturation detection of an IGBT is explained in the following chapter.

### 3.1.1 DESAT IGBT external components calculation

*Note: Use the Calculator_EiceDRIVER for the estimation of the DESAT IGBT external components.*

The connection of the DESAT pin via three external components to the SiC/ IGBT module provides the following three functionalities:

1. A resistor with a minimum value of 1 kΩ limits the current flowing through the DESAT pin.
2. An HV-diode protects the DESAT pin from high-voltages when the IGBT/ SiC MOSFET is turned off.
3. A capacitor is used to define a filtering time together with the internal current source and to increase the robustness against false triggering of DESAT for short term voltage peaks during runtime.

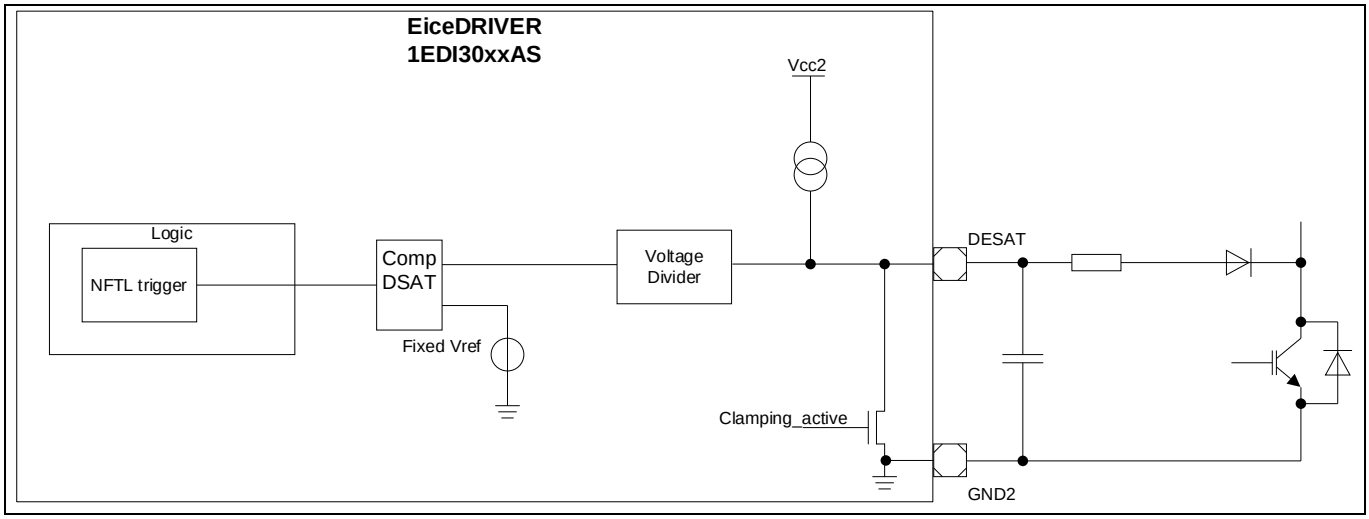



**Figure 13 Internal and external components DESAT detection**

#### Sample calculation for the capacity

Typical values of the IGBT module are shown in Table 2.

**Table 2 Typical values of the IGBT module**

| Description | IGBT |
|---|---|
| Falltime from VGS = 15 V to VGS = 0 V/8 V | ~2 µs |
| Short circuit capability at 400 Vdc | <3 µs |
| External filter/blanking time | 1 µs |
| DESAT threshold voltage | 9 V |

Based on the typical values stated above, the following capacitor values are recommended to be used.

#### Calculation of DESAT filter capacitance

$I_{\mathrm{DESAT,th}} = 500\ \mu\mathrm{A}$ typical; $V_{\mathrm{DESAT,IGBT}} = 9\ \mathrm{V}$ typical; $t_{\mathrm{Filter}} \leq 1\ \mu s$

$$C_{\mathrm{DESAT,IGBT}} = \frac{I_{\mathrm{DESAT}} \cdot t_{\mathrm{FILTER}}}{V_{\mathrm{DESAT,IGBT}}} \leq 56\ pF$$

### Current limitation to the DESAT pin via $R_{Desat}$

During the switching period the body diode can forward conduct current. In this condition the voltage on the DESAT pin will be negative with respect to GND2. The resistor at the desaturation Pin is required to limit the current flowing from GND2 through the internal clamping transistor. The resistor needs to be at least 1 kΩ.

### DESAT diode

The DESAT diode must be chosen carefully, this diode has to withstand reverse peak currents of up to 1 A depending of the DC bus voltage. Apart from this it must not be too large and limit the injected stress to the DESAT and OCP circuitry due to its self-induced reverse recovery charge (Qrr).

Usually a 600 V/1 A diode or a 1200 V/1 A diode is the right choice for the application.

## 3.2 Overcurrent detection of SiC MOSFETs via the DESAT pin

The EiceDRIVER™'s DESAT also offers the possibility to detect an increased voltage drop due to an overcurrent in the SiC MOSFET. According to the output characteristics the voltage drop over the drain/source channel is proportional to the current through the channel.

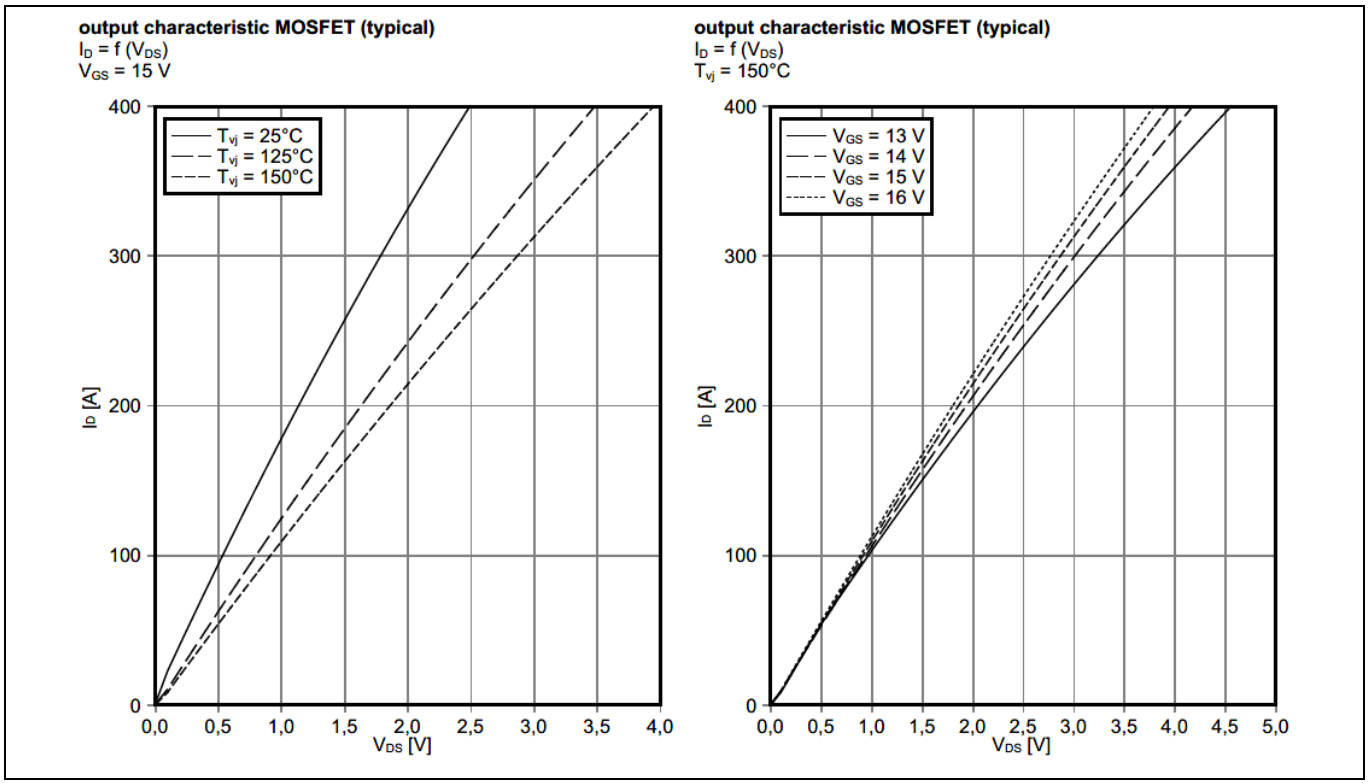



**Figure 14 Characteristics diagrams SiC MOSFETs**

The desaturation level of the SiC MOSFET is much higher than the level of an IGBT when assuming an identical chip size for both components. Therefore the detection of this failure in the main inverter system needs to be placed at a lower threshold level of the internal desaturation comparator.

The EiceDRIVER™ offers an optimized system solution with defined thresholds and timings for dedicated usage of SiC MOSFETs in the main inverter application.

### 3.2.1 DESAT SiC external components calculation

*Note: Use the Calculator_EiceDRIVER for the estimation of the DESAT SiC external components.*

The schematics of the internal and external components are the same as for the IGBT configuration (see Figure 13). The values of the components need to be calculated according the application conditions.

**Sample calculation for the capacity**

Typical values of the SiC MOSFET module are shown in the following table.

**Table 3 Typical values of the SiC MOSFET module**

| Power semiconductor technology | SiC MOSFET |
|---|---|
| Falltime from VGS = 18 V to VGS = 0 V/5 V | 1.2 µs |
| Short circuit capability at 600 Vdc | < 2 µs |
| External filter time | ~800 ns |
| DESAT threshold voltage | Up to 6 V |

Based on the typical values the following capacitor values are recommend to be used.

**Internal current source at DESAT pin**

$I_{\mathrm{DESAT}} = 500\ \mu\mathrm{A}$ typically

**DESAT filter SiC**

$I_{\mathrm{DESAT,th}} = 500\ \mu\mathrm{A}$ typical; $V_{\mathrm{DESAT,SiC}} = 6\ \mathrm{V}$ typical; $t_{\mathrm{Filter}} \leq 800\ ns$

$$C_{\mathrm{DESAT,SiC}} = \frac{I_{\mathrm{DESAT}} \cdot t_{\mathrm{FILTER}}}{V_{\mathrm{DESAT,SiC}}} \leq 67\ pF$$

**Current limitation to the DESAT pin via $R_{\mathrm{Desat}}$**

The resistance on the Pin DESAT needs to be at least 1 kΩ to prevent destruction inside the driver IC.

**DESAT diode**

The DESAT diode must be chosen carefully; this diode has to withstand reverse peak currents of up to 1 A depending of the DC bus voltage. Furthermore it must not be too large and limit the injected stress to the DESAT and OCP circuitry due to its self-induced reverse recovery charge (Qrr).

Usually a 600 V/1 A diode or a 1200 V/1 A diode is the right choice for the application.

## 3.3 DESAT below ground

Switching inductive loads causes large instantaneous forward voltage transients across the freewheeling diodes of an IGBT. These transients result in large negative voltage spikes on the DESAT pin, which can lead to substantial current flow out of the DESAT pin. To limit this current below potentially damaging levels a 1 kΩ resistor must be connected in series with the HV-DESAT diode.

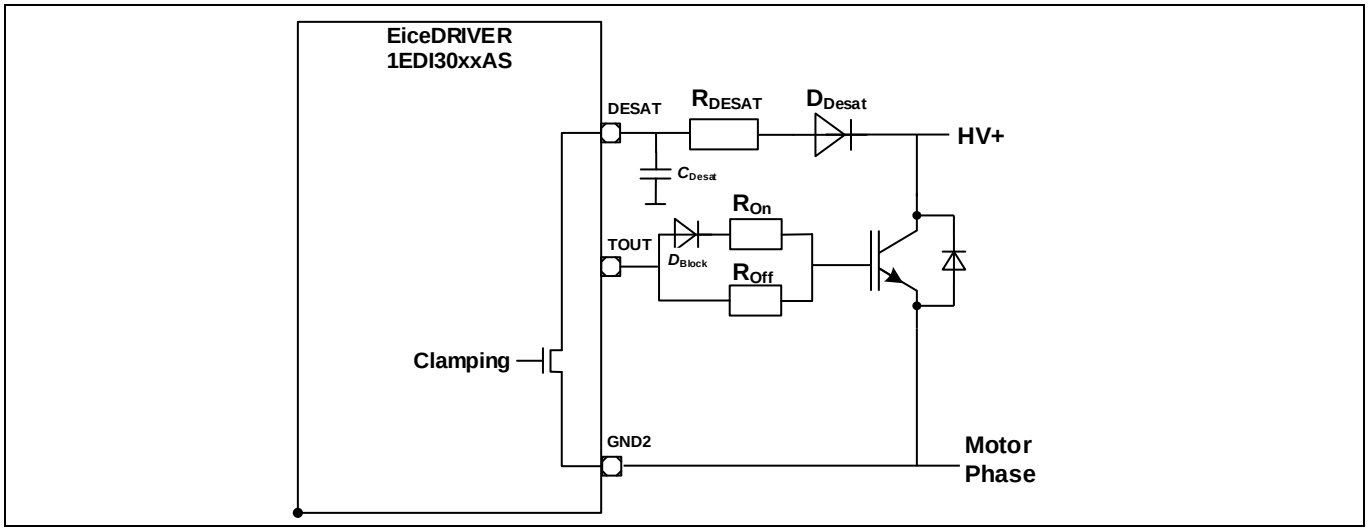



**Figure 15 DESAT below ground schematic**

The robustness of the DESAT pin below ground was tested in Figure 16. In order to ensure the correct functionality in this case an energy loss of the internal clamping transistor during a switching period below ground (reverse bias) needs to be at:

$$E_{\mathrm{LOSS,DESAT}} \leq V_{\mathrm{DESAT,diode}} \cdot I_{\mathrm{DESAT}} \cdot t_{\mathrm{TOUT,ON}} = 700\,mV \cdot 20\,mA \cdot \mu s$$

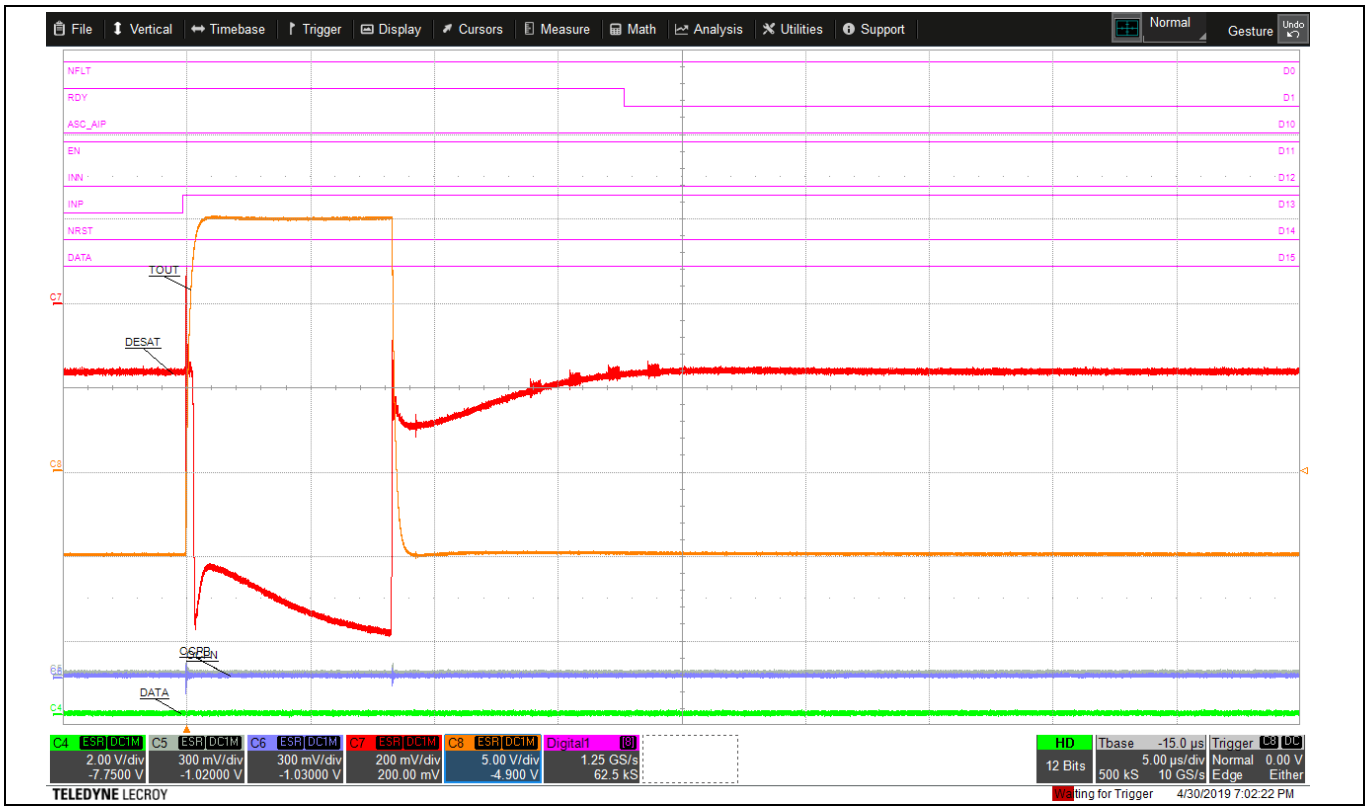



**Figure 16 DESAT below ground: Force –2 V/20 mA at DESAT pin**

## 3.4 Overcurrent protection of a power semiconductor

The EiceDRIVER™ 1EDI302xAS and 1EDI303xAS family offers the possibility to check the current through the power semiconductor via a comparator on the OCP pin. A fraction of the power semiconductor current is usually provided via a current mirror and converted to a voltage on the OCP pin with the means of a sense resistor.

If this current mirror is not available, the comparator inside the OCP pin can alternatively be used as a redundant monitoring of the desaturation voltage.

### 3.4.1 Using a current mirror of a power semiconductor module

If a current mirror is available in the power module, the necessary external sense resistor can be calculated in the following way:

The predefined value of the internal comparator is defined according the variants in the upcoming table:

**Table 4 Predefined values of the internal comparator**

| Name | Description and features | Predefined typical OCP threshold |
|---|---|---|
| 1EDI3020AS | Driver IGBT with integrated ADC for temperature | 300 mV |
| 1EDI3021AS | Driver for IGBT with integrated ASC | 300 mV |
| 1EDI3023AS | Driver for IGBT with integrated ADC for NTC and DC-link | 300 mV |
| 1EDI3030AS | Driver for SiC with integrated ADC for temperature | 600 mV |
| 1EDI3031AS | Driver for SiC with integrated ASC | 600 mV |
| 1EDI3033AS | Driver for SiC with integrated ADC for NTC and DC-link | 600 mV |

A current mirror pin is available in Infineon's HybridPACK™ DSC IGBT module. This pin can be monitored via the overcurrent protection functionality of the device.

**6 Current Sensor**

| Parameter | Conditions | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Output voltage | $V_{CE}$ = 2.35 V, $I_C$ = 800 A<br>$R_{sense}$ = 1.60 Ω, $T_{vj}$ = 25°C<br>VGE = 15 V | $V_{sense}$ | | 0.64 | | V |

**Figure 17 Information on integrated current sensor of power module**

The following calculation example explains how to design the overcurrent functionality.

The detection threshold is defined to be 300 mV and 600 mV. If the overcurrent limit is set inside the application, the resistor needs to be calculated according the following graph.

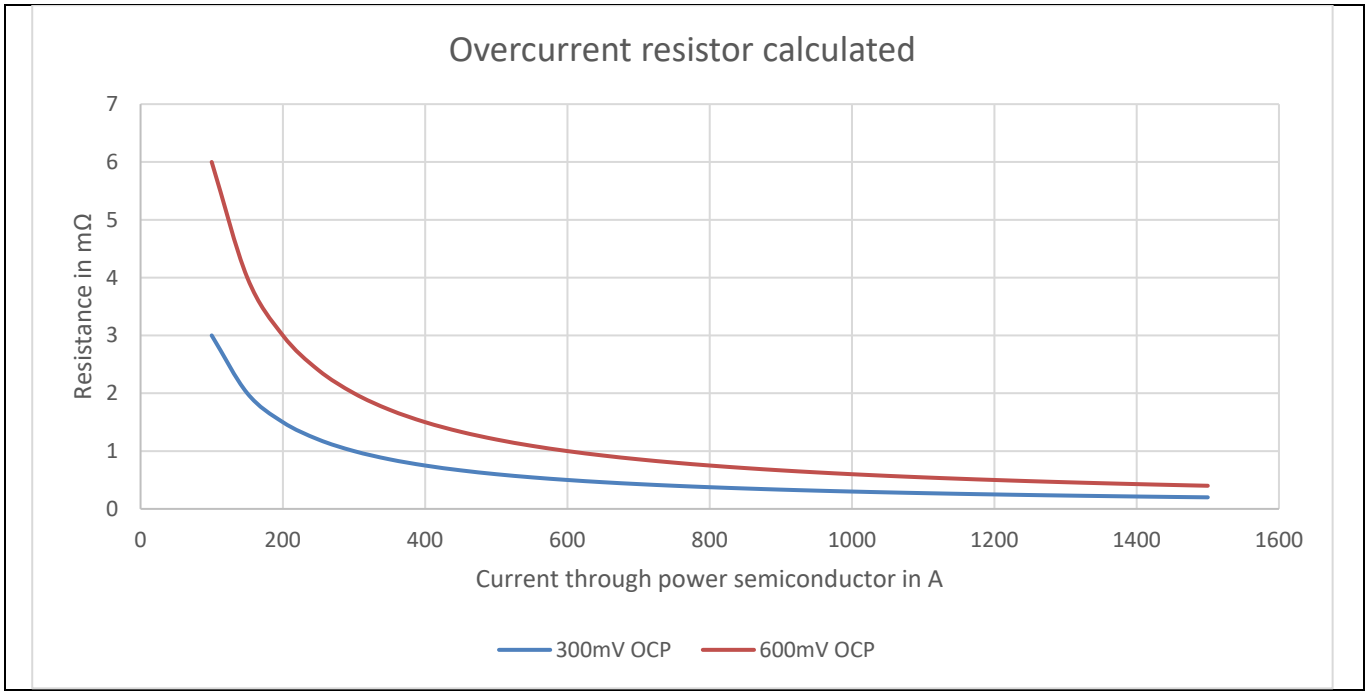



**Figure 18 Calculated typical resistor for overcurrent detection**

### 3.4.2 Using the OCP pin for redundant DESAT monitoring

*Note: Use the Calculator_EiceDRIVER for the estimation of the DESAT via OCP pin calculation.*

Many SiC modules do not offer a current mirror pin in contrast to what can be found in many IGBT modules on the market. In order to make use of the fast reaction of the over current protection, a circuitry for desaturation protection via the OCP pin is proposed in Figure 19.

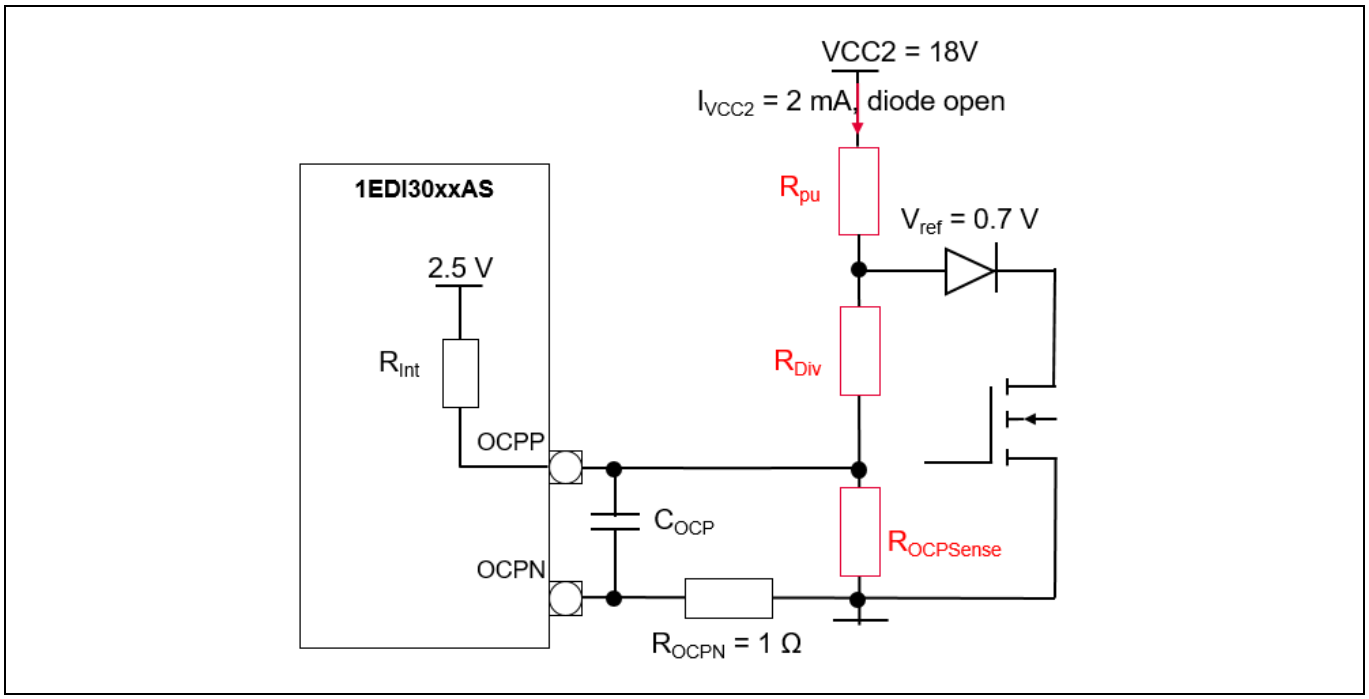


**Figure 19 Desaturation protection circuit via OCP pin**

The DESAT threshold can be configured according to application needs.

The required component calculations are shown in the following section:

### Resistor network calculation

**Input parameters:** $V_{DESAT}$ = 6.0 V, $V_{Ref}$, diode = 0.7 V, $I_{VCC2}$ = 2 mA, $V_{CC2}$ = 18 V, $V_{OCP,th}$ = 300 mV and $R_{OCPN}$ = 1 Ω

First, a margin for the OCP threshold trigger is defined as 1.6:

$$V_{\mathrm{OCP,max}} = V_{\mathrm{OCP,th}} \cdot 1.6 = 480\ mV$$

OCP threshold margin

The resistors are calculated as follows:

$$R_{\mathrm{Pu}} = \frac{V_{\mathrm{VCC2}} - V_{\mathrm{Ref}} - V_{\mathrm{DESAT}}}{I_{\mathrm{VCC2}}} = 5.65\ k\Omega$$

Pull-up resistor

$$R_{\mathrm{Div}} = \frac{V_{\mathrm{DESAT}} + V_{\mathrm{Ref}} - V_{\mathrm{OCP,max}}}{I_{\mathrm{VCC2}}} = 3.11\ k\Omega$$

Voltage divider resistor

$$R_{\mathrm{OCPSense}} = \frac{V_{\mathrm{OCP,max}}}{I_{\mathrm{VCC2}}} = 240\ \Omega$$

Sense resistor

### Equivalent voltage generator and resistor

Once the resistances are calculated, the following equivalent voltage generator and equivalent resistance to charge the capacity $C_{\mathrm{OCP}}$ can be defined:

$$V_{eq} = \frac{V_{cc2} \cdot R_{\mathrm{OCPSense}}}{R_{\mathrm{sense}} + R_{\mathrm{Div}} + R_{\mathrm{pu}}} = 0.48\ V$$

equivalent voltage generator

$$R_{eq} = \frac{R_{\mathrm{OCPSense}} \cdot (R_{\mathrm{pu}} + R_{\mathrm{Div}})}{R_{\mathrm{sense}} + R_{\mathrm{Div}} + R_{\mathrm{pu}}} = 233.6\ \Omega$$

equivalent resistance

### OCP filter capacitance calculation

To calculate the OCP filter capacitance following additional values are required.

**Input parameters:** $V_{DS,\,op}$ = 0.5 (Voltage drop during operating mode over DS of the SiC) $T_{\mathrm{Filter}}$ = 1.5 µs

$$V_{OCP,\,op} = \frac{R_{\mathrm{OCPsense}} \cdot (V_{\mathrm{DS,op}} + V_{\mathrm{ref}})}{R_{\mathrm{OCPsense}} + R_{\mathrm{Div}}} = 0.086\ V$$

Voltage across Cocp during normal operation

Plugin in all the values yields the capacity to choose for the desired filtering time.

$$C_{\mathrm{OCP}} = \frac{T_{\mathrm{Filter}}}{R_{\mathrm{eq}}} \cdot \frac{1}{ln\left(\frac{V_{\mathrm{eq}} - V_{\mathrm{OCP,op}}}{V_{\mathrm{eq}} - V_{\mathrm{OCP,th}}}\right)} = 8.2\ nF$$

Cocp capacity

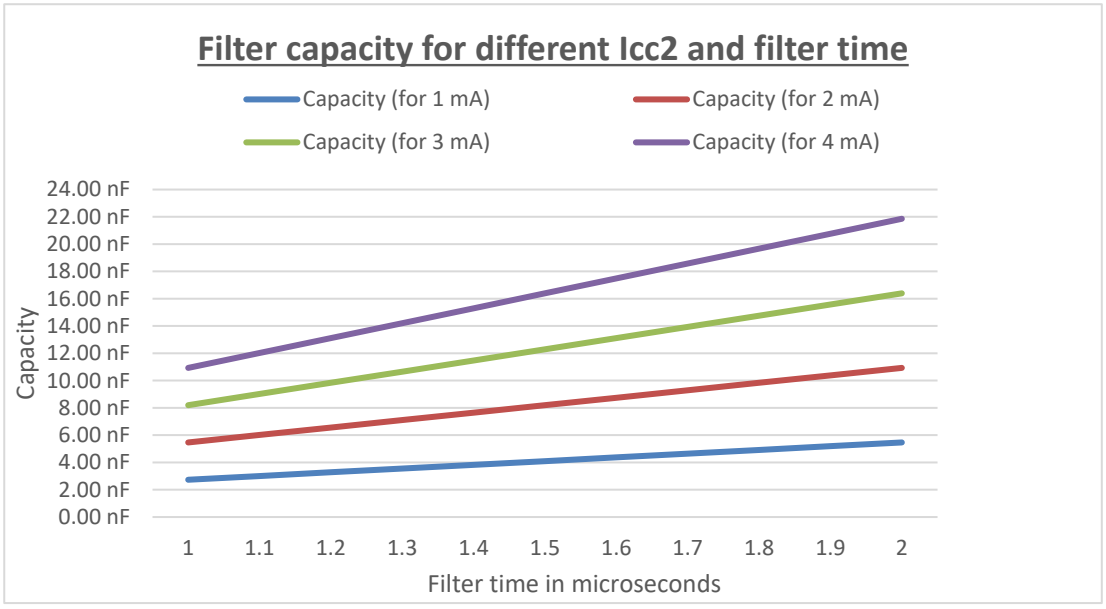



**Figure 20 Filter capacities for different Icc2 and filter time**

**Table 5 Filter capacities for different Icc2 and filter time**

| Tfil (in Microseconds) | 1 | 1,2 | 1,4 | 1,6 | 1,8 | 2 |
|---|---|---|---|---|---|---|
| Capacity (for 1 mA) | 2,73 nf | 3,28 nf | 3,82 nf | 4,37 nf | 4,92 nf | 5,46 nf |
| Capacity (for 2 mA) | 5,46 nf | 6,56 nf | 7,65 nf | 8,74 nf | 9,84 nf | 10,93 nf |
| Capacity (for 3 mA) | 8,20 nf | 9,84 nf | 11,47 nf | 13,11 nf | 14,75 nf | 16,39 nf |
| Capacity (for 4 mA) | 10,93 nf | 13,11 nf | 15,30 nf | 17,48 nf | 19,67 nf | 21,86 nf |

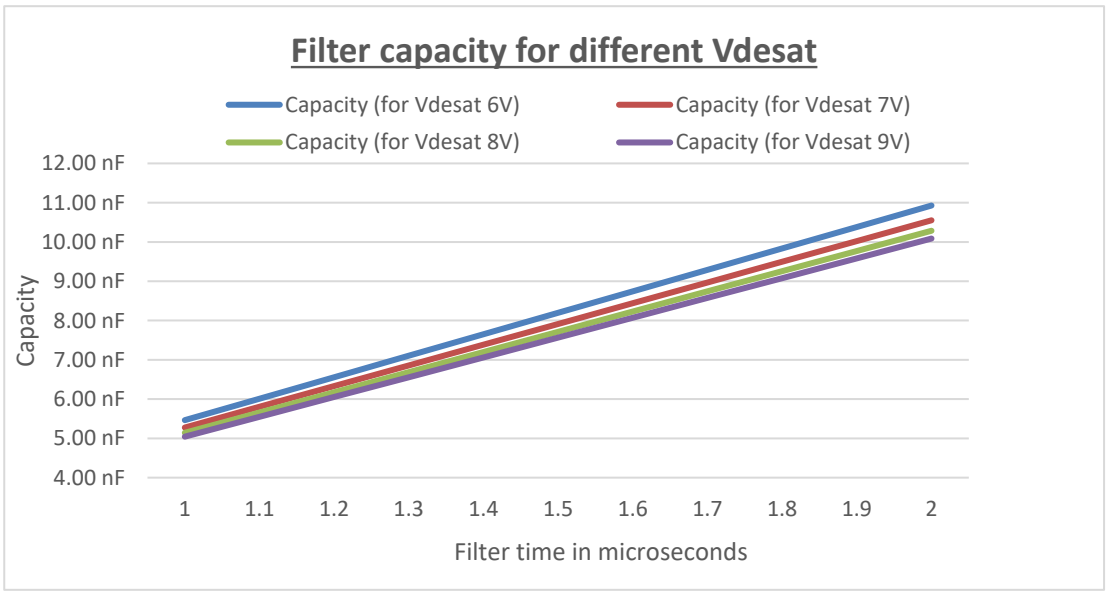



**Figure 21 Filter capacities for different DESAT voltages**

**Table 6 Filter capacities for different DESAT voltages**

| Tfil (in Microseconds) | 1 | 1,2 | 1,4 | 1,6 | 1,8 | 2 |
|---|---|---|---|---|---|---|
| Capacity (for Vdesat 6 V) | 5,46 nf | 6,56 nf | 7,65 nf | 8,74 nf | 9,84 nf | 10,93 nf |
| Capacity (for Vdesat 7 V) | 5,28 nf | 6,33 nf | 7,39 nf | 8,44 nf | 9,50 nf | 10,55 nf |
| Capacity (for Vdesat 8 V) | 5,14 nf | 6,17 nf | 7,20 nf | 8,23 nf | 9,26 nf | 10,29 nf |
| Capacity (for Vdesat 9 V) | 5,04 nf | 6,05 nf | 7,06 nf | 8,07 nf | 9,08 nf | 10,09 nf |

#### Advantage of DESAT detection via OCP

The detection of the failure in the power semiconductor via overcurrent protection provides the following main advantages in the main inverter application. The overcurrent protection is a complete redundant functionality of the driver IC and offers the customer a higher coverage of system failures to achieve the overall required safety goals metrics.

### 3.4.3 Using the OCP pin to trigger a safe turn off from the secondary side

The overcurrent protection pin of the EiceDRIVER™ can also be used to trigger a safe turn off from the secondary side via the OCP pin, when the OCP pin is not connected to the current mirror of the power semiconductor. An example is shown in Figure 22. The applied safe state logic needs to switch on the transistor “Q1” during normal operation. Once “Q1” is turned on, the current flow through R1 can be used to trigger the OCP and provoke a safe turn off. The resistor R1 has to be scaled accordingly using Ohm’s law, so that the voltage visible between OCPP and OCPN exceeds the internal OCP protection comparator threshold. The following two level turn off is described in more detail in Chapter 3.10.

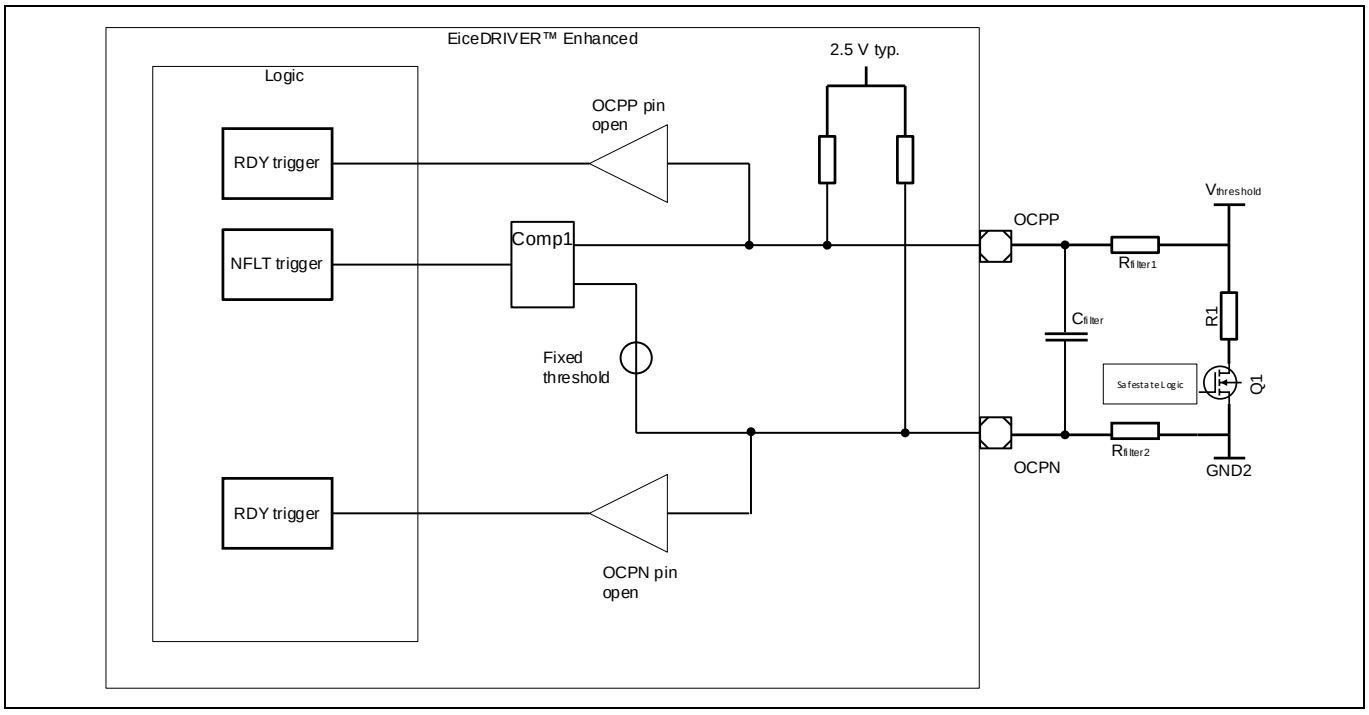



**Figure 22 Schematics of a safe turn off trigger from the secondary side**

A filter symmetrical filter consisting of $C_{filter}$, $R_{filter1}$ and $R_{filter2}$ can be added to suppress the influence of external disturbance or noise.

The overcurrent protection also features a so-called “pin open detection”, which is also shown in Figure 22. The “pin open detection” issues a normal turn-off of the EiceDRIVER™ if the circuit connection to one or both of the OCP pins is interrupted. In case of such an event either pin is pulled up to an internal voltage of typically 2.5 V. This voltage is then detected by the OCPP or OCPN pin open detection comparators. Please refer to the datasheet for detailed information about the threshold.

If a hard switch-off from the secondary side is needed the voltage on the OCP Pin needs to be above the defined pin open detection threshold written in the according datasheet. If a pin open is detected via the gate driver the overall system reaction is defined as a hard switch-off event.

## 3.5 Active Miller clamping

In a switching event of a halfbdrige topology the Miller capacitor between Gate & Drain / Gate & Collector will be discharged. This discharge of the capacitor leads to a current through the gate’s OFF resistors if no additional clamping structure is available. This voltage drop over the resistor generates a parasitic turn ON of the respective power semiconductor if it reaches the turn-on threshold voltage.

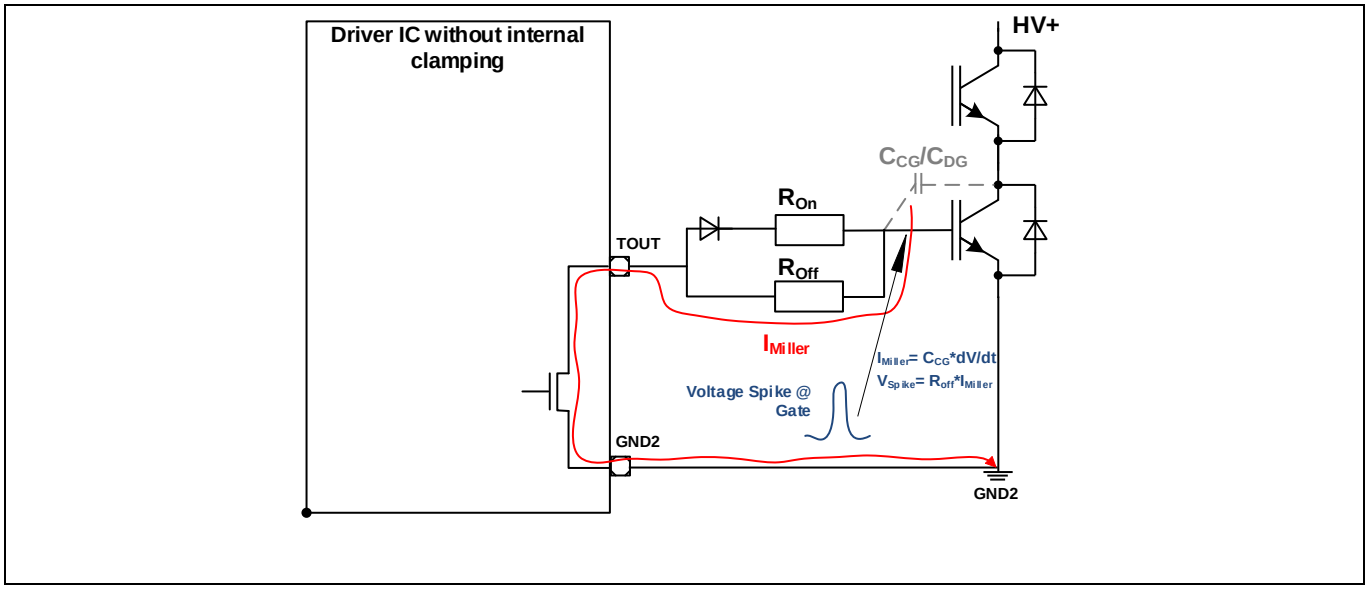



**Figure 23 Explanation of parasitic turn ON due to Miller current in halfbridge topologies**

In the EiceDRIVER™ there is a very low ohmic internal additional clamping structure implemented to keep the device in an OFF state when the complementary driver IC switches in ON transition with a very fast dVce/dt, which causes a current which is flowing into the driver IC. This low ohmic clamping structure can be seen in the following measurement result:

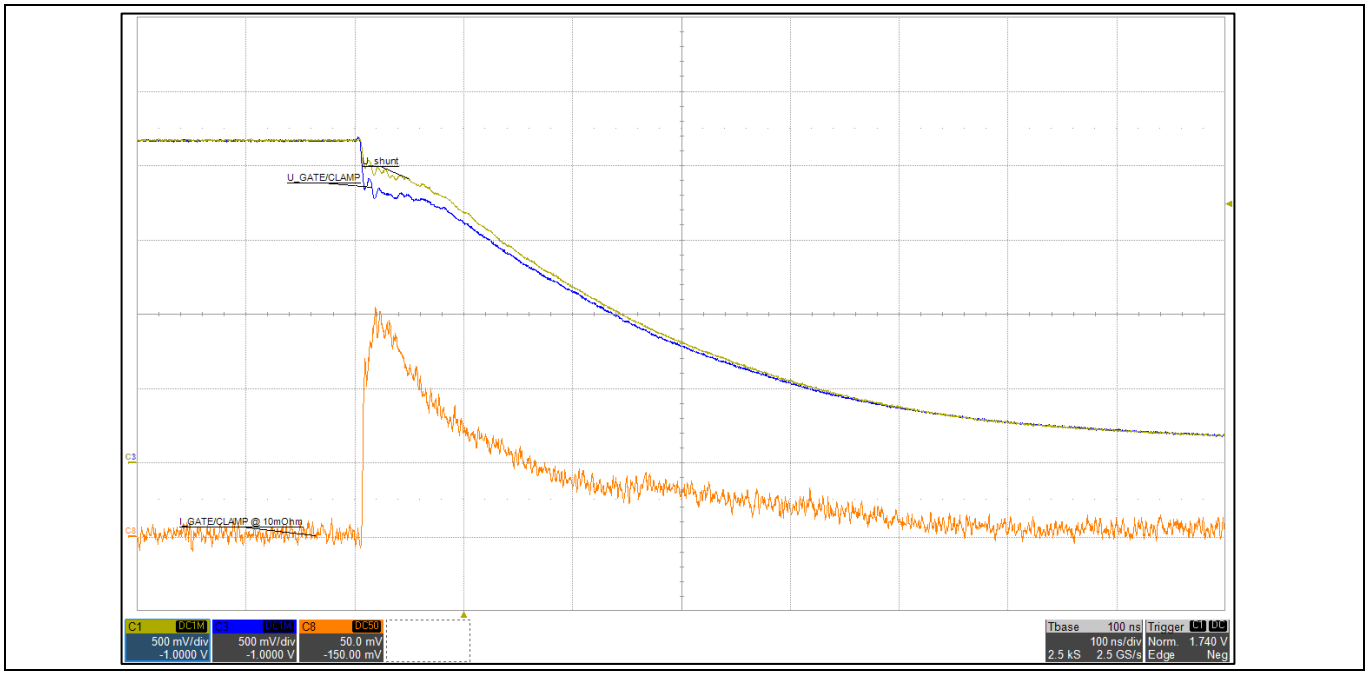



**Figure 24 Measurement result of active miller clamping structure**

In the picture above it is shown that the current consumption of the EiceDRIVER™ clamping circuitry can reach up to 15 A as shown in channel 8. The current is indirectly measured with a resistor. This strong clamping structure enables the customer to keep the gate in a defined condition even if the miller current is rising.

The active miller clamping structure is based on the negative switching voltage Vee2 and gets active according to the defined threshold inside the datasheet.

## 3.6 Passive gate clamping

In case of a missing supply on Vcc2 the gate voltage is clamped passively to the Vee2 potential. This feature ensures that the state of the gate of the MOSFET/IGBT is OFF in case of a missing supply of the secondary die.

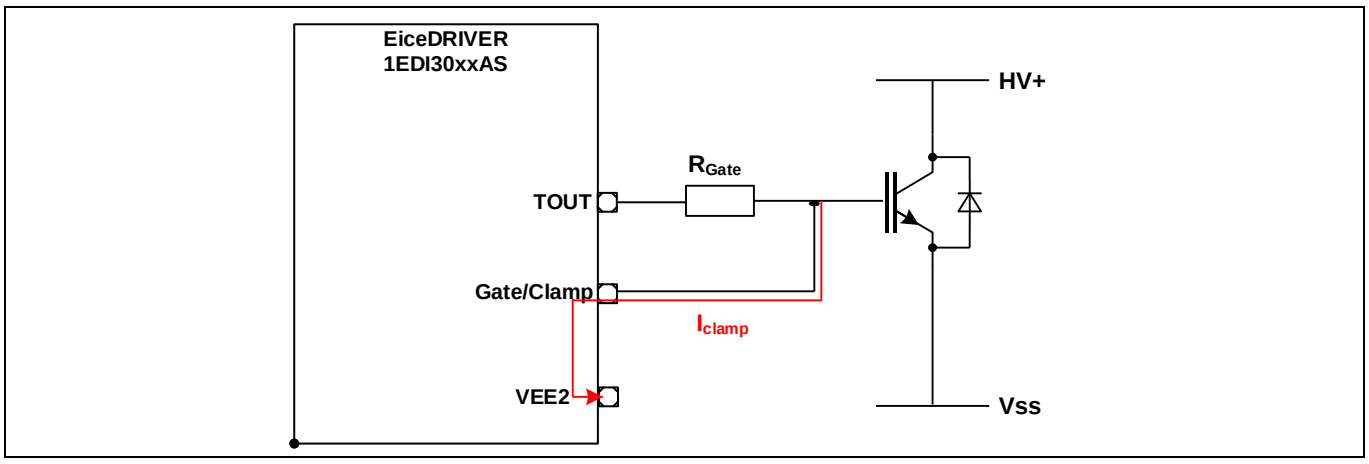



**Figure 25 Passive gate clamping overview**

## 3.7 Static gate monitoring

The gate monitoring is a key diagnostic feature inside the EiceDRIVER™ to validate the integrity of the output stage signal to the input signal by monitoring the voltage at the CLAMP/GATE pin. In the following measurements the static monitoring functionality is described in detail. The monitoring is referred to as “static” because it monitors the gate for disruptions after the voltage has already settled.

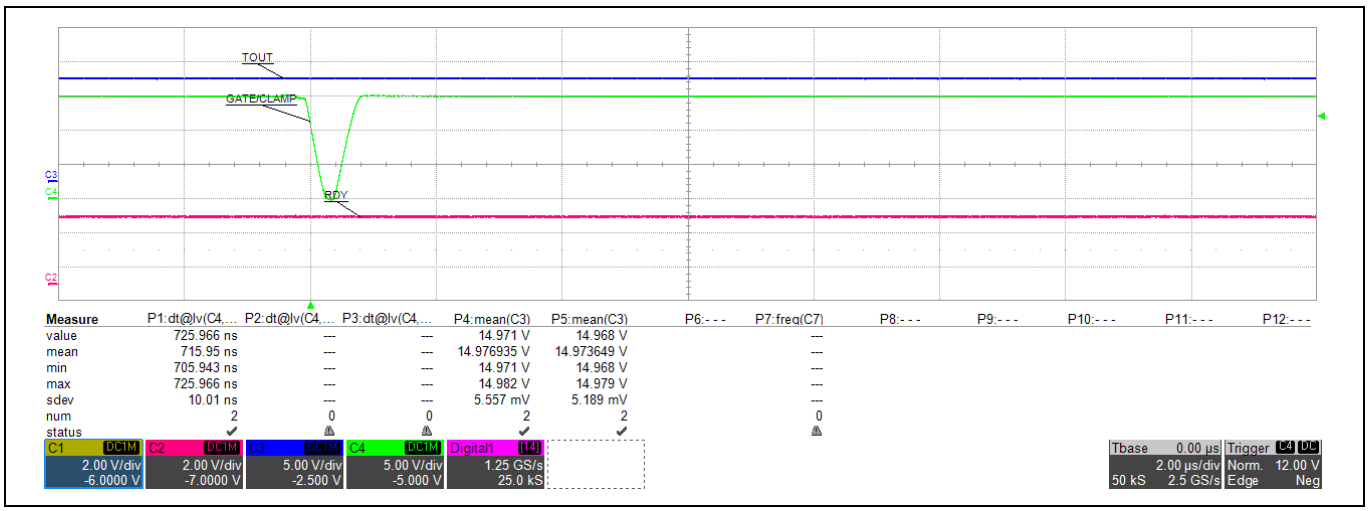



**Figure 26 Blanked static gate monitoring**

Figure 26 shows the blanking functionality of the gate monitoring function. If the signal of gate clamping is disrupted for a period of time which is less than the minimum blanking time of the gate monitoring, the output stage stays activated.

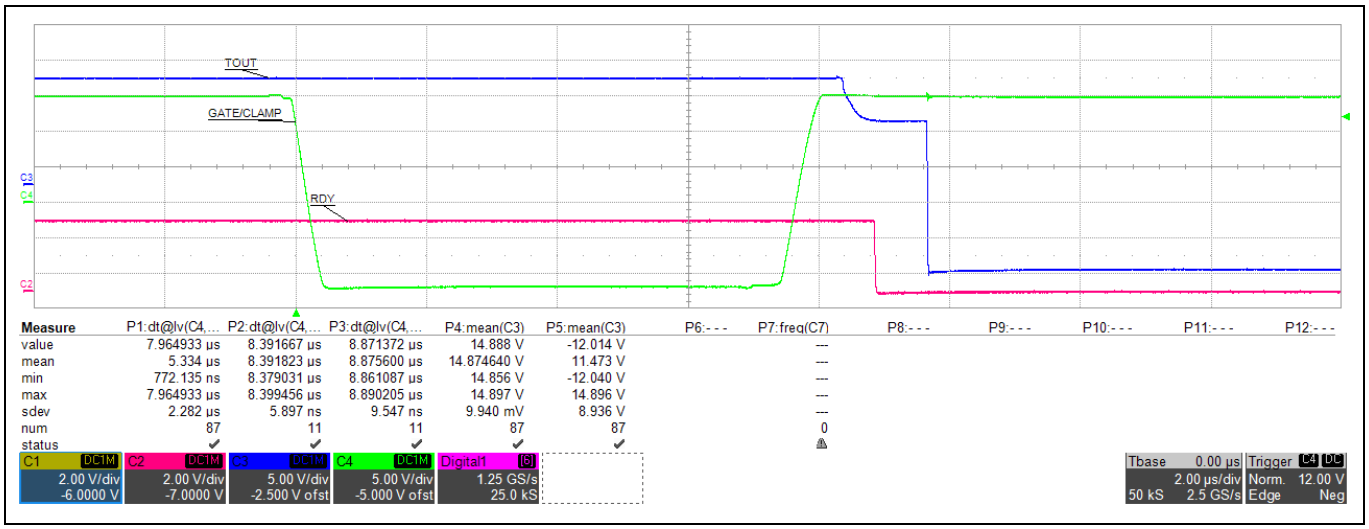



**Figure 27 Activated static gate monitoring case I**

Figure 27 shows the activation of the gate monitoring after the internal blanking time is elapsed. The gate clamping voltage is shorted to ground for a defined period of time. After this time the voltage on gate clamp is released to Vcc2. As the time of the grounded signal on gate clamp exceeds the defined static gate monitoring blanking time the output stage is driven into the defined safe condition via safe turn off.

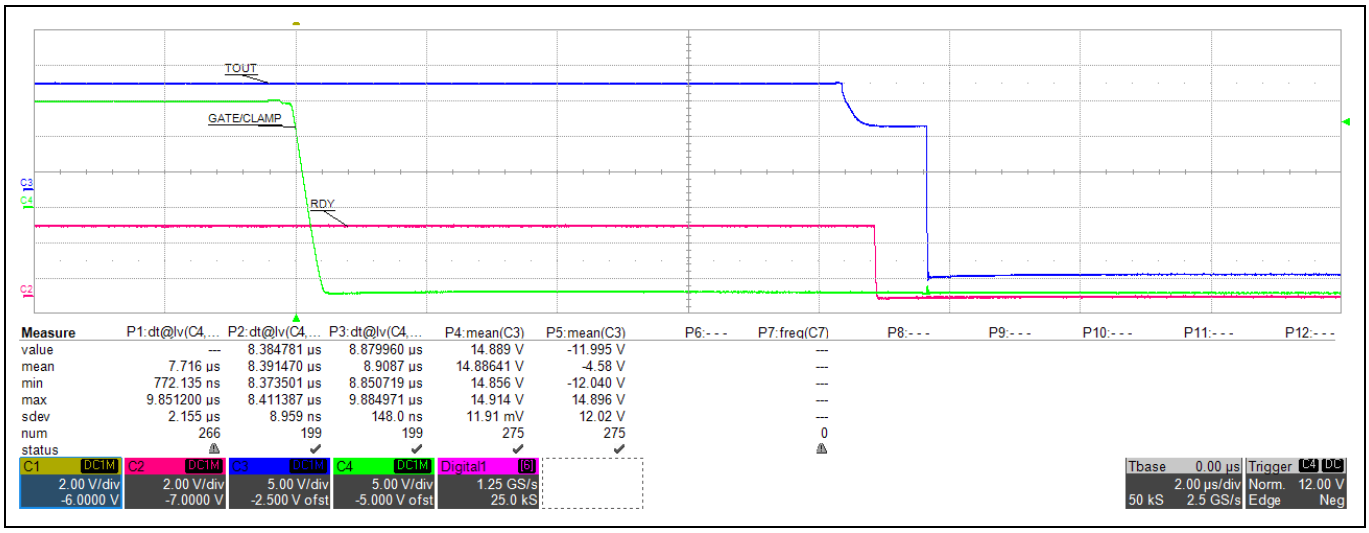



**Figure 28 Activated static gate monitoring case II**

Figure 28 shows that if the pulse disruption is longer than the minimum blanking time of the gate monitoring, the safe turn OFF is triggered after the detection and reaction time of the gate monitoring functionality.

## 3.8 Dynamic gate monitoring

In contrast to the static gate monitoring, the dynamic monitoring observes the gate signal integrity during switching transitions.

In the measurement result shown in Figure 29 the functionality of the dynamic gate monitoring can be observed.

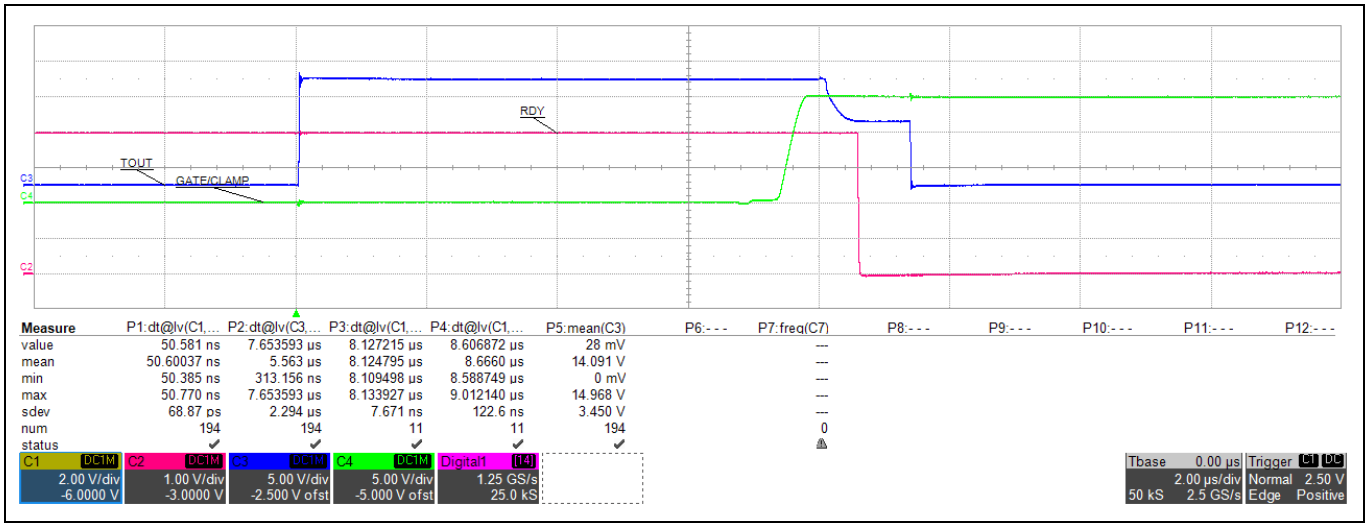



**Figure 29 Activated dynamic gate monitoring**

## 3.9 Output stage monitoring

The device offers a continuous activated output stage monitoring in static working condition and in switching conditions of the power semiconductor. The output stage monitoring can be distinguished from the aforementioned gate monitoring, since it checks the integrity of the signal on TOUT only from device perspective. In the following measurement results shown in Figure 30 the working principle is shown in detail.

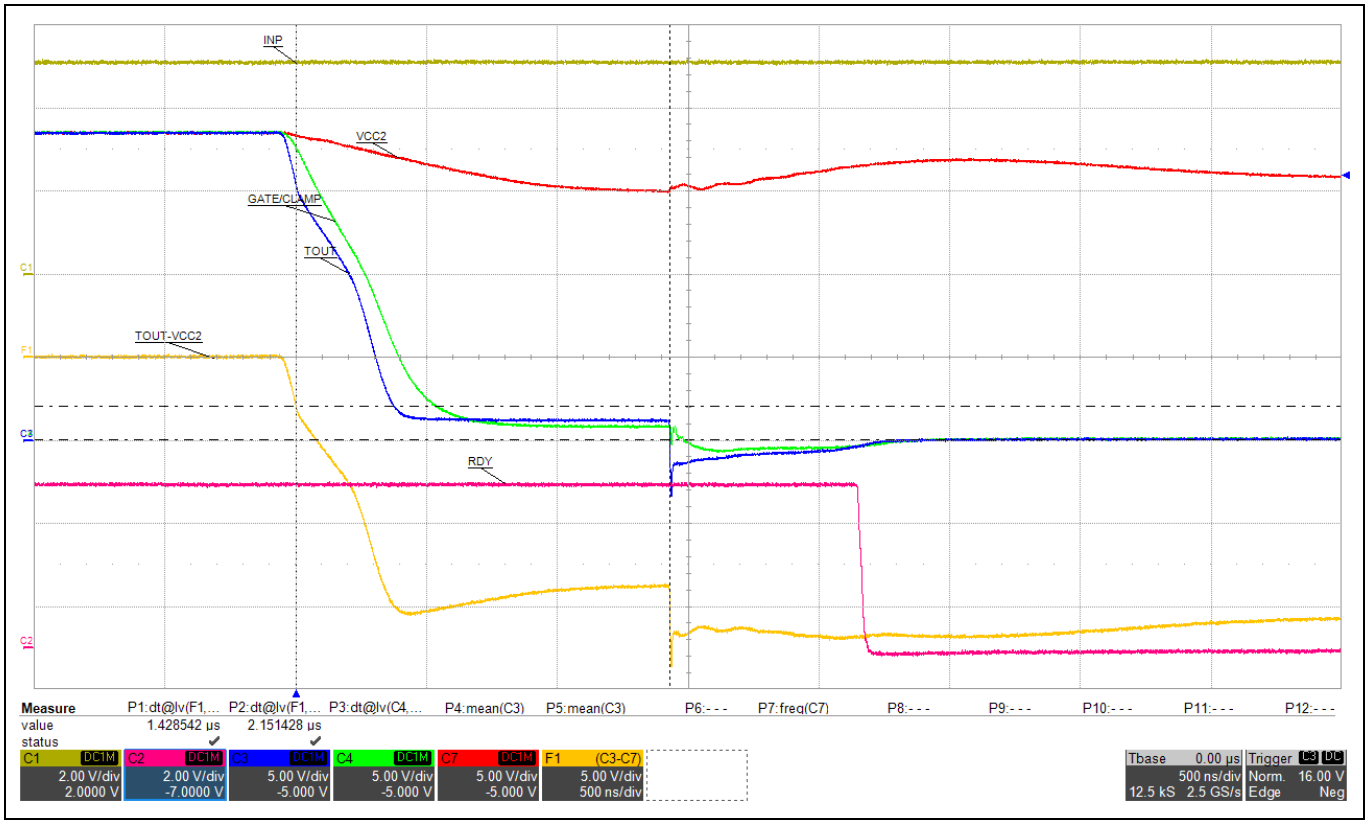



**Figure 30 Activated output stage monitoring**

## 3.10 Two-level turn-off

In case of any high current failure of the observed output stage described in Chapter 3.1 (DESAT) and Chapter 3.2 (OCP) the gate driver will initiate a safe turn-off.

This turn-off sequence is described in the diagram below:

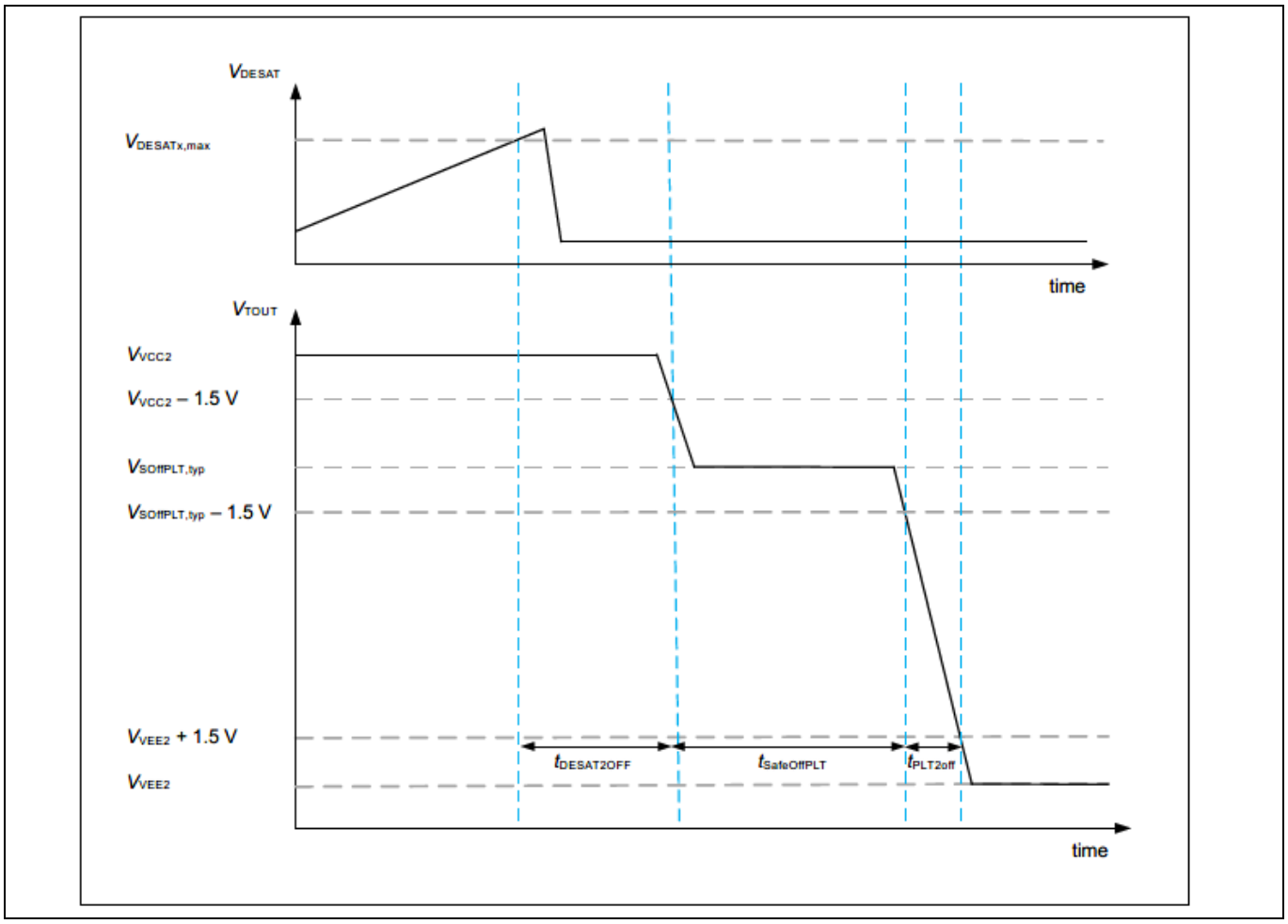



**Figure 31 Principle of two-level turn-off**

As the EiceDRIVER™ family is a fully compliant product for IGBT and SiC MOSFET usage, the safe turn-off is developed to suit the timings and needs of the dedicated technology. The safe turn-off feature with the dedicated timing for the IGBT can be seen in the following measurement shown in Figure 32.

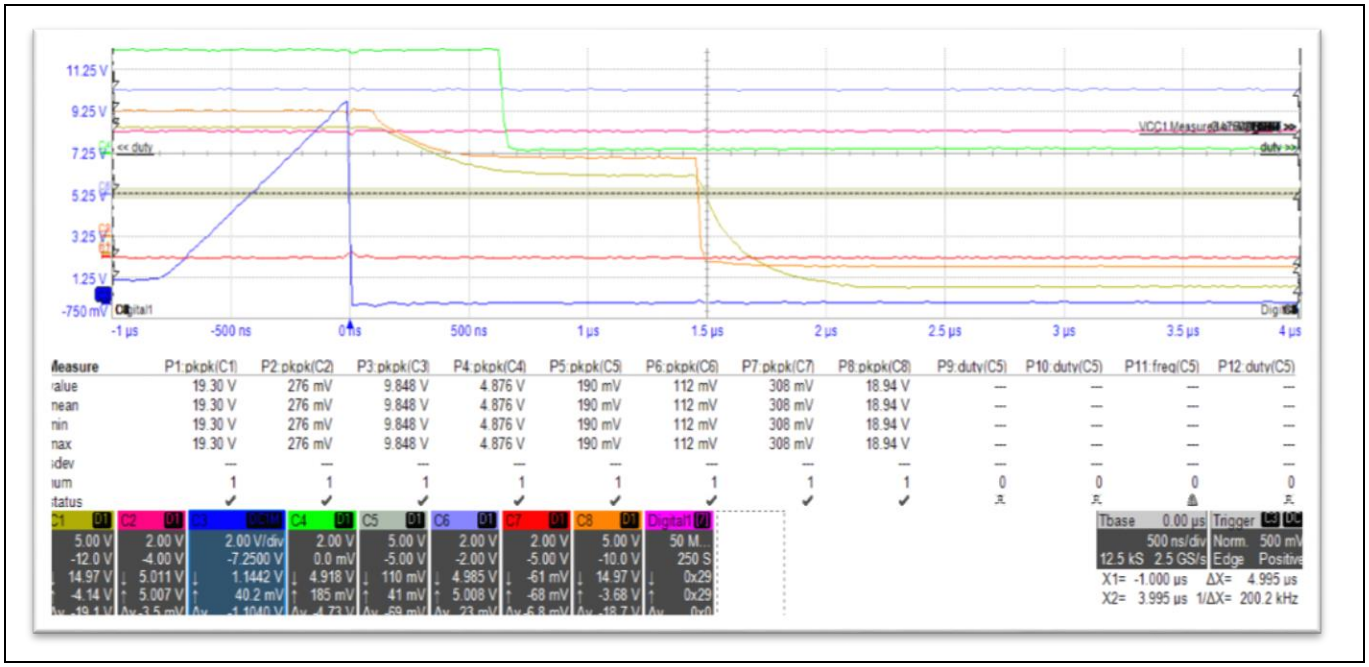



**Figure 32 Measurement result of two-level turn-off functionality**

## 3.11 ASC on secondary side

The EiceDRIVER™ family offers a variant with the active short circuit (ASC) feature on the secondary side. The ASC feature can be used to ensure the safe state for the electrical machine from the secondary side by forcing a turn-on of the power switch.

To trigger the output stage of the driver IC into ON state the voltage on the ASC pin needs to exceed the minimum defined threshold found in the datasheet. The detailed scheme can be found in the picture below.

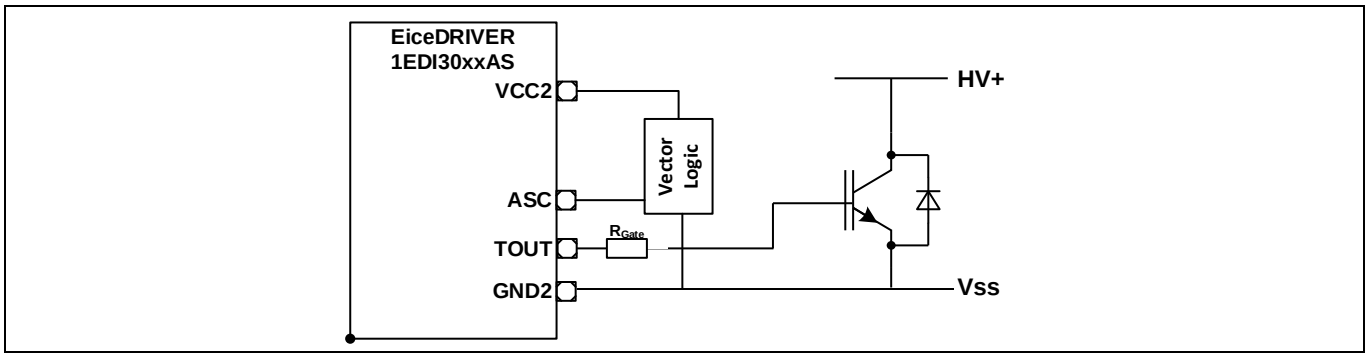



**Figure 33 ASC schematic on secondary side with 0 vector logic**

Together with the safe state logic from Chapter 3.4.3 it offers the customer to have the redundant safety logic on the secondary side. This can save the customer additional isolated digital channels from the low voltage side to the high voltage side.

## 3.12 INP & INN

The EiceDRIVER™ family offers a hardware based shoot-through protection with INP & INN Pins on the primary side of the device. Connecting the INP & INN vice versa as shown in Figure 34, an interlock logic between both the high-side and the low-side driver can be established.

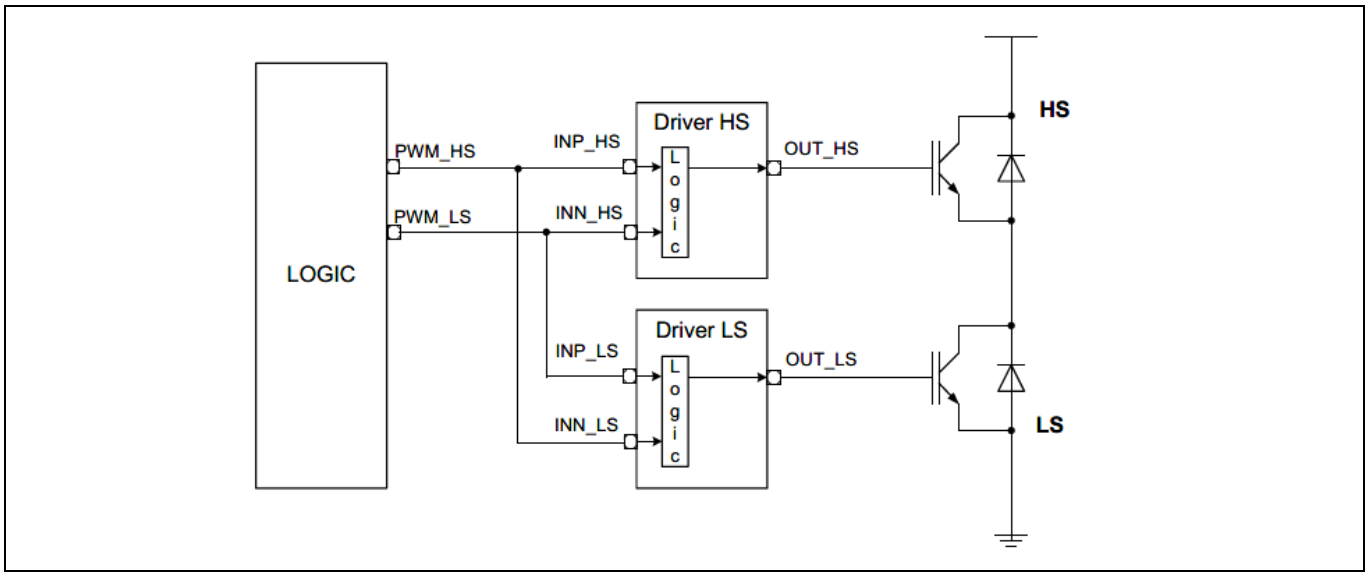



**Figure 34 Shoot through protection application schematic**

Having the INP & INN inputs on both of the driver ICs of the halfbdrige connected in this scheme, it is possible to have the minimum internal deadtime implemented into the gate driver IC.

The respective products of the EiceDRIVER™ family are one-time programmed to ensure that the internal deadtime timings are optimized for the usage with either IGBTs or SiC MOSFETs.

The difference in the minimum internal deadtime for all variants of the EiceDRIVER™ family is shown in the following table:

**Table 7 Different minimum internal dead times**

| Variant | Minimum internal deadtime |
|---|---|
| 3020AS, 3021AS, 3023AS | 800 ns (typical) |
| 3030AS, 3031AS, 3033AS | 140 ns (typical) |

In addition, there is a keep state transition implemented into the shoot-through protection which needs to be highlighted and described in detail.

### Keep state explanation

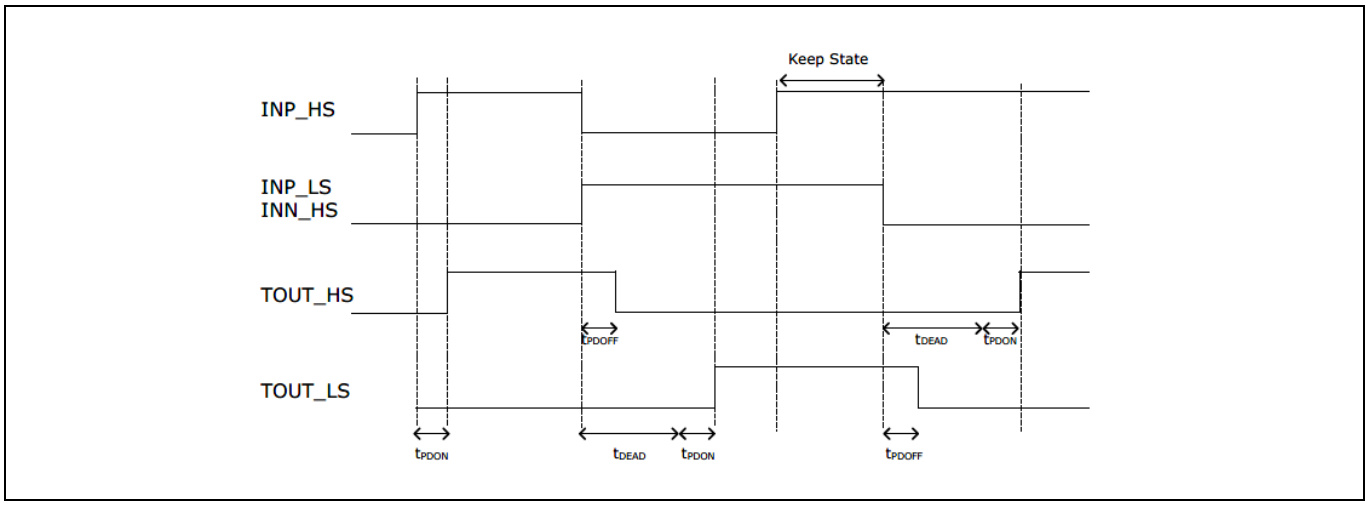



**Figure 35 Keep state detailed principle**

When turning off the positive input signal (INP) of the high-side driver IC and turning on the positive input signal of the low-side driver IC, the output signal will be delayed according to the sum of the propagation delay and the internal deadtime of the used variant.

When turning on the high-side gate driver during the time the low-side driver is active, the signal will not be active on the output stage of the high-side driver. The low-side driver will remain in ON state. The low-side driver remains in the so called “keep state”.

The low-side driver will leave the keep state once the INP_LS transitions from high to low and will turn off. Once the high-side dead time and propagation delay have elapsed, the high-side driver will turn on.

This functionality offers the possibility to switch the high-side and the low-side driver at the same time while the driver ICs ensure that the output stage is just switched after the defined internal deadtime has elapsed.

# 4 Delta Sigma Analog/Digital Converter

The EiceDRIVER Variants 1EDI3020AS/3023AS/3030AS/3033AS offer an integrated accurate 12 BIT Delta Sigma Analog/Digital Converter (DSADC).

The DSADC is used to convert an external signal to a stream of discrete digital values. The DSADC continuously measures an external signal, connected to port pin AIP to GND2. It converts the analog signal to a data stream and provides this conversion result galvanically isolated on the DATAPWM output pin on the primary side.

The DSADC can be used to measure the following quantities in the application.

## 4.1 Measurement of temperature diodes on chip

*Note: Use the Calculator_EiceDRIVER for additional insight into the temperature measurement functionality.*

The measurement principle of measuring the temperature of power semiconductor is based on the forward voltage dependency of the diode on its junction temperature.

With an integrated accurate current source it is possible to measure the voltage drop over the temperature diodes. You can see this dependency of the diode in the following figure which is extracted from the Infineon HybridPACK™ DSC module.

**5 Temperature Sensor**

| Parameter | Conditions | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Forward voltage | $I_{TS}$ = 1.00 mA, $T_{vj}$ = 150°C<br>$I_{TS}$ = 1.00 mA, $T_{vj}$ = 25°C | $V_{TS}$ | | 2.120<br>2.910 | | V |

**Figure 36 Temperature dependency of the forward voltage in the FF400 DSC module**

This information can be transferred to following graph which shows the dependency of the forward voltage of the diode vs its junction temperature:

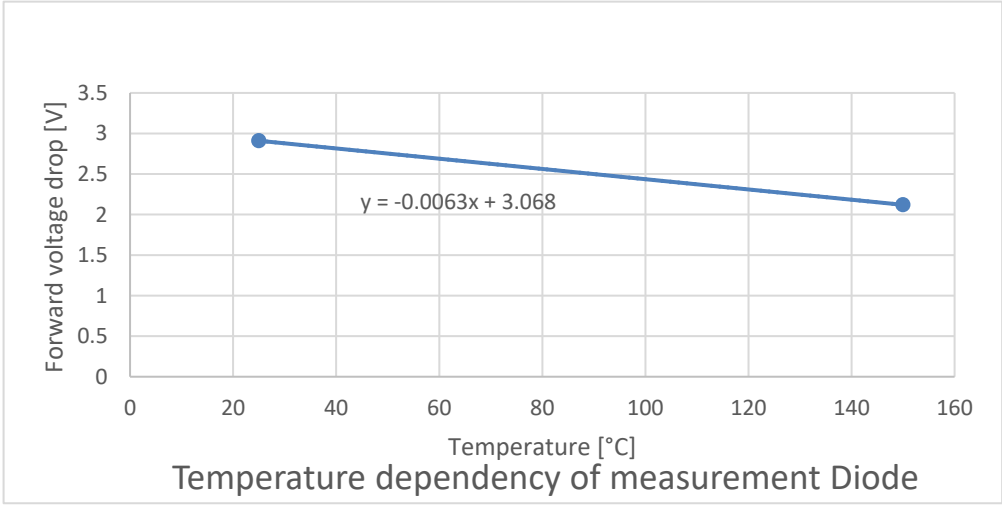



**Figure 37 Forward voltage temperature dependency**

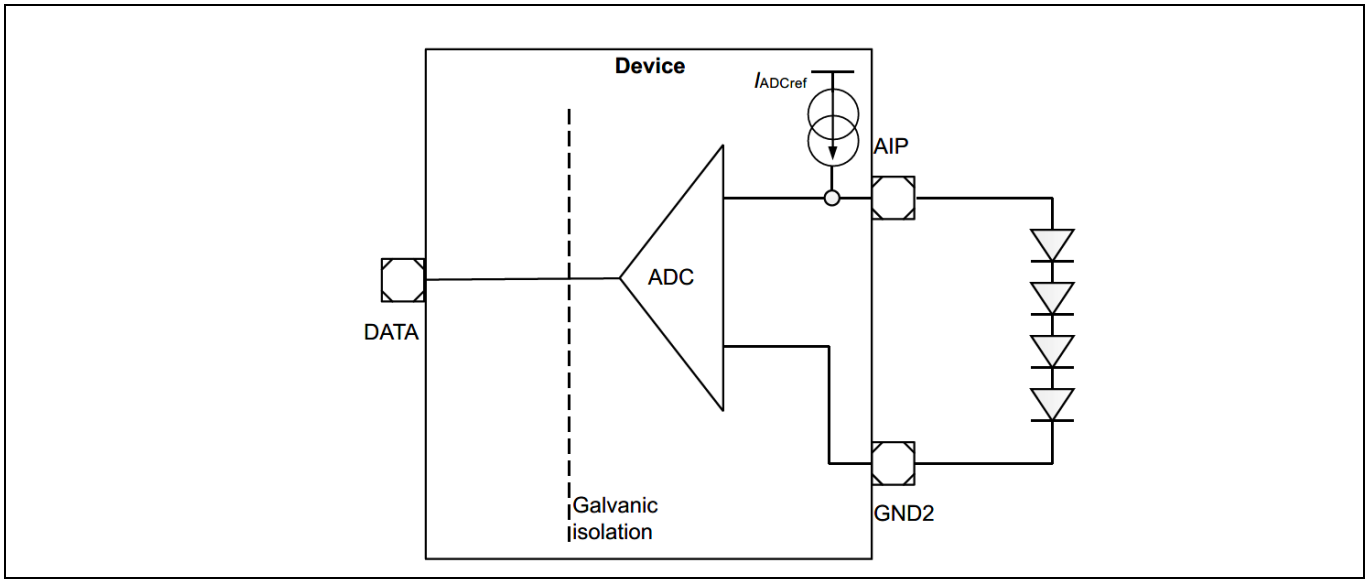



**Figure 38 Application schematic of temperature diode measurement**

## 4.2 Measurement of temperature through NTC

Since not all of the given power modules on the market offer an integrated temperature diode, the DSADC can be taken as well to measure the accurate temperature of an NTC and transfer this information to the primary side.

For this functionality there are dedicated variants of the device available where the integrated current source is disabled to achieve a higher accuracy of the measurement. The variant for IGBT is 1EDI3023AS and for SiC MOSFET is 1EDI3033AS.

The following application diagram shows a possible measurement principle supplied by VCC2. As the resistance of the NTC will change over the complete operating temperature, it is necessary to define the area of lowest tolerances and errors.

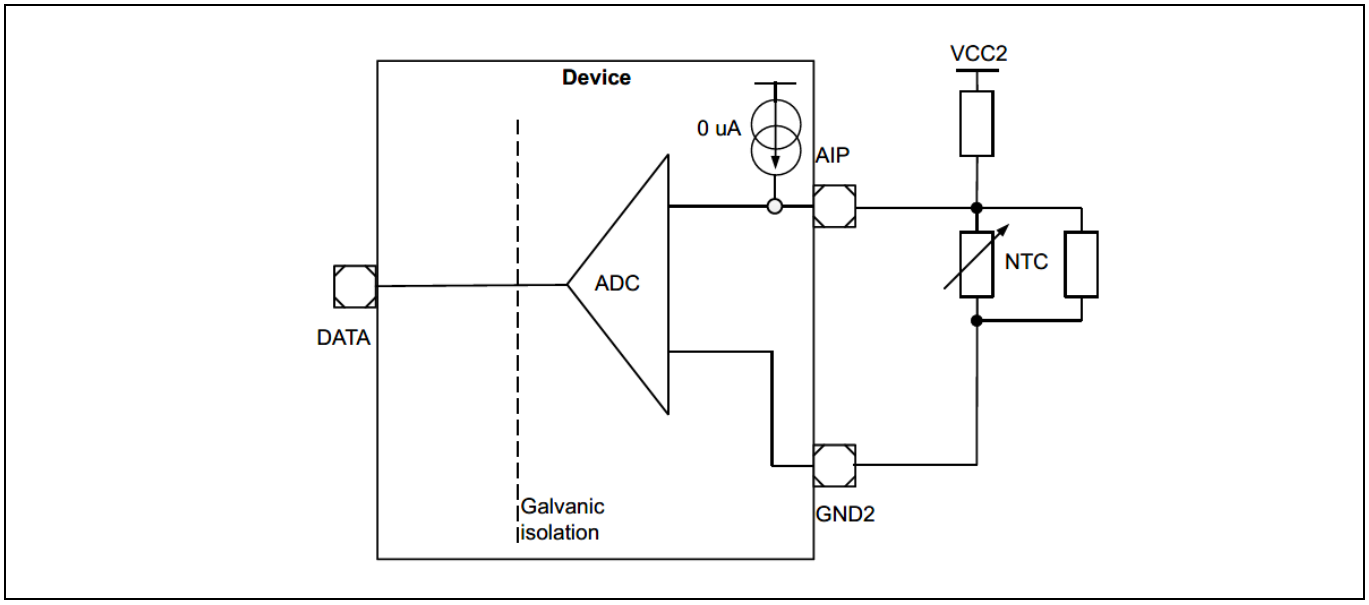



**Figure 39 Application schematic of temperature measurement through NTC**

## 4.3 DC-link voltage measurement

The integrated ADC can also be used for the measurement of the DC-link voltage. For this purpose the variant 1EDI30x3AS with a deactivated current source to increase the accuracy of the integrated 12 BIT ADC is available.

As the device ADC is referencing to the GND2 potential which is shifting during switching conditions between HV+ potential and HV- potential, it is recommended to use the low-side driver IC for measuring the DC-link voltage.

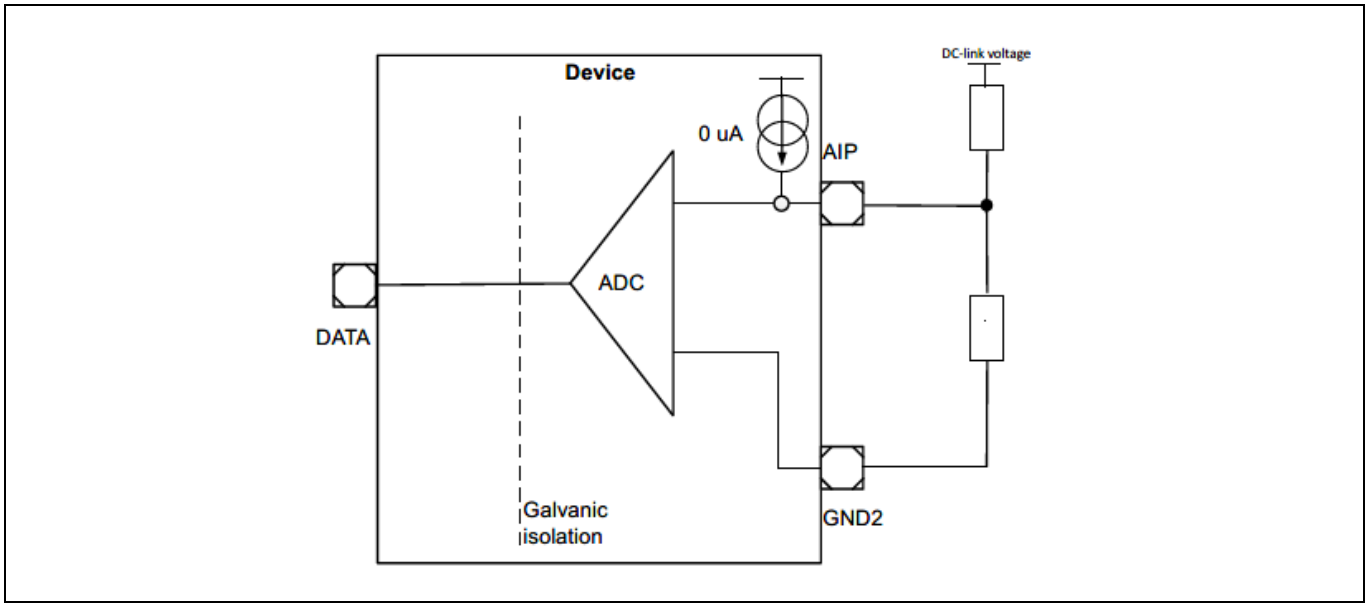



**Figure 40 Measuring the DC-link voltage of the system**

## 4.4 PWM read-out at DATA pin

The DATA pin delivers two types of information depending on the operation mode and the enable pin:

EN = 1 (Normal mode or error mode): ADC value read-out

EN = 0 (Error mode): detailed diagnosis read-out via duty cycle of PWM signal

## 4.5 ADC result read-out

In the following diagram the full range of the DSADC can be seen, showing the relation between measured voltage and the output duty cycle on the DATA pin.

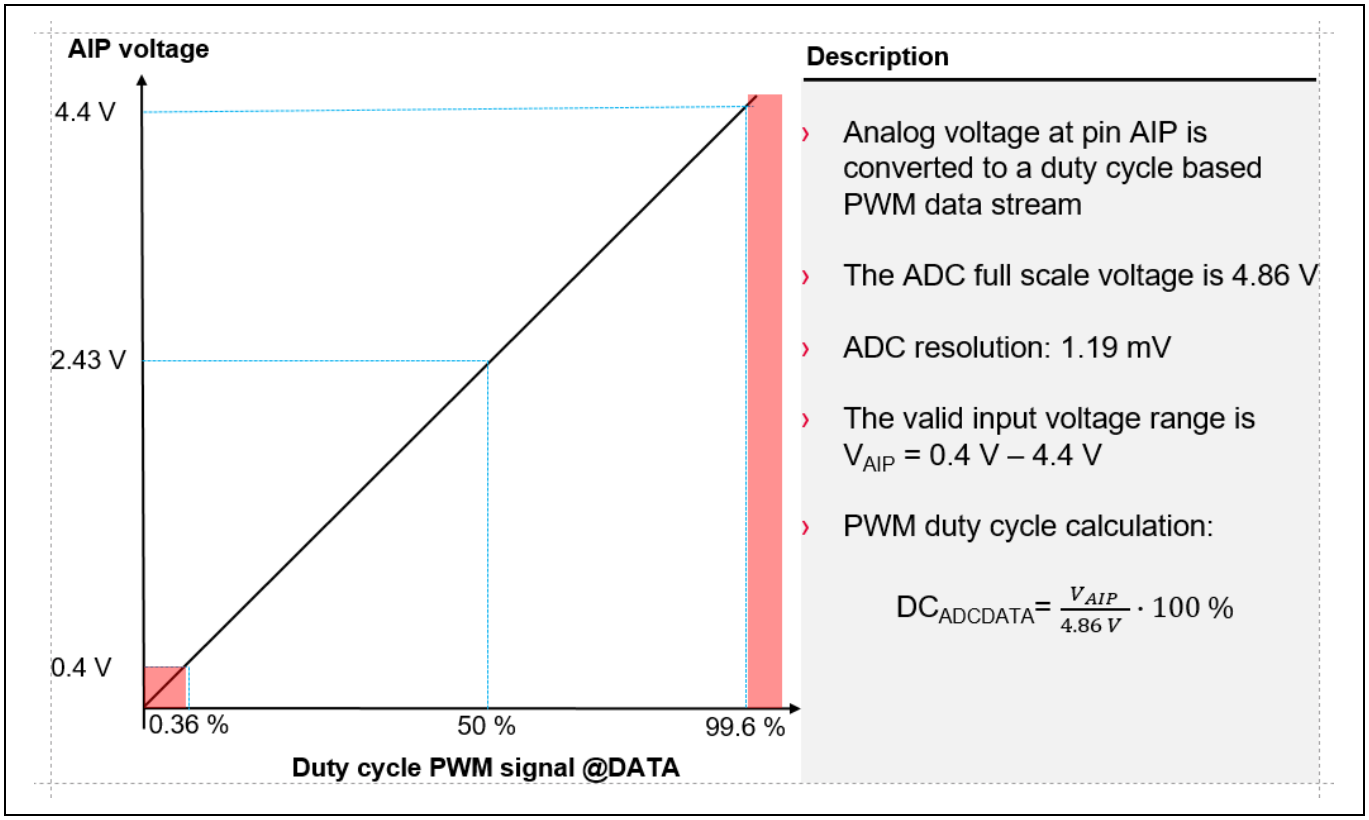



**Figure 41 Voltage range of ADC measurement input**

The ADC can measure within a defined range of 0.4 V to 4.4 V.

Various failure scenarios can be derived from this information. These failures are summarized in the table below.

**Table 8 Failure indication at output ADC**

| Failure | Output of ADC | System failure detection possibility |
|---|---|---|
| AIP is shorted to GND | 0% | Duty cycle below 0.36% |
| AIP is shorted to Vcc2 | 100% | Duty cycle above 99.6% |
| AIP Pin is open | Capacitor on ADC charges up due to integrated current source. | Duty cycle increases over time above 99.6% due to internal current source charging. |

# 5 Diagnosis read-out

*Note: Use the Calculator_EiceDRIVER for the estimation of the DESAT and OCP external components.*

The DATA pin shows the detailed diagnosis in case of an error. For ADC variants (1EDI30x0AS) it returns a high-low signal with a defined duty cycle that is based on the scheme presented in Figure 42.

| BIT# | Value | Description | Value | Description | Value |
|---|---|---|---|---|---|
| BIT 0 | 0 | PRIM NOT READY | 1 | PRIM READY | 1 |
| BIT 1 | | | | | |
| BIT 2 | | | | | |
| BIT 3 | | | | | |
| BIT 4 | 0 | RESERVED | | | |
| BIT 5 | 0 | no OSM error | 1 | OSM error | 0 |
| BIT 6 | | no GATEMON error | | GATEMON error | 0 |
| BIT 7 | | no DESAT error | | DESAT error | 1 |
| BIT 8 | | no OCP error | | OCP error | 0 |
| BIT 9 | | no UVLO2 error | | UVLO2 error | 0 |
| BIT 10 | | no OVLO2 error | | OVLO2 error | 0 |
| BIT 11 | | SEC READY | | SEC NOT READY | 0 |

**Figure 42 Overview of the BITs used for error indication**

*Note: If the primary side is not ready, DATA output is kept to GND1 (DATA = 0).*

The duty cycle follows the following formula: $DC = \frac{(\sum_{x=0}^{11} BIT_x * 2^x)}{4096\ bits}$

The whole cycle has a period of 100 µs/10 kHz: 4096 bit*25 ns = 100 µs

**Sample calculation:**

In case the primary side is in Ready_Mode and a DESAT error BIT 0 – BIT 3 and BIT 7 are set to 1 according to Figure 42. The formula yields the following result:

$$DC = \frac{(\sum_{x=0}^{11} BIT_x * 2^x)}{4096\ bits} = \frac{(BIT_0 * 2^0 + BIT_1 * 2^1 + BIT_2 * 2^2 + BIT_3 * 2^3 + BIT_7 * 2^7)}{4096\ bits} = \frac{(1 * 1 + 1 * 2 + 1 * 4 + 1 * 8 + 1 * 128)}{4096} = 3{,}49\%$$

Further examples for other types/combinations of errors and their duty cycle are shown in Figure 43.

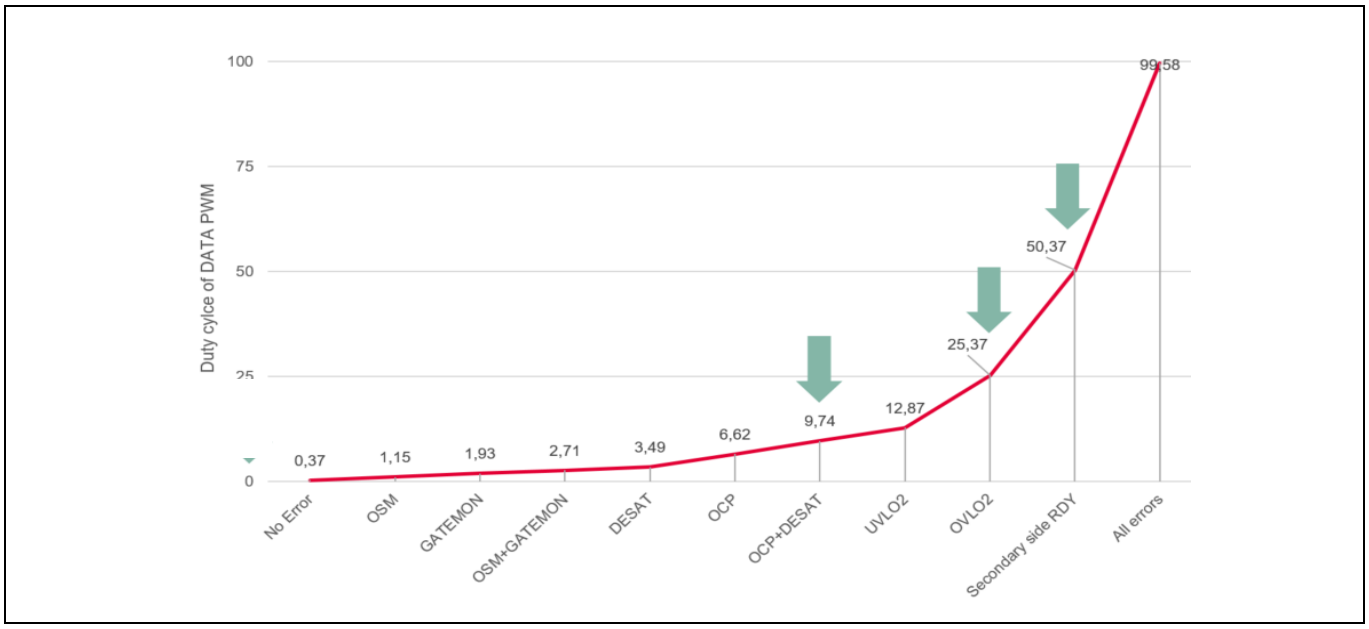



**Figure 43 Examples of duty cycle over different error combinations**

In the calculator tool provided all combinations of errors and their according duty cycle can be calculated.

## 5.1 Readout via Aurix™ TC3xx microcontroller

The PWM signal can be read out via a generic timer module of the microcontroller. The following section describes a possible solution.

The timer input module in PWM measurement mode is used.

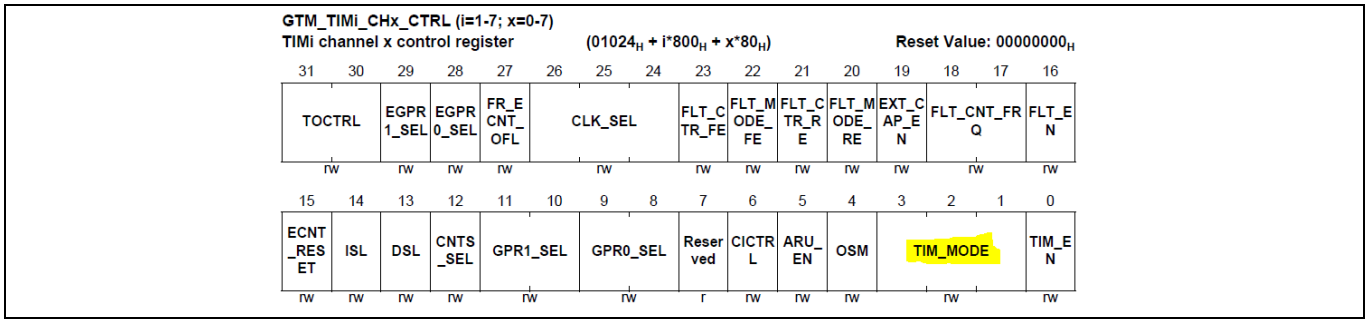



**Figure 44 Timer input module register description**

With this module the following approach is used:

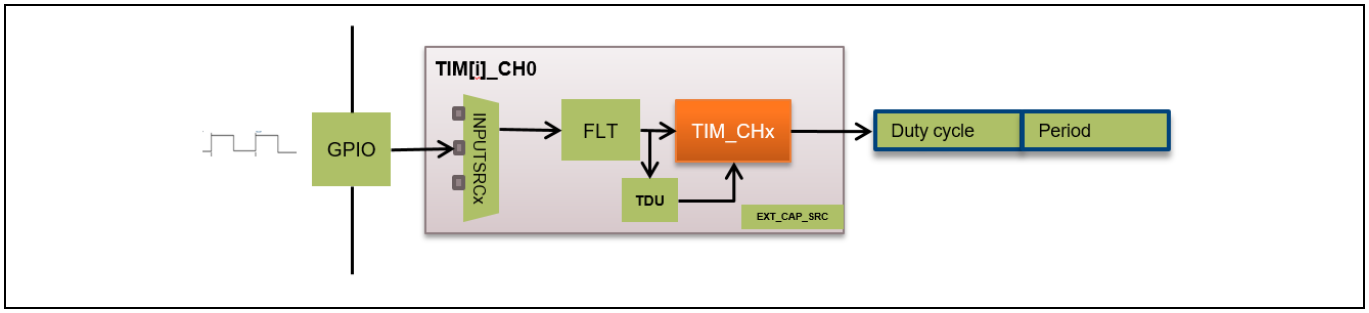



**Figure 45 Timer input module**

In the example source code which can be downloaded via the following link the configuration is TIM2 channel 0 connected to P15.5: Example Source Code

For further information about the timer input module refer to Chapter 28.13 of the AurixTM TC3xx User Manual.

## 5.2 Transition from ADC value read-out to diagnosis read out

In Normal_Mode the ADC value can be read-out at the data pin. The transition in case of an error follows the scheme presented in Figure 46.

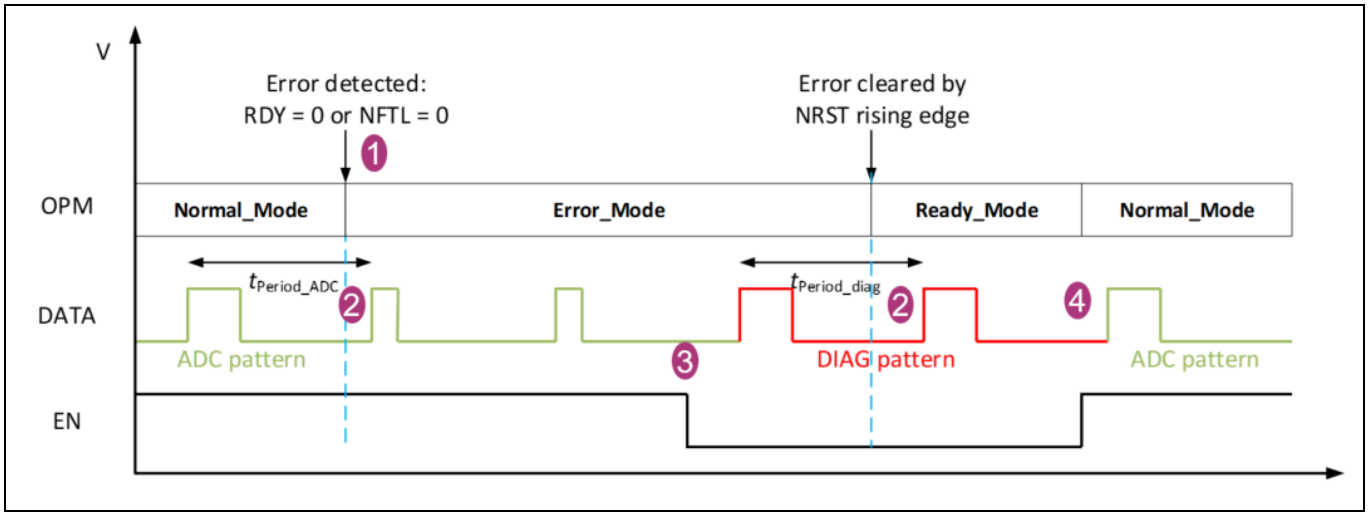



**Figure 46 Data pin read-out at operating mode transition**

1. Error is detected. OPM switches from Normal_Mode to Error_Mode. ADC signal is received at DATA pin.
2. The last ADC/diagnosis pattern is completed and remains as long as EN = 1/0.
3. To switch to diagnosis pattern EN is set to low and the ADC frame is completed. Once the ADC frame is completed, the diagnosis signal is available.
4. After the error is cleared, the device goes back to Normal_Mode (EN = 1) and DATA pin is receiving ADC signal.

# 6 Additional design considerations

This chapter describes additional design hints to be considered to enable optimized and secured performance of the EiceDRIVER™ in the main inverter application.

## 6.1 Overvoltage clamping on power semiconductor

In case of an overvoltage event on the power semiconductor the customer needs to ensure the defined maximum working conditions. To achieve this the customer can choose between the different possible solutions which are described in the following sections.

### 6.1.1 Active overvoltage clamping on power semiconductor

In any possible overcurrent condition without the possibility of a safe turn off it must be ensured that the breakdown voltage of the power semiconductor is not violated.

Possible failure cases where a safe turn off of the driver IC cannot be ensured (this list is not exhaustive):

- Undervoltage lockout primary/secondary during high current phase
- Overvoltage lockout during high current phase
- Overcurrent detected through hall-based sensor and trigger via primary side control

To ensure the working conditions of the power semiconductor are below the defined maximum operation conditions for the breakdown voltage in any failure case that can appear in the application, it may be necessary to place an additional TVS diode directly next to the gate.

This diode makes sure the gate is kept closed to reactivate the collector emitter channel for the time within which the overvoltage event occurs. This diode is placed on the available evaluation board as well.

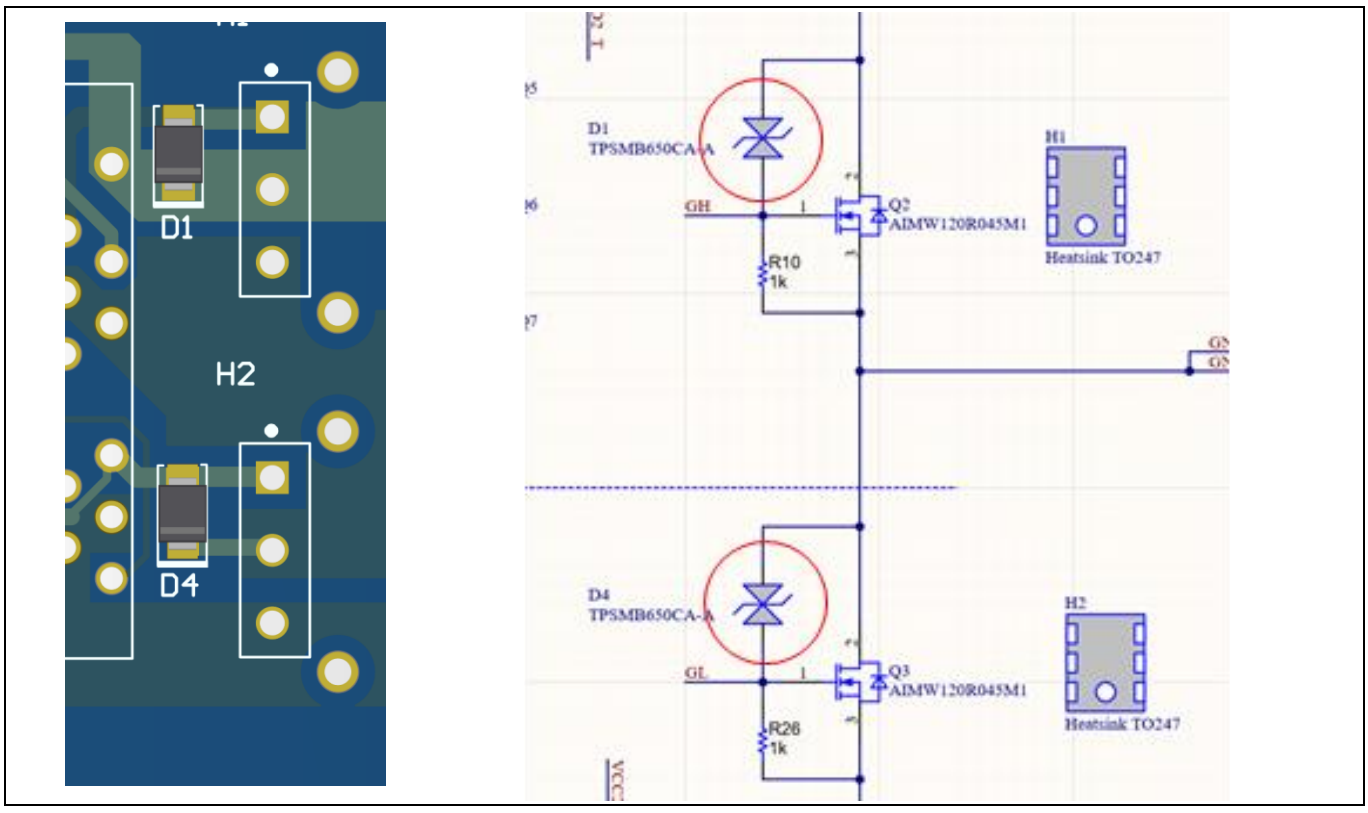



**Figure 47 Active overvoltage clamping**

### 6.1.2 Passive clamping of overvoltage events on the power semiconductor

To ensure the working conditions are below the defined maximum values of the dedicated power semiconductor, a passive R/C network can be placed directly next to the collector/emitter or drain/source channel to clamp the induced energy into the capacitor.

A possible solution is shown in Figure 48.

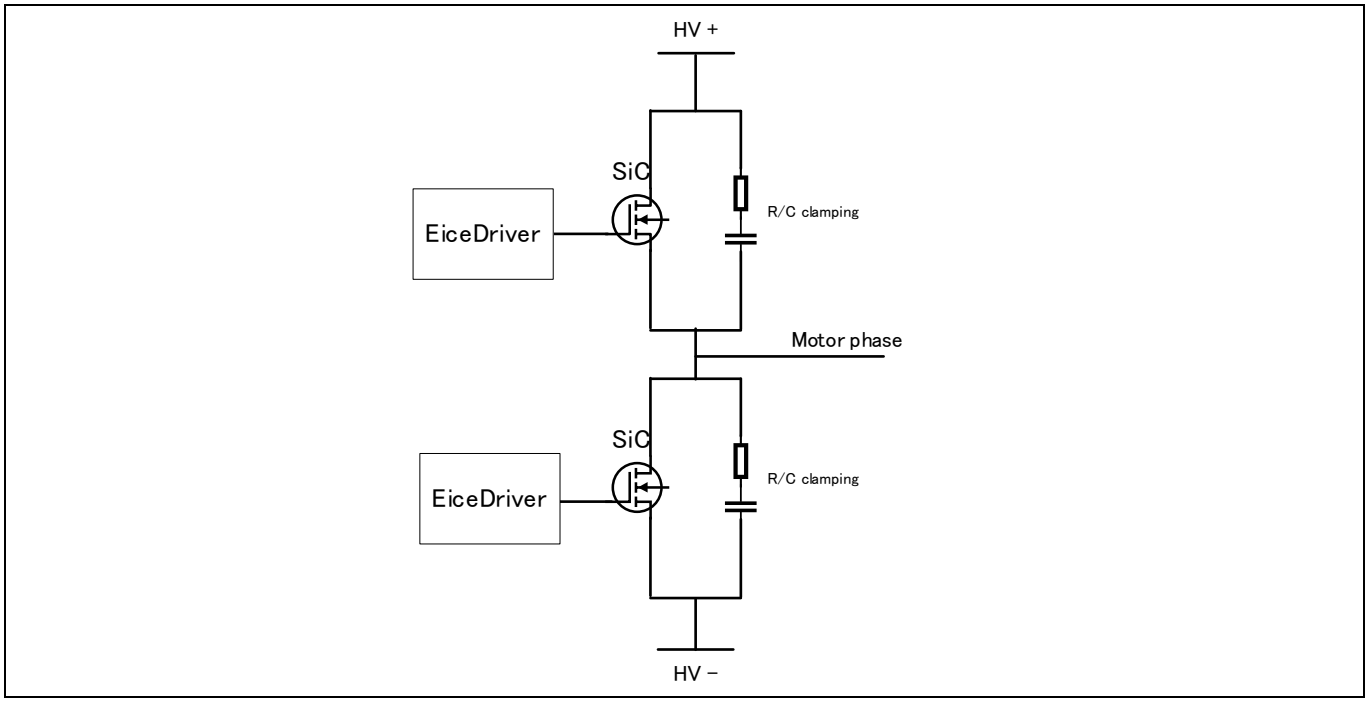



**Figure 48 RC clamping network**

The R/C clamping circuit needs to be designed according to the maximum allowed thermal dissipation of the clamping components.

## 6.2 Typical application components

*Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.*

**Table 9 Component values for typical application example**

| Parameter | Symbol | Values | | | Unit | Test condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Decoupling capacitance (between VCC1 and GND1) | $C_{dVCC1}$ | 0.55 | 1.1 | - | µF | Total capacitance refers to 1 µF capacitance + 0.1 µF close to the device. Max. value depends on $t_{RP1}$. |
| Decoupling capacitance (between VCC2 and GND2) | $C_{dVCC2}$ | - | 11 | - | µF | Total capacitance refers to 10 µF capacitance + 1 µF close to the device. Values depend on external $C_{LOAD}$. Max. value depends on $t_{RP2}$. |
| Decoupling capacitance (between VEE2 and GND2) | $C_{dVEE2}$ | - | 11 | - | µF | Total capacitance refers to 10 µF capacitance + 1 µF close to the device. Max. value depends on $t_{RP3}$. |
| Pull-up resistance | $R_{pu}$ | - | 10 | - | kΩ | Min. value depends on $I_{OUTx\_MAX}$. |
| Filter resistance | $R_{Filter}$ | - | 1 | - | kΩ | Value must fit to application. |
| Filter capacitance | $C_{Filter}$ | - | 47 | - | pF | Value must fit to application. |
| DESAT filter resistance | $R_{Desat}$ | 1 | 2.2 | - | kΩ | Depends on maximum current and on $V_{DESATx}$ deviation. |
| DESAT filter capacitance | $C_{Desat}$ | 50 | 100 | - | pF | Depends on required response time. |
| OCP sense resistor | $R_{OCPSense}$ | - | 0.47 | - | Ω | Value depends on IGBT/SiC specification, voltage rating of OCP pin has to be considered. |
| OCPP filter resistance | $R_{OCPP}$ | - | 10 | - | Ω | Depends on required response time. Consider internal pull-up. |
| OCPP filter capacitance | $C_{OCP}$ | - | 10 | - | pF | Depends on required response time. |
| OCPN filter resistance | $R_{OCPN}$ | - | 10 | - | Ω | Should match to OCPP filter resistor. Consider internal pull-up. |
| TOUT resistance ON | $R_{gON}$ | 1,7 | - | - | Ω | Min. resistor value required according to maximum output current in functional range. Max. value limited by gate monitoring feature. |
| TOUT resistance OFF | $R_{gOFF}$ | 1,7 | - | - | Ω | Min. resistor value required according to maximum output current in functional range. Max. value limited by gate monitoring feature. |
| GATE/CLAMP series resistance | $R_{GATE}$ | - | 0 | - | Ω | Optional component. Voltage across resistor impacts Active Miller Clamping feature. |

## 6.3 Typical application examples

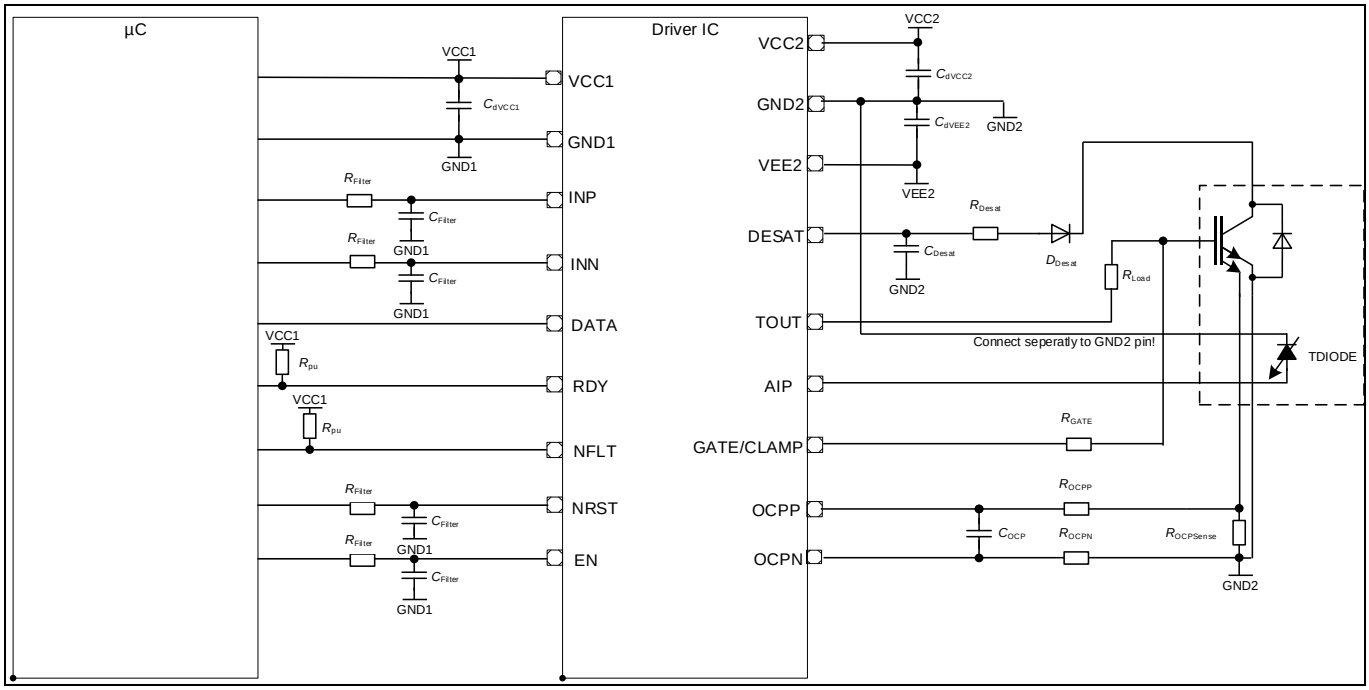



**Figure 49 Typical application example with ADC function**

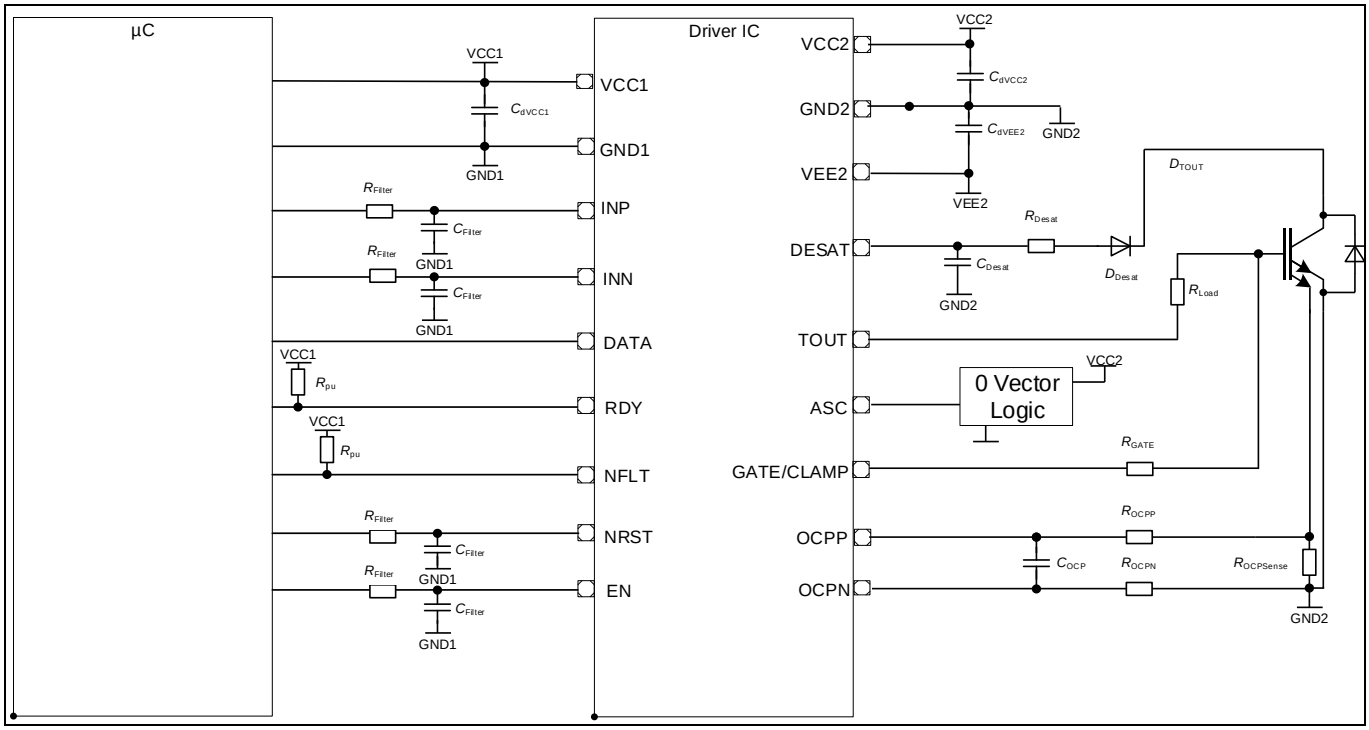



**Figure 50 Typical application example with ASC function**

## 6.4 Maximum output current on TOUT

The maximum output peak current is limited by the internal bond wire. It can be calculated according to the gate charge on TOUT pin. The following formula is valid for the graph in Figure 51:

$$I_{TOUT} = \frac{2 \cdot T \cdot I_{Eff}^2}{C_{Gate}}$$

Whereas an maximum DC bond wire current of $I_{Eff}$ = 1.1 A is assumed. The repetion rate T = 50 µs is used as an example. A maximum peak current of $I_{TOUT}$ = 20 A is the limit, independent of varying application parameters like repetion rate or gate charge. Hence in the example below for $C_{Gate}$ < 6 µC a maximum output peak current of 20 A can be assumed.

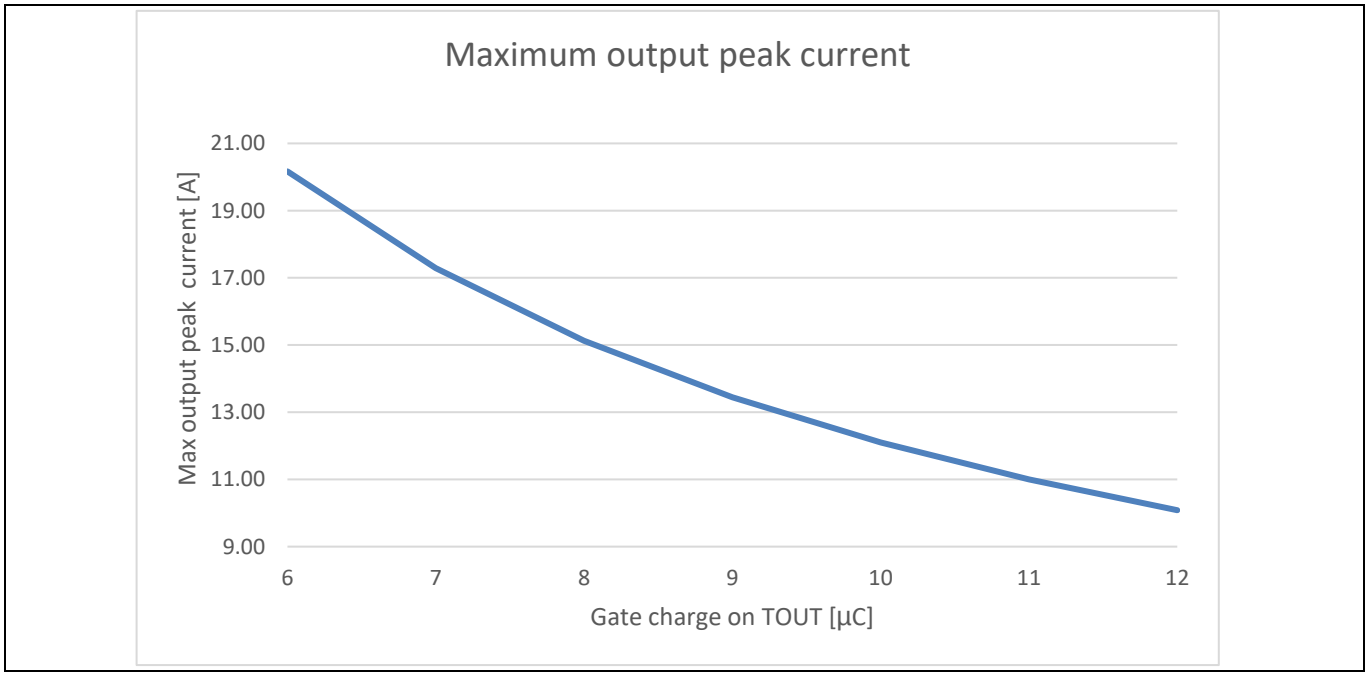



**Figure 51 Output peak current depending on gate charge TOUT**

*Note: The external components need to be designed in a way that $T_j$ < 150°C*

## 6.5 Splitted output via external diode

The 1EDI30xxAS has a single channel output for turn-on and turn-off operations. Figure 52 shows how to enable a splitted output with extra external components for independent turn-on and turn-off switching times of the power semiconductor.

In this case an additional high current diode (B540CQ-13-F used in reference design) and a dedicated Rgoff is used.

### Turn-on

During the turn ON of the IGBT/SiC MOSFET the parallel resistance between Rgoff and Rgon is effective.

### Turn-off

During the turn-off of the IGBT/SiC MOSFET the resistance of the Rgoff is effective. The Rgon is blocked by the junction of the diode.

This enables the customer to have a dedicated turn-on/ turn-off timings to optimize the system efficiency.

With the application solution below the turn-on time is always shorter than the turn-off time due to the parallelization of the resistors during turn-on. If the turn off time should be shorter than the turn-on time, the diode needs to be shifted to block the turn-on current.

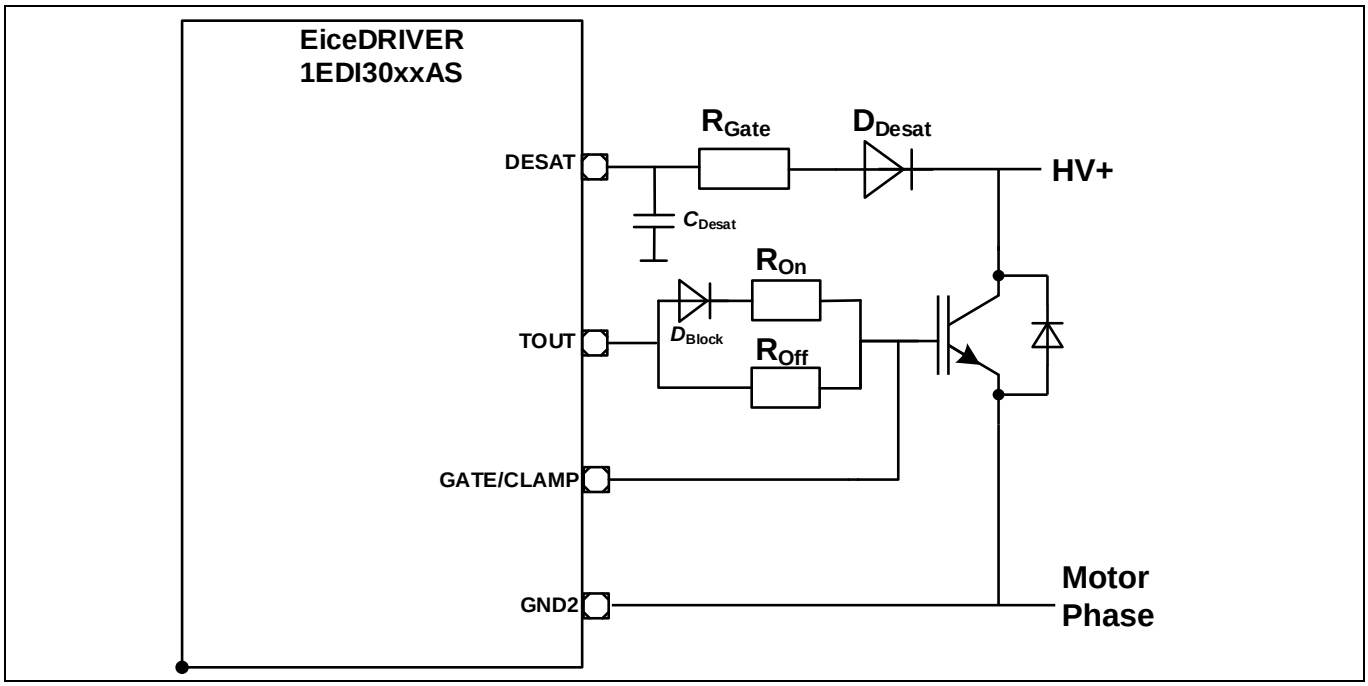



**Figure 52 Enable split output for setting different Rgon and Rgoff settings via external diode**

## 6.6 External gate resistor calculation example

During the design phase of the external gate resistors the following topics have to be taken into consideration:

RgON:

- The power losses on the gate resistor have to be applicable over the complete temperature range of the resistor.
- To achieve the required EMC constraints the switching times have to be chosen accordingly.
- The switching times must not exceed the maximum rated di/dt of the power module and the isolation of the motor windings.

RgOFF:

- The power losses on the gate resistor have to be applicable over the complete temperature range of the resistor.
- The switching times have to be chosen according the maximum allowed breakdown of the power semiconductor in the worst case conditions (e.g. highest voltage/highest current/lowest temperature).
- The switching times must not exceed the max rated di/dt of the power module and the isolation of the motor windings.

For more detailed information on designing the gate resistors according to pulse power capability please refer to the calculation sheet of the EiceDRIVER at the following link: Calculator_EiceDRIVER

## 6.7 Power supply considerations

On the primary side the Vcc1 power supply is recommended to be decoupled via at least 1 µF to increase the robustness of the driver IC against coupled noise. A 0.1 µF capacitor should be placed close to the Vcc1 supply pin to increase the robustness against high frequency ripples on the supply line. This leads to an improvement of the EMC performance of the device.

To achieve a stable voltage on Vcc2 and Vee2 for a stable switching conditions, it is recommended to place decoupling capacitors on the supply. The capacitors stabilize the voltage in case high pulse currents are taken required due to the switching of the power semiconductor. The capacitor value should be at least 10 µF dependent on the chosen switching frequency and the gate charge of the semiconductor.

In addition, it is recommended to place the 1 µF capacitor directly next to the supply lines to be more robust regarding high frequency voltage ripple. In Figure 53 this capacitor is named Vcc1_A.

# 7 Layout hints

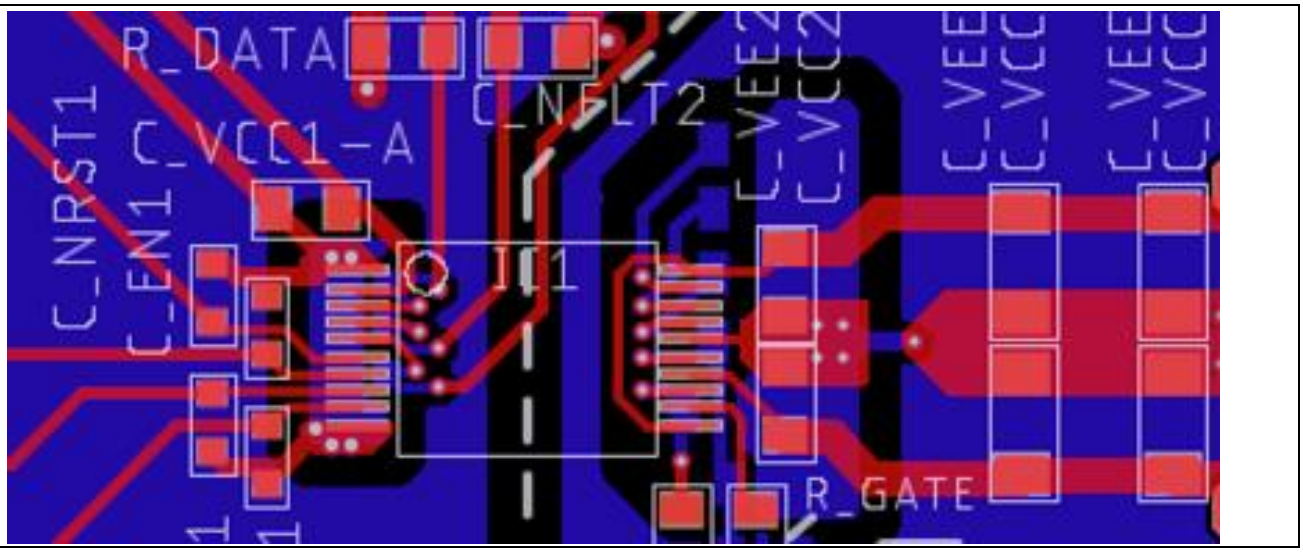



**Figure 53 Layout hints for optimized EMC performance**

The following overview provides a few hints for an improvement of the EMC performance:

**Primary side hints:**

- A ground island directly below the driver IC can be used to stabilize the GND potential of the internal control logic.
- Each pin which is driven with a long wire in the layout should be stabilized directly by placing 47 pF between the pin and the GND island.
- The localized GND island of the driver IC should be connected to the global GND of the primary side directly at the buffer capacitor on Vcc1 (1 µF).
- The recommended 0.1 µF capacitor on Vcc1 should be connected to the GND island of the driver IC directly below in a different layer.

**Secondary side hints:**

- Similar to the primary side there should be a localized decoupled GND island directly below the driver IC.
- Each pin which is driven with a long wire in the layout should be stabilized directly by placing 47 pF between the pin and the GND island.
- The localized GND island of the driver IC should be connected to the global GND of the primary side directly at the buffer capacitor on Vcc1 (1 µF). The wire should be routed directly next to /below the power supply to the buffer capacitor.

**Keep out zone**

To increase the robustness and to achieve the necessary creepage requirement there should be now wiring directly below the package body of the driver IC.

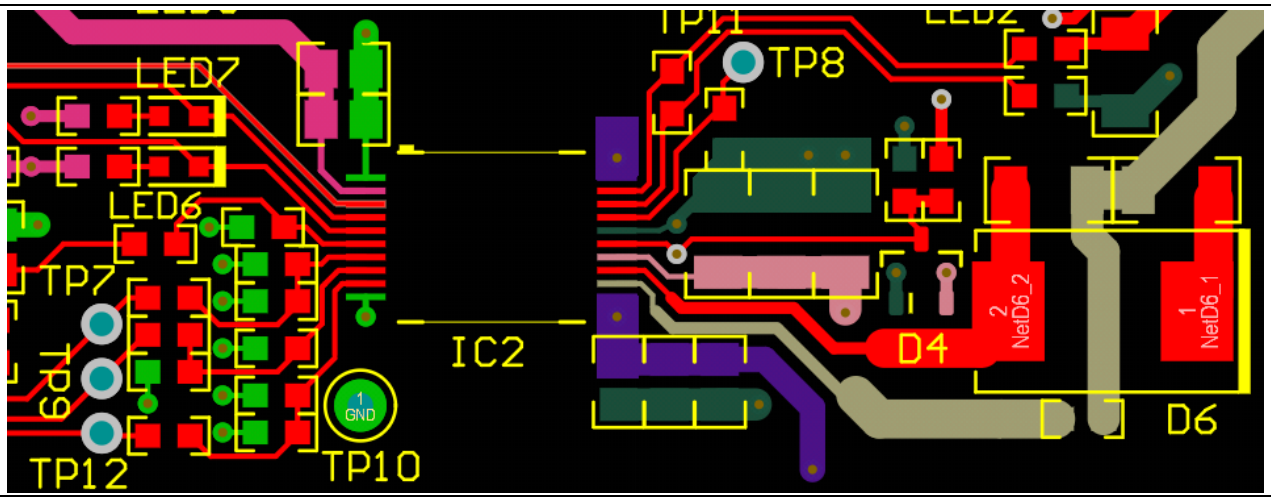



**Figure 54 Example layout for keep out zone**

# 8 References

[1] HybridPACK Automotive Power Modules (infineon.com)

[2] CoolSiC™ 1200 V SiC MOSFET (infineon.com)

[3] Silicon Carbide (SiC) MOSFETs using EiceDRIVER™ - Advanced Gate Drive Options (infineon.com)

[4] 02_Application Notes - All Documents (infineon.com)

# Revision history

| Document version | Date of release | Description of changes |
|---|---|---|
| 1.1 | 18.02.2021 | Entire document: Editorial changes<br>Chapter 3.3 updated: DESAT below GND more details added |
| 1.0 | 18.12.2020 | Initial version |
| | | |
| | | |

**Trademarks**
All referenced product or service names and trademarks are the property of their respective owners.

**Edition 2021-02-18**

**Published by**

**Infineon Technologies AG**

**81726 Munich, Germany**



**Do you have a question about this document?**

**Email:** erratum@infineon.com

**Document reference**
**Z8F80039908**

**IMPORTANT NOTICE**

The information contained in this application note is given as a hint for the implementation of the product only and shall in no event be regarded as a description or warranty of a certain functionality, condition or quality of the product. Before implementation of the product, the recipient of this application note must verify any function and other technical information given herein in the real application. Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind (including without limitation warranties of non-infringement of intellectual property rights of any third party) with respect to any and all information given in this application note.

The data contained in this document is exclusively intended for technically trained staff. It is the responsibility of customer's technical departments to evaluate the suitability of the product for the intended application and the completeness of the product information given in this document with respect to such application.

For further information on the product, technology delivery terms and conditions and prices please contact your nearest Infineon Technologies office (**www.infineon.com**).

**WARNINGS**

Due to technical requirements products may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies office.

Except as otherwise explicitly approved by Infineon Technologies in a written document signed by authorized representatives of Infineon Technologies, Infineon Technologies' products may not be used in any applications where a failure of the product or any consequences of the use thereof can reasonably be expected to result in personal injury.