EiceDRIVER™ and CoolMOS™ CFD2 Join for High Efficiency in Refrigeration

Home appliances, which run 24h and 7 days a week, have high efficiency requirements. Therefore, the use of MOSFETs is preferred over IGBTs. Modern MOSFET technologies based on the superjunction principle are nevertheless difficult to control in motor drive applications. This article describes the basic considerations for a successful gate drive circuit design and explains the benefits of combining EiceDRIVER™ ICs and CoolMOS™ CFD2.

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Commutation cell analysis of BLDC drives

A half-bridge cell as depicted in Figure 1 is enough to study the switching behaviour of all FETs. S1 and S2 are switching in a buck configuration, S4 is turned on permanently to provide the return current path. S1 is the active switch. The inductor current ramps up when S1 is turned on. S2 is the rectifier switch, its body diode carries the inductor current when S1 is off and the inductor current ramps down. This mode of operation takes place for one third of the motor's cycle. Then the same operation moves to the next half-bridge. The switch mode operation of MOSFETs causes high *dv/dt* and *di/dt*.

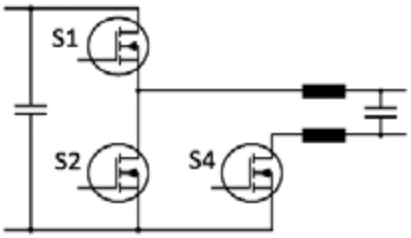

Figure 1: Switching cell

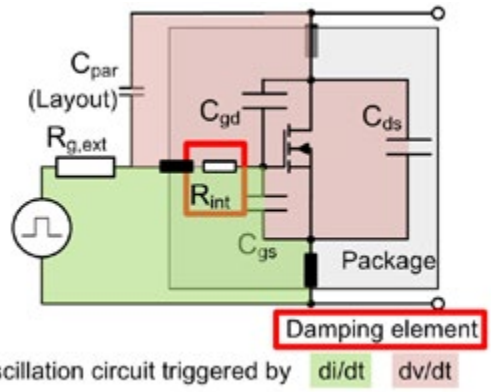

Figure 2: Parasitic elements of the MOSFET, package, layout and driver

A major risk of high *dv/dt* is shoot through. S1 is turned on and the resulting *dv/dt* across S2 couples to its gate and a voltage spike appears. If the coupling spike is high enough to reach the FET's gate threshold voltage, then both FETs in the bridge will be on for a short period of time, causing failures also in components such as shunt resistors or electrolytic capacitors.

Another risk is gate oscillation, which can be triggered at turn-on. High *di/dt* causes a voltage drop across the source inductance of the FET's package and layout. This voltage forms a negative feedback to the driving voltage, causing the FET's gate to resonate as depicted in Figure 3.

Additionally, high *dv/dt* at turn-off can couple to the gate through the drain-gate capacitance, causing oscillations.

These concerns are related to the FET's parameters, package and layout parasitics as shown in Figure 2. These have to be addressed by the gate driver design.

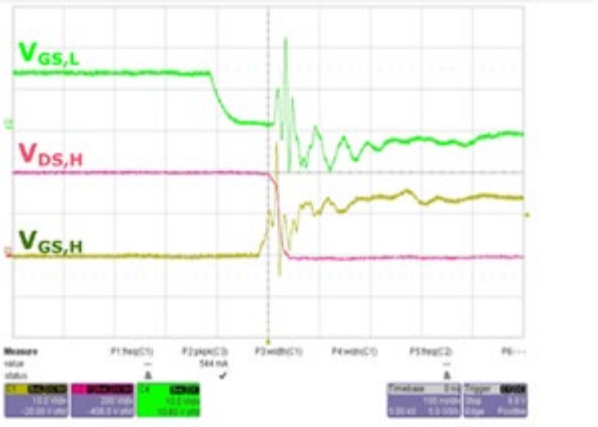

Figure 3: Strong oscillations during turn-on of a MOSFET

Origin of *dv/dt* and application effects

The *dv/dt* takes place during the charging period of the reverse capacitance C_{rss}, according to Figure 2 represented by the charge Q_{gd}. Hence, the C_{gd} value and the charging current level are two factors that affect *dv/dt*. Higher gate resistance R_g value means charging C_{rss} with lower current which extends the miller plateau time and reduces *dv/dt*.

The current change rate dI_{rec}/dt during reverse recovery of the MOSFET´s body diode generates a voltage across the parasitic source inductance which is a positive feedback to the driving voltage. It causes a faster charging of C_{rss} and higher *dv/dt*. Diodes with snappy recovery behavior lead to higher *dv/dt*. Moreover, the snappiness increases the voltage overshoot on S2, caused by the loop inductance.

During turn-off, the non-linear capacitance C_{oss} in Super-Junction FETs like CoolMOS™ CFD2 and the low C_{oss} values at high voltages V_{ds} lead to increased *dv/dt*. This provides a low switching loss and fast voltage transition but also requires careful layout- and gate driver design techniques considering the higher *dv/dt*.

Proposed gate circuit design for CoolMOS™ CFD2

Figure 4 shows a proposed schematic using CoolMOS™ IPD65R420CFD. Mainly a capacitor C_{ds}=0.47nF is added to each bridge´s switch node to limit and linearize the *dv/dt*. This is the most reliable approach to prevent the shoot-through and resonance problems. In motor drive applications, the typical switching frequency is low, therefore the added capacitor C_{ds} only has a minor impact on the switching losses. Other driving parameters are chosen considering:

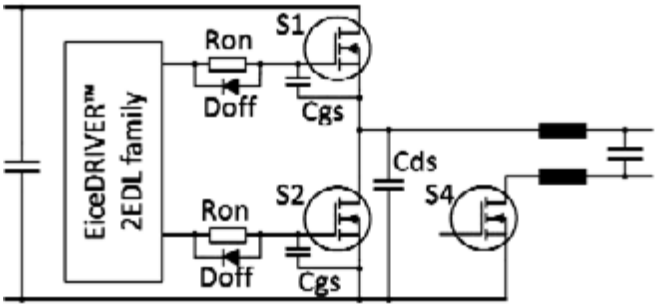

Figure 4: Proposed gate circuit schematic for CoolMOS™ CFD2 using EiceDRIVER™2EDL family

- R_{on} = 1000 Ω → slower turn on, longer plateau, reduced *dv/dt*.
- R_{off} = 0 Ω → Lower impedance to GND when turned off, lower voltage coupling spike.
- C_{gs} = 0.47nF → reduced C_{rss}/C_{iss} ratio, reduced drain-gate or Miller coupling gain.
- C_{ds} = 0.47nF → controlled / linearized *dv/dt* at turn on, this has the benefit of removing gate oscillation and reduce EMI.

The circuit is operated by a 2EDL05N06PF EiceDRIVER™ IC. Based on Infineon´s SOI technology, it provides excellent robustness against negative transient voltages [3]. The excellent properties of the integrated bootstrap diode supports the requirements of high power density and cost-performance ratio.

Layout recommendations

Figure 5 depicts a layout with minimized stray inductance due to the short distance between high side source terminal and low side drain terminal. The low side transistors on the bottom layer are shifted to the left side with respect to the high side transistors on the top layer. This leads to a thermal decoupling of both transistors. Furthermore, the low side transistors move even closer to the respective gate resistors. The shift also allows that the drain terminals of the low side transistors move directly underneath the source terminals, so that an appropriate number of vias provides a close connection to the high side source terminals. Hence, the loop inductance is minimized. A double sided assembly can be avoided when placing the low side transistors appropriately onto the top layer. This of course will lead to higher area consumption.

In general, these layout guidelines are recommended for reducing noise and resonance in the gate drive loop:

- Gate driver as close as possible to the gate.
- Minimum external capacitance gate to drain.
- Slow down *dv/dt* by properly choosing gate resistor R_g.
- Separate power ground from gate driver ground.
- R_g as close as possible to the gate pin.
- Use thick trace between gate driver and gate.

The physical proximity of the gate resistors to the gate terminals in combination with the reduced stray inductances leads to an improved performance and excellent switching behavior of the CoolMOS™ transistors. A turn-on waveform of the proposed driving circuit design is given in Figure 6. It shows a clean gate signal free of oscillations and the drain-source voltage slowly ramping down to 0V during the Miller plateau region, too.

The same behavior can be expected for the other two switching bridges given that the layout and driving circuit is the same.

Conclusion

CoolMOS™ CFD2 offers efficiency benefits in motor drive applications. The proposed gate drive circuit design using the EiceDRIVER™ 2EDL family ensures an oscillation-free switching. This leads to the conclusion that CoolMOS™ CFD2 can be efficiently and reliably operated in drives systems. Additionally, Infineon´s SOI technology which is used for the 2EDL family provides a high robustness with respect to *dv/dt* in motor drive applications and an excellent controllability of CoolMOS™ CFD2.

References

1. R. Mente, F. Di Domenico, M.A. Kutschak, A. Steiner: CoolMOS™ CFD2 first 650 V rated super junction mosfet with fast body diode suitable for resonant topologies, Application Note, Infineon Technologies, February 2011.
2. W. Choi, D. Son, M. Hallenberger S. Young: Driving and Layout Requirements for Fast Switching MOSFETs, Fairchild Semiconductor Power Seminar 2010-2011, Fairchild, 2011.
3. J. Song, W. Frank: Robustness of level shifter gate driver ICs concerning negative gate voltages; Proceedings of PCIM 2015, Nuremberg, Germany, 2015.

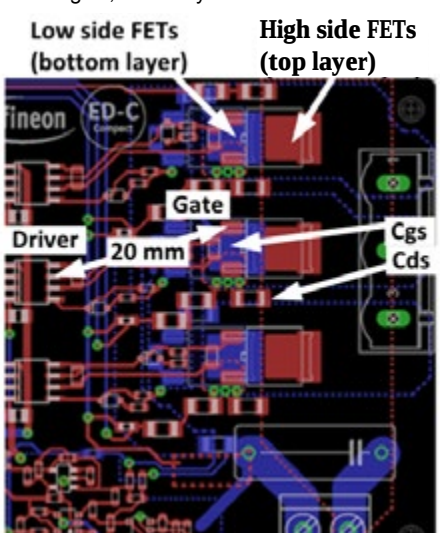

Figure 5: Example of a layout with minimized stray inductances by means of double side assembly

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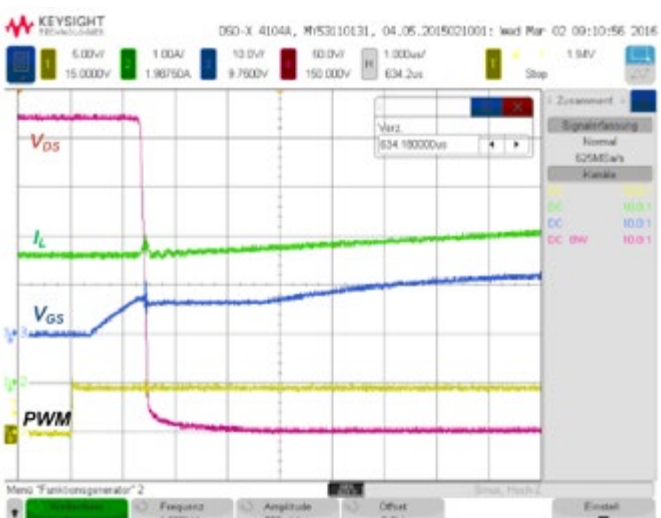

Figure 6: Turn-on waveforms at DC-link voltage V_{DC} = 320 V and load current I_L = 2.5 A. V_{DS} (red, 50 V/div), I_L (green, 1 A/div), V_{GS} (blue, 10 V/div), PWM (yellow, 5 V/div), time scale 1 µs/div]