EZ-PD™ CCG7SC multiport charger and adapter solution (REF_CCG7SC_120W_3C) test report

Product_sales code – REF_CCG7SC_120W_3C

Devices – EZ-PD™ CCG7SC

About this document

Scope and purpose

This test report provides test results of EZ-PD™ CCG7SC USB Type-C Power Delivery (PD) and buck-boost controller-based 120 W 3-port adapter solution (REF_CCG7SC_120W_3C).

Intended audience

This test report is intended for the charger and adapter applications hardware designers using EZ-PD™ CCG7SC USB Type-C PD and buck-boost controller.

Abbreviations and definitions

Table 1 Abbreviations

Abbreviation	Definition
CC-CV	Constant current - constant voltage
CE	Conducted emission
CH'x'	Oscilloscope channel numbers
DCM	Discontinuous current mode
DP/DM	USB data positive/data negative lines
DUT/EUT	Device under test/equipment under test
FCCM	Forced continuous conduction mode
FET	MOSFET (metal oxide semiconductor field effect transistor)
Io/I_{OUT}	Output current of the DUT
NGDO	NFET gate driver output
OCP	Overcurrent protection
OVP	Overvoltage protection
P1/P2/P3	Port #1/Port #2/Port #3
PAT	Power adapter tester
PDO	Power delivery output
P-P	Peak-to-peak
PPS	Programmable power supply
PSM	Pulse skip mode
SCP	Short-circuit protection

SW1	Buck converter switch node
UI	User interface
V_{BUS_C}	Bus voltage at USB Type-C
V_{BUS_C}/V_{OUT}	Output voltage of the DUT
V_{IN}/V_{IN_DC}	Input DC voltage to the DUT
USB PD	Universal Serial Bus Power Delivery

References

[1] USB Implementers Forum, Inc.: *Document Library*

[2] USB Implementers Forum, Inc.: *USB Type-C and connector specification (Release 2.2)*

[3] Infineon Technologies AG: EZ-PD™ Configuration Utility

[4] Infineon Technologies AG: *EZ-PD™ CCG7DC Dual-port USB-C Power Delivery & DC-DC controller (Document number: 002-32352)*

[5] Infineon Technologies AG: *EZ-PD™ CCG7SC Single-port USB-C Power Delivery & DC-DC controller (Document number: 002-35643)*

[6] Infineon Technologies AG: EZ-PD™ CCG7xC controller based forced buck power stage design calculator (*Document number:* 002-37312)

[7] Infineon Technologies AG: Hardware design guidelines for EZ-PD™ CCG7XC in multiport charger and adapter applications (*Document number: 002-37425*)

[8] *XDPS2221* – Driving giGaNtic performance in adapters and chargers – industry's first PFC + hybrid flyback combo IC

Table of contents

Table of contents

Table of contents

1 Introduction

The EZ-PD™ CCG7SC 120W 3-port adapter solution (REF_CCG7SC_120W_3C) test report provides the electrical performance parameters like efficiency, ripple, regulation, constant voltage, constant current operation, output current transient response, output voltage transition, startup turn-on delay, startup rise time, and fault protections. This test report also provides the thermal performance of REF_CCG7SC_120W_3C at room temperature.

EZ-PD™ CCG7SC is a highly integrated single-port USB Type-C PD solution with an integrated buck-boost controller. Following are the key features of EZ-PD™ CCG7SC:

- Complies with the latest USB Type-C and USB-PD specifications, and is targeted at charger and adapter applications.
- CCG7SC integration reduces the bill of materials (BOM); additionally, provides the footprint-optimized solution for the charger and adapter
- CCG7SC has integrated gate drivers for V_{BUS} NFET on the provider path or for the buck bypass switch control.
- Includes hardware-controlled protection features on the V_{BUS}
- Supports a wide input voltage range (4 V to 24 V with 40-V tolerance) and programmable switching frequency (150 kHz to 600 kHz) in an integrated PD solution
- Integrates monitoring, protection, and communication features that are needed to build a robust charger and adapter USB-C charging system

CCG7SC is the most programmable USB-PD solution with an on-chip 32-bit Arm® Cortex®-M0 processor, 128 kB flash, 16 kB RAM, and 32 kB ROM that leaves most of the flash available for user application. It also includes various analog and digital peripherals such as analog to digital converters (ADCs), pulse-width modulators (PWMs), I^2C/SPI/UART interfaces, and timers. The inclusion of a fully programmable MCU with analog and digital peripherals allows the implementation of custom system management functions such as power throttling, load sharing, temperature monitoring, and fault logging or event data recording.

The Power Delivery (PD) technology is designed to provide the fastest charging possible through a USB Type-C (USB-C) cable. The USB-PD Standard Power Range (SPR) standard defines the maximum power that can be delivered over a USB-C cable up to 100 W. This allows for providing multiple USB-C ports (Figure 1) on universal AC-DC adapters that can charge a wide range of devices, from smartphones to gaming laptops, power tools, and even e-bikes.

However, these new requirements for higher power and multiport have presented challenges for the converter topologies used until now. Electromagnetic compatibility, power factor correction, standby power, and average efficiency are just a few factors that need to be considered to ensure that the chargers and adapters are both effective and efficient. The size (and consequently, the power density), as well as load sharing and scaling up multiple ports, have also become more critical factors for design engineers and users. The power efficiency of USB-C chargers and adapters plays a crucial role in determining their power density. Hence, converter topology, usage model, integration, and flexibility of controller functionalities are all key factors to consider when selecting the right adapter architecture for your needs.

A typical block diagram of a multiport adapter is illustrated in Figure 1. The front-end AC-DC converter is responsible for producing the requested output voltage while ensuring power factor correction (PFC) at the front end for up to 120 W of power. On the other hand, the buck converter (connected at the output of the AC-DC converter) ensures that the defined USB-C PD specifications and performance are met for multiport adapter applications.

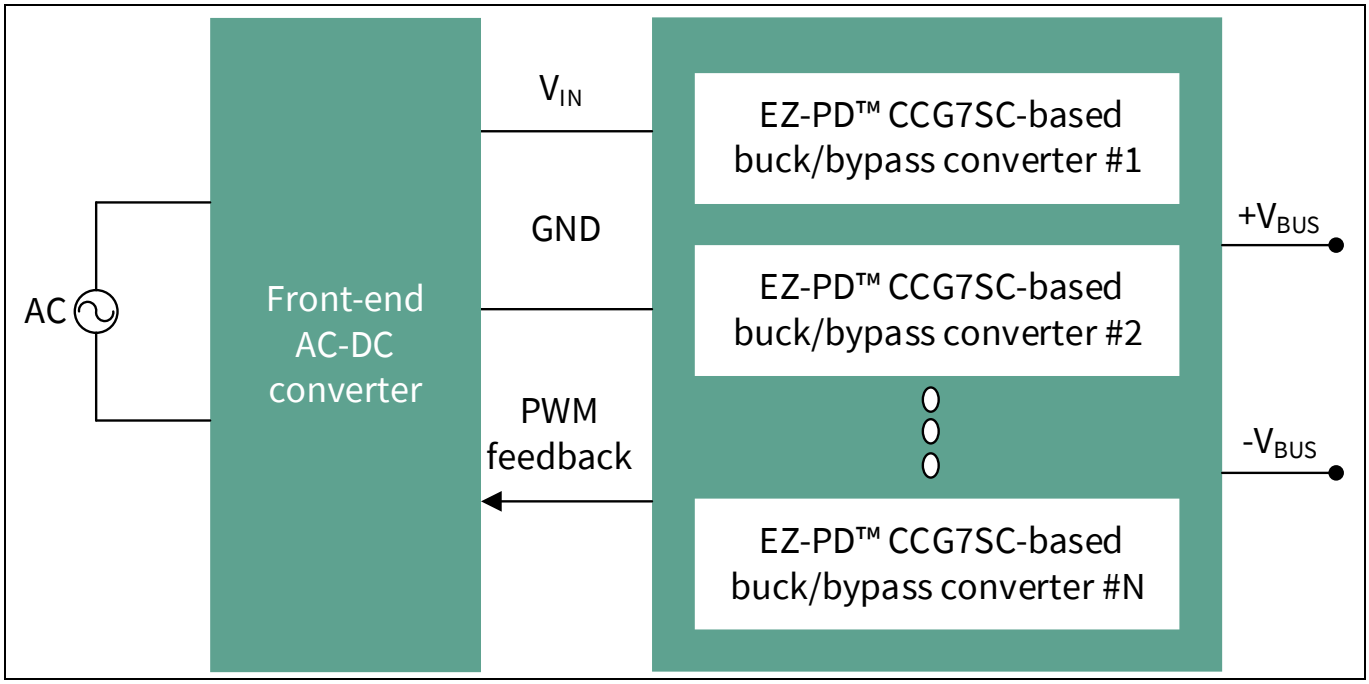


Figure 1 High-level block diagram of a multiport adapter

The XDP™ XDPS2221 [8] controller is a highly integrated device including the valley-switching PFC controller, the HFB (asymmetrical half-bridge) controller and three gate drivers for the main switches. The internal handshaking between the PFC and HFB controller and the adaptive bus voltage setting makes this controller a perfect fit for applications with wide AC input and wide output voltage range, such as USB-PD adapters and battery chargers. The engineering report XDP™ 140W USB-PD reference board with PFC + hybrid flyback combo IC XDPS2221 can be referenced for additional details [8].

The EZ-PD™ CCG7SC is designed to support a single USB PD/PPS port, featuring an integrated buck controller and gate driver, allowing easy scaling to multiport output.

A high-level block diagram of the EZ-PD™ CCG7SC-based adapter and charger solution is shown in Figure 2 and Figure 3.

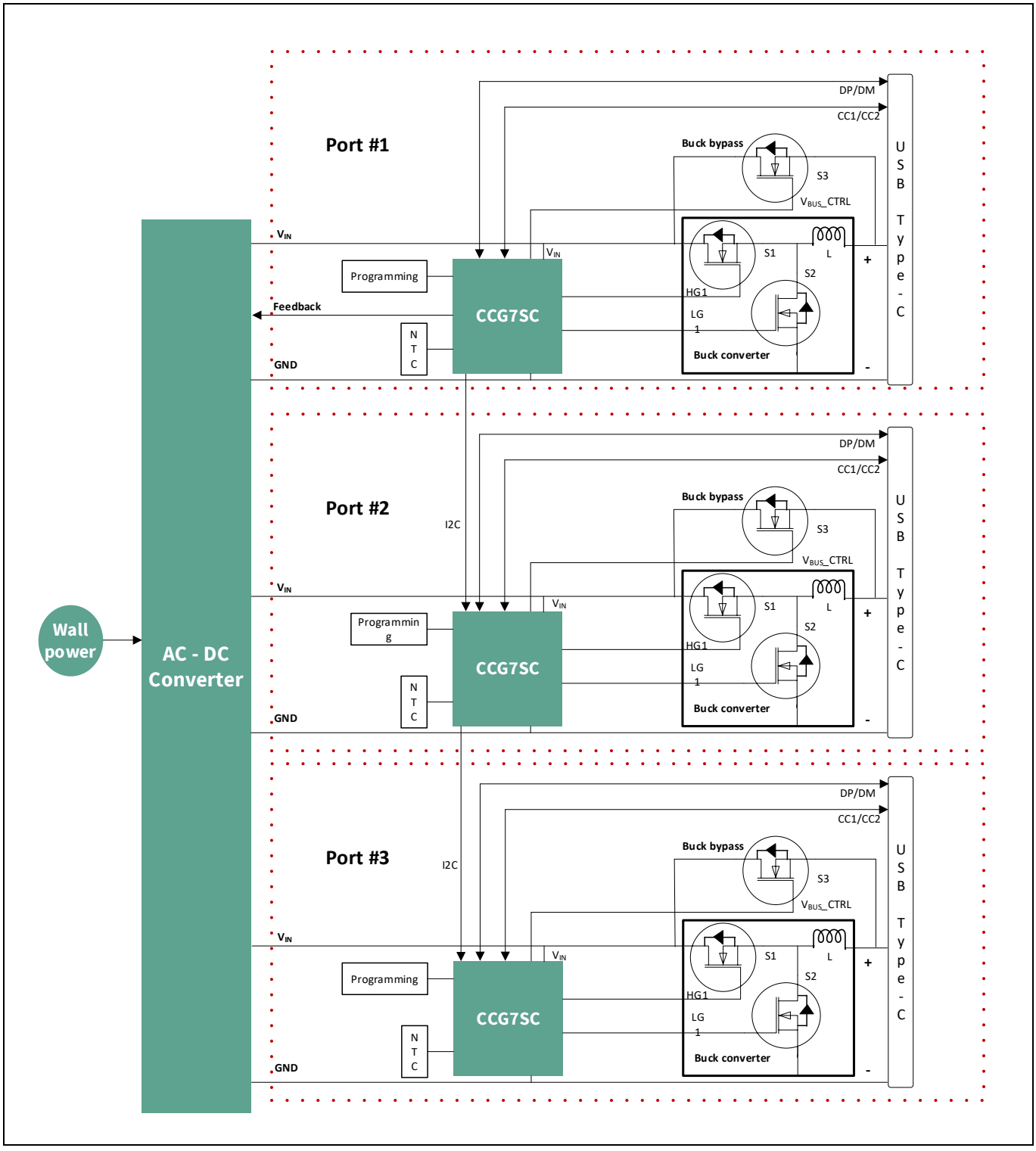


Figure 2 High-level block diagram of EZ-PD™ CCG7SC based charger and adapter solution

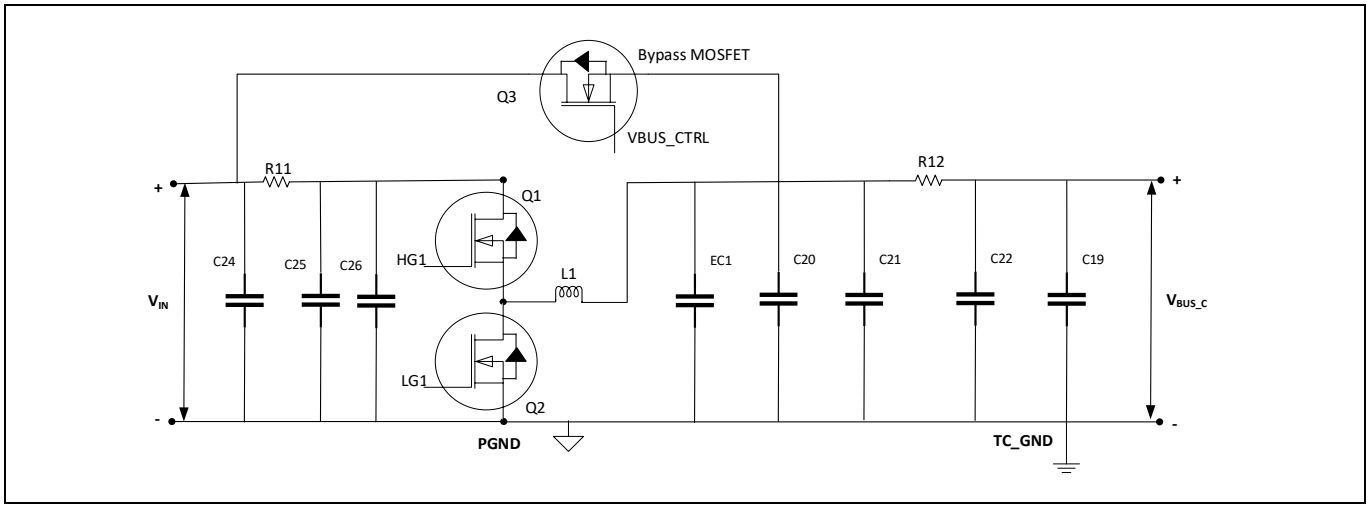


Figure 3 High-level block diagram of EZ-PD™ CCG7SC buck topology with bypass FET

Table 2 Critical components BOM

Designator	Description	Part number	Manufacturer
U1	EZ-PD™ CCG7SC single-port USB Type-C with PD and buck-boost controller	CYPD7171-40LQXQ	Infineon Technologies
Q1, Q2, Q3	MOSFET N-CH 40 V 15 A/40 A	BSZ063N04LS6ATMA1	Infineon Technologies
L1	6.8 µH Shielded Drum Core, Wirewound Inductor 7.2 A 13.5mOhm	74439358068	Würth Elektronik
C20, C21, C24	CAP CER 10 µF 50V X7R 1206	CL31B106KBHNNNE	Samsung Electronics
C22	CAP CER 0.1 µF 50V X7R 0603	885012206095	Würth Elektronik
C19	4.7 µF 50V 0805	GRM21BZ71H475KE15K	Murata Electronics
C25, C26	CAP CER 4.7 µF 50V X7R 0805	CGA4J1X7R1H475K125AE	TDK Corporation
EC1	CAP ALUM POLY HYB 270UF 25V T/H	EEH-AZK1E271B]	Panasonic Electronic Components
R11	Current sense resistors - SMD 0.005 Ω 1% 1.5 W	KRL3216E-C-R005-F-T1	Susumu
R12	RES 0.005 Ω 1 W 0805 WIDE	KRL2012E-M-R005-F-T5	Susumu

Table 3 Test results description

Test results	Description
Single port power management test results of REF_CCG7SC_120W_3C	Port #1 performance results With REF_CCG7SC_120W_3C
Three port power management test results of REF_CCG7SC_120W_3C	3 ports performance results With REF_CCG7SC_120W_3C
Single port power management test results of XDPS2221 + REF_CCG7SC_120W_3C	Port #1 performance results With XDPS2221 + REF_CCG7SC_120W_3C
Three port power management test results of XDPS2221 + REF_CCG7SC_120W_3C	3 ports performance results With XDPS2221 + REF_CCG7SC_120W_3C

Table 4 Printed circuit board (PCB) details of REF CCG7SC_100W_R2 daughter board

PCB layer	Copper thickness	Details
Top layer	2 oz	Components, power traces
Second layer	2 oz	High-frequency traces, control signal traces
Third layer	2 oz	Ground layer
Bottom layer	2 oz	Components, power traces
Board size	–	33 mm x 21.66 mm
Board thickness	–	1.6 mm

Table 5 Printed circuit board (PCB) details of REF_CCG7SC_BASE_120W_3C_R2 baseboard

PCB layer	Copper thickness	Details
Top layer	2 oz	Components, power traces
Second layer	2 oz	High-frequency traces, control signal traces
Third layer	2 oz	Ground layer
Bottom layer	2 oz	Components, power traces
Board size	–	60.15 mm x 45 mm
Board thickness	–	1.6 mm

The EZ-PD™ CCG7SC-based multiport charger and adapter base board with three daughter boards is shown in Figure 4. The base board with three daughter boards can operate up to 120 W and each daughter board can operate up to 100 W.

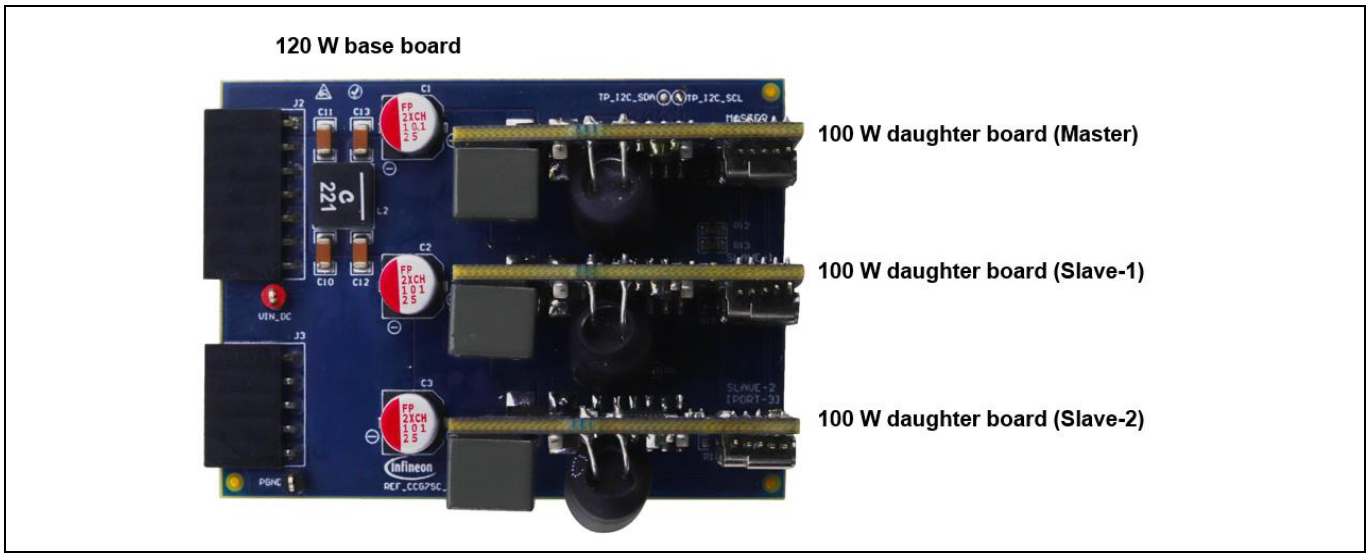


Figure 4 EZ-PD™ CCG7SC multiport charger and adapter solution base board and EZ-PD™ CCG7SC 100 W daughter board

The EZ-PD™ CCG7SC controller-based standalone daughter board is shown in Figure 5. Each daughter board can deliver the power up to 100 W with a maximum load current of 5.0 A.

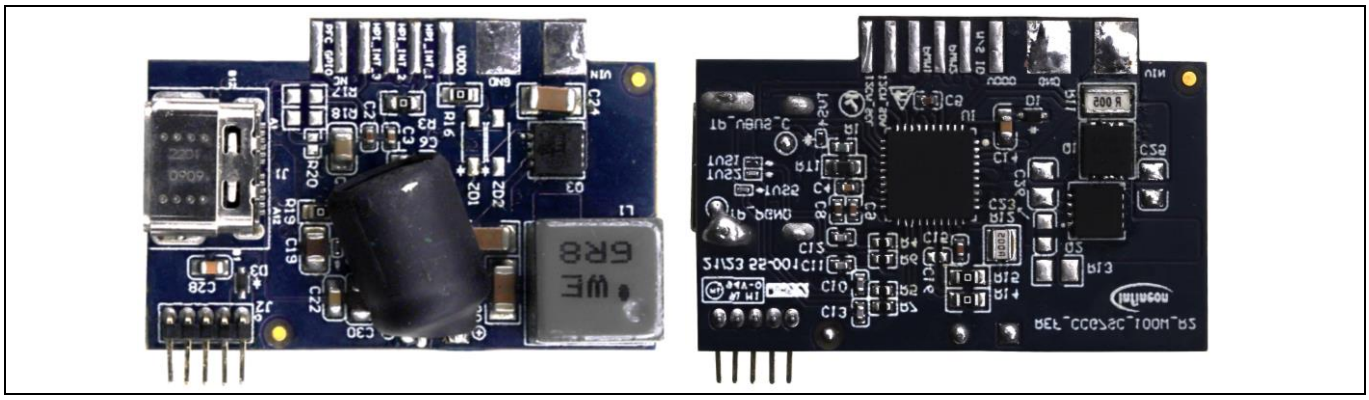


Figure 5 Standalone EZ-PD™ CCG7SC 100 W daughter board

The XDPS2221 + EZ-PD™ CCG7SC 3 port 120 W AC/DC charger and adapter is shown in Figure 6. Total power is 120 W, and each daughter board can deliver power up to 100 W with a maximum load current of 5.0 A.

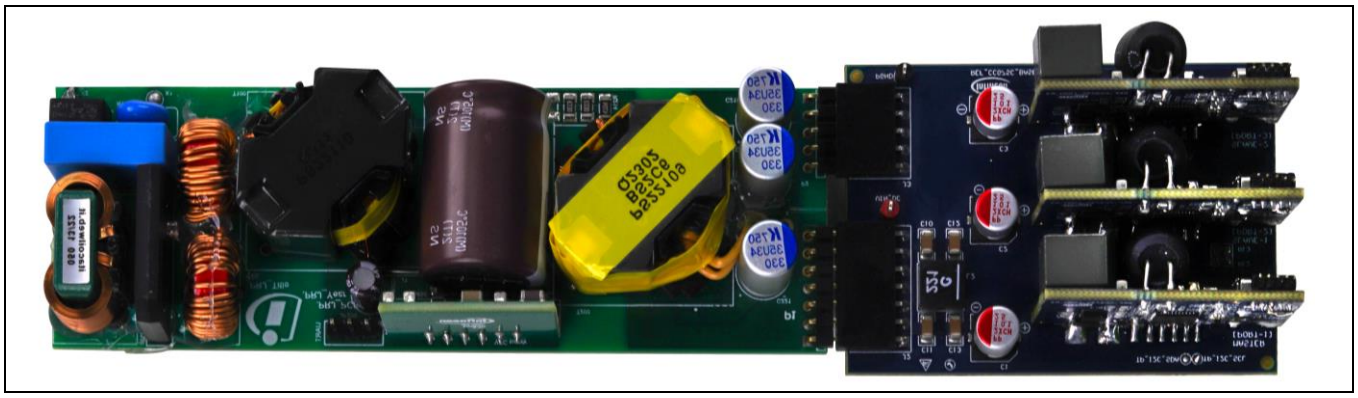


Figure 6 XDPS2221 + EZ-PD™ CCG7SC 3 port 120 W AC/DC charger and adapter

2 CCG7SC multiport charger and adapter solution (REF_CCG7SC_120W_3C) specifications

Table 6 Test specifications

Parameter	Value
Input voltage	5.0 V_{DC} – 22.5 V_{DC}
Max output power	120 W system power with base board + daughter boards 100 W on each daughter board with a max load current of 5.0 A
Output voltage	Fixed PDOs: 5.0 V/5.0 A, 9.0 V/5.0 A, 15.0 V/5.0 A, 20.0 V/5.0 A PPS: 3.3 V to 11.0 V, 5.0 A; 3.3 V to 16.0 V, 5.0 A; 3.3 V to 21.0 V, 5.0 A with PPS power limit
Peak efficiency	> 98%
Protections	1. Input overvoltage protection 2. Input undervoltage protection 3. V_{BUS_C} overvoltage protection (OVP) 4. V_{BUS_C} undervoltage protection (UVP) 5. Overcurrent protection (OCP) 6. Short-circuit protection (SCP) 7. Over temperature protection (OTP) 8. V_{BUS_C} to CC short protection
Charging standards supported	1. USB-C PD v3.1 including programmable power supply (PPS) mode 2. Apple charging 2.4 A 3. Qualcomm QC 2.0, 3.0, 4.0, 5.0 4. Samsung AFC 5. USB BC 1.2

3 Test setup

The REF_CCG7SC_120W_3C solution board, firmware version details, and CCG7SC configuration details are shown in Table 7.

Table 7 DUT hardware and software configurations

DUT contents	Description	Remarks
Hardware configuration		
REF_CCG7SC_120W_3C	Rev.2	Circuit schematics
Firmware		
Firmware version	Power_SDK_4.0	
CCG7SC configuration		
System clock	24 MHz	Default configuration
Gate drive strength – Pull-up drive strength: LG1 = 2.9 Ω, HG1 = 3.3 Ω Pull-down drive strength: LG1 = 3.1 Ω, HG1 = 3.4 Ω	0x7	Default configuration
Spread spectrum – triangle	10%	Default configuration (nominal switching frequency of 400 kHz)

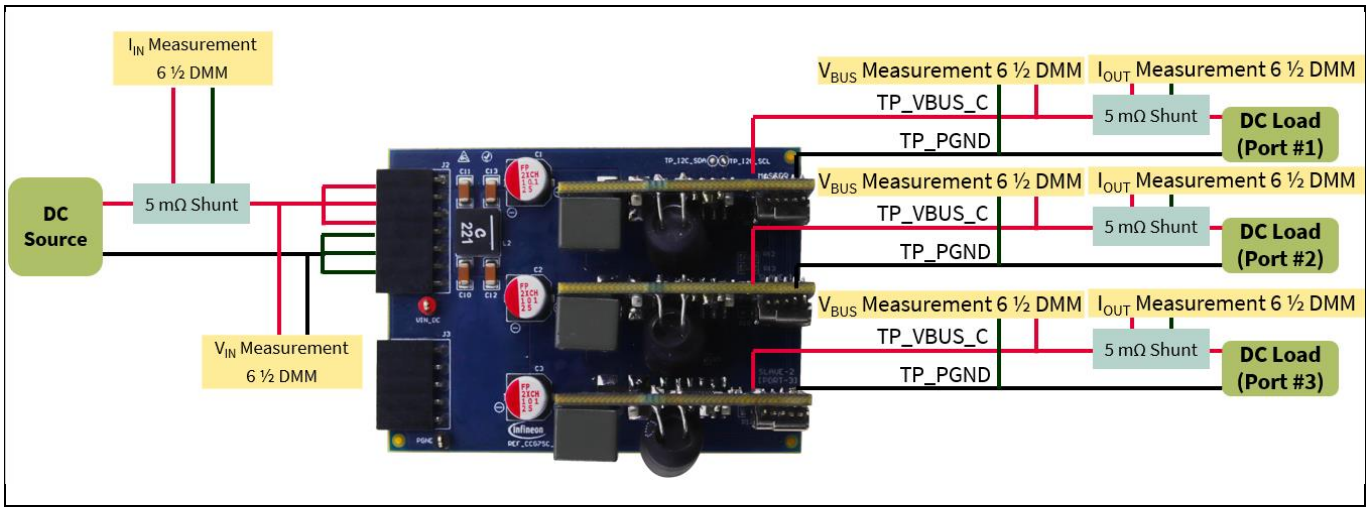


Figure 7 Test equipment connected to the standalone EZ-PD™ CCG7SC multiport charger and adapter solutions

3.1 DUT setup

The DUT is connected to a power adapter tester (PAT) (CCPROG PAT) using a USB Type-C cable. After a successful connection is established, the PAT UI does a PDO discovery and displays the results. The REF_CCG7SC_120W_3C solution board is pre-configured with seven PDOs:

- Fixed PDOs: 5 V/5 A, 9 V/5 A, 15 V/5 A, 20 V/5 A
- PPS: 3.3 V – 11 V, 5 A; 3.3 V – 16 V, 5 A; 3.3 V – 21 V, 5 A (PPS power limited)

You can either choose the suitable pre-configured PDO or configure it in the firmware. Tests in the following sections use pre-configured PDOs.

For more details on PAT tester, see USBCEE webpage.

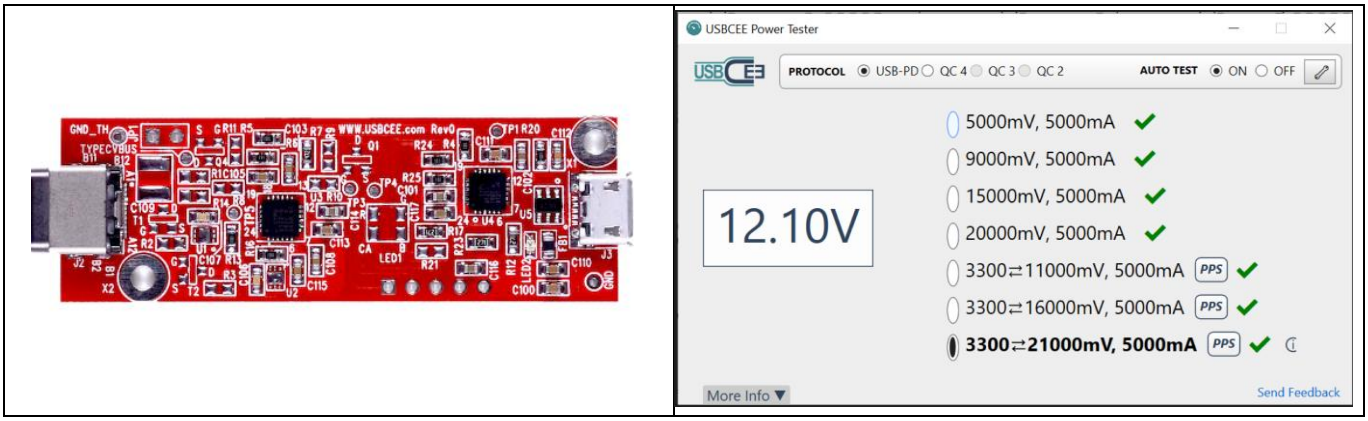


Figure 8 PAT tester and user interface

3.2 Test equipment

The test equipment used to measure the efficiency, ripple, regulation, and transient response are shown in Table 8.

Table 8 Test equipment details

Test setup	Description
Programmable DC source	GwINSTEK PSB 2400L
Oscilloscope	LECROY 8108HD
Data logger (I_{IN}, V_{IN}, V_{BUS}, and I_{OUT})	Keysight 34970 A
Electronic load	GwINSTEK PEL-3021
Input current (I_{IN} and I_{OUT}) measurement shunt	Vishay Y14730R00500B0R
Power meter	Hioki PW3335
AC source	GWinstek ASR2100

4 Single port power management test results of REF_CCG7SC_120W_3C

Efficiency captured using the test setup shown in the Appendix: Efficiency measurement test setup.

Here only port #1 (master port) was loaded with 5 A current.

4.1 Peak efficiency and full load efficiency table

Peak efficiency test results are tabulated in Table 9.

Table 9 Peak efficiency

V_{BUS_C} (V)	V_{IN} = 16.5 V	V_{IN} = 22.5 V
03.30 V	93.37% – 2.60 A	92.53% – 2.80 A
05.00 V	95.02% – 2.75 A	94.37% – 3.20 A
09.00 V	96.81% – 2.75 A	96.20% – 3.40 A
12.00 V	97.60% – 2.60 A	96.96% – 3.80 A
15.00 V	98.14% – 2.50 A	97.56% – 3.60 A
20.00 V	NA	97.76% – 4.40 A
21.00 V	NA	98.41% – 2.40 A

Note: Peak efficiency: 98.41% (At V_{IN}: 22.5 V_{DC}, V_{BUS_C}: 21 V, I_{OUT}: 2.4 A)

Full load efficiency test results are tabulated in Table 10.

Table 10 Full load efficiency

V_{BUS_C} (V)	V_{IN} = 16.5 V	V_{IN} = 22.5 V
3.30 V	92.49% – 4.75 A	91.7% – 5.00 A
5.00 V	94.38% – 5.00 A	93.93% – 5.00 A
9.00 V	96.44% – 5.00 A	96.01% – 5.00 A
12.00 V	97.26% – 4.75 A	96.81% – 5.00 A
15.00 V	97.73% – 5.00 A	97.42% – 5.00 A
20.00 V	NA	97.71% – 5.00 A
21.00 V	NA	98.22% – 4.60 A

4.2 Efficiency graphs

Efficiency measurements were taken at 22.5 V DC input to the DUT. V_{BUS_C} PDO, PPS voltages are 3.3 V, 5 V, 9 V, 12 V, 15 V, 20 V and 21 V, and 16.5 V DC input to the DUT. V_{BUS_C} PDO, PPS voltages are 3.3 V, 5 V, 9 V, 12 V, 15 V. The port was loaded from 0 A to the maximum rated output current of 5 A. The efficiency and power loss graphs are based on the test setup of Figure 95.

Efficiency, losses at 16.5 V DC input, V_{BUS_C} 3.3 V, 5 V, 9 V, 12V, 15 V and I_{OUT} 0 A to 5 A maximum on the port as shown in Figure 9.

Efficiency, losses at 22.5 V DC input, V_{BUS_C} 3.3 V, 5 V, 9 V, 12 V, 15 V, 20 V, 21 V, and I_{OUT} 0 A to 5 A maximum on the port as shown in Figure 10.

4.2.1 Efficiency and power losses at 16.5 V_{DC} input

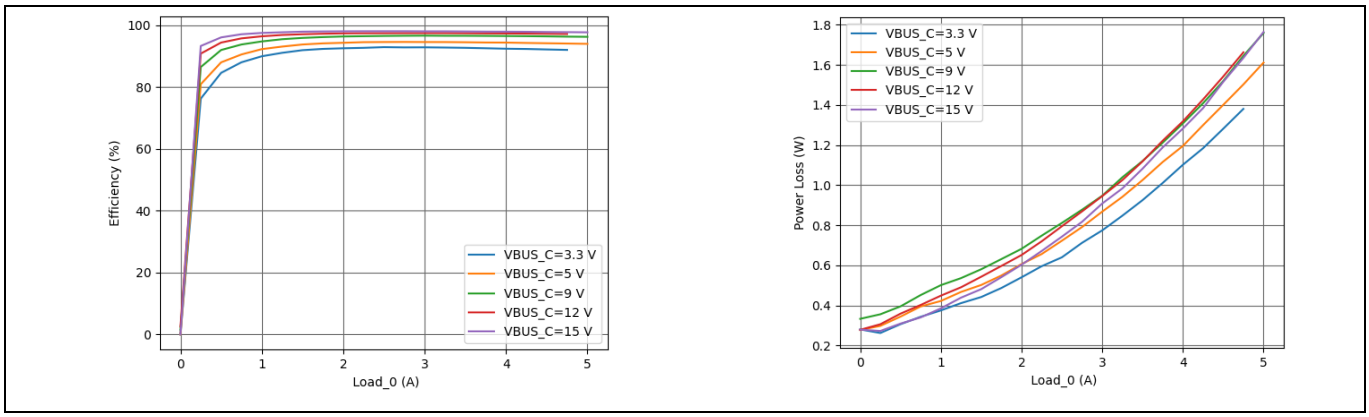


Figure 9 Efficiency and power losses at 16.5 V_{DC} input

4.2.2 Efficiency and power losses at 22.5 V_{DC} input

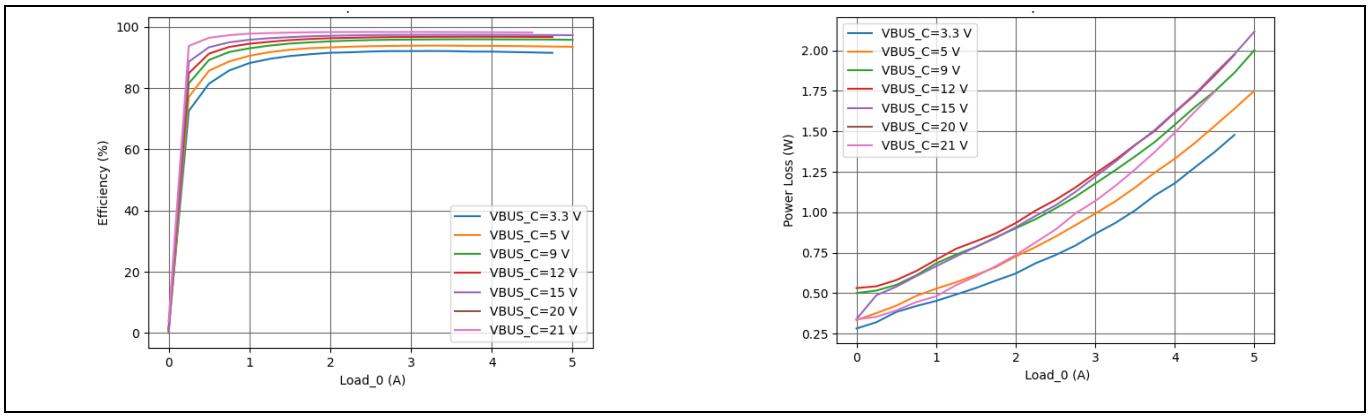


Figure 10 Efficiency and power losses at 22.5 V_{DC} input

4.3 Output voltage and current regulation

Output voltage regulation was measured both in the constant voltage (CV) and constant current (CC) modes.

4.3.1 Output voltage regulation (CV mode)

Output constant voltage regulation measured at 0 A and 5 A load currents are shown in Figure 11 and Figure 12.

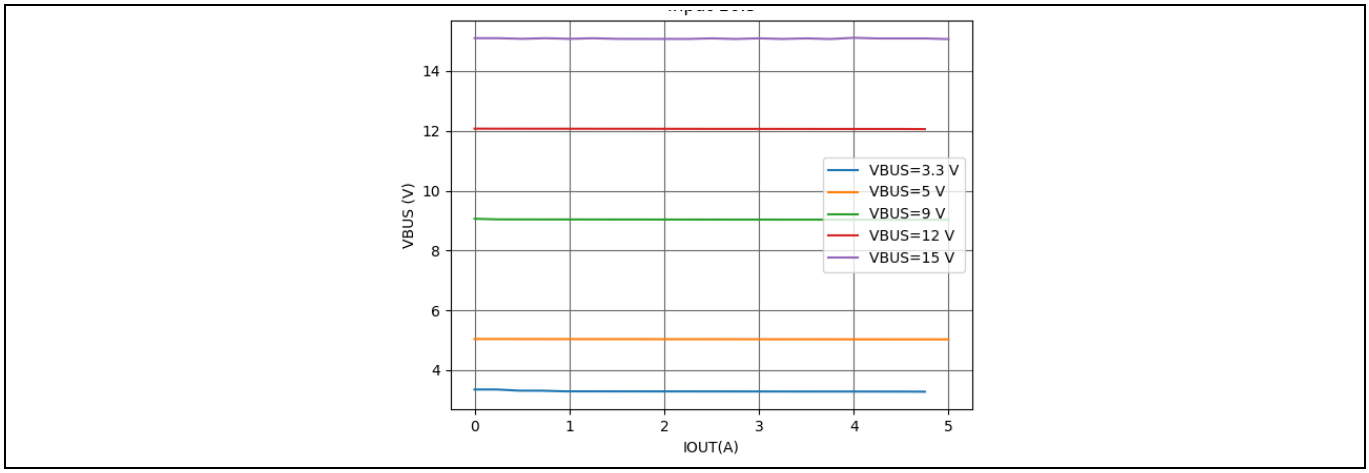


Figure 11 CV regulation at 16.5 V_{DC} input

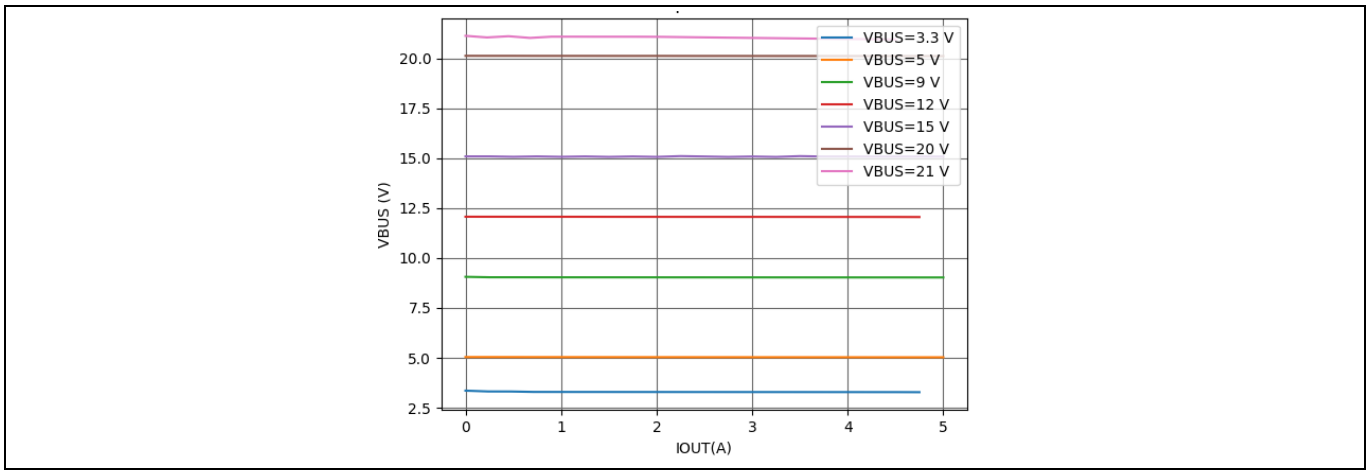


Figure 12 CV regulation at 22.5 V_{DC} input

4.3.2 Output current regulation (CC mode)

Output constant current (CC) regulation of port measured at 3 A and 5 A output currents are shown in Figure 13, Figure 14, Figure 15, and Figure 16.

4.3.3 CC regulation curve at 16.5 V_{DC} input and rated output current of 3 A

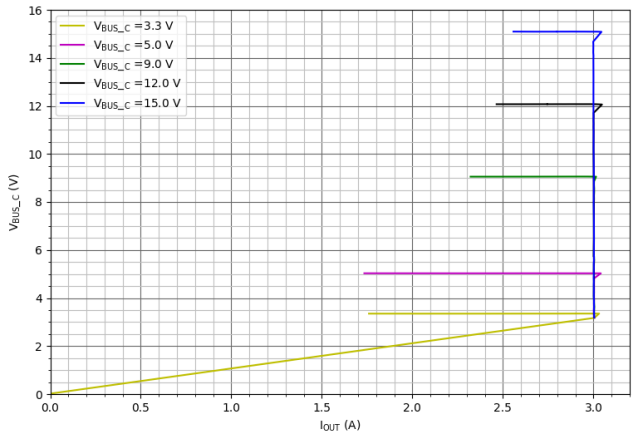


Figure 13 CC regulation curve at 16.5 V_{DC} input and 3 A output current

4.3.4 CC regulation curve at 22.5 V_{DC} input and rated output current of 3 A

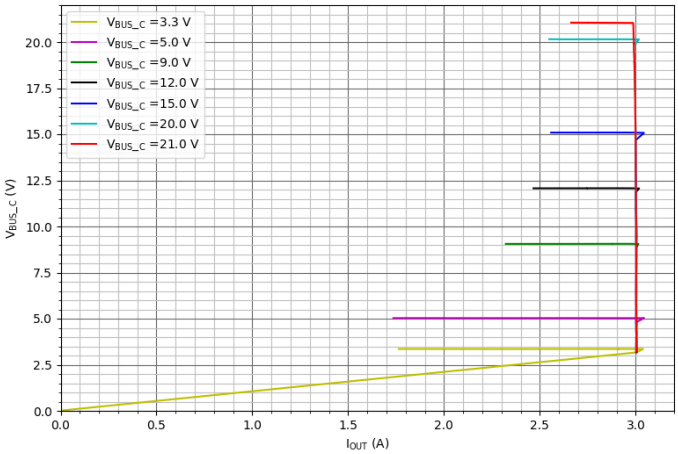


Figure 14 CC regulation curve at 22.5 V_{DC} input and 3 A output current

4.3.5 CC regulation curve at 16.5 V_{DC} input and rated output current of 5 A

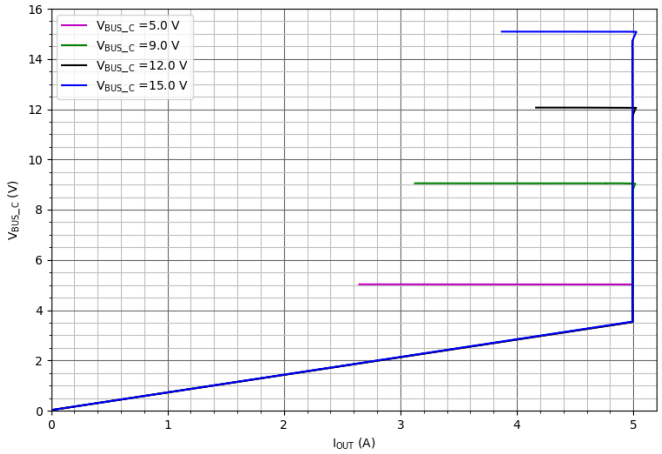


Figure 15 CC regulation curve at 16.5 V_{DC} input and 5 A (full load) output current

4.3.6 CC regulation curve at 22.5 V_{DC} input and rated output current of 5 A

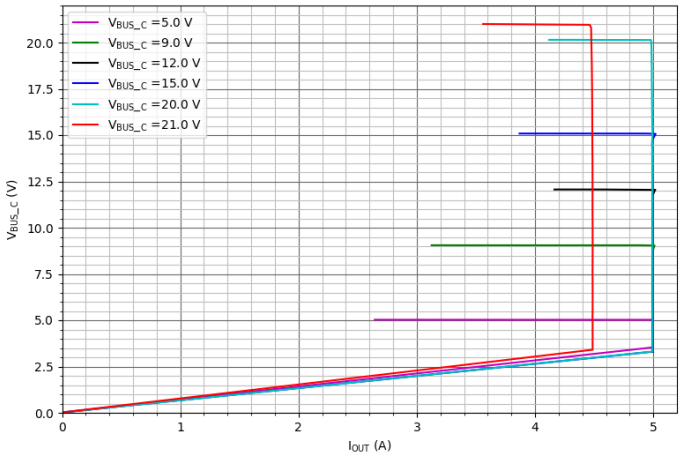


Figure 16 CC regulation curve at 22.5 V_{DC} input and 5 A (full load) output current

4.4 Output voltage regulation

Output voltage regulation measured at V_{IN} = 16.5 V_{DC}, 22.5 V_{DC}, V_{BUS_C} = 3.3 V, 5 V, 9 V, 12 V, 15 V, 20 V, 21 V; I_{OUT} = 0 A and 5 A are shown in Table 11 and Table 12.

Table 11 Regulation at 16.5 V_{DC} input

I_{OUT} (A)	V_{BUS_C} (V_{DC})	V_{IN} = 16.5 V % Regulation
0.00	03.355	2.25%
4.75	03.281	
0.00	05.042	0.24%
5.00	05.030	
0.00	09.060	0.35%
5.00	09.028	
0.00	12.071	0.12%
4.75	12.056	
0.00	15.095	0.21%
5.00	15.064	

Table 12 Regulation at 22.5 V_{DC} input

I_{OUT} (A)	V_{BUS_C} (V_{DC})	V_{IN} = 22.5 V % Regulation
0.00	03.357	2.35%
4.75	03.280	
0.00	05.042	0.24%
5.00	05.030	
0.00	09.061	0.36%
5.00	09.028	
0.00	12.071	0.12%
4.75	12.056	
0.00	15.095	0.07%
5.00	15.085	
0.00	20.133	0.06%
5.00	20.120	
0.00	21.136	0.88%
4.50	20.952	

4.5 Output voltage ripple measurement

Output voltage peak-to-peak ripple was measured across the output capacitors C19 using a short ground loop connected to the probe.

4.5.1 Output voltage ripple measurement test setup

Ripple has been measured using the oscilloscope probe as shown in Figure 17.

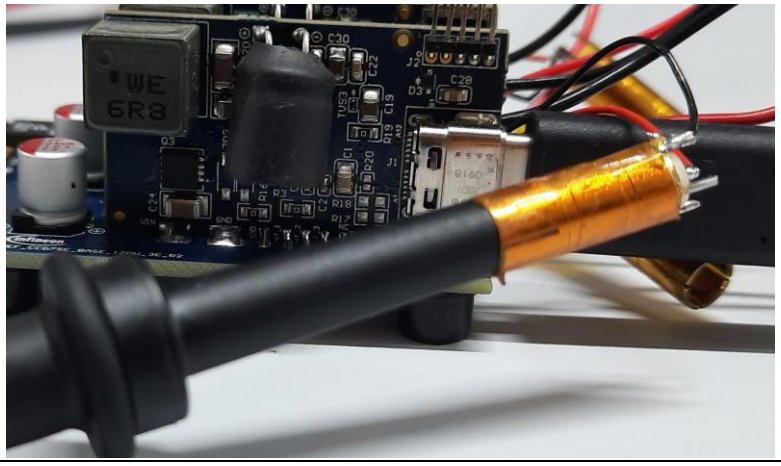


Figure 17 Output voltage ripple measurement test setup

4.5.2 Output voltage ripple peak-to-peak (mV)

Output voltage peak-to-peak ripple tabulated in Table 13 and Table 14.

Table 13 Peak-to-peak ripple (mV) at V_{IN} = 16.5 V

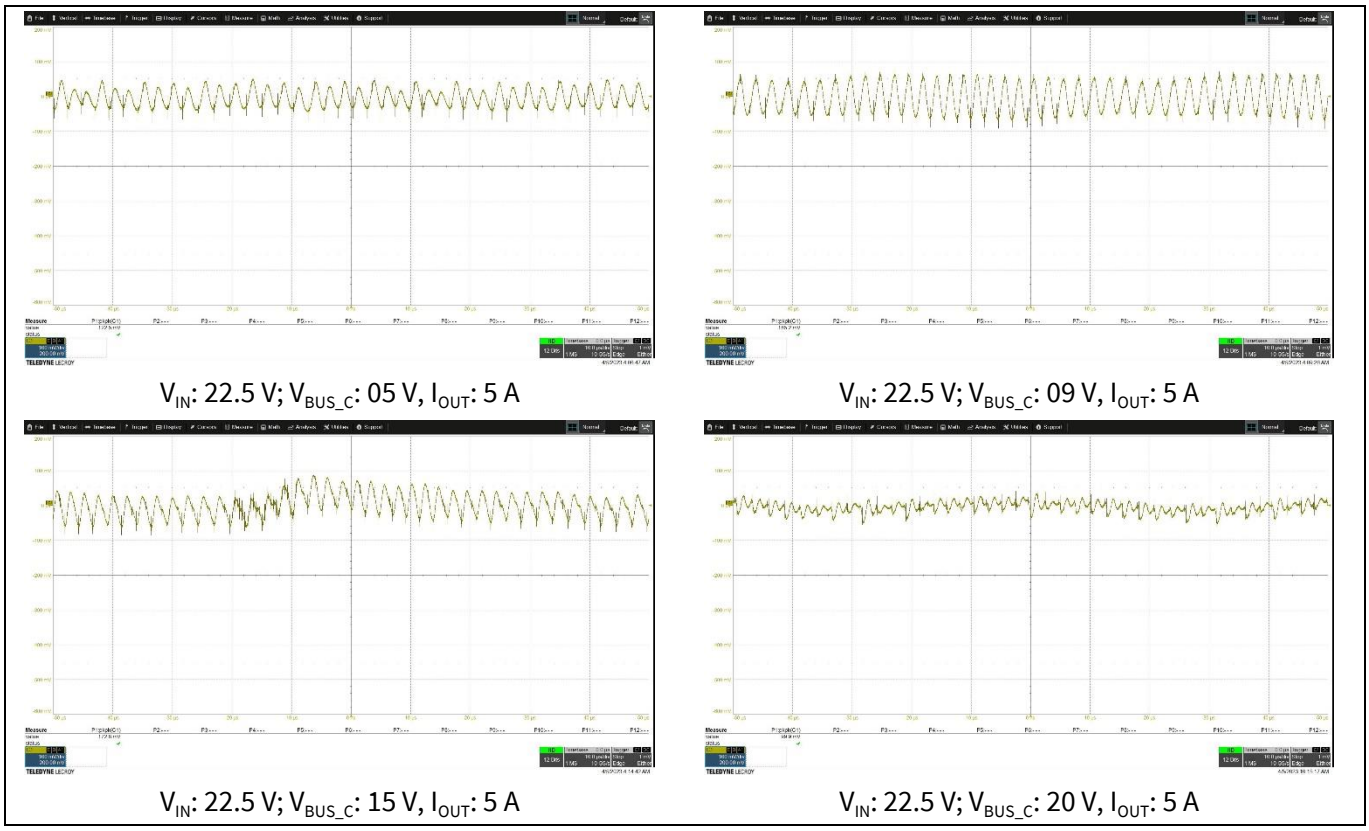
V_{BUS_C} – I_{OUT}	V_{IN} = 16.5 V Ripple (mV)
03.3 V – 0.00 A	079.037
03.3 V – 4.75 A	096.410
05.0 V – 0.00 A	100.419
05.0 V – 5.00 A	101.575
09.0 V – 0.00 A	103.259
09.0 V – 5.00 A	125.385
12.0 V – 0.00 A	119.321
12.0 V – 4.75 A	110.287
15.0 V – 0.00 A	107.255
15.0 V – 5.00 A	101.113

Table 14 Peak-to-peak ripple (mV) at V_{IN} = 22.5 V

V_{BUS_C} – I_{OUT}	V_{IN} = 22.5 V Ripple (mV)
3.3 V – 0.00 A	062.911
3.3 V – 4.75 A	125.116
05 V – 0.00 A	057.746
05 V – 5.00 A	127.364
09 V – 0.00 A	049.728
09 V – 5.00 A	139.546
12 V – 0.00 A	141.023
12 V – 4.75 A	150.789
15 V – 0.00 A	065.044
15 V – 5.00 A	142.141
20 V – 0.00 A	046.772
20 V – 5.00 A	121.376
21 V – 0.00 A	097.862
21 V – 4.75 A	088.238

4.5.3 Output voltage ripple peak-to-peak measurement graphs

Output voltage peak-to-peak ripple waveforms at full load are shown in Figure 18 and Figure 19.



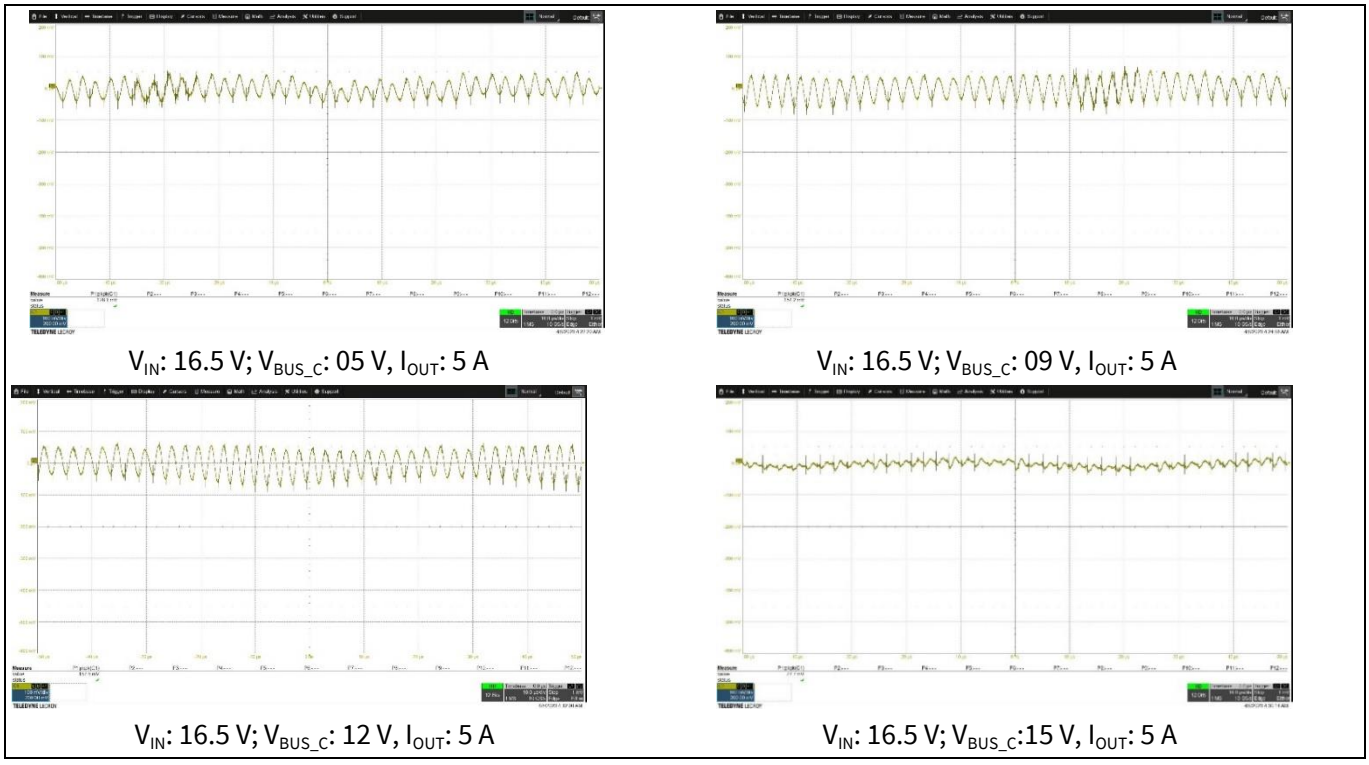
V_{IN}: 22.5 V; V_{BUS_C}: 05 V, I_{OUT}: 5 A

V_{IN}: 22.5 V; V_{BUS_C}: 09 V, I_{OUT}: 5 A

V_{IN}: 22.5 V; V_{BUS_C}: 15 V, I_{OUT}: 5 A

V_{IN}: 22.5 V; V_{BUS_C}: 20 V, I_{OUT}: 5 A

Figure 18 Ripple measurement – input voltage: 22.5 V_{DC} (CH1: V_{BUS_C})



V_{IN}: 16.5 V; V_{BUS_C}: 05 V, I_{OUT}: 5 A

V_{IN}: 16.5 V; V_{BUS_C}: 09 V, I_{OUT}: 5 A

V_{IN}: 16.5 V; V_{BUS_C}: 12 V, I_{OUT}: 5 A

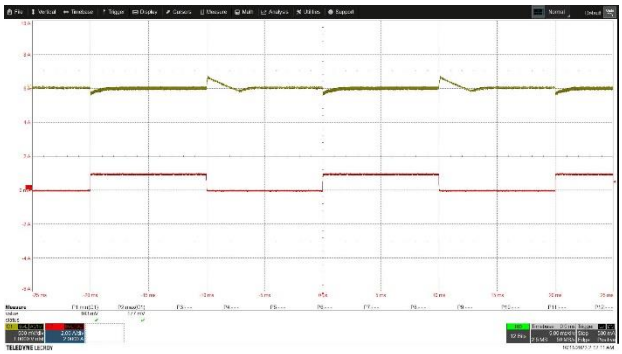
V_{IN}: 16.5 V; V_{BUS_C}:15 V, I_{OUT}: 5 A

Figure 19 Ripple measurement – input voltage: 16.5 V_{DC} (CH1: V_{BUS_C})

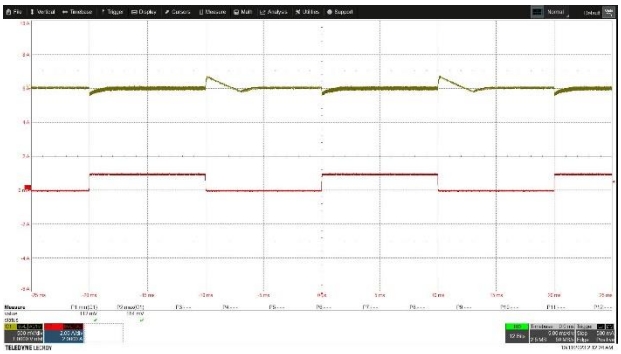
4.6 Output voltage dynamic response waveforms

V_{IN}: 22.5 V, output voltage response when the output current is from 0 A – 1 A – 0 A is shown in Figure 20.

V_{IN}: 22.5 V, output voltage response when the output current is from 3.5 A – 4.5 A – 3.5 A is shown in Figure 21.

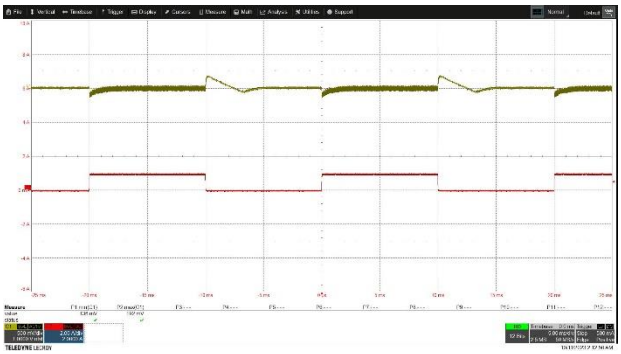


V_{BUS_C}: 3.3 V; (CH1: V_{BUS_C}; CH7: I_{OUT})



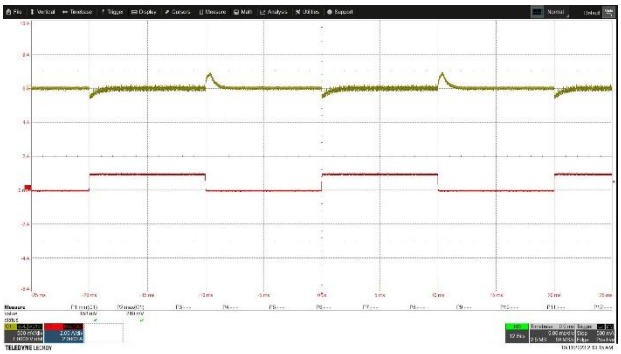
V_{BUS_C}: 5.0 V; (CH1: V_{BUS_C} ; CH7: I_{OUT})

V_{BUS_C}: 9.0 V; (CH1: V_{BUS_C}; CH7: I_{OUT})



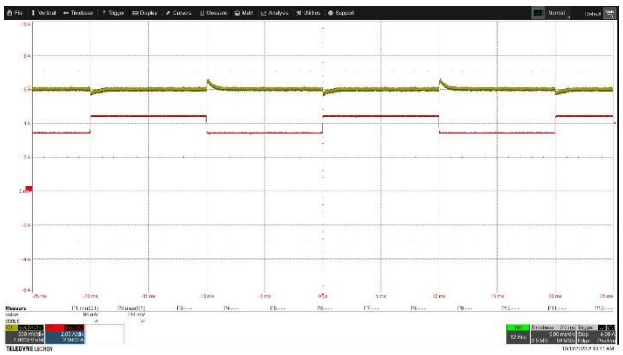
V_{BUS_C}: 12.0 V; (CH1: V_{BUS_C} ; CH7: I_{OUT})

V_{BUS_C}: 15.0 V; (CH1: V_{BUS_C}; CH7: I_{OUT})

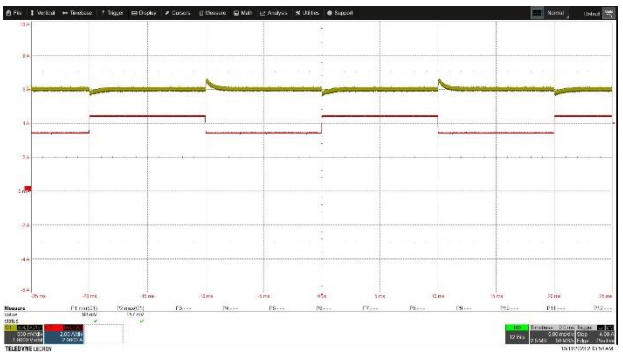


V_{BUS_C}: 20.0 V; (CH1: V_{BUS_C} ; CH7: I_{OUT})

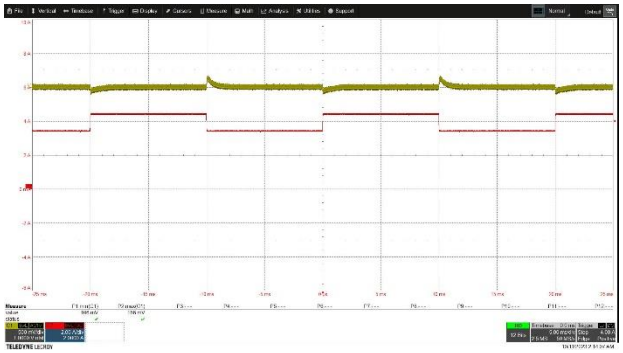
Figure 20 Output dynamic response waveforms – input 22.5 V_{DC}; load current transition 0 A to 1 A to 0 A



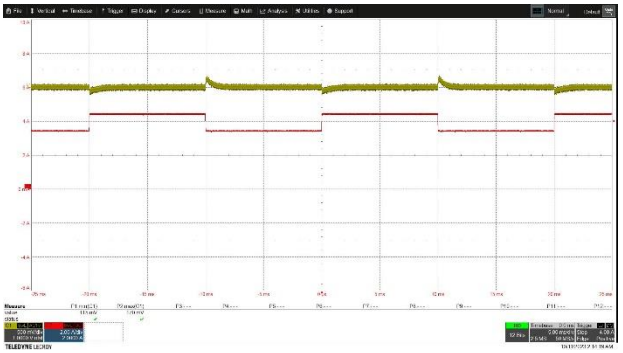
V_{BUS_C}: 3.3 V; (CH1: V_{BUS_C}; CH7: I_{OUT})



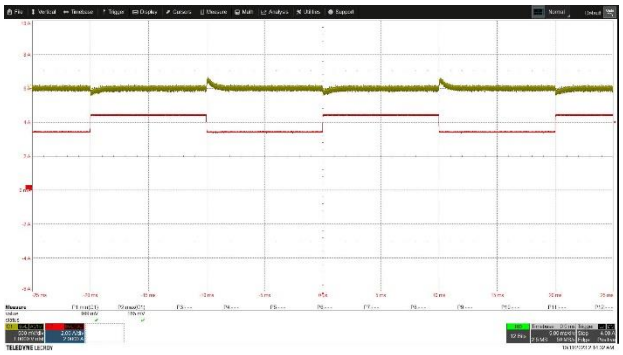
V_{BUS_C}: 5.0 V; (CH1: V_{BUS_C} ; CH7: I_{OUT})



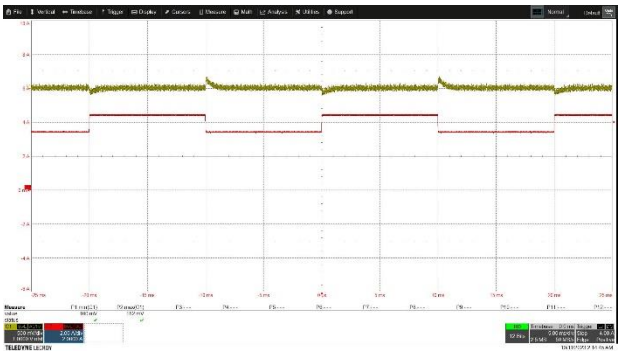
V_{BUS_C}: 9.0 V; (CH1: V_{BUS_C}; CH7: I_{OUT})



V_{BUS_C}: 12.0 V; (CH1: V_{BUS_C} ; CH7: I_{OUT})



V_{BUS_C}: 15.0 V; (CH1: V_{BUS_C}; CH7: I_{OUT})

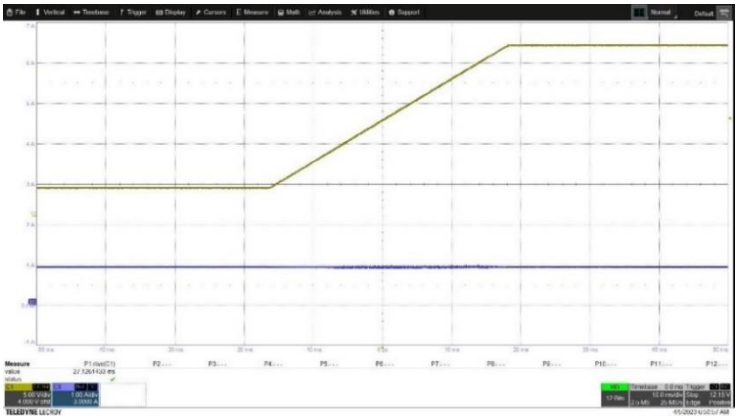


V_{BUS_C}: 20.0 V; (CH1: V_{BUS_C} ; CH7: I_{OUT})

Figure 21 Output dynamic response waveforms – input 22.5 V_{DC}; load current transition 3.5 A to 4.5 A to 3.5 A

4.7 Output voltage transition

Output voltage transition at 22.5 V_{DC} input and load 1 A is measured, as shown in Figure 22, Figure 23, Figure 24, and Figure 25.



I_{OUT}: 1 A (CH1: V_{BUS_C}; CH6: I_{OUT})

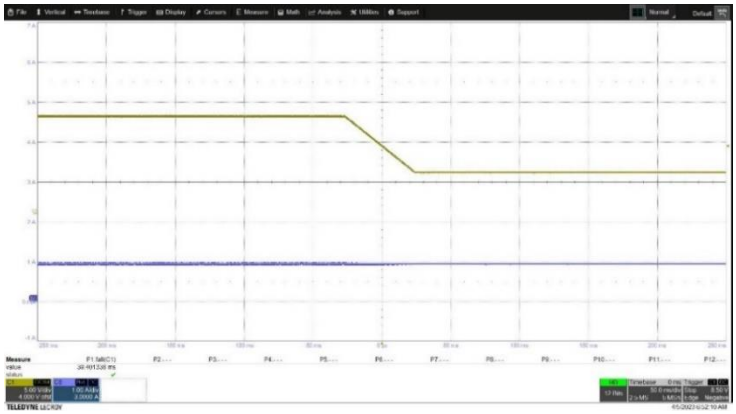
Figure 22 Input 22.5 V_{DC}; V_{BUS_C} transition from 3.3 V to 21.0 V

I_{OUT}: 1 A (CH1: V_{BUS_C}; CH6: I_{OUT})

Figure 23 Input 22.5 V_{DC}; V_{BUS_C} transition from 21.0 V to 3.3 V

I_{OUT}: 1 A (CH1: V_{BUS_C}; CH6: I_{OUT})

Figure 24 Input 22.5 V_{DC}; V_{BUS_C} transition from 5.0 V to 12 V

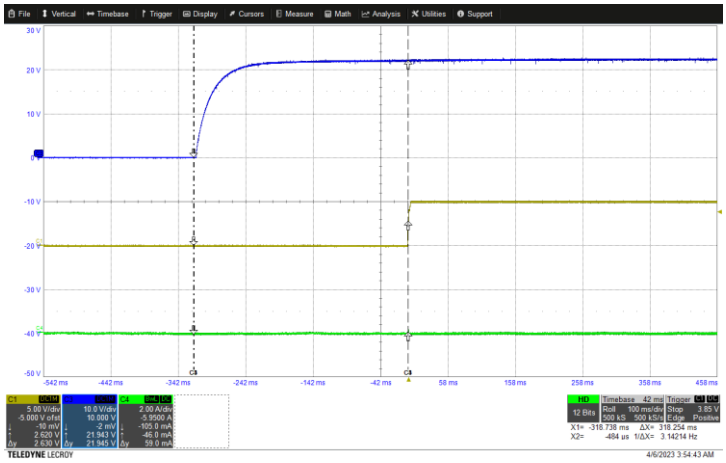


I_{OUT}: 1 A (CH1: V_{BUS_C}; CH6: I_{OUT})

Figure 25 Input 22.5 V_{DC}; V_{BUS_C} transition from 12 V to 5 V

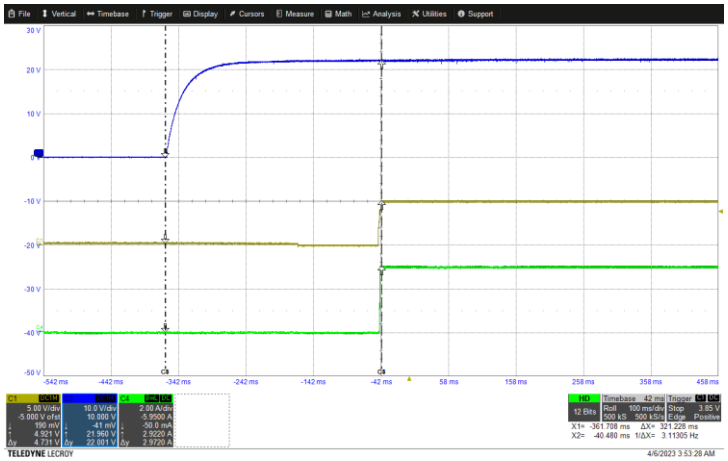
4.8 Start-up turn-on delay

Turn-on delay with respect to DUT input voltage and the output voltage is measured at no load and 3-A load is shown in Figure 26 and Figure 27.



CH1: V_{BUS_C}; CH3: V_{IN}; CH4: I_{OUT}

Figure 26 Input 22.5 V_{DC}; V_{BUS_C}: 5 V; I_{OUT}: 0 A



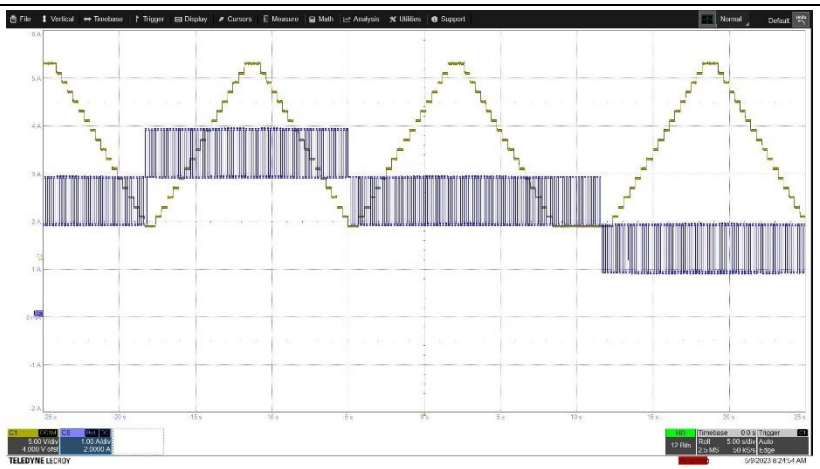
CH1: V_{BUS_C}; CH3: V_{IN}; CH4: I_{OUT}

Figure 27 Input 22.5 V_{DC}; V_{BUS_C}: 5 V; I_{OUT}: 3 A

4.9 Stress test waveforms

The REF_CCG7SC_120W_3C solution board with one port connected was subjected to electrical stress conditions.

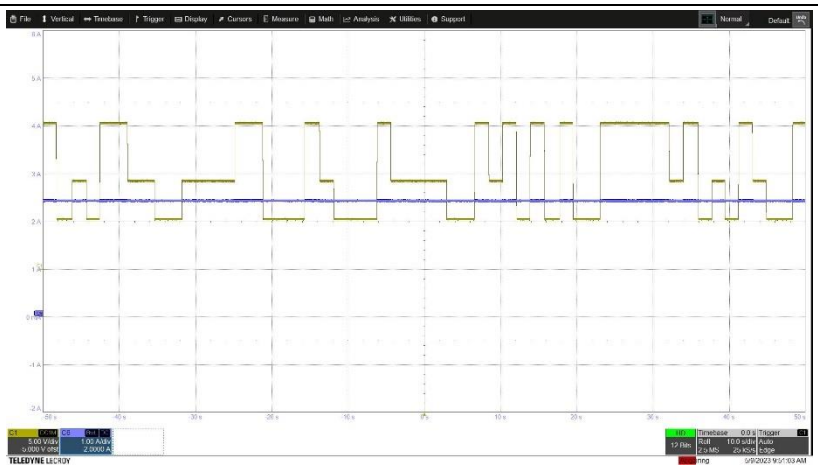
- **Electrical stress test #1** V_{IN} = 22.5 V_{DC}; V_{BUS_C} – continuously changing from 3.3 V – 21 V with 1 V step and vice versa (PPS); I_{OUT} = 0 A to 4 A with 1 A step for a duration of 60 minutes. Captured waveforms are shown in Figure 28.



CH1: V_{BUS_C}; CH6: I_{OUT}

Figure 28 V_{IN} = 22.5 V_{DC}; V_{BUS_C} – continuously changing from 3.3 V – 21 V (PPS) and vice versa; I_{OUT} = 0 A to 4 A with 1 step

- **Electrical stress test #2** V_{IN}= 22.5 V_{DC}; V_{BUS_C} – randomly changing from 5 V to 9 V to 15 V (PDO); I_{OUT} = 2.5 A for a duration of 60 minutes. Captured waveforms are shown in Figure 29.



CH1: V_{BUS_C}; CH6: I_{OUT}

Figure 29 V_{IN} = 22.5 V_{DC}; V_{BUS_C} – continuously changing from 5 V to 9 V to 15 V (PDO); I_{OUT} = 2.5 A

5 Three port power management test results of REF_CCG7SC_120W_3C

Efficiency captured using the test setup shown in the Appendix: Efficiency measurement test setup. Here all three ports were loaded and each of the ports was loaded with equal amount of current.

5.1 Peak efficiency and full load efficiency table

Peak efficiency test results are tabulated in Table 15.

Table 15 Peak efficiency

V_{BUS_C} (V)	V_{IN} = 22.5 V
03.30 V	92.52% – 3*3.00 A
05.00 V	94.34% – 3*3.20 A
09.00 V	96.10% – 3*3.60 A
12.00 V	96.86% – 3*3.40 A
15.00 V	97.42% – 3*2.60 A
20.00 V	97.27% – 3*2.00 A
21.00 V	98.32% – 3*1.80 A

*Note: Peak efficiency: 98.32% (At V_{IN}:22.5 V_{DC}, V_{BUS_C}: 21 V, I_{OUT}: 3*1.80 A)*

Full load efficiency test results are tabulated in Table 16.

Table 16 Full load efficiency

V_{BUS_C} (V)	V_{IN} = 22.5 V
3.30 V	91.51% – 3*5.00 A
5.00 V	93.78% – 3*5.00 A
9.00 V	95.99% – 3*4.44 A
12.00 V	96.86% – 3*3.40 A
15.00 V	97.42% – 3*2.60 A
20.00 V	97.27% – 3*2.00 A
21.00 V	98.32% – 3*1.80 A

5.2 Efficiency graphs

Efficiency measurements were taken at 22.5 V DC input to the DUT; V_{BUS_C} PDO, PPS voltages are 3.3 V, 5 V, 9 V, 12 V, 15 V, 20 V, and 21 V for all the three ports.

Each port was loaded from 0 A to the maximum output current to make total system power 120 W. The efficiency is based on the test setup of Figure 95.

5.2.1 Efficiency at 22.5 V_{DC} input

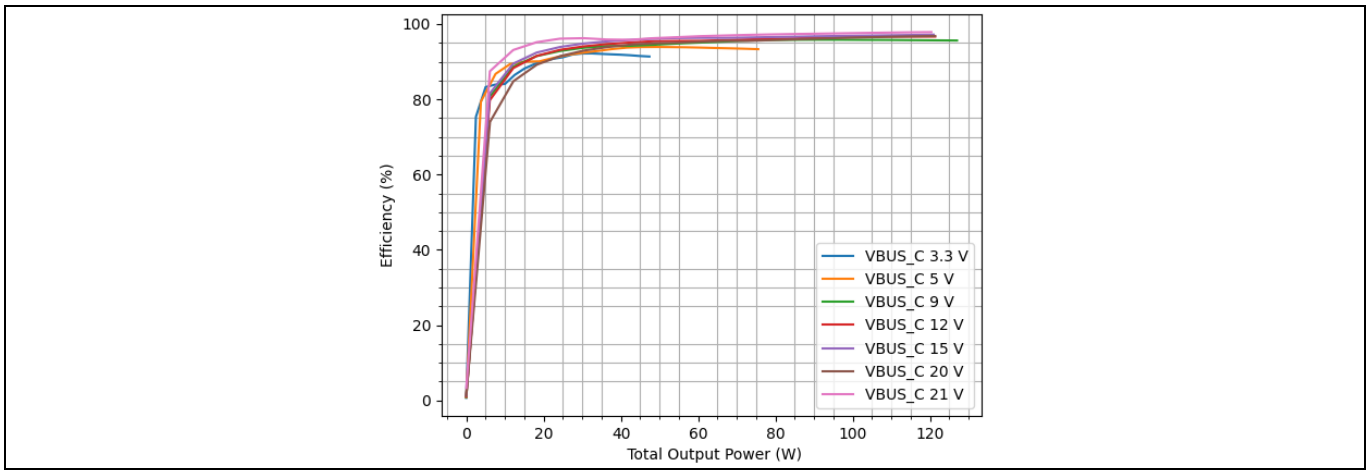


Figure 30 Efficiency at 22.5 V_{DC} input

5.3 Output voltage and current regulation

Output voltage regulation was measured both in the constant voltage (CV) and constant current (CC) modes.

5.3.1 Output voltage regulation (CV mode)

Output constant voltage regulation measured from 0 A to maximum load currents that each port can take to have maximum system power of 120 W, are shown in Figure 31, Figure 32, and Figure 33.

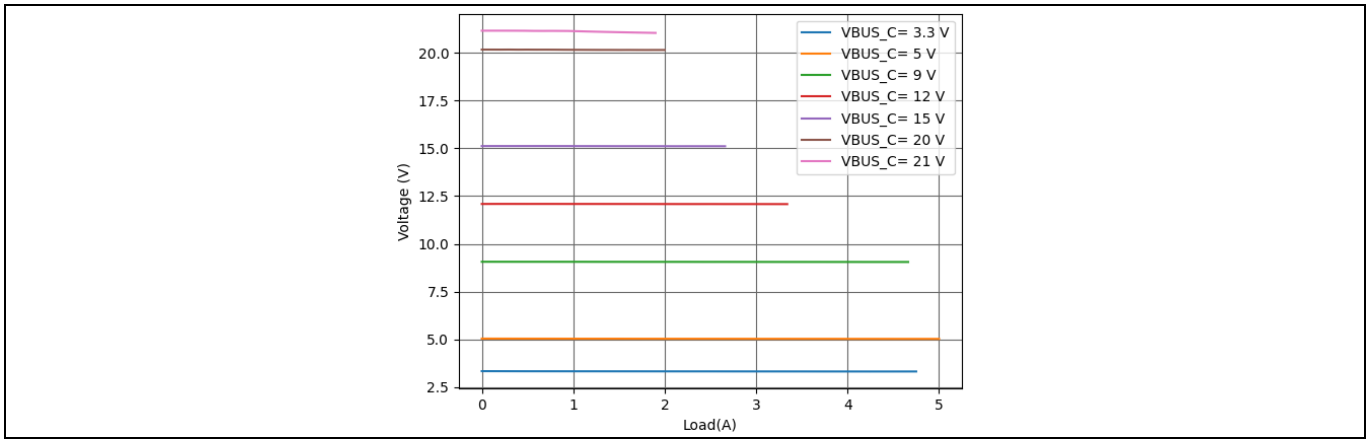


Figure 31 CV regulation at 22.5 V_{DC} input port #1

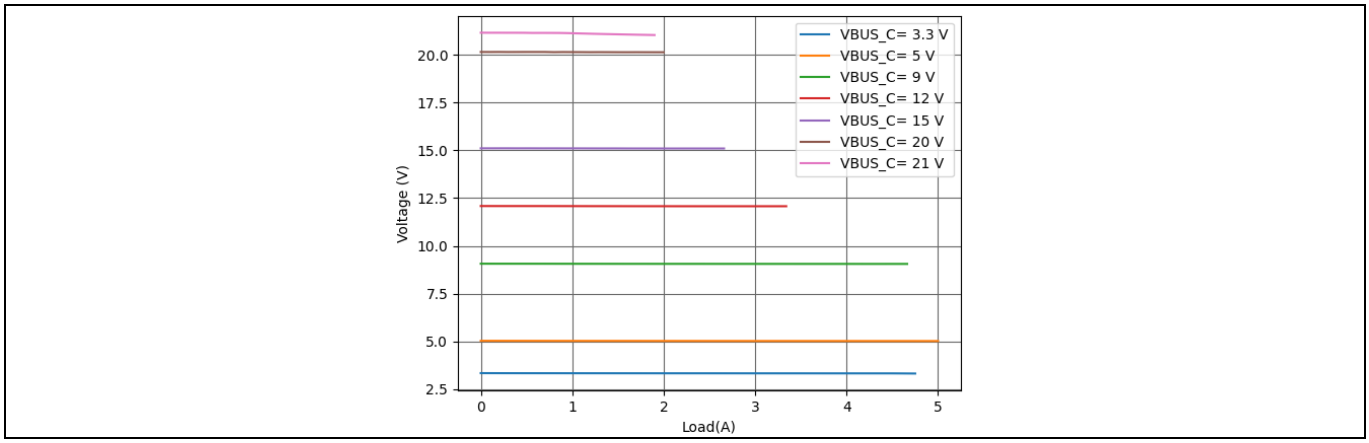


Figure 32 CV regulation 22.5 VDC input port #2

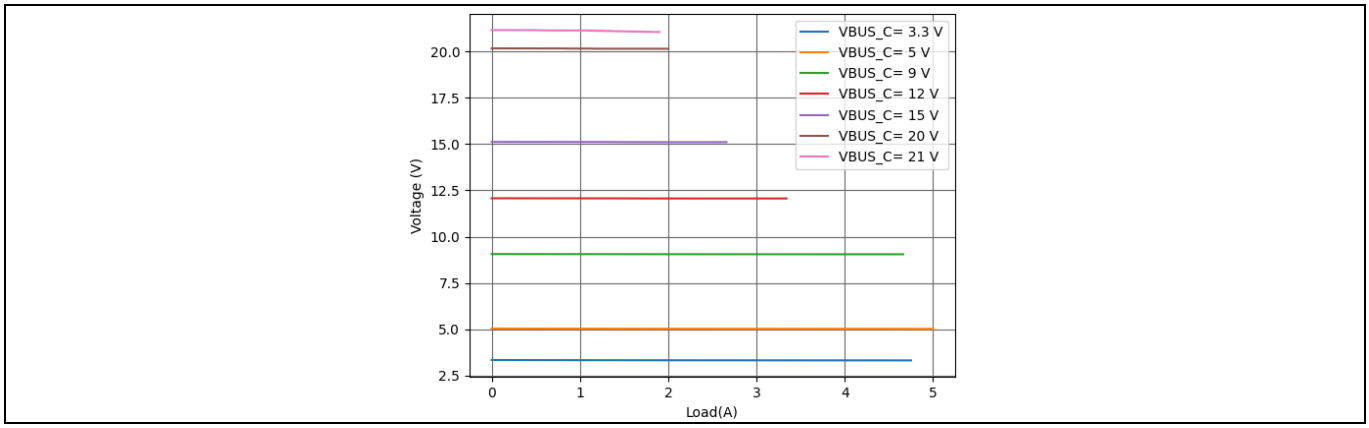


Figure 33 CV regulation 22.5 V_{DC} input port #3

5.3.2 Output current regulation (CC mode)

Output constant current (CC) regulation of each port measured at 1.5 A output currents are shown in Figure 34.

5.3.3 CC regulation curve at 22.5 V_{DC} input and rated output current of 1.5 A

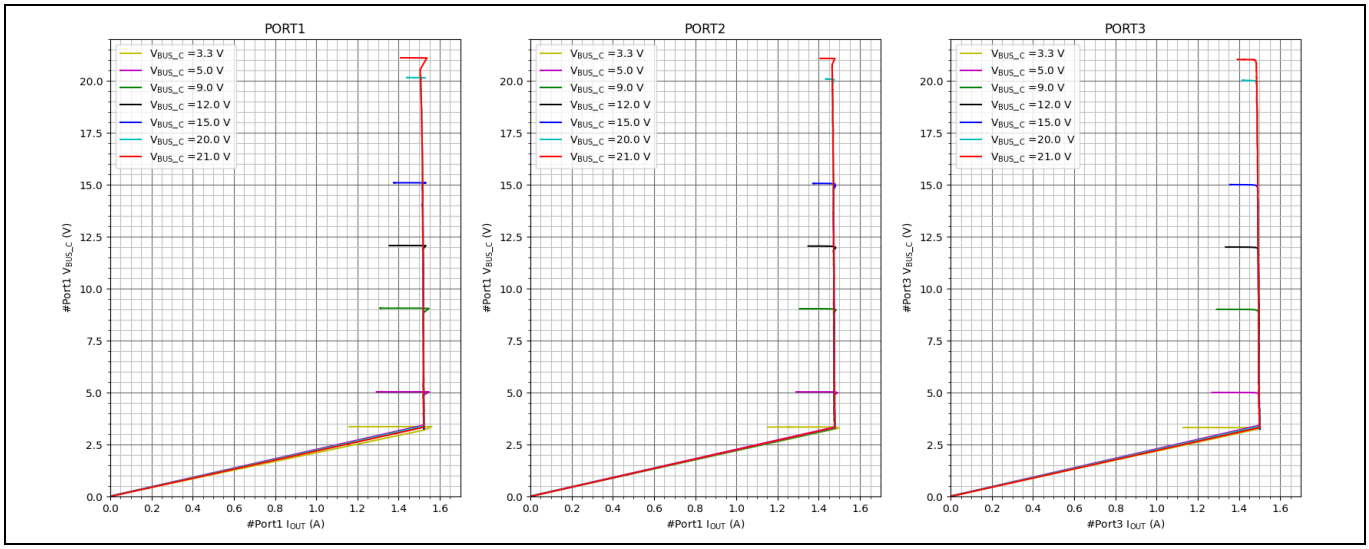


Figure 34 CC regulation curve at 22.5 V_{DC} input and 1.5 A output current

5.4 Output voltage ripple measurement

Output voltage peak-to-peak ripple was measured across the output capacitors C19 using a short ground loop connected to the probe.

5.4.1 Output voltage ripple peak-to-peak (mV)

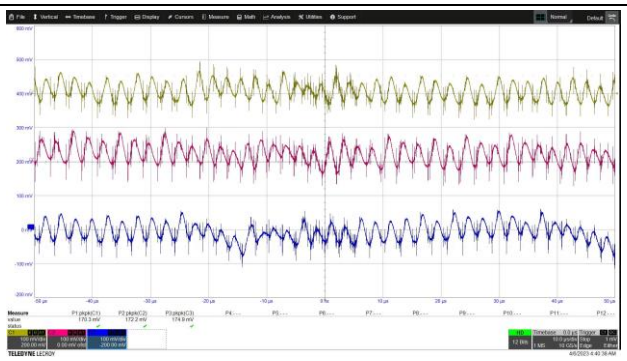
Output voltage peak-to-peak ripple tabulated in Table 17.

Table 17 Peak-to-peak ripple (mV) at 22.5 V input

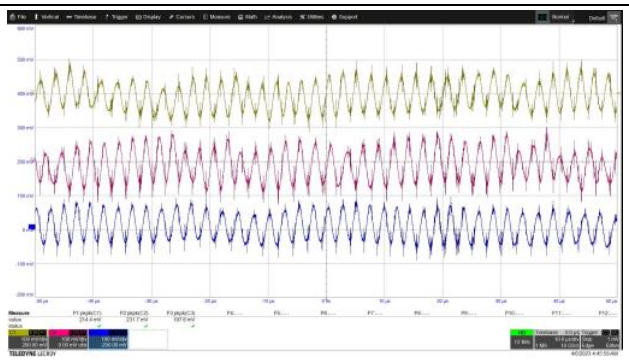
V_{BUS_C} - I_{OUT}	Port #1 ripple (mV)	Port #2 ripple (mV)	Port #3 ripple (mV)
03.3 V – 0.00 A	180.80	034.80	180.80
03.3 V – 5.00 A	117.13	086.29	117.13
05.0 V – 0.00 A	057.37	024.09	057.37
05.0 V – 5.00 A	134.74	109.73	134.74
09.0 V – 0.00 A	050.85	027.35	050.85
09.0 V – 4.44A	165.32	143.78	165.32
12.0 V – 0.00 A	048.16	027.92	048.16
12.0 V – 3.33 A	126.33	138.51	126.33
15.0 V – 0.00 A	057.25	029.20	057.25
15.0 V – 2.66 A	121.58	123.54	121.58
20.0 V – 0.00 A	072.60	053.67	072.60
20.0 V – 2.00 A	102.51	120.51	102.51
21.0 V – 0.00 A	169.22	109.29	169.22
21.0 V – 1.90 A	069.24	093.78	069.24

5.4.2 Output voltage ripple peak-to-peak measurement graphs

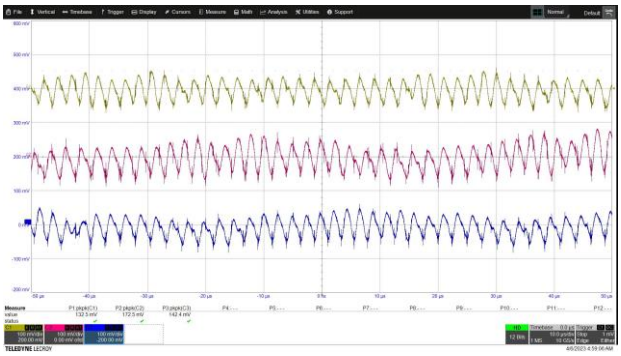
Output voltage peak-to-peak ripple waveforms at full load are shown in Figure 35.



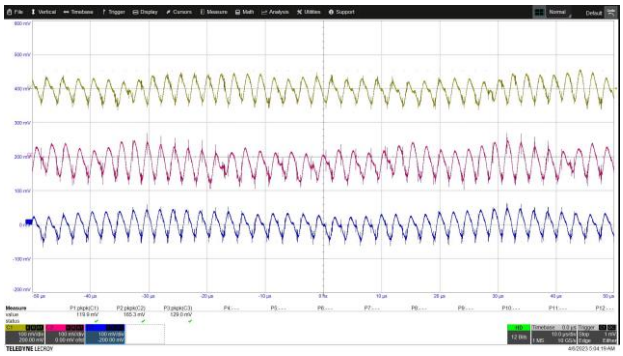
Port #1 V_{BUS_C}: 05 V (CH1); port #2 V_{BUS_C}: 05 V (CH2); port #3 V_{BUS_C}: 05 V (CH3) I_{OUT}: 5 A



Port #1 V_{BUS_C}: 09 V (CH1); port #2 V_{BUS_C}: 09 V (CH2); port #3 V_{BUS_C}: 09 V (CH3) I_{OUT}: 4.6 A



Port #1 V_{BUS_C}: 15 V (CH1); port #2 V_{BUS_C}: 15V (CH2); port #3 V_{BUS_C}: 15 V(CH3) I_{OUT}: 2.67 A



Port #1 V_{BUS_C}: 20 V (CH1); port #2 V_{BUS_C}: 20 V (CH2); port #3 V_{BUS_C}: 20 V(CH3) I_{OUT}: 2 A

Figure 35 Ripple measurement – input voltage: 22.5 VDC

5.5 Output voltage regulation

Output voltage regulation measured at V_{IN}= 22.5 V_{DC}, V_{BUS_C}= 3.3 V, 5 V, 9 V, 12 V, 15 V, 20 V,21 V; I_{OUT} = 0 A to maximum current are shown in Table 18.

Table 18 Regulation at 22.5 V_{AC} input

I_{OUT} (A)	Port #1 V_{BUS_C} (V_{DC})	Port #1 % Regulation	I_{OUT} (A)	Port #2 V_{BUS_C} (V_{DC})	Port #2 % Regulation	I_{OUT} (A)	Port #3 V_{BUS_C} (V_{DC})	Port #3 % Regulation
0.00 A	03.361	1.85%	0.00 A	03.323	1.37%	0.00 A	03.344	1.52%
4.75 A	03.300		4.75 A	03.278		4.75 A	03.294	
0.00 A	05.045	0.29%	0.00 A	04.996	0.38%	0.00 A	05.023	0.36%
5.00 A	05.030		5.00 A	04.977		5.00 A	05.005	
0.00 A	09.062	0.36%	0.00 A	08.981	0.40%	0.00 A	09.031	0.15%
4.40 A	09.029		4.40 A	08.945		4.40 A	09.017	
0.00 A	12.073	0.11%	0.00 A	11.981	0.23%	0.00 A	12.046	0.12%
2.56 A	12.060		2.56 A	11.954		2.56 A	12.032	
0.00 A	15.097	0.05%	0.00 A	14.968	0.04%	0.00 A	15.070	-0.08%
2.66 A	15.089		2.66 A	14.962		2.66 A	15.082	
0.00 A	20.141	0.07%	0.00A	20.001	0.08%	0.00A	20.121	0.01%
2.00 A	20.127		2.00A	19.985		2.00A	20.101	

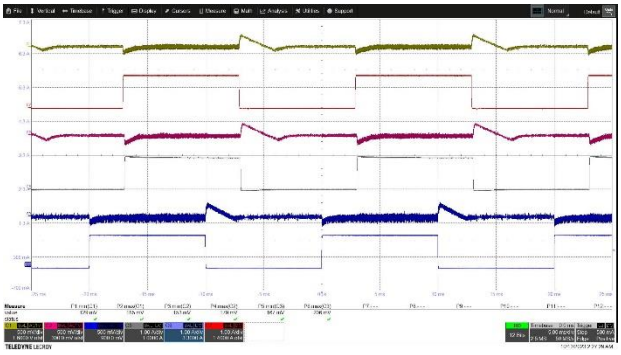
5.6 Output voltage dynamic response waveforms

V_{IN} = 22.5 V, output voltage response when the output current is from 0 A – 1 A – 0 A is shown in Figure 36.

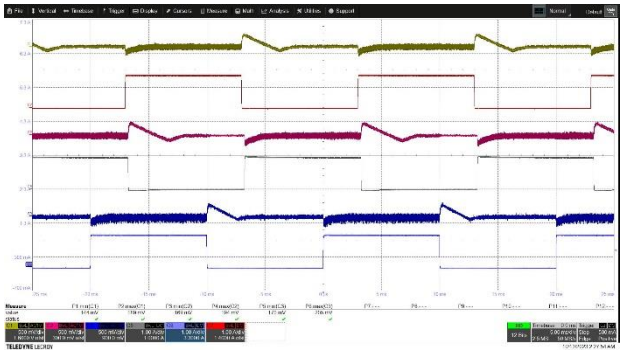
Port #1: V_{BUS_C} (CH1); I_{OUT} (CH6);

Port #2: V_{BUS_C} (CH3); I_{OUT} (CH7);

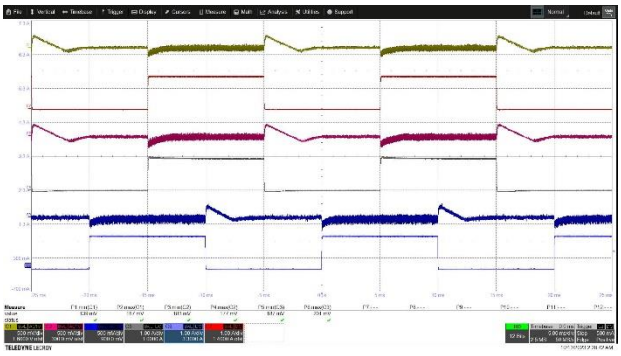
Port #3: V_{BUS_C} (CH2); I_{OUT} (CH5);



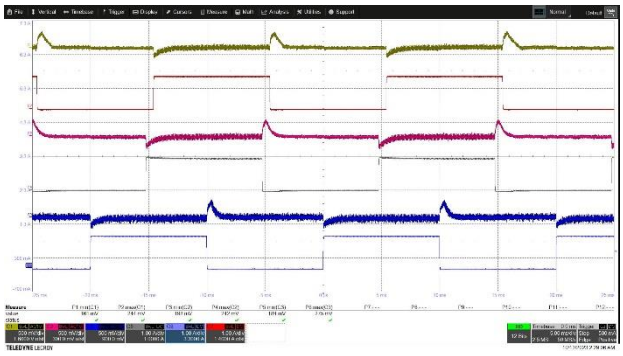
Port #1 V_{BUS_C}: 05 V (CH1); port #2 V_{BUS_C}: 05 V (CH2); port #3 V_{BUS_C}: 05 V (CH3) I_{OUT}: 0 A to 1 A to 0 A



Port #1 V_{BUS_C}: 09 V (CH1); port #2 V_{BUS_C}: 09 V (CH2); port #3 V_{BUS_C}: 09 V (CH3) I_{OUT}: 0 A to 1 A to 0 A



Port #1V_{BUS_C}: 15 V (CH1); port#2 V_{BUS_C}: 15 V(CH2); port #3 V_{BUS_C}: 15 V (CH3) I_{OUT}: 0 A to 1 A to 0 A



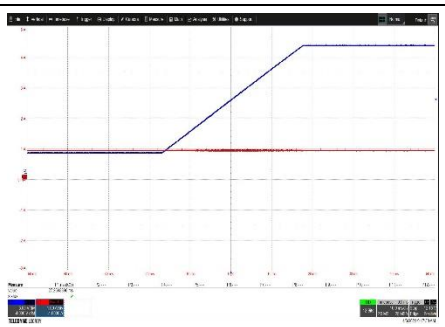
Port #1 V_{BUS_C}: 20 V (CH1); port#2 V_{BUS_C}: 20 V (CH2); port #3 V_{BUS_C}: 20 V (CH3) I_{OUT}: 0 A to 1 A to 0 A

Figure 36 Output dynamic response waveforms - input 22.5 V_{DC}; load current transition 0 A to 1 A to 0 A

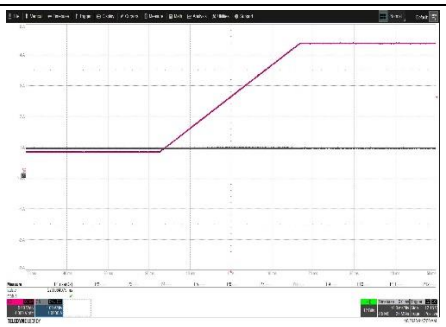
5.7 Output voltage transition

Output voltage transition at 22.5 V_{DC} input and load 1 A is measured, as shown in Figure 37, Figure 38, and Figure 39.

Port #1; I_{OUT}: 1 A (CH1: V_{BUS_C}; CH6: I_{OUT})

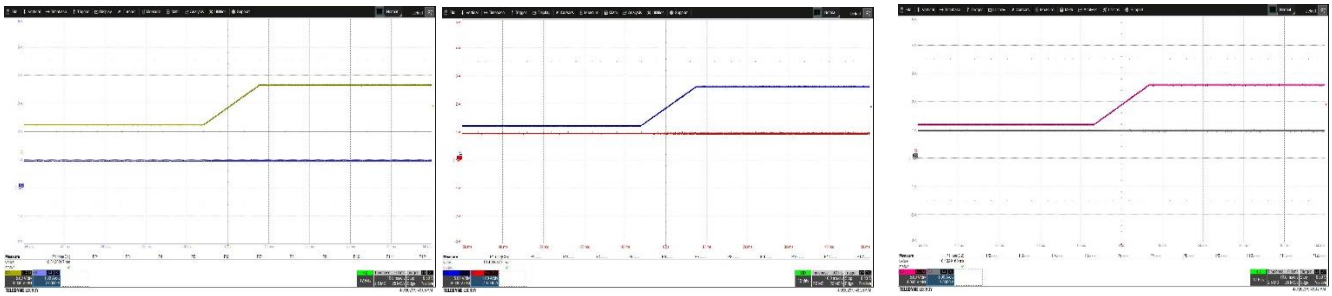


Por t#2; I_{OUT}: 1 A (CH3: V_{BUS_C}; CH7: I_{OUT})



Port #3; I_{OUT}: 1 A (CH2: V_{BUS_C}; CH5: I_{OUT})

Figure 37 Input 22.5 V_{DC}; V_{BUS_C} transition from 3.3 V to 21 V



Port #1; I_{OUT}: 1 A (CH1: V_{BUS_C}; CH6: I_{OUT}) Port #2; I_{OUT}: 1 A (CH3: V_{BUS_C}; CH7: I_{OUT}) Port #3; I_{OUT}: 1 A (CH2: V_{BUS_C}; CH5: I_{OUT})

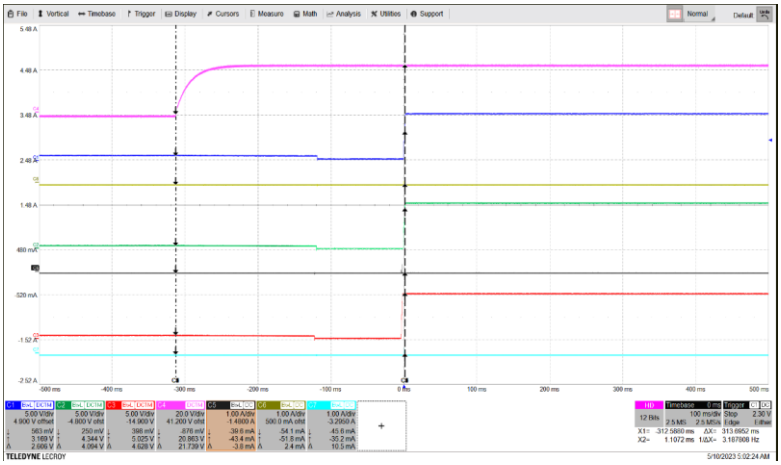
Figure 38 Input 22.5 V_{DC}; V_{BUS_C} transition from 5.0 V to 12 V

Port #1; I_{OUT}: 1 A (CH1: V_{BUS_C}; CH6: I_{OUT}) Port #2; I_{OUT}: 1 A (CH3: V_{BUS_C}; CH7: I_{OUT}) Port #3; I_{OUT}: 1 A (CH2: V_{BUS_C}; CH5: I_{OUT})

Figure 39 Input 22.5 V_{DC}; V_{BUS_C} transition from 21 V to 3.3 V

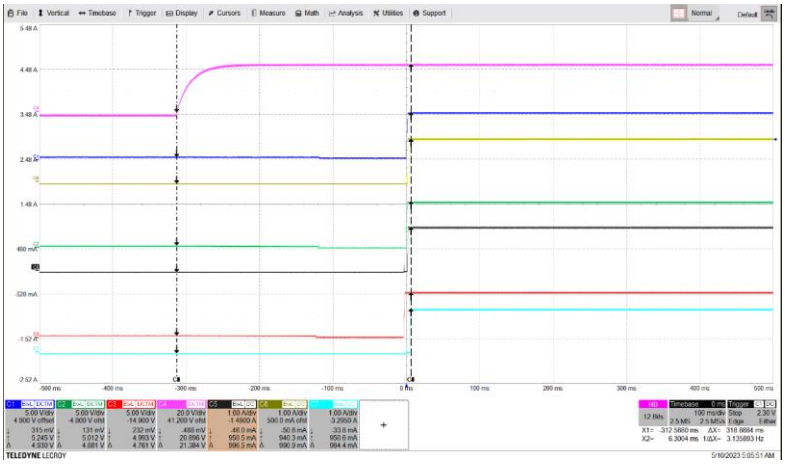
5.8 Start-up turn-on delay

Turn-on delay with respect to DUT input voltage and the output voltage is measured at no load and 1 A load is shown in Figure 40 and Figure 41 .



CH1:port #1 V_{BUS_C}; CH6:port #1 I_{OUT}; CH2:port #1 V_{BUS_C}; CH5:port #1 I_{OUT}; CH3:port #1 V_{BUS_C}; CH7:port #1 I_{OUT}

Figure 40 Input 230 V_{AC}; V_{BUS_C}: 5 V; I_{OUT}: 0 A



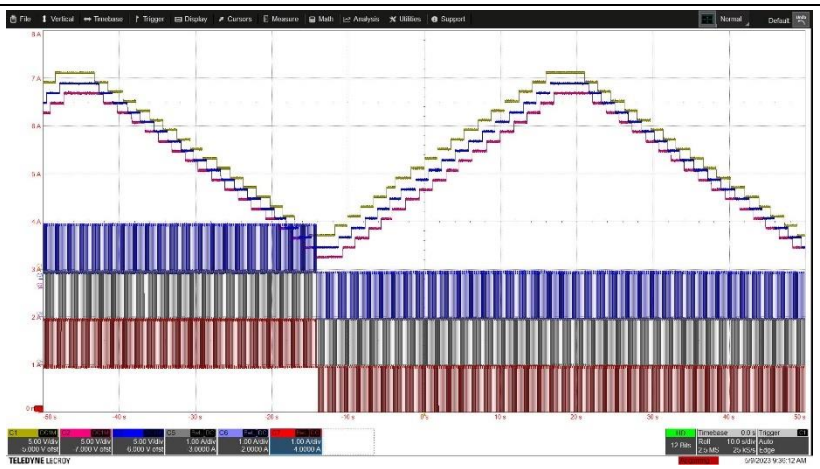
CH1:port #1 V_{BUS_C}; CH6:port #1 I_{OUT}; CH2:port #1 V_{BUS_C}; CH5:port #1 I_{OUT}; CH3:port #1 V_{BUS_C}; CH7:port #1 I_{OUT}

Figure 41 Input 230 V_{DC}; V_{BUS_C}: 5 V; I_{OUT}: 1 A

5.9 Stress test waveforms

The REF_CCG7SC_120W_3C solution board with three ports connected was subjected to electrical stress conditions.

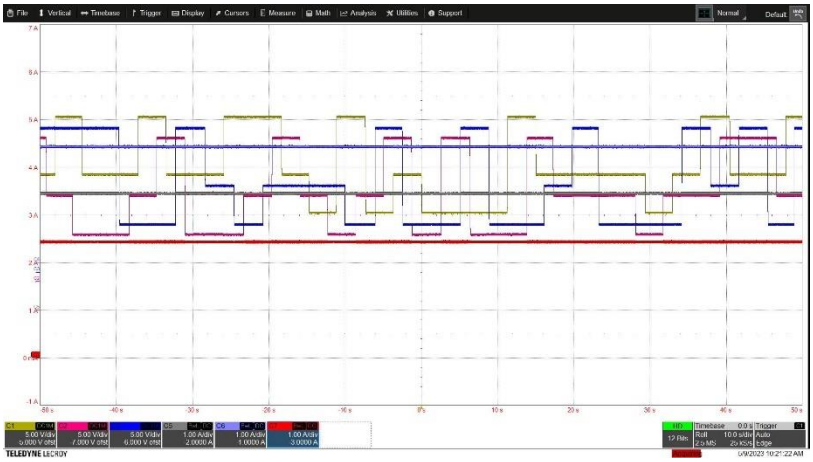
- **Electrical stress test #1** V_{IN} = 22.5 V_{DC}; V_{BUS_C} – continuously changing from 3.3 V – 21 V with 1 V step and vice versa (PPS); I_{OUT} = 0 to 2 A with 1 A step for a duration of 60 minutes. Captured waveforms are shown in Figure 42 .



CH1: port #1 V_{BUS_C}; CH6: port #1 I_{OUT}; CH2: port #2 V_{BUS_C}; CH5: port #2 I_{OUT}; CH3: port #3 V_{BUS_C}; CH7: port #3 I_{OUT}

Figure 42 V_{IN}: 22.5 V_{DC}; V_{BUS_C}: continuously changing from 3.3 V–21 V (PPS) vice versa; I_{OUT}: 0 to 4 A with 1 step

- **Electrical stress test #2** V_{IN}: 22.5 V_{DC}; V_{BUS_C}: randomly changing from 5 V to 9 V to 15V (PDO); I_{OUT}: 2.5 A for a duration of 60 minutes. Captured waveforms are shown in Figure 43 .



CH1: port #1 V_{BUS_C}; CH6: port #1 I_{OUT}; CH2: port #2 V_{BUS_C}; CH5: port #2 I_{OUT}; CH3: port #3 V_{BUS_C}; CH7: port #3 I_{OUT}

Figure 43 V_{IN}: 22.5 V_{DC}; V_{BUS_C}: continuously changing from 5 V to 9 V to 15 V (PDO); I_{OUT}: 2.5 A

6 Single port power management test results of XDPS2221 + REF_CCG7SC_120W_3C

Efficiency captured by connecting XDPS2221 to REF_CCG7SC_120W_3C.

Here only port #1 (master port) was loaded with 5 A current.

6.1 Peak efficiency and full load efficiency table

Peak efficiency test results are tabulated in Table 19.

Table 19 Peak efficiency

V_{BUS_C} (V)	115 V_{AC}/60 Hz	230 V_{AC}/50 Hz
03.3 V	86.58% – 3.80 A	86.95% – 4.75 A
05.0 V	89.36% – 4.00 A	89.68% – 4.50 A
09.0 V	90.78% – 4.50 A	92.49% – 4.50 A
12.0 V	92.07% – 3.56 A	93.40% – 4.27 A
15.0 V	92.70% – 4.25 A	93.97% – 3.75 A
20.0 V	93.46% – 4.50 A	94.84% – 5.00 A
21.0 V	92.88% – 4.05 A	94.07% – 4.50 A

Note: Peak efficiency: 94.84% (At V_{IN}:230 V_{AC}, V_{BUS_C}: 20 V, I_{OUT}: 5.00 A)

Full load efficiency test results are tabulated in Table 20.

Table 20 Full load efficiency

V_{BUS_C} (V)	115 V_{AC}/60 Hz	230 V_{AC}/50 Hz
03.30 V	86.42% – 4.75 A	86.95% – 4.75 A
05.00 V	89.21% – 5.00 A	89.60% – 5.00 A
09.00 V	90.65% – 5.00 A	92.39% – 5.00 A
12.00 V	91.62% – 4.75 A	93.39% – 4.75 A
15.00 V	92.39% – 5.00 A	93.31% – 5.00 A
20.00 V	93.38% – 5.00 A	94.84% – 5.00 A
21.00 V	92.79% – 4.50 A	94.07% – 4.50 A

Four-point efficiency average test results are tabulated in Table 21.

Table 21 Efficiency 4-pt average

Parameter	DOE level-VI limit	EU (CoC) Tier2	Unit	Test conditions	Test results (%)	
					230 V/50 Hz	Remarks
Four-point average efficiency (Average of 25%, 50%, 75%, and 100% load)	81.97	82.47	%	V_{BUS} = 03.3 V; I_{OUT} = 5.00 A	85.43%	Pass
	84.25	85.00	%	V_{BUS} = 05.0 V; I_{OUT} = 5.00 A	88.42%	Pass
	87.73	88.85	%	V_{BUS} = 09.0 V; I_{OUT} = 5.00 A	91.25%	Pass
	88.00	89.00	%	V_{BUS} = 12.0 V; I_{OUT} = 5.00 A	91.97%	Pass
	88.00	89.00	%	V_{BUS} = 15.0 V; I_{OUT} = 5.00 A	92.40%	Pass
	88.00	89.00	%	V_{BUS} = 20.0 V; I_{OUT} = 5.00 A	92.81%	Pass
	88.00	89.00	%	V_{BUS} = 21.0 V; I_{OUT} = 4.76 A	91.56%	Pass

6.2 Efficiency graphs

Efficiency measurements were taken at 115 V/60 Hz, and 230 V/50 Hz AC input to the DUT; V_{BUS_C} PDO, PPS voltages are 3.3 V, 5 V, 9 V, 12V, 15 V, 20 V, and 21 V. The port was loaded from 0 A to the maximum rated output current of 5 A.

Efficiency and power losses at 230 V AC input, V_{BUS_C} 3.3 V, 5 V, 9 V, 12V, 15 V, 20 V, 21 V, and I_{OUT} 0 A to 5 A maximum on the port are shown in Figure 44.

Efficiency and power losses at 115 V AC input, V_{BUS_C} 3.3 V, 5 V, 9 V, 12 V, 15 V, 20 V, 21 V, and I_{OUT} 0 A to 5 A maximum on the port are shown in Figure 45.

6.2.1 Efficiency and power losses at 230 V_{AC} input and 50 Hz frequency

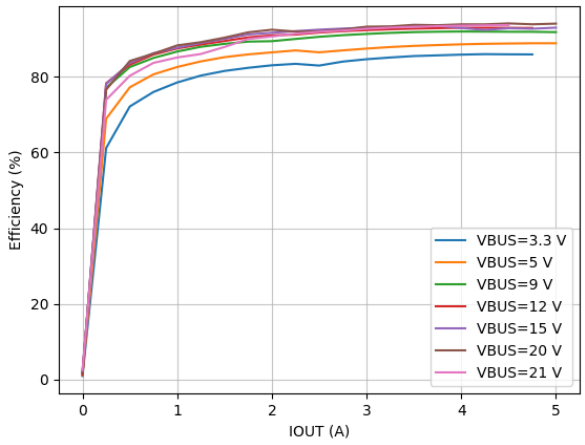


Figure 44 Efficiency and power losses at 230 V_{AC} input

6.2.2 Efficiency and power losses at 115 V_{AC} input and 60 Hz frequency

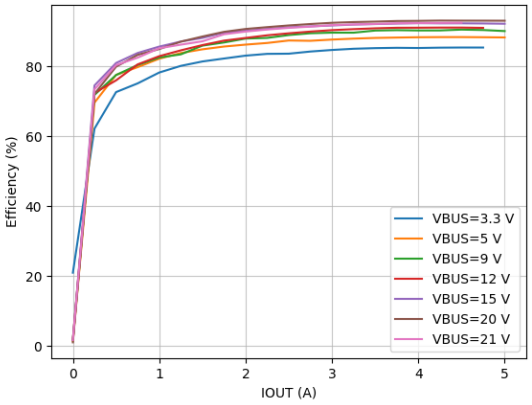


Figure 45 Efficiency and power losses at 115 V_{AC} input

6.3 Output voltage and current regulation

Output voltage regulation was measured both in the constant voltage (CV) and constant current (CC) modes.

6.3.1 Output voltage regulation (CV mode)

Output constant voltage regulation measured from 0 A and 5 A load currents is shown in Figure 46 and Figure 47.

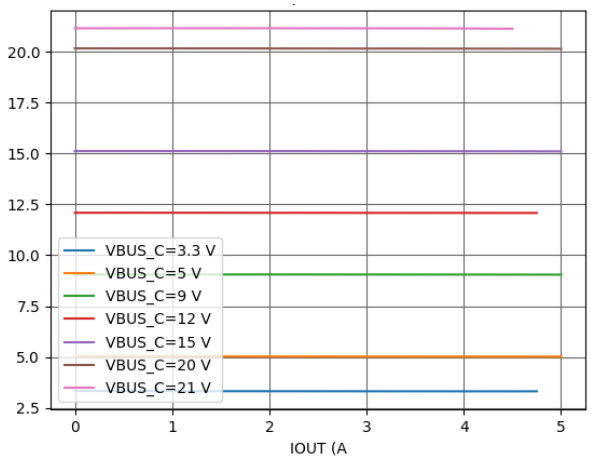


Figure 46 CV regulation at 230 V_{AC} input

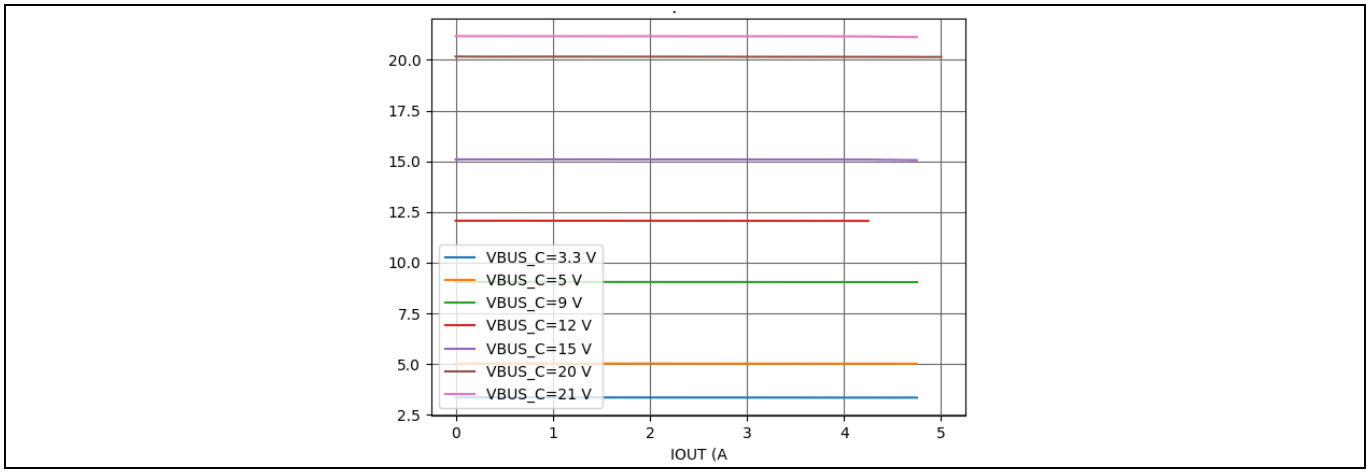


Figure 47 CV regulation at 115 V_{AC} input

6.3.2 Output current regulation (CC mode)

Output constant current (CC) regulation of port measured at 3 A and 5 A output currents is shown in Figure 48 and Figure 49.

6.3.3 CC regulation curve at 230 V_{AC} input,50 Hz frequency and rated output current of 3 A

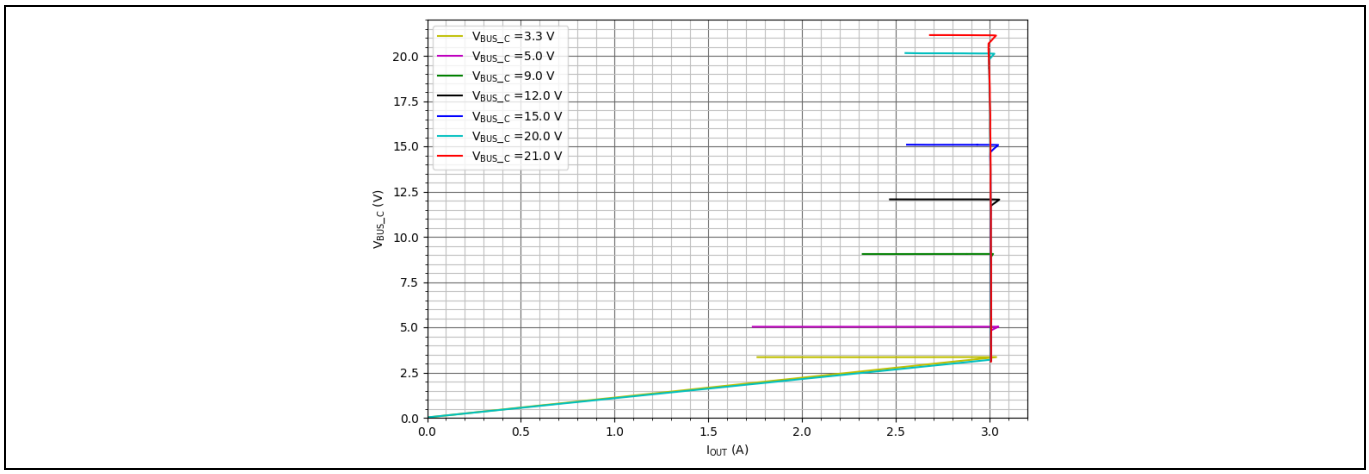


Figure 48 CC regulation curve at 230 V_{AC} input and 3 A output current

6.3.4 CC regulation curve at 230 V_{AC} input,50 Hz frequency and rated output current of 5 A

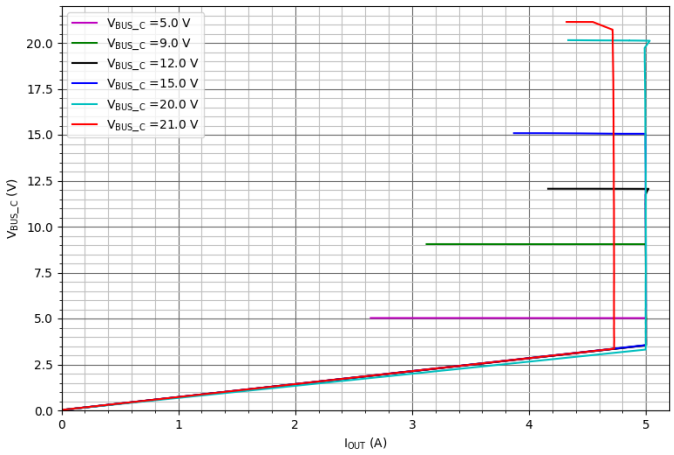


Figure 49 CC regulation curve at 230 V_{DC} input and 5 A output current

6.4 Output voltage regulation

Output voltage regulation measured at V_{IN} = 230 V_{AC} and 115 V_{AC}, V_{BUS_C}: 3.3 V, 5 V, 9 V, 12 V, 15 V, 20 V, 21 V;

I_{OUT} = 0 A and 5 A is shown in Table 22.

Table 22 Regulation at V_{IN} = 230 V_{AC}

I_{OUT} (A)	V_{BUS_C} (V_{DC})	V_{IN} = 230 V_{AC} % Regulation	I_{OUT} (A)	V_{BUS_C} (V_{DC})	V_{IN} = 115 V_{AC} % Regulation
0.00	03.359	1.73%	0.00	03.357	1.69%
4.75	03.302		4.75	03.301	
0.00	05.043	0.29%	0.00	05.043	0.28%
5.00	05.028		4.75	05.029	
0.00	09.058	0.35%	0.00	09.059	0.35%
5.00	09.026		4.75	09.027	
0.00	12.068	0.11%	0.00	12.070	0.29%
4.75	12.055		4.25	12.035	
0.00	15.096	-0.05%	0.00	15.096	0.08%
5.00	15.104		4.75	15.084	
0.00	20.264	0.86%	0.00	20.259	0.86%
5.00	20.090		5.00	20.086	
0.00	21.140	0.29%	0.00	21.140	0.39%
4.50	21.078		4.75	21.057	

6.5 Output voltage ripple measurement

Output voltage peak-to-peak ripple was measured across the output capacitors C19 using a short ground loop connected to the probe.

6.5.1 Output voltage ripple peak-to-peak (mV)

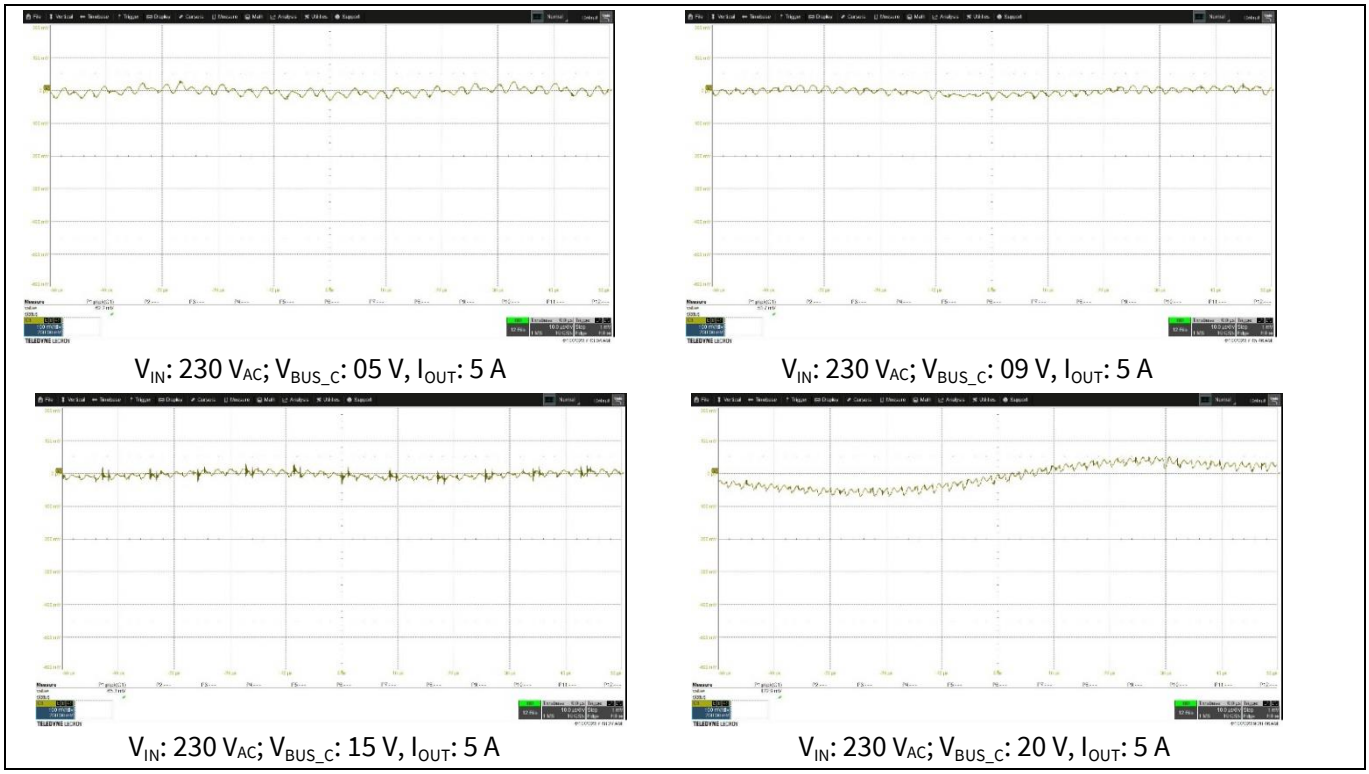
Output voltage peak-to-peak ripple tabulated in Table 23.

Table 23 Peak-to-peak ripple (mV) at 115 V_{AC} and 230 V_{AC}

V_{BUS_C} - I_{OUT}	V_{IN} = 115 V_{AC} Ripple (mV)	V_{BUS_C} - I_{OUT} Ripple (mV)	V_{IN} = 230 V_{AC} Ripple (mV)
03.3 V – 0.00 A	07.350	03.3 V – 0.00 A	07.016
03.3 V – 4.75 A	22.551	03.3 V – 4.75 A	20.906
05.0 V – 0.00 A	08.326	05.0 V – 0.00 A	09.162
05.0 V – 5.00 A	29.811	05.0 V – 5.00 A	30.209
09.0 V – 0.00 A	12.747	09.0 V – 0.00 A	11.513
09.0 V – 5.00 A	62.037	09.0 V – 5.00 A	47.235
12.0 V – 0.00 A	16.216	12.0 V – 0.00 A	16.769
12.0 V – 4.75 A	67.486	12.0 V – 4.75 A	54.431
15.0 V – 0.00 A	23.874	15.0 V – 0.00 A	22.718
15.0 V – 5.00 A	71.379	15.0 V – 5.00 A	70.364
20.0 V – 0.00 A	26.264	20.0 V – 0.00 A	24.671
20.0 V – 5.00 A	47.158	20.0 V – 5.00 A	31.867
21.0 V – 0.00 A	40.219	21.0 V – 0.00 A	41.080
21.0 V – 4.50 A	85.809	21.0 V – 4.50 A	87.094

6.5.2 Output voltage ripple peak-to-peak measurement graph

Output voltage peak-to-peak ripple waveforms at full load are shown in Figure 50 and Figure 51.



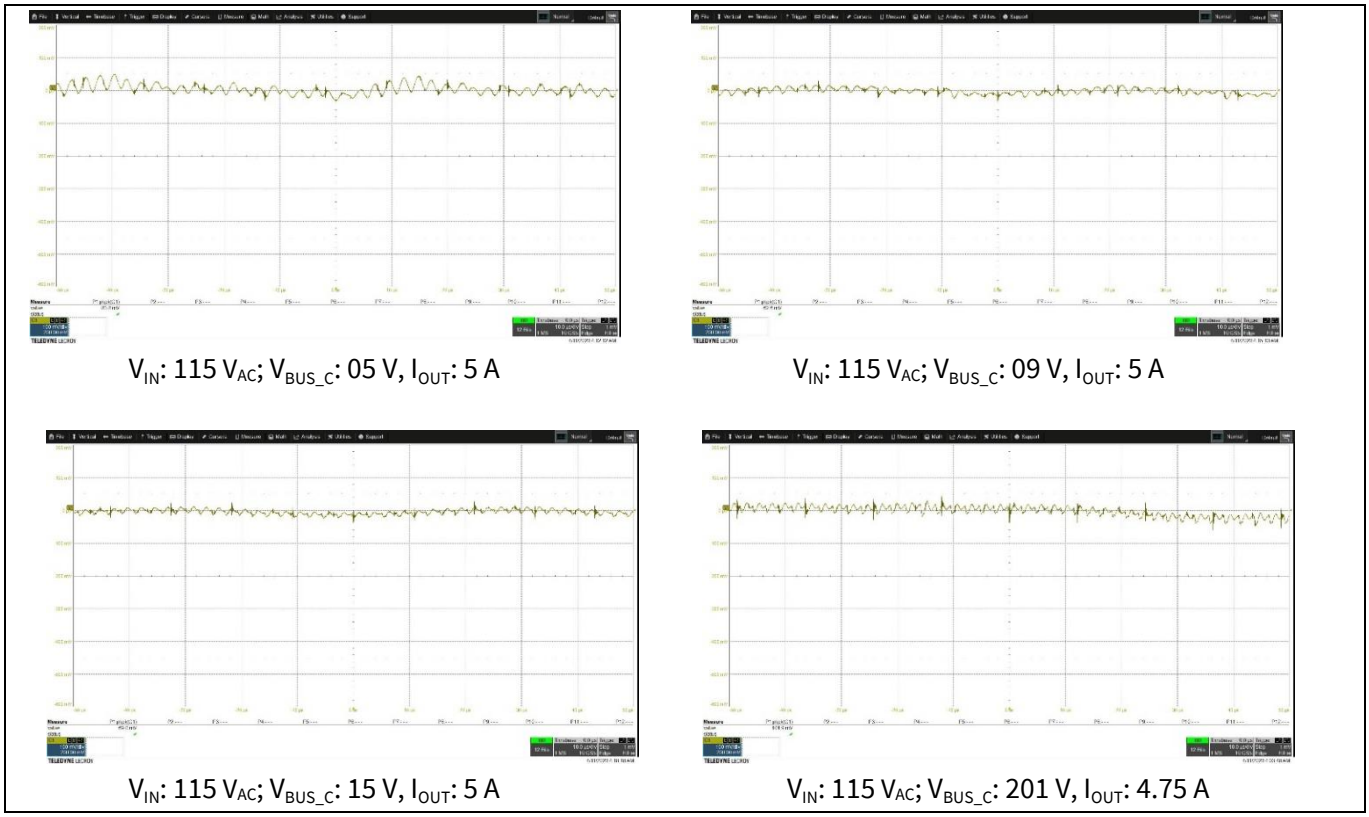
V_{IN}: 230 V_{AC}; V_{BUS_C}: 05 V, I_{OUT}: 5 A

V_{IN}: 230 V_{AC}; V_{BUS_C}: 09 V, I_{OUT}: 5 A

V_{IN}: 230 V_{AC}; V_{BUS_C}: 15 V, I_{OUT}: 5 A

V_{IN}: 230 V_{AC}; V_{BUS_C}: 20 V, I_{OUT}: 5 A

Figure 50 Ripple measurement – input voltage: 230 V_{AC} (CH1: V_{BUS_C})



V_{IN}: 115 V_{AC}; V_{BUS_C}: 05 V, I_{OUT}: 5 A

V_{IN}: 115 V_{AC}; V_{BUS_C}: 09 V, I_{OUT}: 5 A

V_{IN}: 115 V_{AC}; V_{BUS_C}: 15 V, I_{OUT}: 5 A

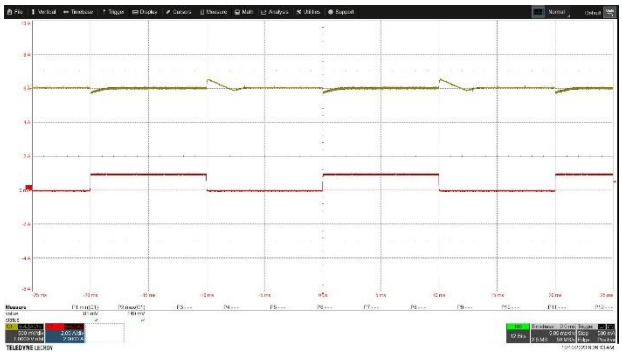
V_{IN}: 115 V_{AC}; V_{BUS_C}: 201 V, I_{OUT}: 4.75 A

Figure 51 Ripple measurement – input voltage: 115 V_{AC} (CH1: V_{BUS_C})

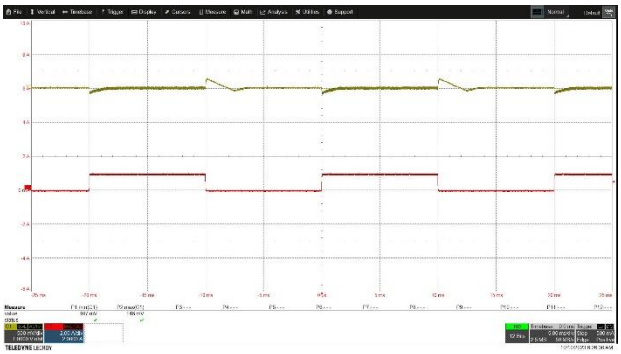
6.6 Output voltage dynamic response waveforms

V_{IN} = 230 V_{AC}/50 Hz, output voltage response when the output current is from 0 A – 1 A – 0 A, is shown in Figure 52.

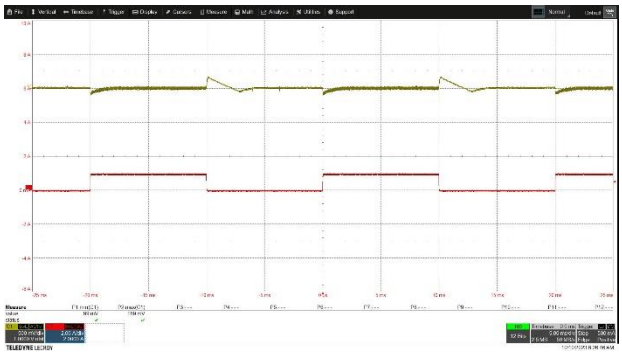
V_{IN} = 115 V_{AC}/60 Hz, output voltage response when the output current is from 3.5 A – 4.5 A – 3.5 A is shown in Figure 53.



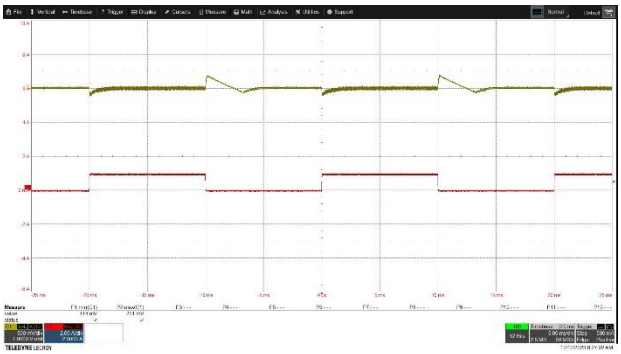
V_{BUS_C}: 3.3 V; (CH1: V_{BUS_C}; CH7: I_{OUT})



V_{BUS_C}: 5.0 V; (CH1: V_{BUS_C} ; CH7: I_{OUT})

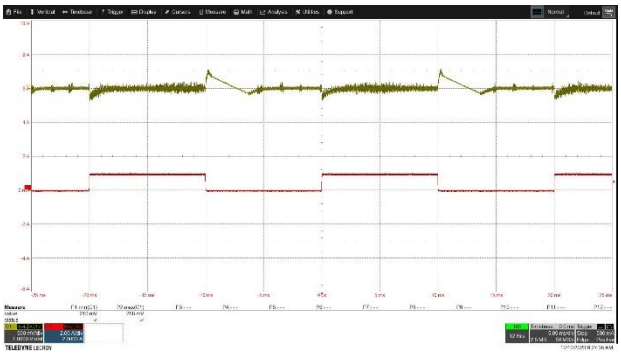


V_{BUS_C}: 9.0 V; (CH1: V_{BUS_C}; CH7: I_{OUT})



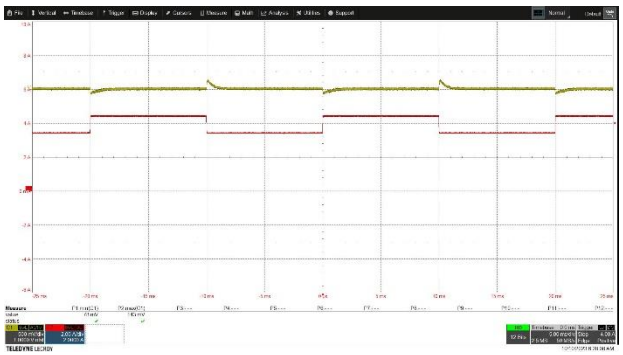
V_{BUS_C}: 12.0 V; (CH1: V_{BUS_C} ; CH7: I_{OUT})

V_{BUS_C}: 15.0 V; (CH1: V_{BUS_C}; CH7: I_{OUT})

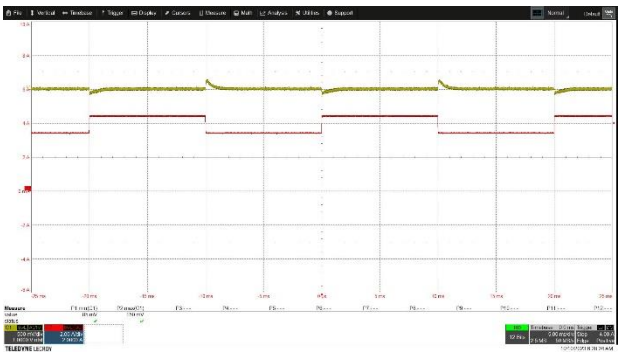


V_{BUS_C}: 20.0 V; (CH1: V_{BUS_C} ; CH7: I_{OUT})

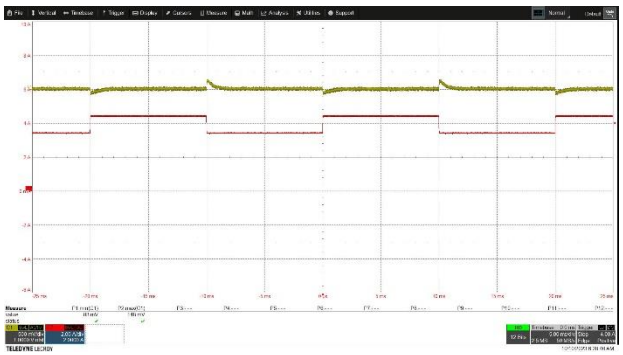
Figure 52 Output dynamic response waveforms – input 230 V_{AC}; load current transition 0 A to 1 A to 0 A



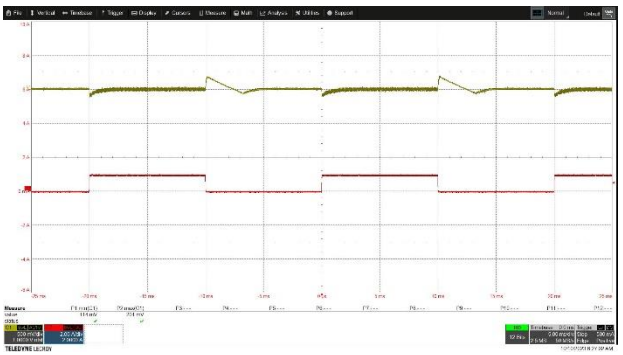
V_{BUS_C}: 3.3 V; (CH1: V_{BUS_C}; CH7: I_{OUT})



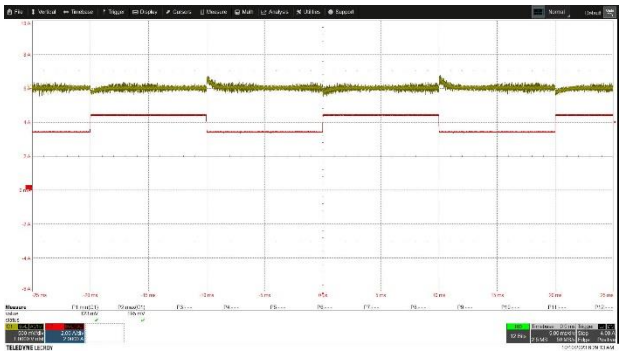
V_{BUS_C}: 5.0 V; (CH1: V_{BUS_C} ; CH7: I_{OUT})



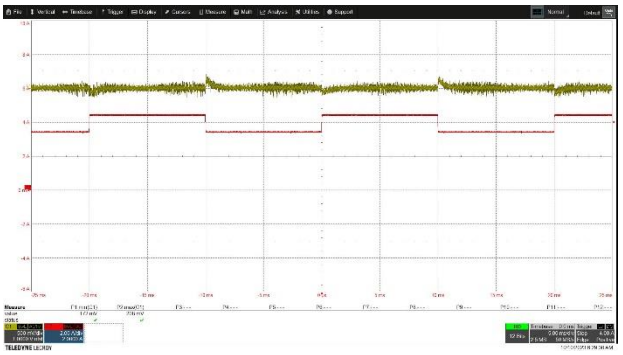
V_{BUS_C}: 9.0 V; (CH1: V_{BUS_C}; CH7: I_{OUT})



V_{BUS_C}: 12.0 V; (CH1: V_{BUS_C} ; CH7: I_{OUT})



V_{BUS_C}: 15.0 V; (CH1: V_{BUS_C}; CH7: I_{OUT})

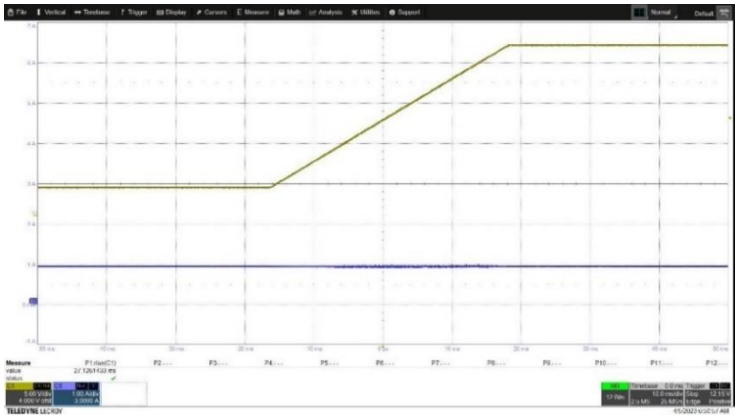


V_{BUS_C}: 20.0 V; (CH1: V_{BUS_C} ; CH7: I_{OUT})

Figure 53 Output dynamic response waveforms – input 230 V_{AC}; load current transition 3.5 A to 4.5 A to 3.5 A

6.7 Output voltage transition

Output voltage transition at 230 V_{AC} input and load 1 A is measured as shown in Figure 54, Figure 55, Figure 56, and Figure 57.



I_{OUT}: 1 A (CH1: V_{BUS_C}; CH6: I_{OUT})

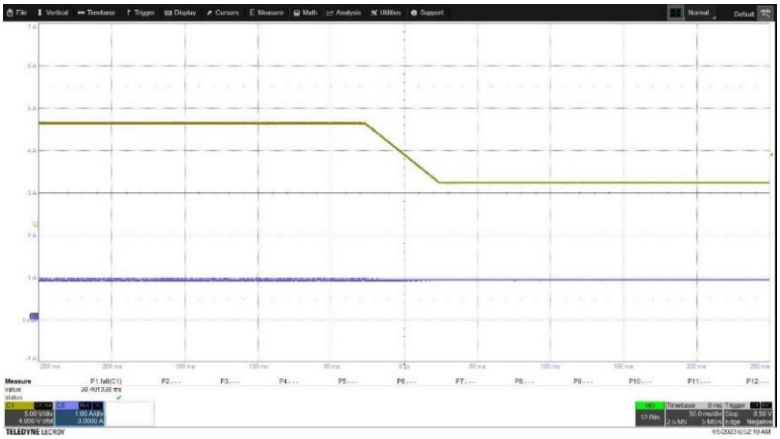
Figure 54 Input 22.5 V_{DC}; V_{BUS_C} transition from 3.3 V to 21.0 V

I_{OUT}: 1 A (CH1: V_{BUS_C}; CH6: I_{OUT})

Figure 55 Input 22.5 V_{DC}; V_{BUS_C} transition from 21.0 V to 3.3 V

I_{OUT}: 1 A (CH1: V_{BUS_C}; CH6: I_{OUT})

Figure 56 Input 22.5 V_{DC}; V_{BUS_C} transition from 5.0 V to 12 V

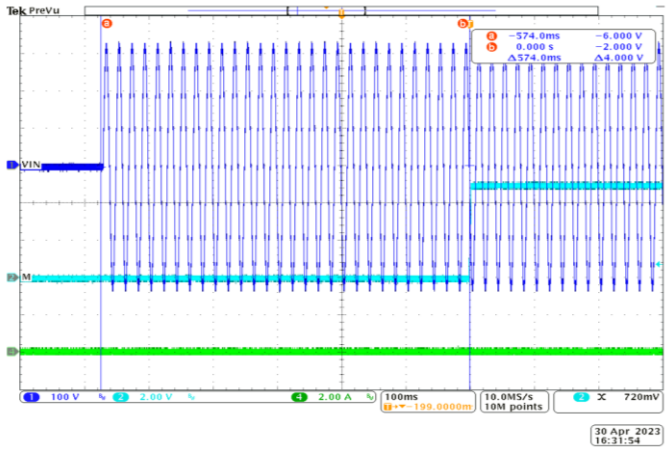


I_{OUT}: 1 A (CH1: V_{BUS_C}; CH6: I_{OUT})

Figure 57 Input 22.5 V_{DC}; V_{BUS_C} transition from 12 V to 5 V

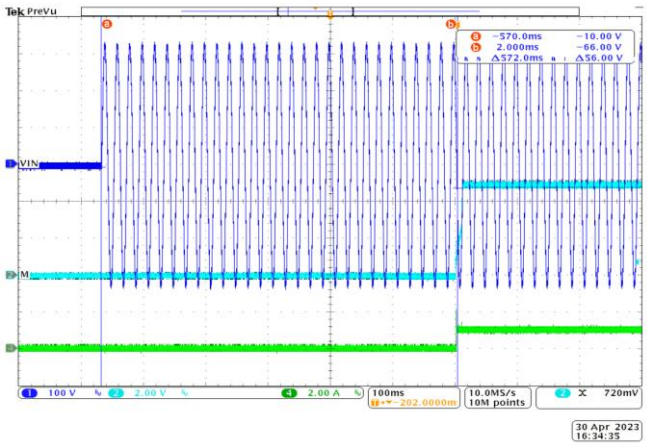
6.8 Start-up turn-on delay

Turn-on delay with respect to DUT input voltage and the output voltage is measured at no load and 1 A load is shown in Figure 58 and Figure 59.



CH1: V_{IN}; CH2: Port #1 V_{BUS}; CH4: Port #1 I_{OUT}

Figure 58 Input 230 V_{AC}; V_{BUS_C} = 5 V; I_{OUT} = 0 A



CH1: V_{IN}; CH2: Port #1 V_{BUS}; CH4: Port #1 I_{OUT}

Figure 59 Input 230 V_{DC}; V_{BUS_C} = 5 V; I_{OUT} = 1 A

6.9 Stress test waveforms

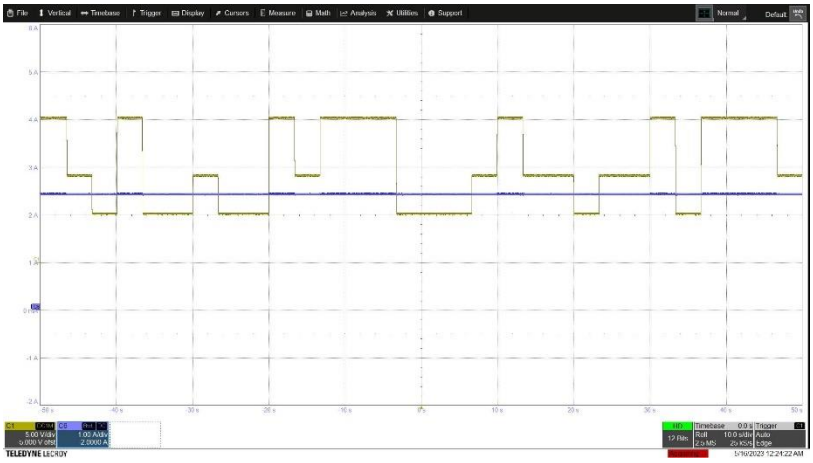
The XDPS2221 + REF_CCG7SC_120W_3C solution board with one port connected was subjected to electrical stress conditions.

- **Electrical stress test #1** V_{IN} = 230 V_{AC}; V_{BUS_C}: continuously changing from 3.3 V – 21 V with 1 V step and vice versa (PPS); I_{OUT} = 0 A to 2 A with 1 A step for a duration of 60 minutes. Captured waveforms are shown in Figure 60.

CH1: V_{BUS_C}; CH6: I_{OUT}

Figure 60 V_{IN} = 230 V_{AC}; V_{BUS_C} – continuously changing from 3.3 V – 21 V (PPS) vice versa; I_{OUT} = 0 A to 2 A with 1 step

- **Electrical stress test #2** V_{IN} = 230 V_{AC}; V_{BUS_C} – randomly changing from 5 V – 9 V – 15V (PDO); I_{OUT} = 1 A for a duration of 60 minutes. Captured waveforms are shown in Figure 61.



CH1: V_{BUS_C}; CH6: I_{OUT}

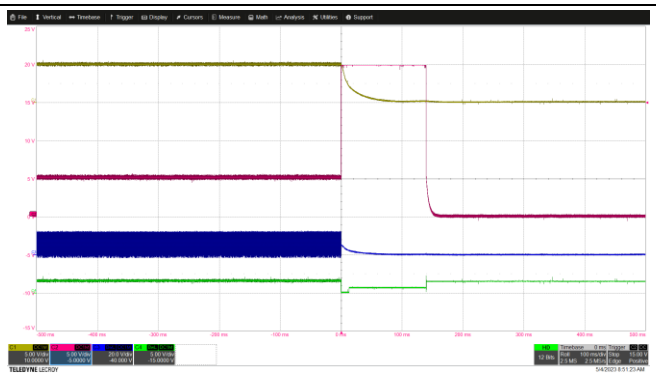
Figure 61 V_{IN} = 230 V_{AC}; V_{BUS_C} – continuously changing from 5 V to 9 V to 15 V (PDO); I_{OUT} = 1 A

6.10 Faults test waveforms

XDPS2221 + REF_CCG7SC_120W_3C was subjected to supported fault protections and the results are displayed in the following section.

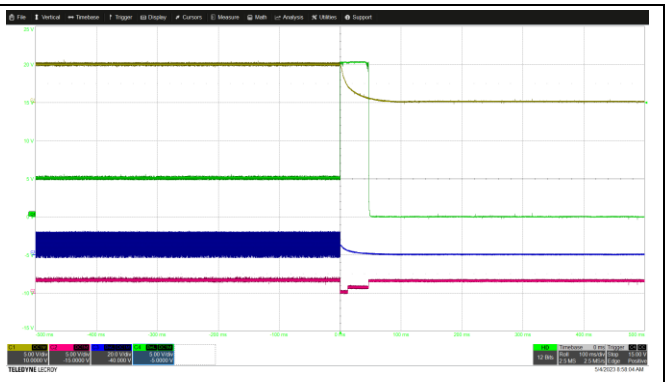
6.10.1 V_{BUS_C} to CCx line faults test waveforms

V_{BUS_C} to CC active line fault is shown in Figure 62 where V_{IN} = 230 V_{AC}; V_{BUS_C} = 5 V



V_{BUS_C} to CC2 fault

CH1: V_{BUS_C}; CH2: CC2; CH3: HG1; CH4: CC1

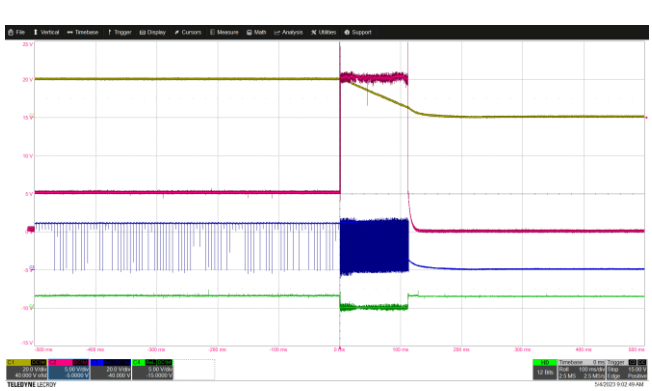


V_{BUS_C} to CC1 fault

CH1: V_{BUS_C}; CH2: CC2; CH3: HG1; CH4: CC1

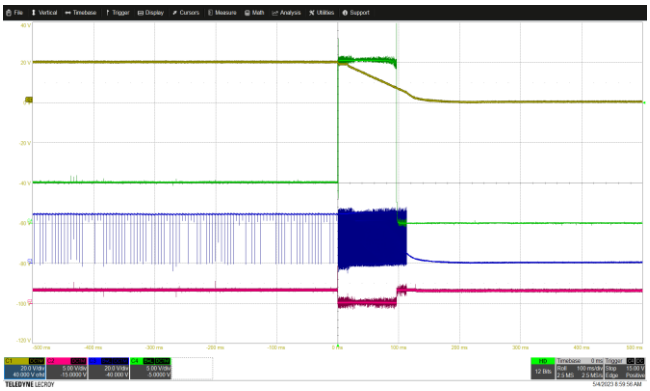
Figure 62 V_{BUS_C} to CC line fault

V_{BUS_C} to CC active line fault is shown in Figure 63 where V_{IN} = 230 V_{AC}; V_{BUS_C} = 20 V



V_{BUS_C} to CC2 fault

CH1: V_{BUS_C}; CH2: CC2; CH3: HG1; CH4: CC1



V_{BUS_C} to CC1 fault

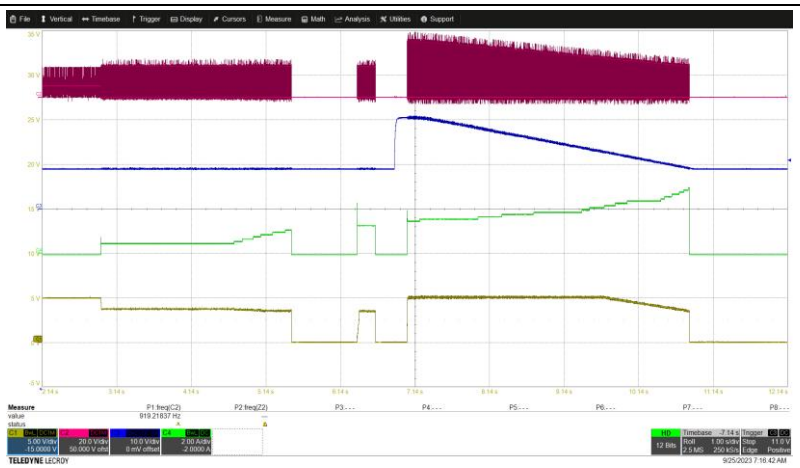
CH1: V_{BUS_C}; CH2: CC2; CH3: HG1; CH4: CC1

Figure 63 V_{BUS_C} to CC line fault

6.10.2 Output undervoltage protection (UVP)

DUT output undervoltage protection waveforms are shown in Figure 64.

Test conditions: V_{IN} = 230 V_{AC}; V_{BUS_C} = 5.0 V



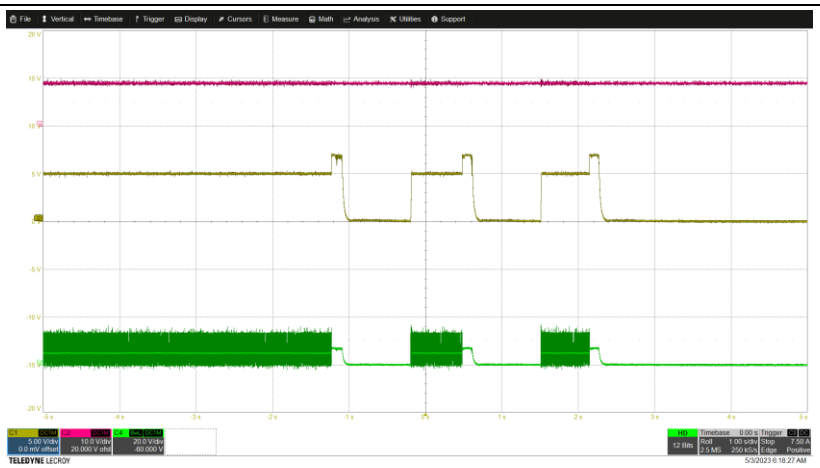
CH1: V_{BUS_C}; CH2: HG1 (wrt GND); CH3: V_{IN} (DC); CH4: I_{OUT}

Figure 64 Output undervoltage protection

6.10.3 Output overvoltage protection (OVP)

DUT output overvoltage protection waveforms are shown in Figure 65.

Test conditions: V_{IN} = 230 V_{AC}; V_{BUS_C} = 5.0 V, I_{OUT} = 0 A



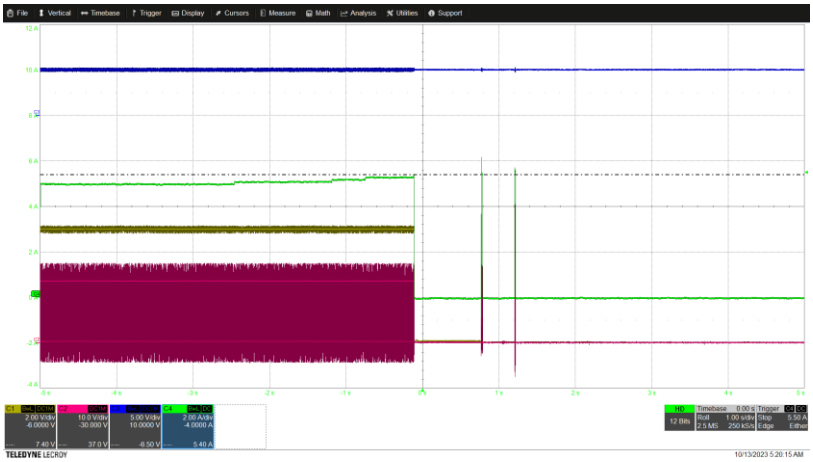
CH1: V_{BUS}; CH2: V_{IN} (DC) ;CH4: HG1 (wrt GND)

Figure 65 Output overvoltage protection

6.10.4 Output overcurrent protection (OCP)

DUT output overcurrent protection waveforms are shown in Figure 66.

Test conditions: V_{IN} = 230 V_{AC}; V_{BUS_C} = 5.0 V



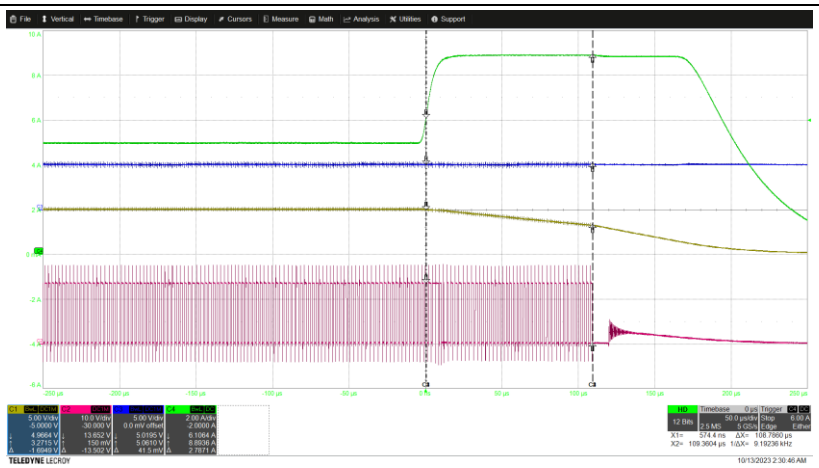
CH1: V_{BUS_C}; CH2: HG1(wrt GND); CH3: VDDD; CH4: I_{OUT}

Figure 66 Output overcurrent protection

6.10.5 Output short-circuit protection (SCP)

DUT output short-circuit protection waveforms are shown in Figure 67.

Test conditions: V_{IN} = 230 V_{AC}; V_{BUS_C} = 5.0 V



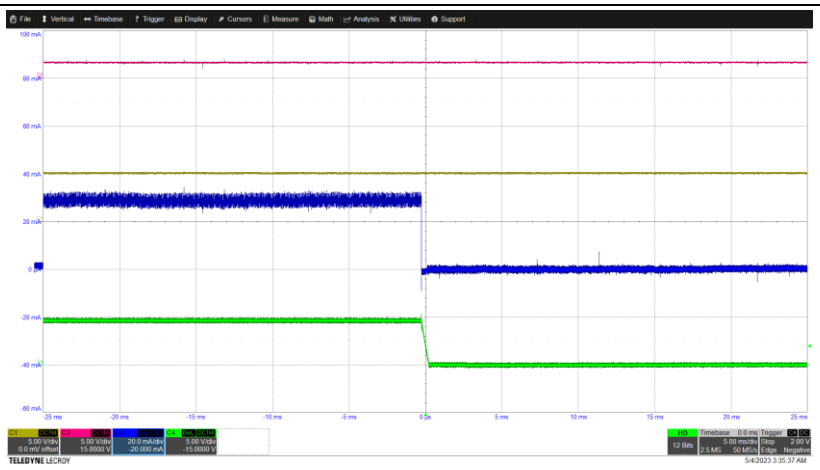
CH1: V_{BUS_C}; CH2: HG1 (wrt GND); CH3: VDDD; CH4: I_{OUT}

Figure 67 Output short-circuit protection

6.10.6 V_{CONN} overcurrent protection (OCP)

DUT V_{CONN} overcurrent protection waveforms when port is shown in Figure 68.

Test conditions: V_{IN} = 230 V_{AC}; V_{BUS_C} = 5.0 V



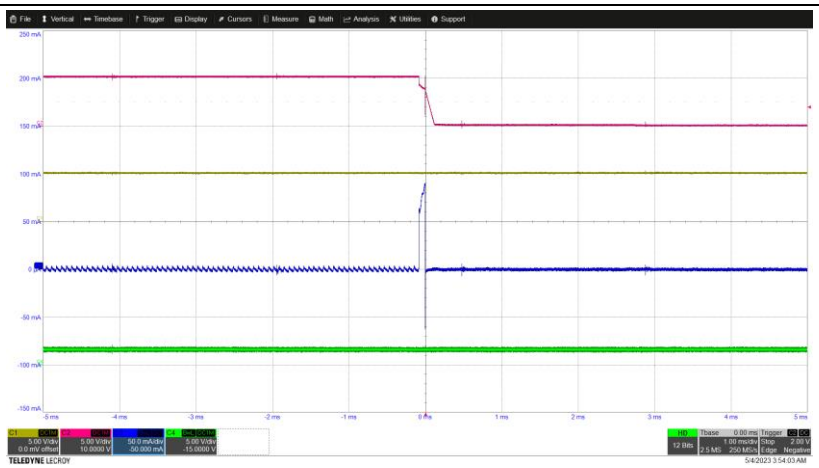
CH1: V_{BUS_C}; CH2: CC1; CH3: I_{LOAD} on CC1 line; CH4: CC2

Figure 68 V_{CONN} overcurrent protection

6.10.7 V_{CONN} short-circuit protection (SCP)

DUT V_{CONN} short-circuit protection waveforms when port is shown in Figure 69.

Test conditions: V_{IN} = 230 V_{AC}; V_{BUS_C} = 5.0 V



CH1: V_{BUS_C}; CH2: CC1; CH3: I_{LOAD} on CC1 line; CH4: CC2

Figure 69 V_{CONN} short-circuit protection

6.11 Current consumption

REF_CCG7SC_120W_3C solution board measured currents are tabulated in Table 24.

Table 24 Current consumption

Chip current	R16 current (external regulator) (mA)	R3 current (V_{in} current to internal regulator) (µA)	V_{IN} (V)	Total silicon consumption (mW)
Unattached condition	00.29	10.88	20.20	01.67
Buck mode (5V/0A)	11.32	36.33	07.97	56.39
Bypass mode (20 V/0 A)	08.18	05.97	20.20	41.02
At fault condition	7.952	23.46	06.97	60.75

6.12 Light load requirements

XDPS2221 + REF_CCG7SC_120W_3C solution board EuP Lot6 results are tabulated in Table 25.

Table 25 EuP Lot6 results

V_{IN}(AC)/Frequency	P_{IN} (avg)	V_{BUS_C}/I_{OUT}	P_{OUT}	Efficiency (%)
230 VAC/50 Hz	0.488 W	20 V/0.0125 A	0.250 W	51.23%
115 VAC/60 Hz	0.496 W	20 V/0.0125 A	0.250 W	50.40%

7 Three port power management test results of XDPS2221 + REF_CCG7SC_120W_3C

Efficiency captured using the test setup shown in the Appendix: Efficiency measurement test setup.

Here all three ports were loaded and each of the ports was loaded with equal amount of current.

7.1 Peak efficiency and full load efficiency table

Peak efficiency test results are tabulated in Table 26.

Table 26 Peak efficiency

V_{BUS_C} (V)	115 V_{AC}/60 Hz	230 V_{AC}/50 Hz
03.3 V	88.11% – 3*3.08 A	89.32% – 3*3.08 A
05.0 V	89.94% – 3*3.50 A	91.05% – 3*3.50 A
09.0 V	91.11% – 3*3.30 A	92.12% – 3*3.08 A
12.0 V	92.04% – 3*2.17 A	93.14% – 3*2.43 A
15.0 V	92.42% – 3*2.21 A	93.53% – 3*2.21 A
20.0 V	92.05% – 3*1.70 A	93.15% – 3*2.00 A

*Note: Peak efficiency: 93.53% (At V_{IN}: 230 V_{AC}, V_{BUS_C}: 20 V, I_{OUT}: 3*2.21 A)*

Full load efficiency test results are tabulated in Table 27.

Table 27 Full load efficiency

V_{BUS_C} (V)	115 V_{AC}/60 Hz	230 V_{AC}/50 Hz
03.3 V	86.32% – 3*4.75 A	88.23% – 3* 4.75 A
05.0 V	89.07% – 3*5.00 A	89.81% – 3*5.00 A
09.0 V	90.72% – 3*4.40 A	91.91% – 3*4.40 A
12.0 V	92.03% – 3*2.56 A	93.03% – 3*2.56 A
15.0 V	92.10% – 3*2.60 A	93.20% – 3*2.60 A
20.0 V	92.00% – 3*1.90 A	93.15% – 3*2.00 A

Four-point efficiency average test results are tabulated in Table 28.

Table 28 Efficiency 4-pt average

Parameter	DOE level VI limit	Unit	Test conditions	Test results (%)	
				230 V/50 Hz	Remarks
Four-point average efficiency (Average of 25%, 50%, 75%, and 100% load)	85.36	%	V_{BUS} = 3.3 V in all 3 ports; Total P_{OUT} = 49.5 W	88.14	Pass
	86.00	%	V_{BUS} = 5 V in All 3 ports; Total P_{OUT} = 75 W	89.39	Pass
	86.00	%	V_{BUS} = 9 V in all 3 ports; Total P_{OUT} = 120 W	90.06	Pass
	86.00	%	V_{BUS} = 12 V in All 3 ports; Total P_{OUT} = 86.4 W	90.81	Pass
	86.00	%	V_{BUS} = 15 V in All 3 ports; Total P_{OUT} = 120 W	91.30	Pass
	86.00	%	VBUS = 20 V in All 3 ports; Total P_{OUT} = 120 W	90.90	Pass
	86.00	%	Port #1 V_{BUS} = 15 V/40 W Port #2 V_{BUS} = 09 V/40 W Port #3 V_{BUS} = 09 V/40 W Total P_{OUT} = 120 W	90.50	Pass
	86.00	%	Port #1 V_{BUS} = 20 V/40 W Port #2 V_{BUS} = 05 V/40 W Port #3 V_{BUS} = 05 V/40 W Total P_{OUT} = 120 W	91.41	Pass

7.2 Efficiency graphs

Efficiency measured at 230 V_{AC}/50 Hz input and to the DUT; V_{BUS_C} PDO, PPS voltages are 3.3 V, 5 V, 9 V, 12 V, 15 V, and 20 V for all the three ports, as shown in Figure 70.

Efficiency measured at 115 V_{AC}/60 Hz input and to the DUT; V_{BUS_C} PDO, PPS voltages are 3.3 V, 5 V, 9 V, 12 V, 15 V, and 20 V for all the three ports, as shown in Figure 71.

Each port was loaded from 0 A to the maximum output current to make total system power 120 W.

The efficiency is based on the test setup of Figure 96.

7.2.1 Efficiency and power losses at 230 V_{AC}/50 Hz input

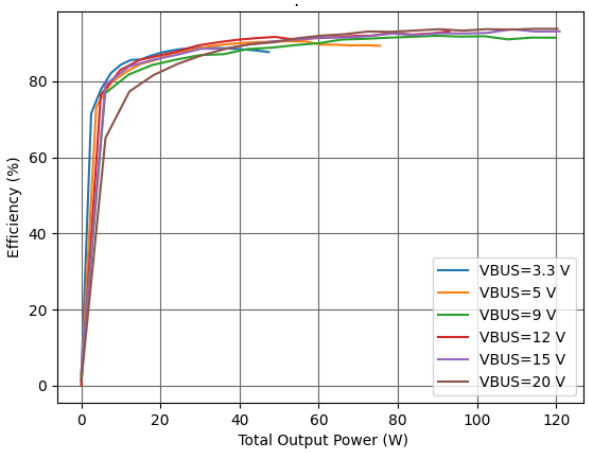


Figure 70 Efficiency at 230 V_{AC} input

7.2.2 Efficiency and power losses at 115 V_{DC}/60 Hz input

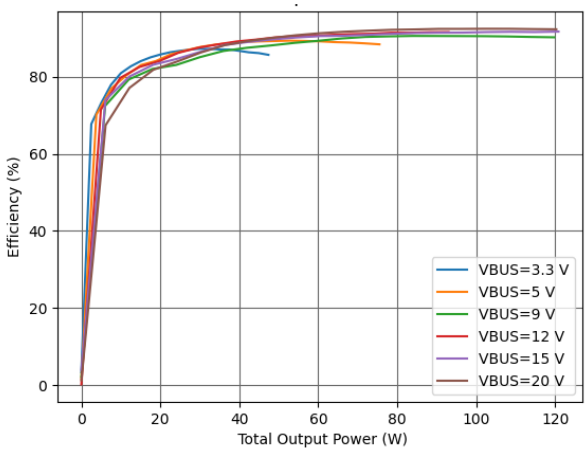


Figure 71 Efficiency at 115 V_{DC} input

7.3 Output voltage and current regulation

Output voltage regulation was measured both in the constant voltage (CV) and constant current (CC) modes.

7.3.1 Output voltage regulation (CV mode)

Output constant voltage regulation measured from 0 A to maximum load currents that each port can take to have maximum system power of 120 W, are shown in Figure 72, Figure 73, and Figure 74.

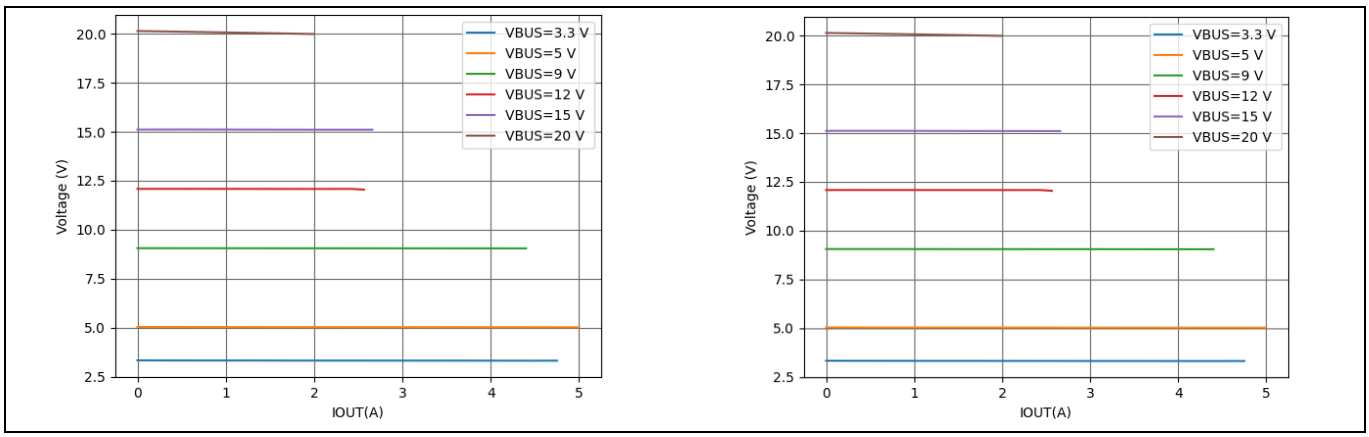


Figure 72 CV regulation at 230 V_{AC} and 115 V_{AC} input of port #1

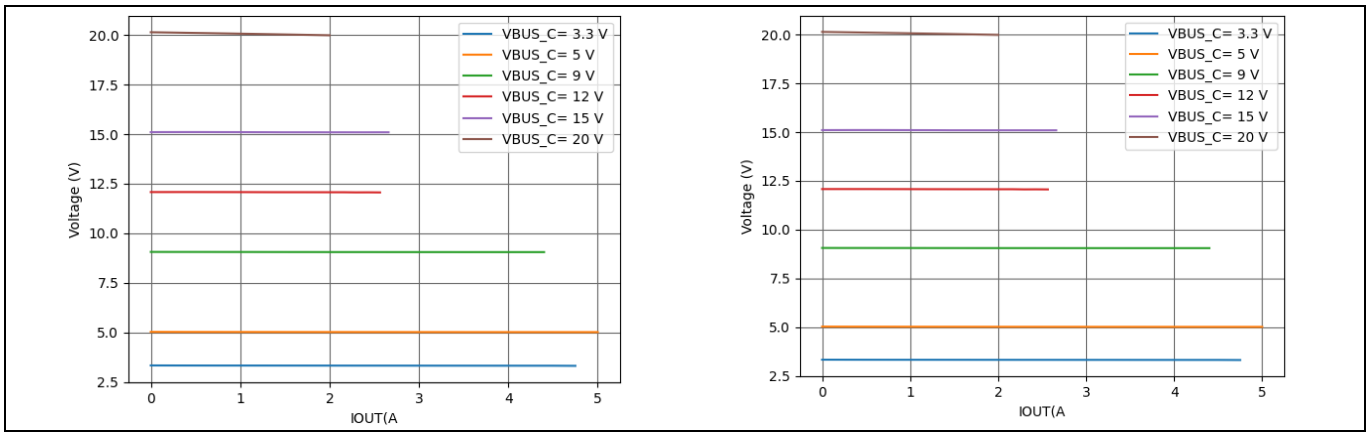


Figure 73 CV regulation 230 V_{AC} and 115 V_{AC} input of port #2

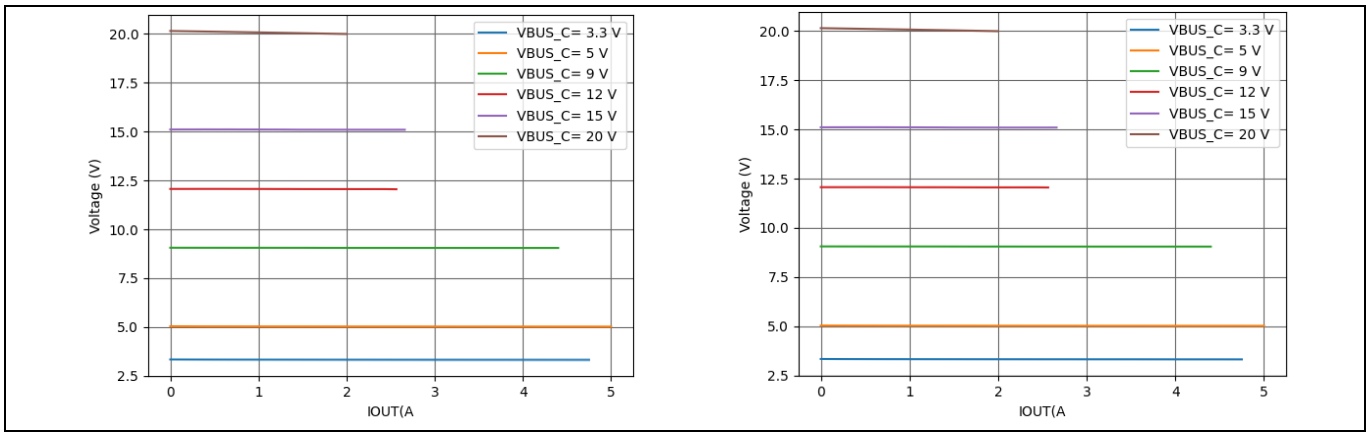


Figure 74 CV regulation 230 V_{AC} and 115 V_{AC} input of port #3

7.3.2 Output current regulation (CC mode)

Output constant current (CC) regulation of each port measured at 1.5 A output currents are shown in Figure 75.

7.3.3 CC regulation curve at 230 V_{AC} input and rated output current of 1.5 A

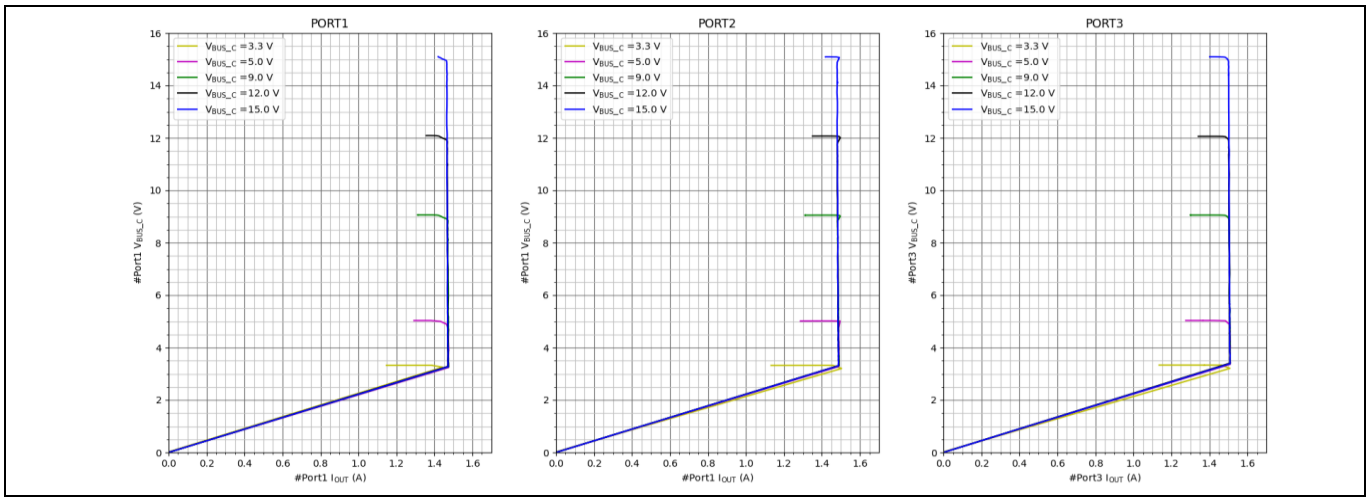


Figure 75 CC regulation curve at 230 V_{AC} input and 1.5 A output current

7.3.4 CC regulation curve at 115 V_{AC} input and rated output current of 1.5 A

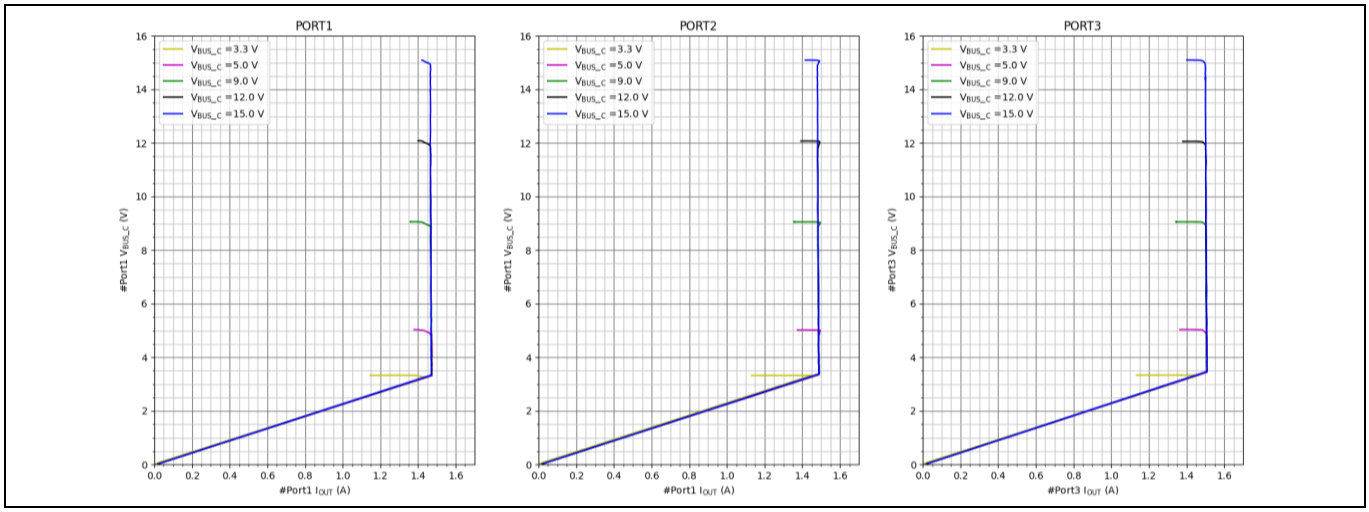


Figure 76 CC regulation curve at 115 V_{AC} input and 1.5 A output current

7.4 Output voltage ripple measurement

Output voltage peak-to-peak ripple was measured across the output capacitors C19 using a short ground loop connected to the probe.

7.4.1 Output voltage ripple peak-to-peak (mV)

Output voltage peak-to-peak ripple tabulated in Table 29 and Table 30.

Table 29 Peak-to-peak ripple (mV) at 230 V_{AC} input

V_{BUS_C} – I_{OUT}	Port #1 ripple (mV)	Port #2 ripple (mV)	Port #3 ripple (mV)
03.3 V – 0.00 A	11.873	06.258	006.039
03.3 V – 4.75A	34.154	39.165	046.143
05.0 V – 0.00 A	13.608	06.823	006.977
05.0 V – 5.00 A	69.349	54.341	083.059
09.0 V – 0.00 A	07.106	05.461	006.039
09.0 V – 4.40 A	71.071	88.726	102.154
12.0 V – 0.00 A	55.651	35.015	062.089
12.0 V – 2.56 A	72.638	83.136	080.091
15.0 V – 0.00 A	17.193	14.944	019.698
15.0 V – 2.73 A	85.719	99.224	105.199
20.0 V – 0.00 A	13.389	27.986	017.797
20.0 V – 2.00 A	24.530	07.645	025.018

Table 30 Peak-to-peak (mV) ripple at 115 V_{AC} input

V_{BUS_C} - I_{OUT}	Port #1 ripple	Port #2 ripple	Port #3 ripple
03.3 V – 0.000 A	11.153	06.849	005.911
03.3 V – 5.000 A	40.129	37.456	052.387
05.0 V – 0.000 A	07.016	12.425	006.605
05.0 V – 5.000 A	70.467	57.964	076.930
09.0 V – 0.000 A	07.260	06.630	016.614
09.0 V – 4.440 A	86.374	99.301	119.590
12.0 V – 0.000 A	07.620	12.708	018.144
12.0 V – 2.565 A	88.854	81.954	100.650
15.0 V – 0.000 A	16.756	19.454	019.377
15.0 V – 2.660 A	116.07	109.067	153.372
20.0 V – 0.000 A	17.874	16.512	049.856
20.0 V – 2.000 A	68.783	33.756	095.896

7.5 Output voltage regulation

Output voltage regulation measured at V_{IN} = 230 V_{AC}, V_{BUS_C} = 3.3 V, 5 V, 9 V, 12 V, 15 V, 20 V;

I_{OUT} = 0 A to maximum current is shown in Table 31.

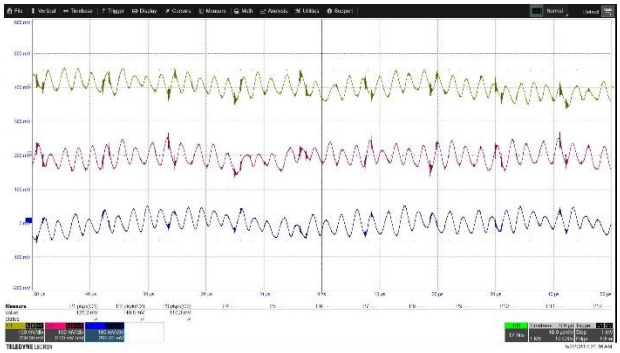
Table 31 Regulation at 230 V_{AC} input

I_{OUT} (A)	Port #1 V_{BUS_C} (V_{DC})	Port #1 % Regulation	I_{OUT} (A)	Port #2 V_{BUS_C} (V_{DC})	Port #2 % Regulation	I_{OUT} (A)	Port #3 V_{BUS_C} (V_{DC})	Port #3 % Regulation
0.00 A	03.36	1.75%	0.00 A	03.323	1.31%	0.00 A	03.345	0.52%
4.75 A	03.302		4.75 A	03.280		4.75 A	03.3276	
0.00 A	05.043	0.28%	0.00 A	04.995	0.39%	0.00 A	05.023	0.35%
5.00 A	05.029		5.00 A	04.976		5.00 A	05.005	
0.00 A	09.061	0.35%	0.00 A	08.981	0.38%	0.00 A	09.031	0.13%
4.40 A	09.029		4.40 A	08.947		4.40 A	09.019	
0.00 A	12.072	0.11%	0.00 A	11.982	0.22%	0.00 A	12.047	0.27%
2.56 A	12.058		2.56 A	11.955		2.56 A	12.014	
0.00 A	15.097	0.18%	0.00 A	14.974	0.21%	0.00 A	15.080	0.20%
2.73 A	15.069		2.66 A	14.943		2.66 A	15.049	
0.00 A	20.253	0.77%	0.00 A	20.252	0.77%	0.00 A	20.253	0.78%
2.00 A	20.098		2.00 A	20.096		2.00 A	20.095	

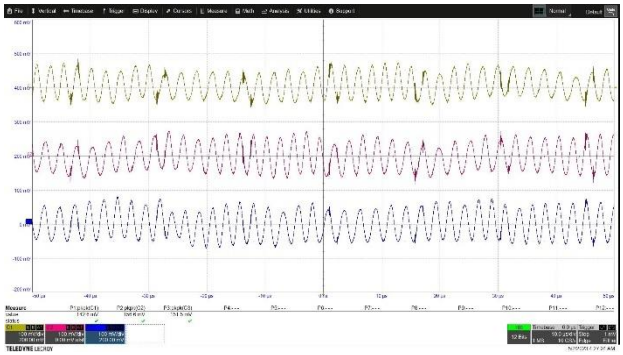
7.5.1 Output voltage ripple peak-to-peak measurement graphs

Output voltage peak-to-peak ripple waveforms for 230 V_{AC} at full load are shown in Figure 77.

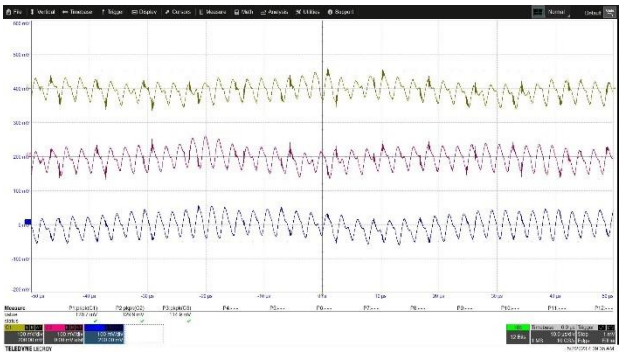
Output voltage peak-to-peak ripple waveforms for 115 V_{AC} at full load are shown in Figure 78.



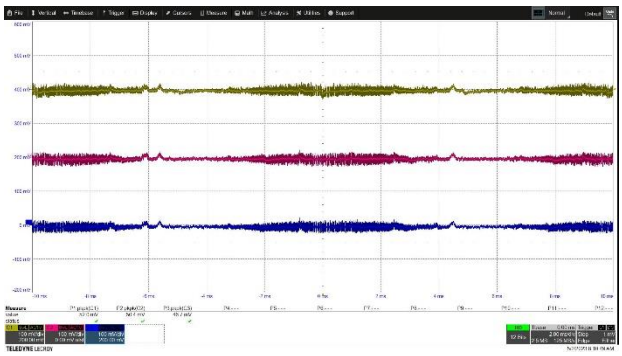
Port #1 V_{BUS_C}: 05 V (CH1); port #2 V_{BUS_C}: 05 V (CH2); port #3 V_{BUS_C}: 05 V (CH3); I_{OUT}: 5 A



Port #1 V_{BUS_C}: 09 V (CH1); port #2 V_{BUS_C}: 09 V (CH2); port #3 V_{BUS_C}: 09 V (CH3); I_{OUT}: 4.6 A

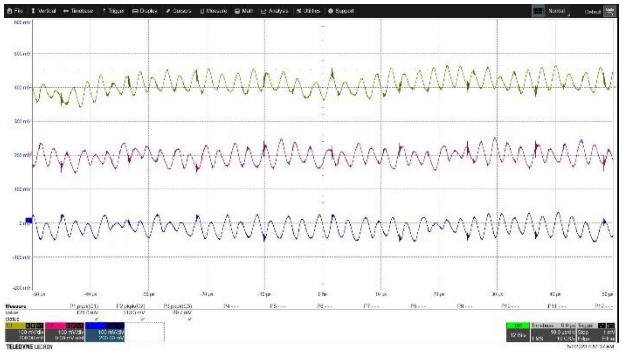


Port #1 V_{BUS_C}: 15 V (CH1); port #2 V_{BUS_C}: 15 V (CH2); port #3 V_{BUS_C}: 15 V (CH3); I_{OUT}: 2.67 A



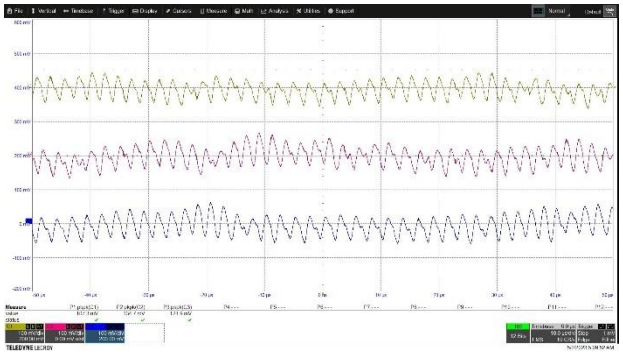
Port #1 V_{BUS_C}: 20 V (CH1); port #2 V_{BUS_C}: 20 V (CH2); port #3 V_{BUS_C}: 20 V (CH3); I_{OUT}: 2 A

Figure 77 Ripple measurement – input voltage: 230 V_{AC}

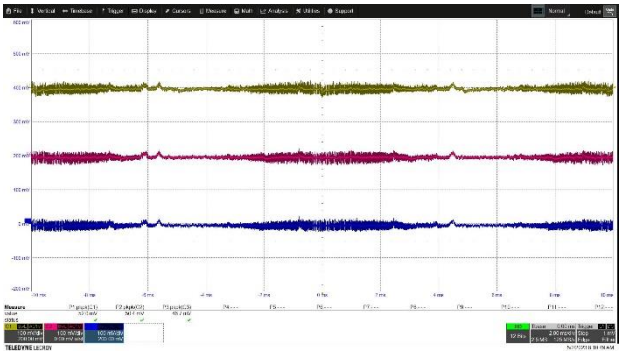


Port #1 V_{BUS_C}: 05 V (CH1); port #2 V_{BUS_C}: 05 V (CH2); port #3 V_{BUS_C}: 05 V (CH3); I_{OUT}: 5 A

Port #1 V_{BUS_C}: 09 V (CH1); port #2 V_{BUS_C}: 09 V (CH2); port #3 V_{BUS_C}: 09 V (CH3); I_{OUT}: 4.6 A



Port #1 V_{BUS_C}: 15 V (CH1); port#2 V_{BUS_C}: 15 V (CH2); port #3 V_{BUS_C}: 15 V (CH3); I_{OUT}: 2.67 A



Port #1 V_{BUS_C}: 20 V(CH1); port #2 V_{BUS_C}: 20 V (CH2); port #3 V_{BUS_C}: 20 V (CH3); I_{OUT}: 2 A

Figure 78 Ripple measurement – input voltage: 115 V_{AC}

7.6 Output voltage dynamic response waveforms

V_{IN} = 230 V, output voltage response when the output current is from 0 A – 1 A – 0 A is shown in Figure 79.

V_{IN} = 115 V, output voltage response when the output current is from 0 A – 1 A – 0 A is shown in Figure 80.

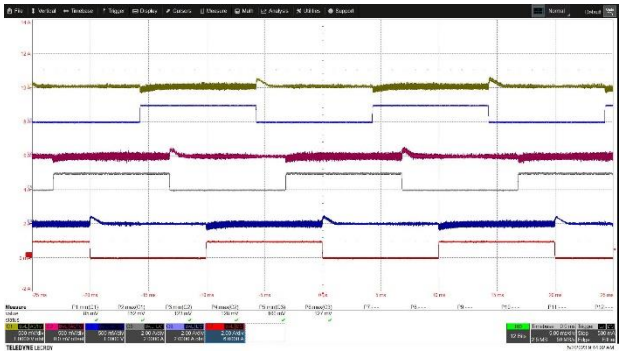
Port #1: V_{BUS_C} (CH1); I_{OUT} (CH6);

Port #2: V_{BUS_C} (CH3); I_{OUT} (CH7);

Port #3: V_{BUS_C} (CH2); I_{OUT} (CH5);

Port #1 V_{BUS_C}: 3.3 V (CH1); port #2 V_{BUS_C}: 3.3 V (CH3); port #3 V_{BUS_C}: 3.3 V (CH2); I_{OUT}: 0 A to 1 A to 0 A

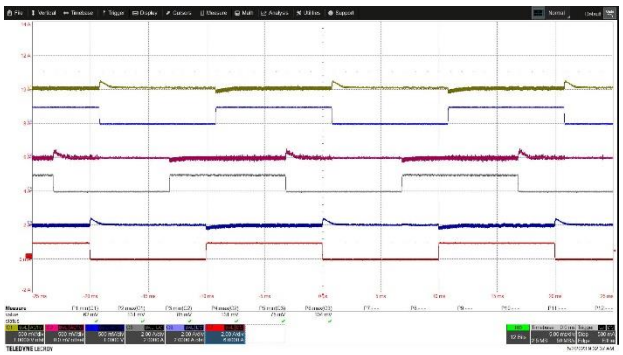
Port #1 V_{BUS_C}: 05 V (CH1); port #2 V_{BUS_C}: 05 V (CH3); port #3 V_{BUS_C}: 05 V (CH2); I_{OUT}: 0 A to 1 A to 0 A



Port #1 V_{BUS_C}: 09 V (CH1); port #2 V_{BUS_C}: 09 V (CH3); port #3 V_{BUS_C}: 09 V (CH2); I_{OUT}: 0 A to 1 A to 0 A

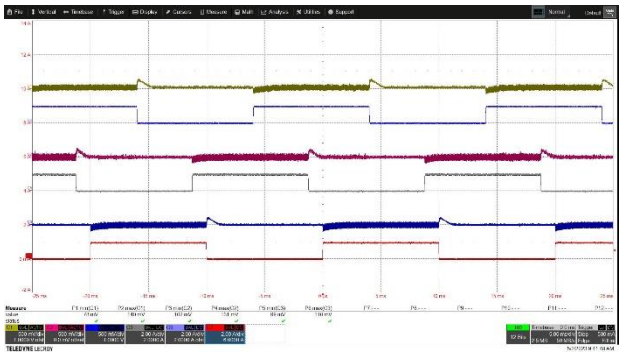
Port #1 V_{BUS_C}: 12 V (CH1); port #2 V_{BUS_C}: 12 V (CH3); port #3 V_{BUS_C}: 12 V (CH2); I_{OUT}: 0 A to 1 A to 0 A

Figure 79 Output dynamic response waveforms - input 115 V_{AC}; load current transition 0 A to 1 A to 0 A



Port #1 V_{BUS_C}: 3.3 V (CH1); port #2 V_{BUS_C}: 3.3 V (CH3); port #3 V_{BUS_C}: 3.3 V (CH2); I_{OUT}: 0 A to 1 A to 0 A

Port #1 V_{BUS_C}: 05 V (CH1); port #2 V_{BUS_C}: 05 V (CH3); port #3 V_{BUS_C}: 05 V (CH2); I_{OUT}: 0 A to 1 A to 0 A



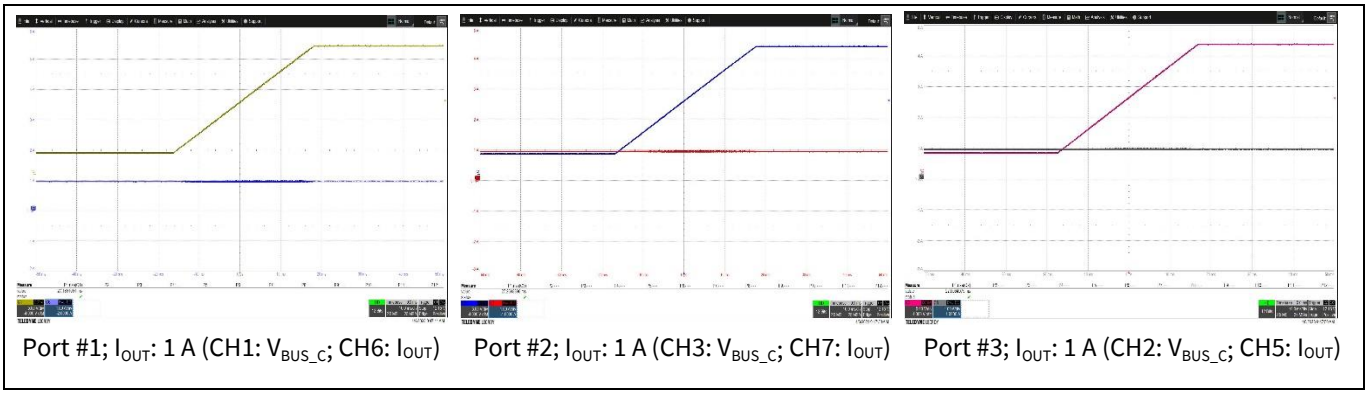
Port #1 V_{BUS_C}: 09 V (CH1); port #2 V_{BUS_C}: 09 V (CH3); port #3 V_{BUS_C}: 09 V (CH2); I_{OUT}: 0 A to 1 A to 0 A

Port #1 V_{BUS_C}: 12 V (CH1); port #2 V_{BUS_C}: 12 V (CH3); port #3 V_{BUS_C}: 12 V (CH2); I_{OUT}: 0 A to 1 A to 0 A

Figure 80 Output dynamic response waveforms - input 230 V_{AC}; load current transition 0 A to 1 A to 0 A

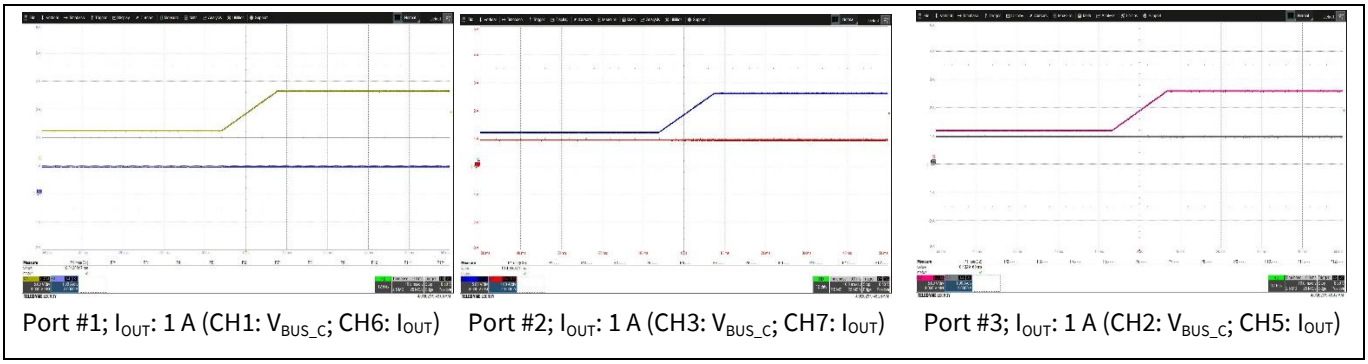
7.7 Output voltage transition

Output voltage transition at 230 V_{AC} input and 1 A load is measured and is shown in Figure 81, Figure 82, and Figure 83.



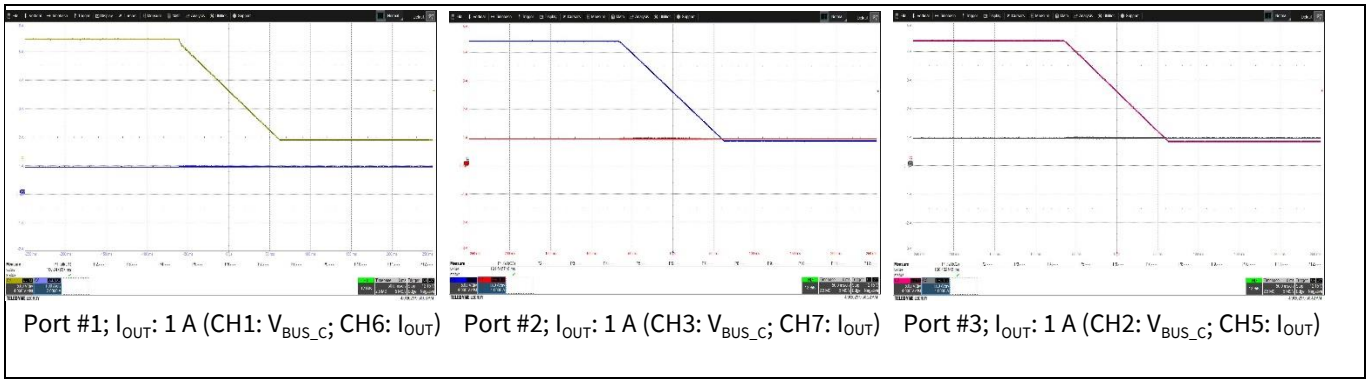
Port #1; I_{OUT}: 1 A (CH1: V_{BUS_C}; CH6: I_{OUT}) Port #2; I_{OUT}: 1 A (CH3: V_{BUS_C}; CH7: I_{OUT}) Port #3; I_{OUT}: 1 A (CH2: V_{BUS_C}; CH5: I_{OUT})

Figure 81 Input 230 V_{AC}; V_{BUS_C} transition from 3.3 V to 21 V



Port #1; I_{OUT}: 1 A (CH1: V_{BUS_C}; CH6: I_{OUT}) Port #2; I_{OUT}: 1 A (CH3: V_{BUS_C}; CH7: I_{OUT}) Port #3; I_{OUT}: 1 A (CH2: V_{BUS_C}; CH5: I_{OUT})

Figure 82 Input 230 V_{AC}; V_{BUS_C} transition from 5.0 V to 12 V

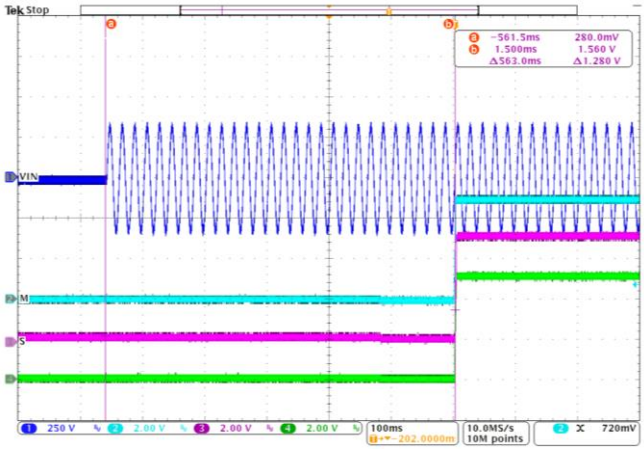


Port #1; I_{OUT}: 1 A (CH1: V_{BUS_C}; CH6: I_{OUT}) Port #2; I_{OUT}: 1 A (CH3: V_{BUS_C}; CH7: I_{OUT}) Port #3; I_{OUT}: 1 A (CH2: V_{BUS_C}; CH5: I_{OUT})

Figure 83 Input 230 V_{AC}; V_{BUS_C} transition from 21 V to 3.3 V

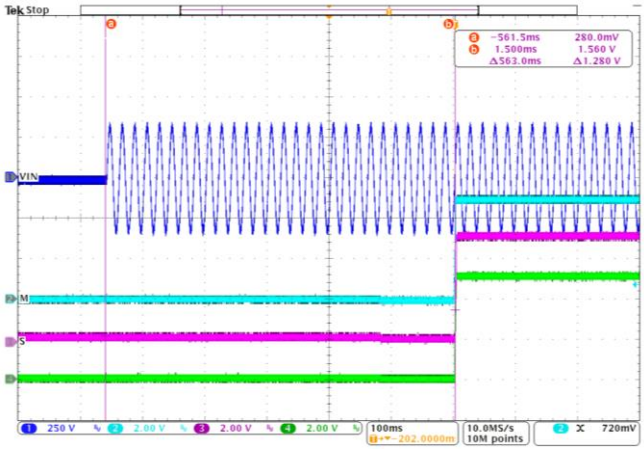
7.8 Start-up turn-on delay

Turn-on delay with respect to DUT input voltage and the output voltage is measured at no load and 1 A load is shown in Figure 84 and Figure 85.



CH1: V_{IN}; CH2: Port#1 V_{BUS}; CH3: Port#2 V_{BUS}; CH4: Port#3 V_{BUS}

Figure 84 Input 230 V_{AC}; V_{BUS_C}: 5 V; I_{OUT}: 0 A



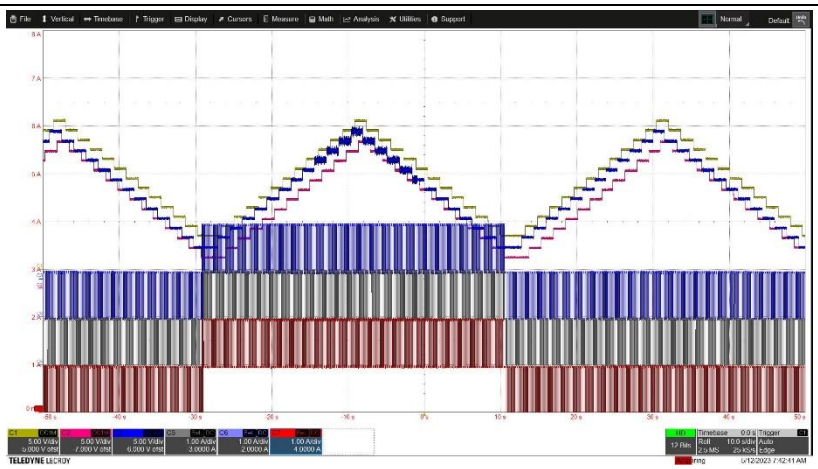
CH1: V_{IN}; CH2: Port#1 V_{BUS}; CH3: Port#2 V_{BUS}; CH4: Port#3 V_{BUS}

Figure 85 Input 230 V_{AC}; V_{BUS_C}: 5 V; I_{OUT}: 3 A

7.9 Stress test waveforms

The XDPS2221 + REF_CCG7SC_120W_3C solution board with three ports connected was subjected to electrical stress conditions.

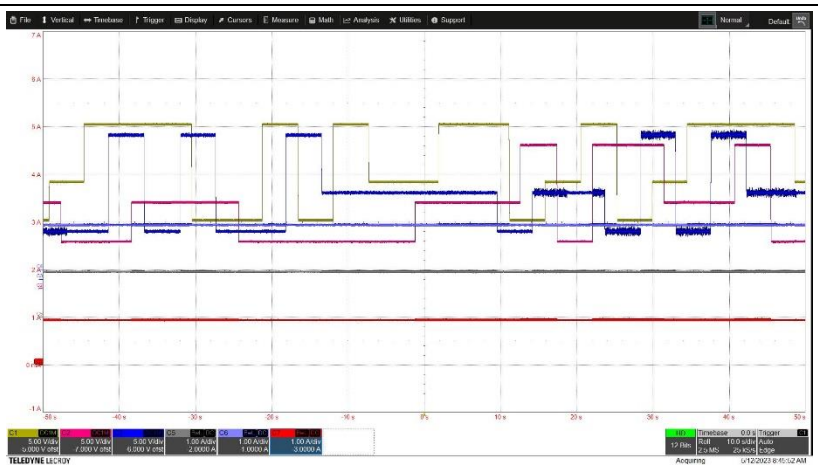
- **Electrical stress test #1** V_{IN} = 230 V_{AC}; V_{BUS_C} – continuously changing from 3.3 V – 21 V with 1 V step and vice versa (PPS); I_{OUT} = 0 A to 2 A with 1 A step for a duration of 60 minutes. Captured waveforms are shown in Figure 86.



CH1:port #1 V_{BUS_C}; CH6:port #1 I_{OUT}; CH2:port #2 V_{BUS_C}; CH5:port #2 I_{OUT}; CH3:port #3 V_{BUS_C}; CH7:port #3 I_{OUT}

Figure 86 V_{IN} = 22.5 V_{DC}; V_{BUS_C} – continuously changing from 3.3 V – 21 V (PPS) and vice versa; I_{OUT} = 0 A to 4 A with 1 step

- **Electrical stress test #2** V_{IN}= 22.5 V_{DC}; V_{BUS_C}: randomly changing from 5 V to 9 V to 15 V (PDO); I_{OUT}: 1 A for a duration of 60 minutes. Captured waveforms are shown in Figure 87 .



CH1:port #1 V_{BUS_C}; CH6:port #1 I_{OUT}; CH2:port #2 V_{BUS_C}; CH5:port #2 I_{OUT}; CH3:port #3 V_{BUS_C}; CH7:port #3 I_{OUT}

Figure 87 V_{IN} = 22.5 V_{DC}; V_{BUS_C} – continuously changing from 5 V to 9 V to 15 V (PDO); I_{OUT} = 1 A

8 Thermal performance

The following section displays the DUT temperature measurements captured at ambient temperature.

8.1 Thermal image

- Test condition: V_{IN} = 22.5 V_{DC}, V_{BUS_C} = 20 V, I_{OUT} = 5 A
- VDDD is powered using external 5 V_{DC} source
- Lab ambient temperature: 26.1°C and thermal scan captured in open-frame after 60 minutes (see Figure 88 and Table 32)

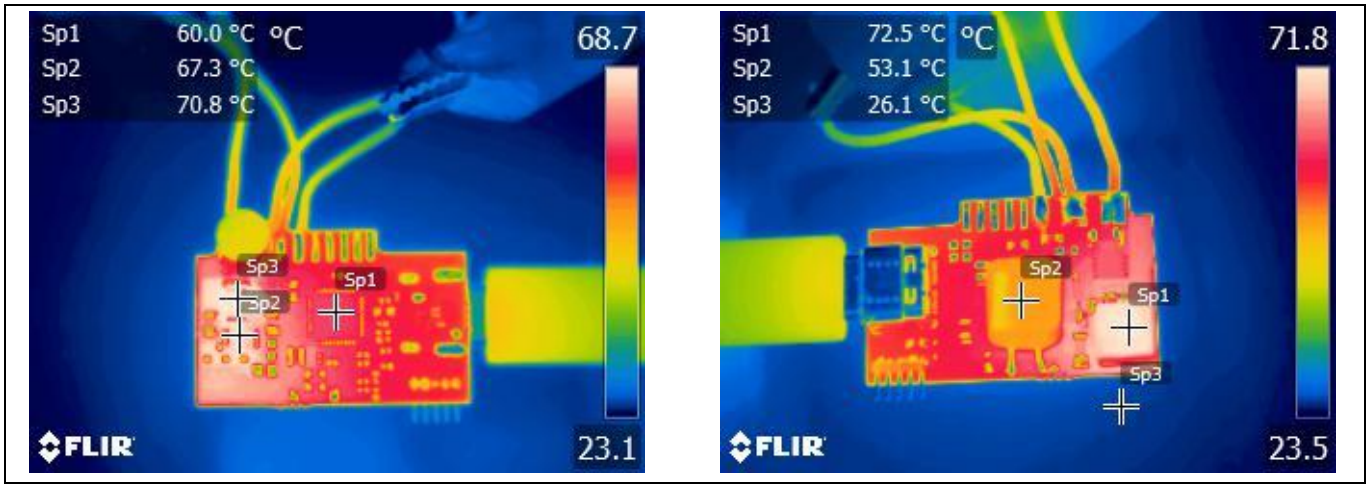


Figure 88 DUT thermal image at ambient temperature, V_{IN} = 22.5 V_{DC}; V_{BUS_C} = 20 V, I_{OUT} = 5 A

Table 32 Temperature measurement

Markers	Designator	Component	Temperature (°C)
Sp1 (left Image)	U1	CCG7SC	60.0
Sp2 (left Image)	Q2	MOSFET	67.3
Sp3 (left Image)	Q1	MOSFET	70.8
Sp1 (right image)	L1	Inductor	72.5
Sp2 (right image)	EC1	Capacitor	53.1

9 Bode plots

Bode plot results are captured by connecting XDPS2221 to REF_CCG7SC_120W_3C.

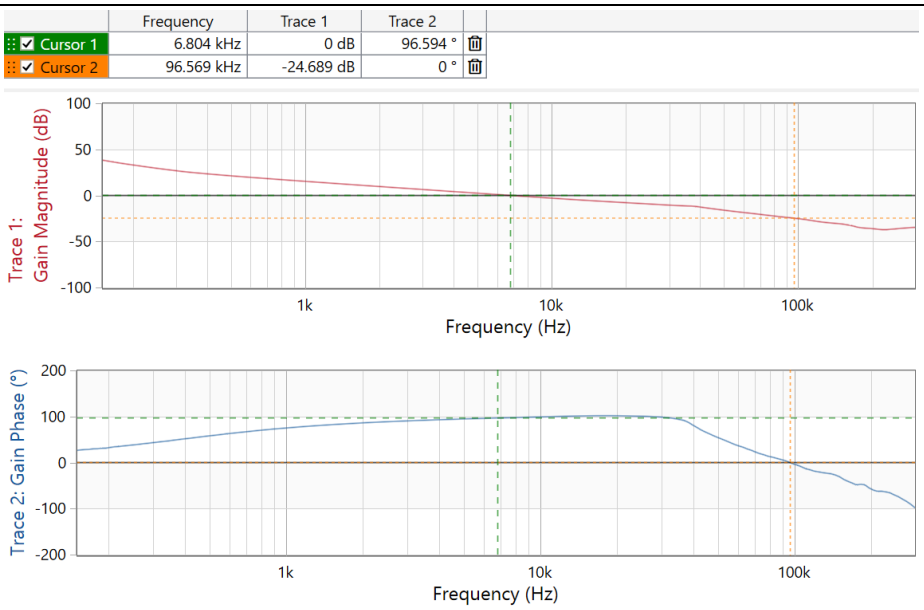


Figure 89 Port #1 (master) Bode plot: V_{IN} = 230 V_{AC}, V_{BUS_C} = 5 V, I_{OUT} = 5 A

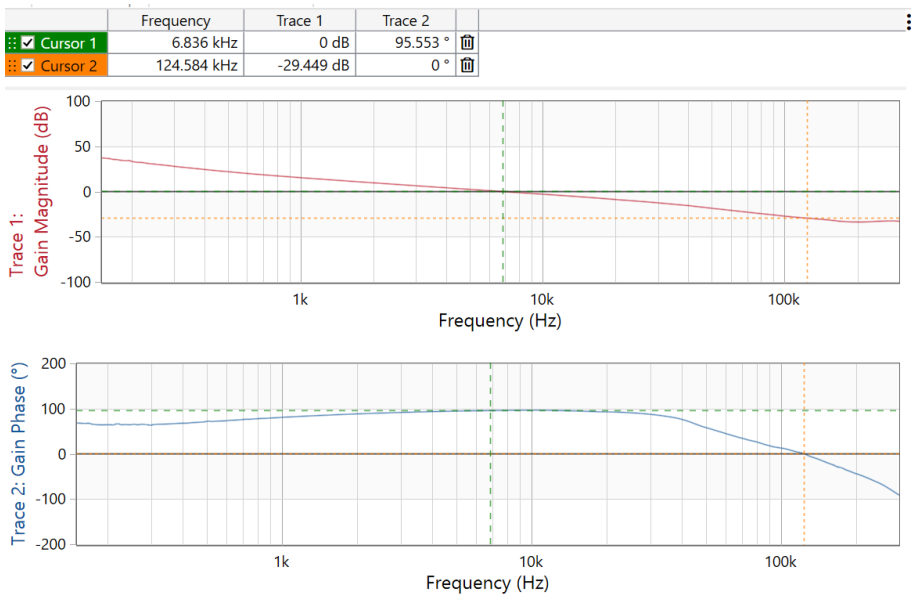


Figure 90 Port #1 (master) Bode plot: V_{IN} = 230 V_{AC}, V_{BUS_C} = 15 V, I_{OUT} = 5 A

Bode plots

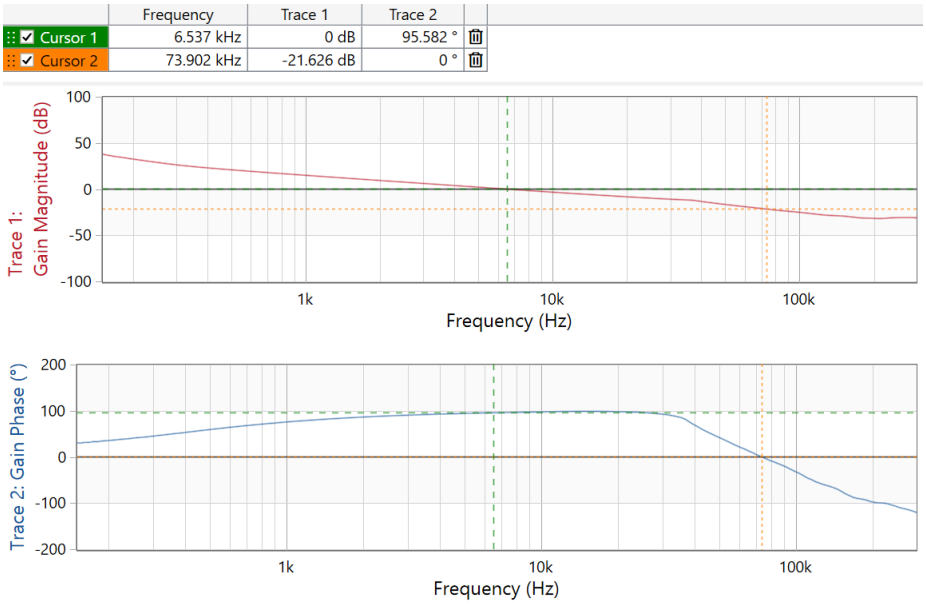


Figure 91 Port #2 (slave-1) Bode plot: V_{IN} = 230 V_{AC}, V_{BUS_C} = 5 V, I_{OUT} = 5 A

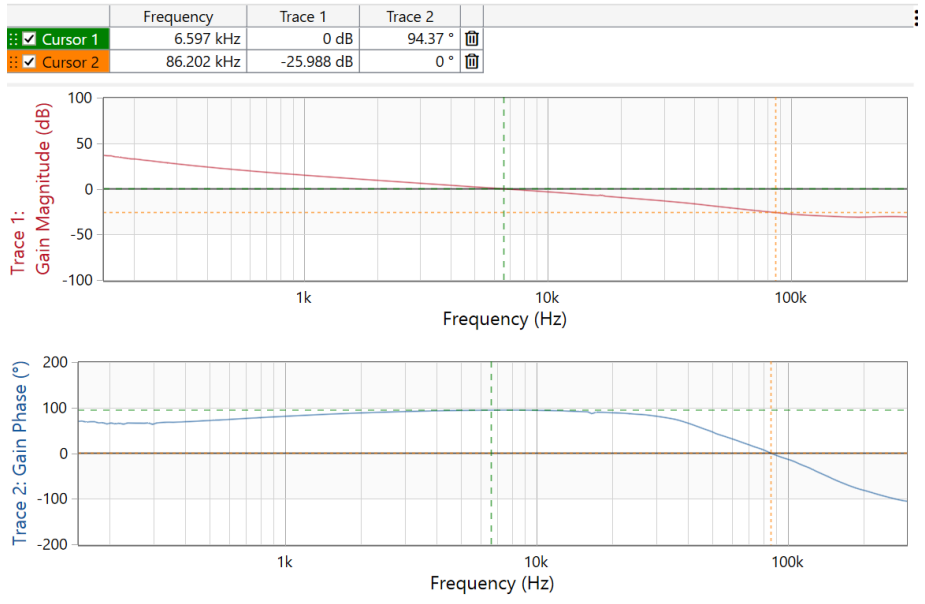


Figure 92 Port #2 (slave-1) Bode plot: V_{IN} = 230 V_{AC}, V_{BUS_C} = 15 V, I_{OUT} = 5 A

10 Circuit schematics

The following sections contain the schematics used for the test equipment setup.

10.1 REF_CCG7SC_100W_R2

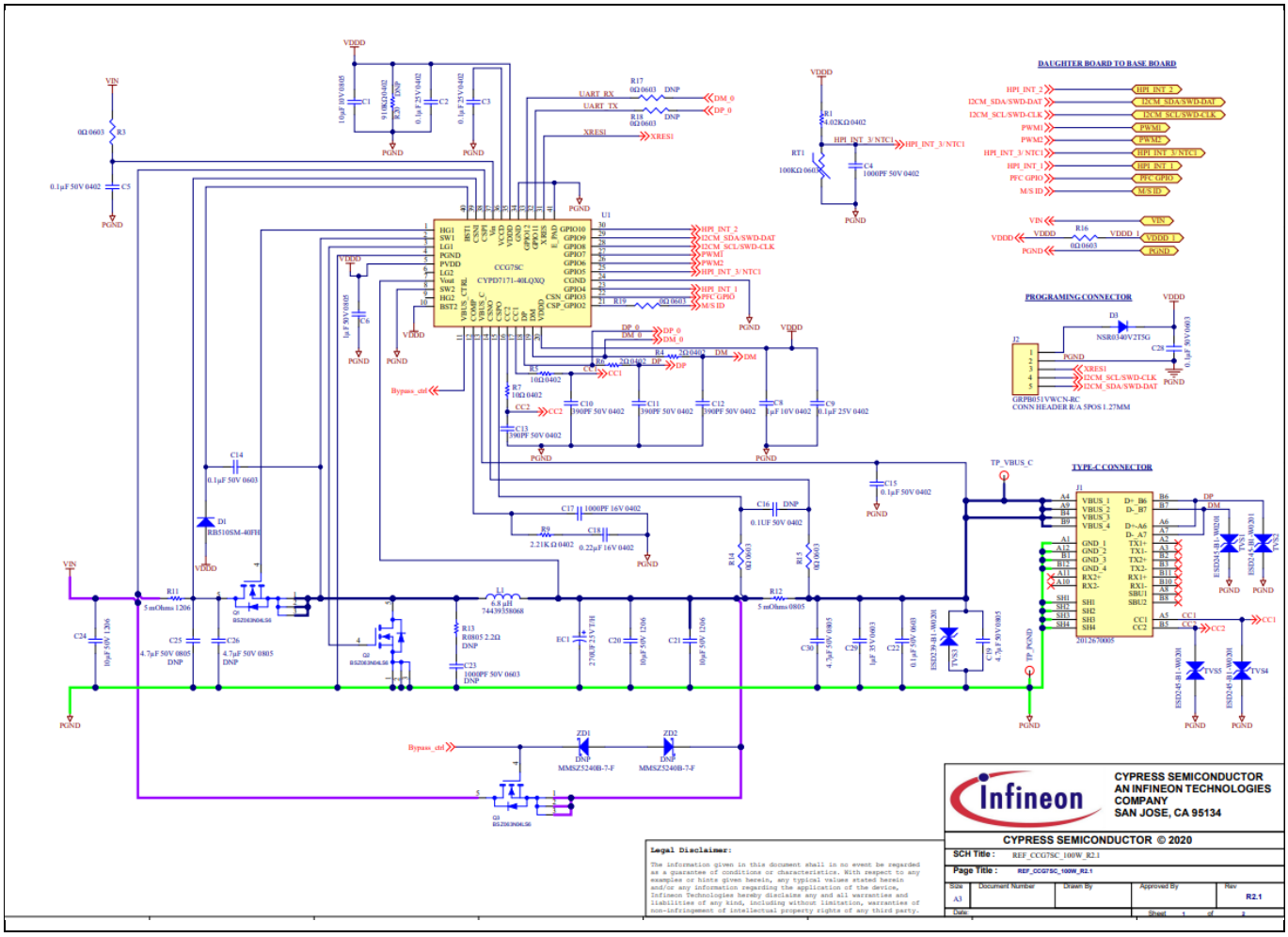


Figure 93 Standalone EZ-PD™ CCG7SC 100 W daughter board schematics

10.2 REF_CCG7SC_BASE_120W_3C_R2

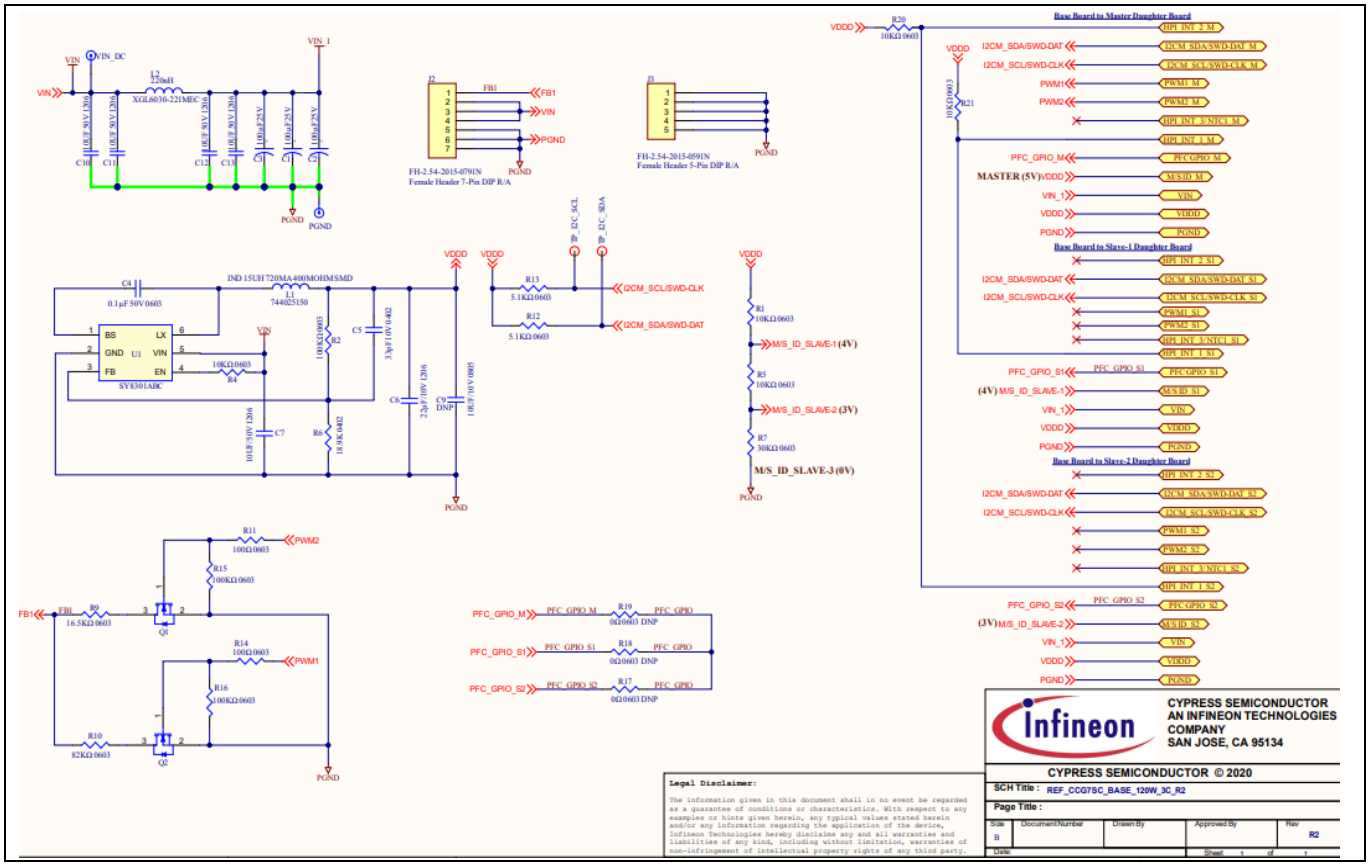


Figure 94 CCG7SC 120 W base board schematics

11 Appendix: Efficiency measurement test setup

Efficiency measurements are captured with the test setup, REF_CCG7SC_120W_3C board input connector to output connector; measurement points are shown in the following sections.

11.1 Efficiency measurement – input connector to the USB Type-C connector on the board

Efficiency measurement connection is done as shown in Figure 95 and Figure 96. For one port measurement, port #1 is connected, and other ports are disconnected. For 3 port measurement, port #1, port #2, and port #3 are connected.

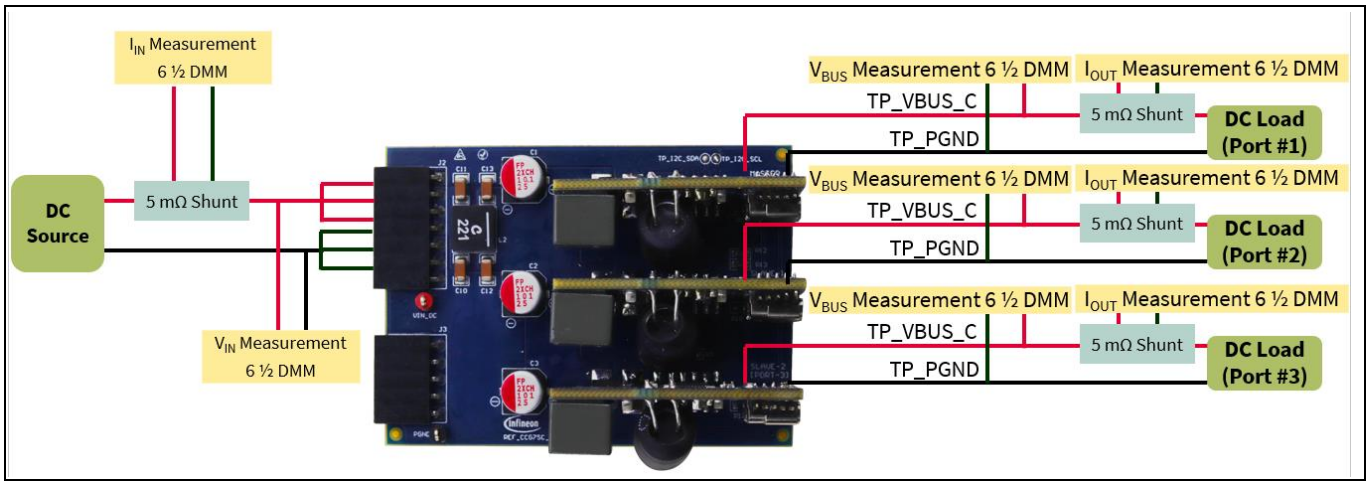


Figure 95 Efficiency measurement of standalone multiport DC-DC converter – input connector to the USB Type-C connector on the board

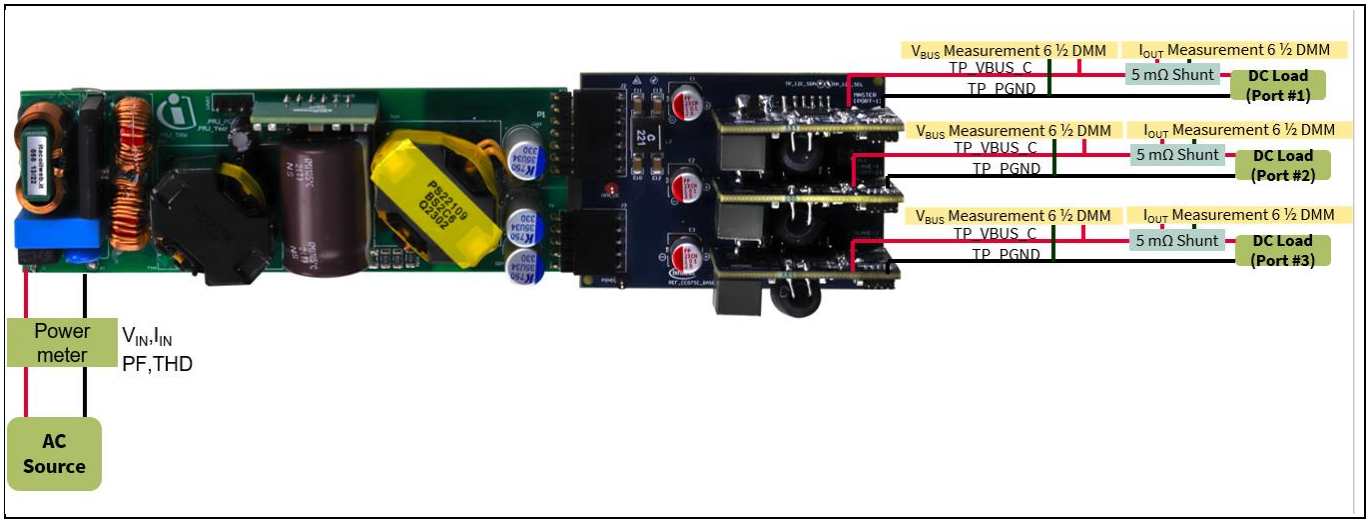


Figure 96 Efficiency measurement of AC-DC multiport adapter and charger – input connector to the USB Type-C connector on the board

Revision history

Document revision	Date	Description of changes
**	2023-06-26	Initial release
*A	2023-11-21	Updated efficiency numbers found in Section 4 and Section 5. Updated Bode plot under Section 9. Added schematics under Section 10.

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Edition 2023-11-21

Published by

Infineon Technologies AG

81726 Munich, Germany

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Document reference

002-37759 Rev. *A

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