User guide for IR38164 evaluation board

for Intel VCCIO rail

About this document

Scope and purpose

The IR38164 is an easy-to-use, fully integrated and highly efficient DC-DC regulator with Intel SVID and I^2C/SMBus interface. The on-board PWM controller and low duty-cycle optimized MOSFETs make IR38164 a space-efficient solution, providing accurate power delivery for low output voltage and high current applications such as VCCIO.

IR38164 is a versatile regulator which offers programmability of switching frequency, output voltage, and fault/warning thresholds and fault responses while operating over a wide input and output voltage range. Thus, it offers flexibility as well as system-level security in the event of fault conditions.

The switching frequency is programmable from 500 kHz to 1.5 MHz for an optimum solution. The on-chip sensors and ADC along with the SVID and PMBus™ interfaces make it easy to monitor and report input voltage, output voltage, output current and temperature.

This user guide contains the schematic and Bill of Materials (BOM) for the IR38164 evaluation board, designed for the Intel VCCIO rail. The guide describes the use of the evaluation board itself. Detailed application information for IR38164 is available in the IR38164 datasheet.

Intended audience

This user guide is intended as a reference for designers evaluating the IR38164 board, Intel VCCIO Rail.

Table of contents

1 Board features

- V_{in} = +12 V
- V_{cc} = 5 V (optional)
- V_{out} = +1.0 V
- I_{DC} = 14 A, I_{pk} = 21 A
- F_s = 978 kHz
- L = 100 nH (12.4 mm × 8.3 mm × 8.0 mm, DCR = 0.15 mΩ)
- C_{in} = 4 × 22 µF (16 V, ceramic 0805) + 1 × 270 µF (16 V, electrolytic, see Note 1)
- C_{out} = 1 × 470 µF (SP-cap/2.5 V/3 mΩ) + 3 × 47 µF (X5R/6.3 V/0805)
  + 4 × 22 µF (X6S/6.3 V/0805) + 15 × 10 µF (X6S/6.3 V/0603)

Note 1: The electrolytic input capacitor is used to damp the parasitic inductance of input supply cables. It can be eliminated if the input is from nearby power planes.

2 Connections and operating instructions

The IR38164 VCCIO demo board requires a single +12 V supply for the input power. It has an internal LDO that can use the +12 V input supply to generate 5 V that is used for the V_{CC} bias voltage. This LDO can be disabled via R17 (see Figure 2) and when this is done, an external +5 V for the V_{CC} is required. The IR38164 can deliver up to 19 A load current. Table 1 lists the connectors, jumpers and test points on the board.

Table 1 Connections

Label		Descriptions
Power connectors	12V_Source	Connect input power (+12 V) to this connector
	GND	Return of input power
Power connectors	V_{out}	V_{out} (+1.0 V), connect a load (19 A max.) to this connector
	GND	Return of V_{out}
V_{CC} inputs	V_{CC}, GND	Apply an external 5 V supply for the bias voltage
SW1	1, 2	Enabled: 1 = on, Disabled: 1 = off
P1	SVID_CLK	SVID bus: SVID_CLK: SVID clock line SVID_DIO: SVID data line SVID_ALERT: SVID alert line
P2	SVID_DIO	
P3	SVID_ALERT	
J1	Mini slammer	An Intel mini slammer could be connected to this connector
J2	ALERT	SMBus line
	GND	
	DATA	
	CLK	
J3	VCCIO_SKT	Test points to sense VCCIO output
J4	SVID_CLK	Test points to sense SVID clock line
J5	SVID_DIO	Test points to sense SVID data line
J6	SVID_ALERT	Test points to sense SVID alert line
Test points	1.8 V, GND	Test points for the internal 1.8 V supply for the digital circuitry
	Pgood	Test point for power good
	VSENSE	Test point for V_{sns} pin
	ADDR	Test point for Address pin
	Enable	Test point for Enable pin
Jumpers	SV_CLK	Not used, should be left open
	SV_DIO	
	SV_ALERT	
SW4	1, 2	Not used, keep 1 = off, 2 = off
Test points	VPVID, GND	Not used

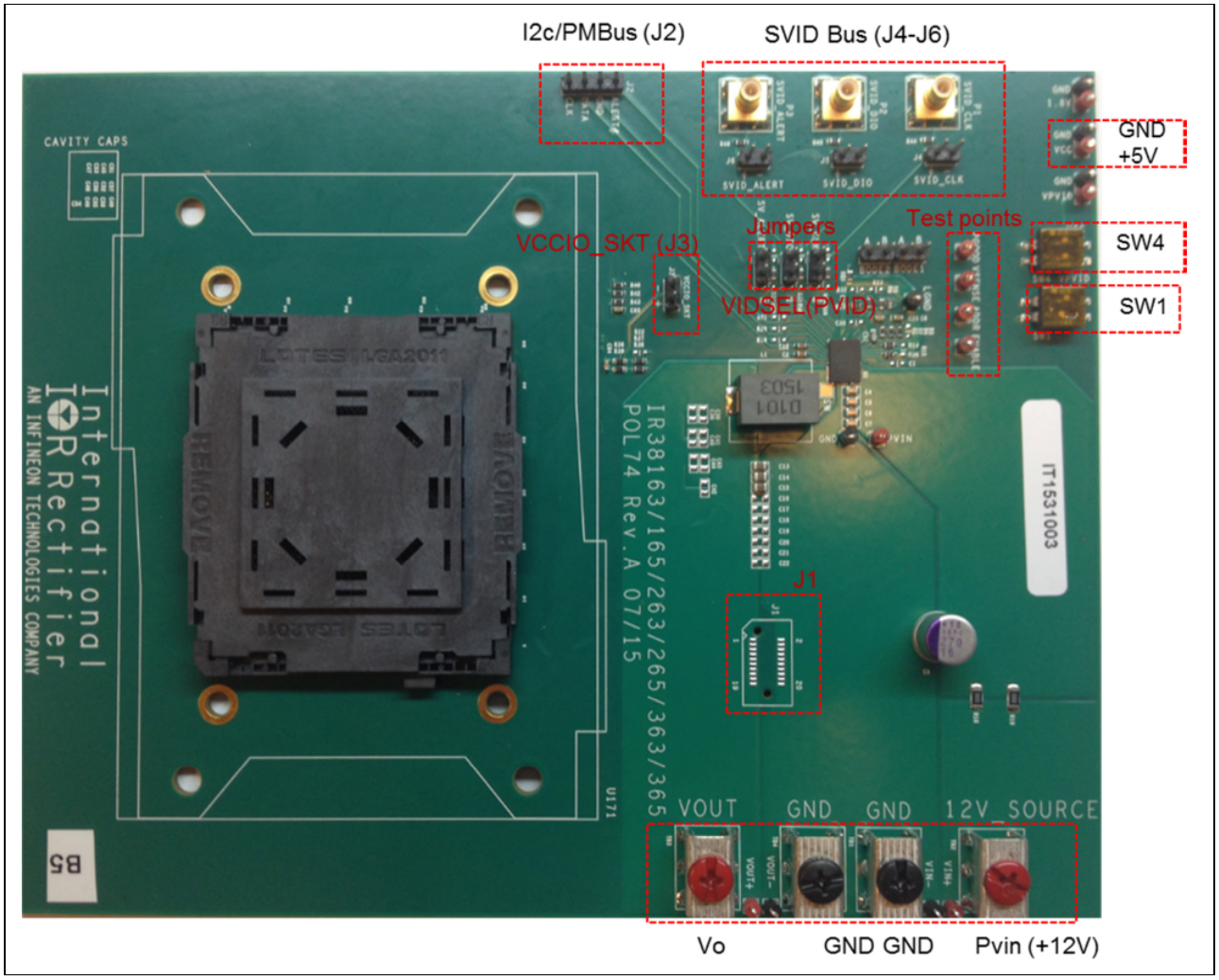

Figure 1 Top view of IR38164 VCCIO evaluation board with R socket

The PCB of the IR38164 demo board is a 5.5" × 7" 10-layer board using FR4 material. All layers use 2 oz. copper. The PCB thickness is 0.072".

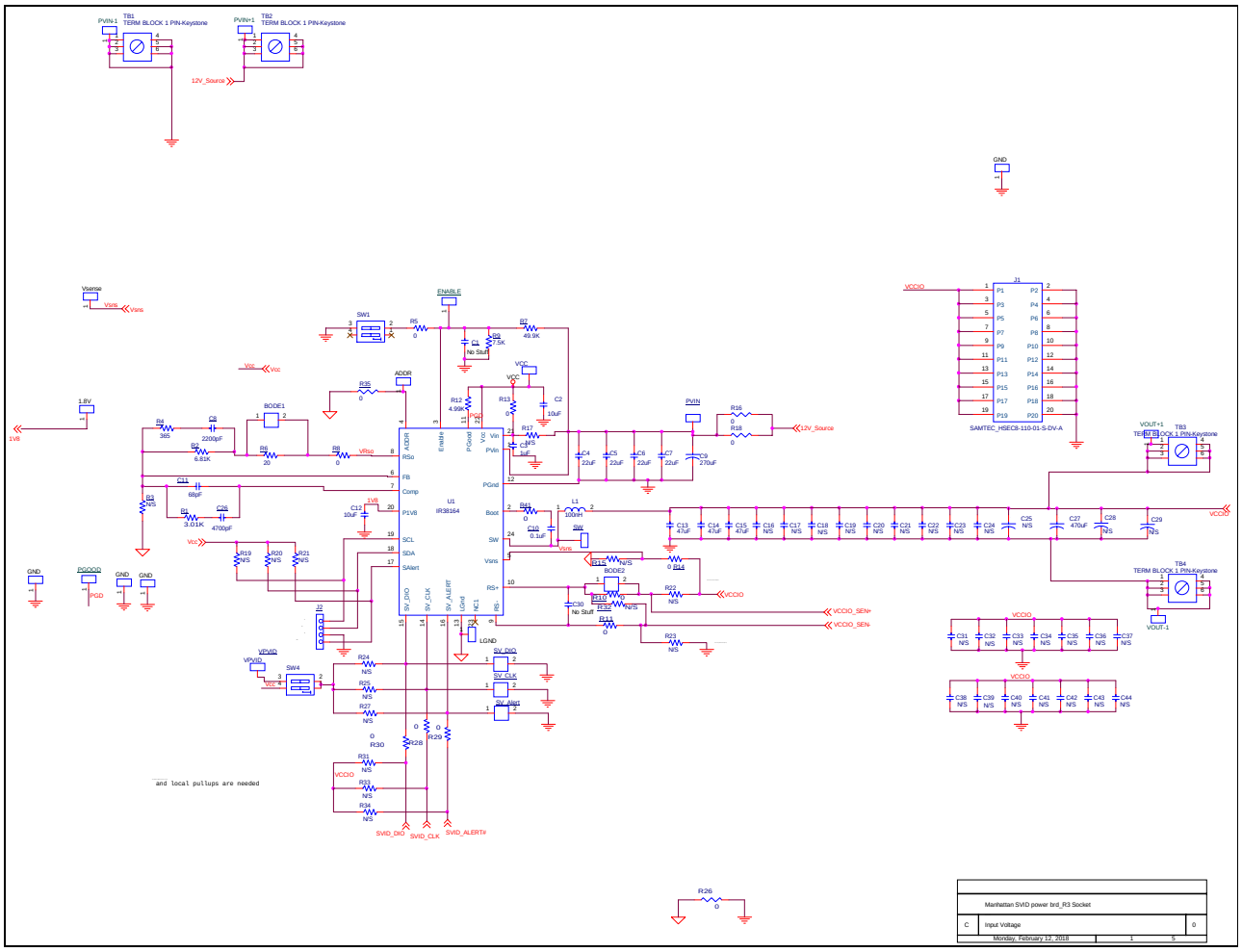

Figure 2 Schematic of the IR38164 VCCIO evaluation board

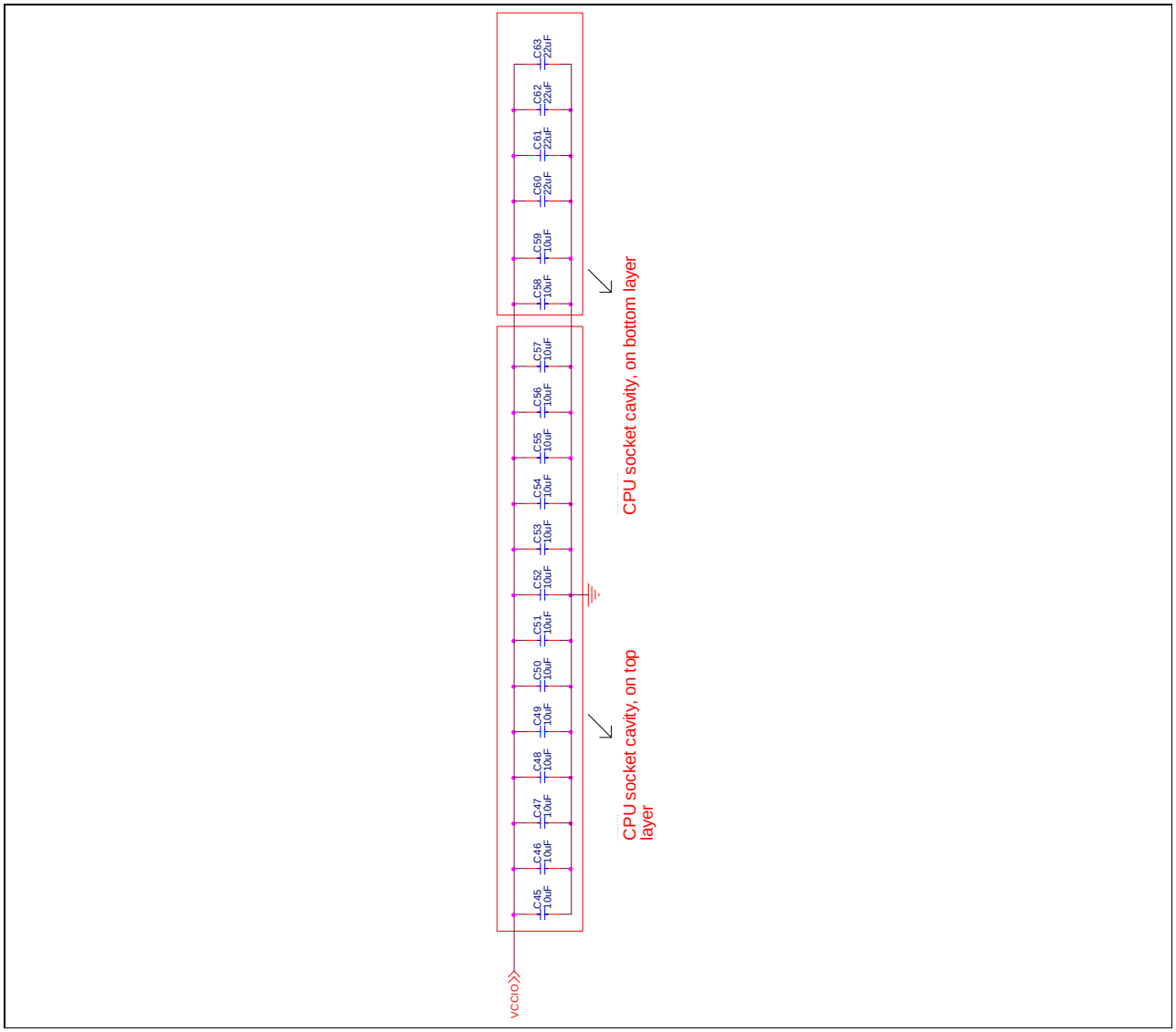

Figure 3 Schematic of the IR38164 VCCIO evaluation board

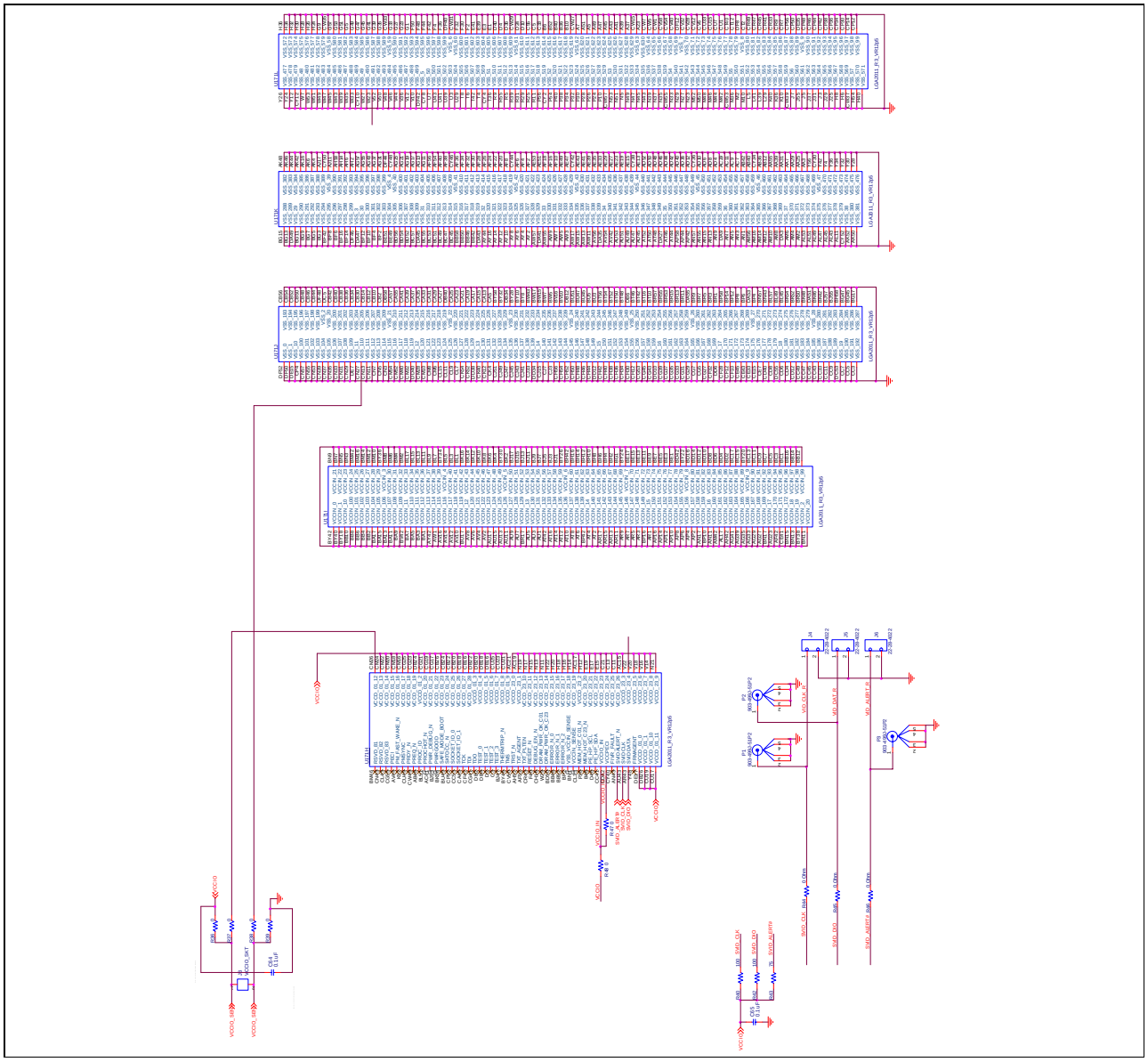

Figure 4 Schematic of the IR38164 VCCIO evaluation board

3 Bill of Materials

Table 2 BOM

Item number	Quantity	Part reference	Value	Description	Manufacturer	Part number
1	10	1.8 ADDR ENABLE PGOOD PVIN+1 PVIN VOUT+1 VSENSE VPVID VCC	0.075" SQ_SMT_TestPoint (red)		Keystone Electronics	5000
2	7	GND1 GND2 GND3 GND4 LGND VOUT -1 PVIN-1	0.075" SQ_SMT_TestPoint (black)		Keystone Electronics	5006
3	8	BODE1 BODE2 SV_ALERT SV_CLK SV_DIO J4 J5 J6	Two-pin header			M20-9990246
4	3	C10 C64 C65	0.1 µF	CAP CER 0.1 µF 25 V 10 percent X7R 0603	Murata	GRM188R71E104KA01D
5	17	C2 C12 C45 C46 C47 C48 C49 C50 C51 C52 C53 C54 C55 C56 C57 C58 C59	10 µF	CAP CER 10 µF 6.3 V 20 percent X6S 0603	TDK	C1608X6S0J106M080AC
6	1	C3	1 µF	0603, X5R, 25 V, 20 percent	TDK	C1608X5R1E105M
7	4	C4 C5 C6 C7	22 µF	0805, X5R, 16 V, 20 percent	TDK	C2012X5R1C226M085AC
8	4	C60 C61 C62 C63	22 µF	0805, X6S, 4 V, 20 percent	Murata	GRM21BC80G226ME39L
9	1	C8	2200 pF	2200 pF, 0603, 50 V, NPO	TDK	C1608C0G1H222J
10	1	C9	270 µF	Electrolytic 16 V	Panasonic	16SEPC270M
11	1	C11	68 pF	0603, NP0, 50 V, 5 percent	Murata	GRM1885C1H680JA01D
12	3	C13 C14 C15	47 µF	0805, X5R, 6.3 V, 20 percent	TDK	C2012X5R0J476M
13	1	C27	470 µF	SP-cap, SMD, 2.5 V, 3 mΩ	Panasonic	EEFGX0E471R
14	1	C26	4700 pF	4700 pF, 0603, 50 V, NPO	TDK	C1608C0G1H472J
15	1	J1	SAMTEC_HSEC8-110-01-S-DV-A		SAMTEC	HSEC8-110-01-S-DV-A
16	1	J2	Header	4 × 1 header	Sullins Connector Solutions	PEC36SAAN
17	1	J3	VCCIO_SKT			M20-9990246
18	1	L1	100 nH	DCR = 0.15 mΩ	Delta	HCB138380D-101
19	3	P1 P2 P3	903-499J-51P2	CONN SMB JACK STR 50 Ω PCB	Amphenol-RF Division	903-499J-51P2
20	1	R1	3.01 K	RES SMD 3.01 kΩ 1 percent 1/10 W 0603	Rohm	MCR03EZPFX3011
21	1	R2	6.81 K	RES SMD 6.81 kΩ 1 percent 1/10 W 0603	Rohm	MCR03EZPFX6801
22	1	R4	365	0603,1/10 W,1 percent	Rohm	MCR03EZPFX3650
23	21	R5 R8 R10 R11 R14 R13 R26 R35 R37 R38 R41 R44 R45 R46 R28 R29 R30 R47 R48 R36 R39	0	RES SMD 0.0 Ω jumper 1/10 W	Panasonic	ERJ-3GEY0R00V
24	2	R16 R18	0	RES SMD 0.0 Ω jumper ¼ W 1206	Panasonic	ERJ-8GEY0R00V
25	1	R6	20	0603, 1/10 W, 1 percent	Vishay	CRCW060320R0FKEA
26	1	R7	49.9 K	0603, 1/10 W, 1 percent	Rohm	MCR03EZPFX4992
27	1	R9	7.5 K	0603, 1/10 W, 1 percent	Rohm	MCR03EZPFX7501
28	1	R12	4.99 K	0603, 1/10 W, 1 percent	Rohm	MCR03EZPFX4991
29	2	R40 R42	100	0603, 1/10 W, 1 percent	Rohm	MCR03EZPFX1000
30	1	R43	75	0603, 1/10 W, 1 percent	Vishay	CRCW060375R0FKEA
31	2	SW1 SW4	SW_DIP_2POS			
32	4	TB1 TB2 TB3 TB4	TERM BLOCK 1 PIN-Keystone			8199
33	1	U1	IR38164	30 A integrated buck regulator with PMBus™ and SVID	Infineon	IR38164MTRBPF
34	1	U171	Intel Socket-R 3 _LGA2011-R3		Intel	Intel

4 Typical operating waveforms

Typical operating waveforms: P_{Vin} = 12.0 V, V_{out} = 1.0 V, I_{out} = 0 A to 19 A, Fs = 978 kHz, room temperature, no airflow

4.1 Waveforms

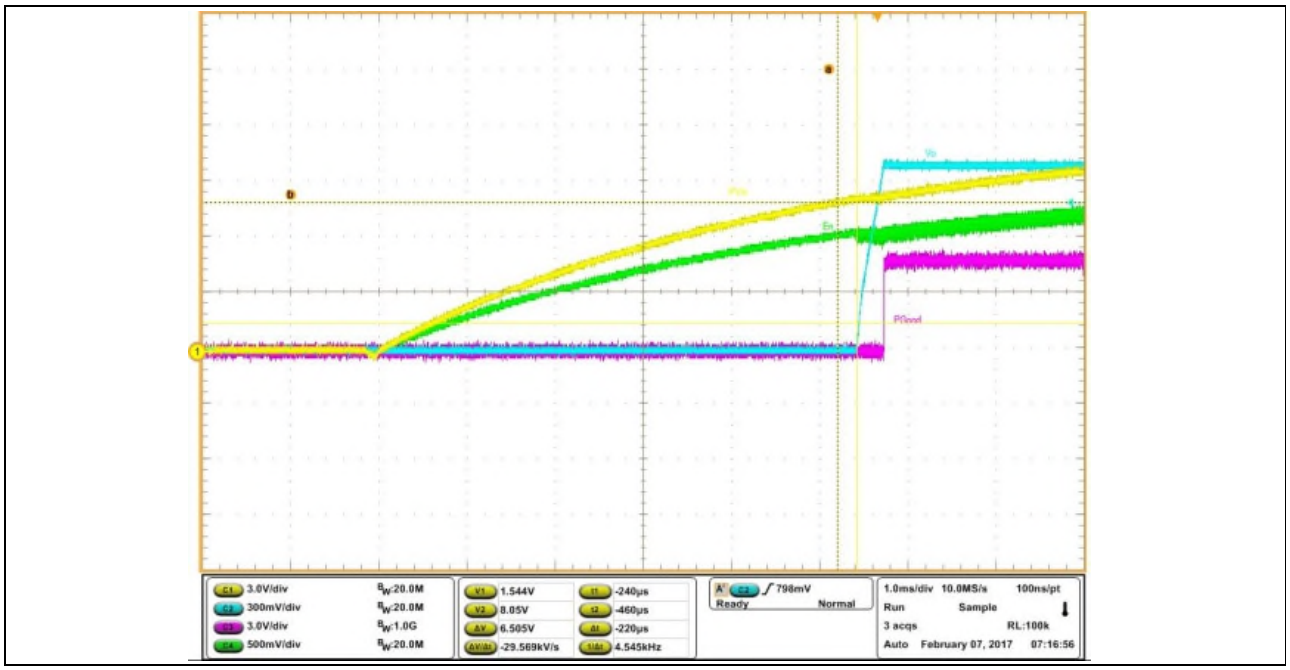

Figure 5 P_{Vin} start-up at 19 A load, Ch_1:P_{Vin}, Ch_2:V_{out}, Ch_3:P_{Good}, Ch_4:Enable

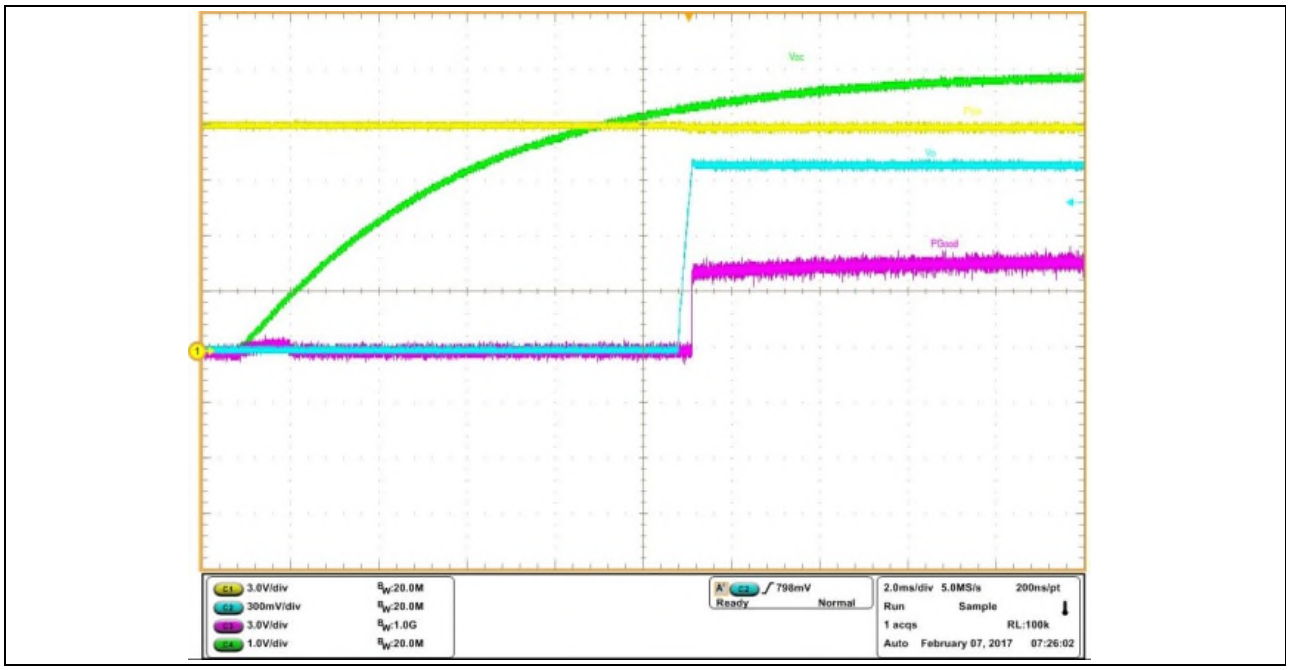

Figure 6 V_{cc} start-up at 19 A load, Ch_1:P_{Vin}, Ch_2:V_{out}, Ch_3:P_{Good}, Ch_4:V_{cc}

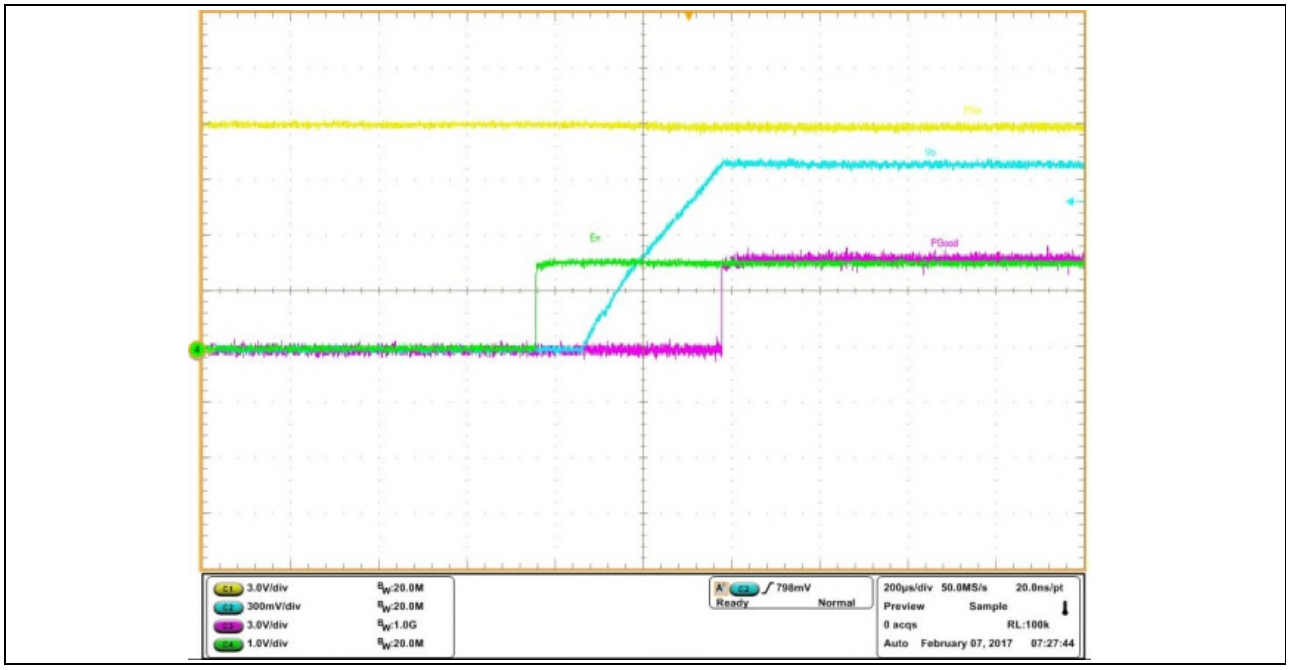

Figure 7 En start-up at 19 A load, Ch_1:P_{Vin}, Ch_2:V_{out}, Ch_3:P_{Good}, Ch_4:Enable

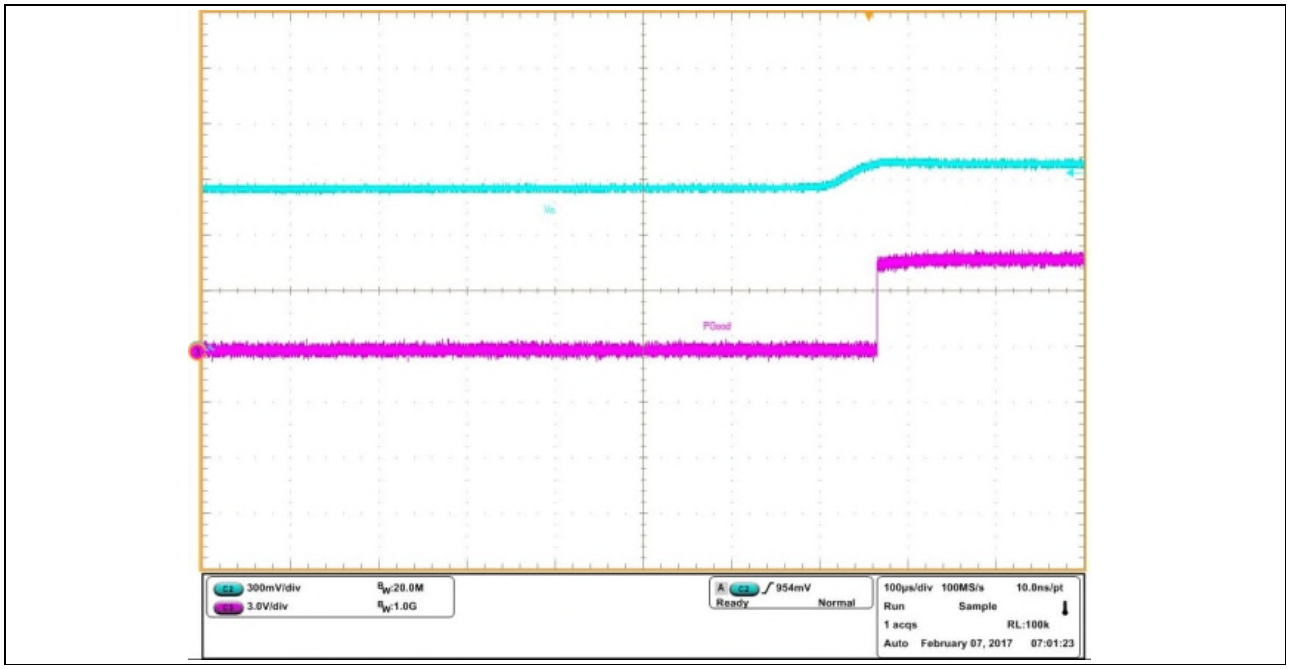

Figure 8 Prebias start-up at 0.9 V, Ch_2:V_{out}, Ch_3:P_{Good}

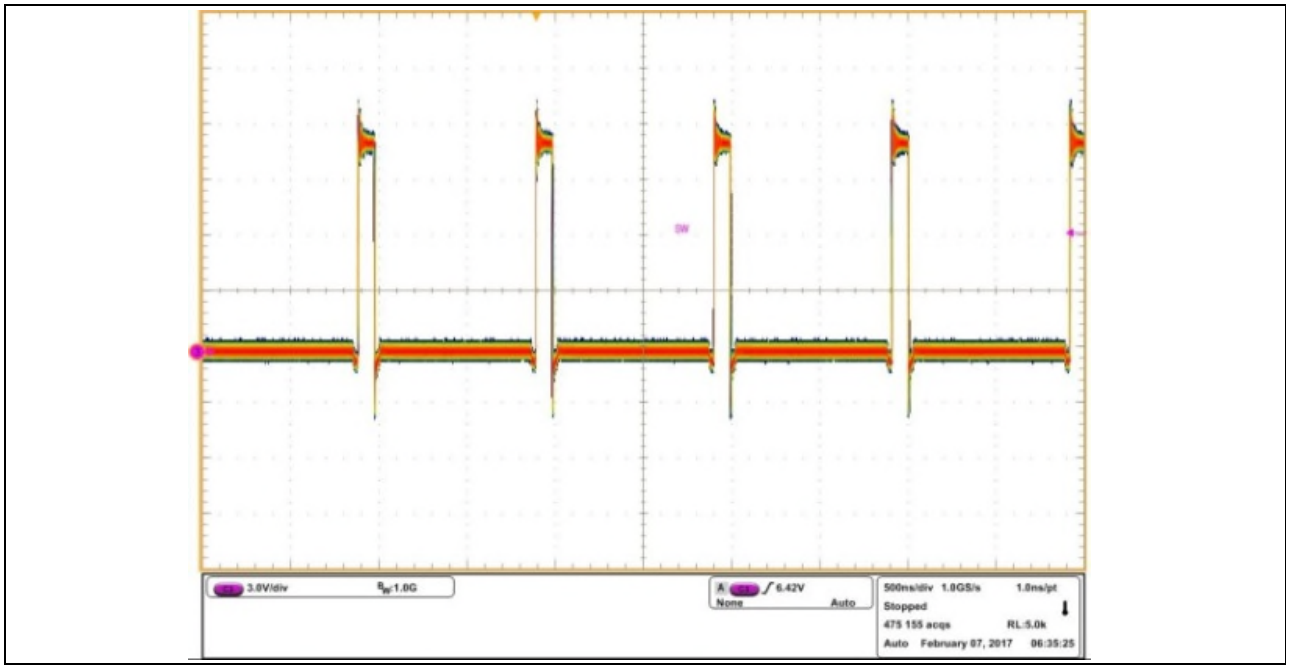

Figure 9 Inductor node at 19 A load, Ch_3:SW node

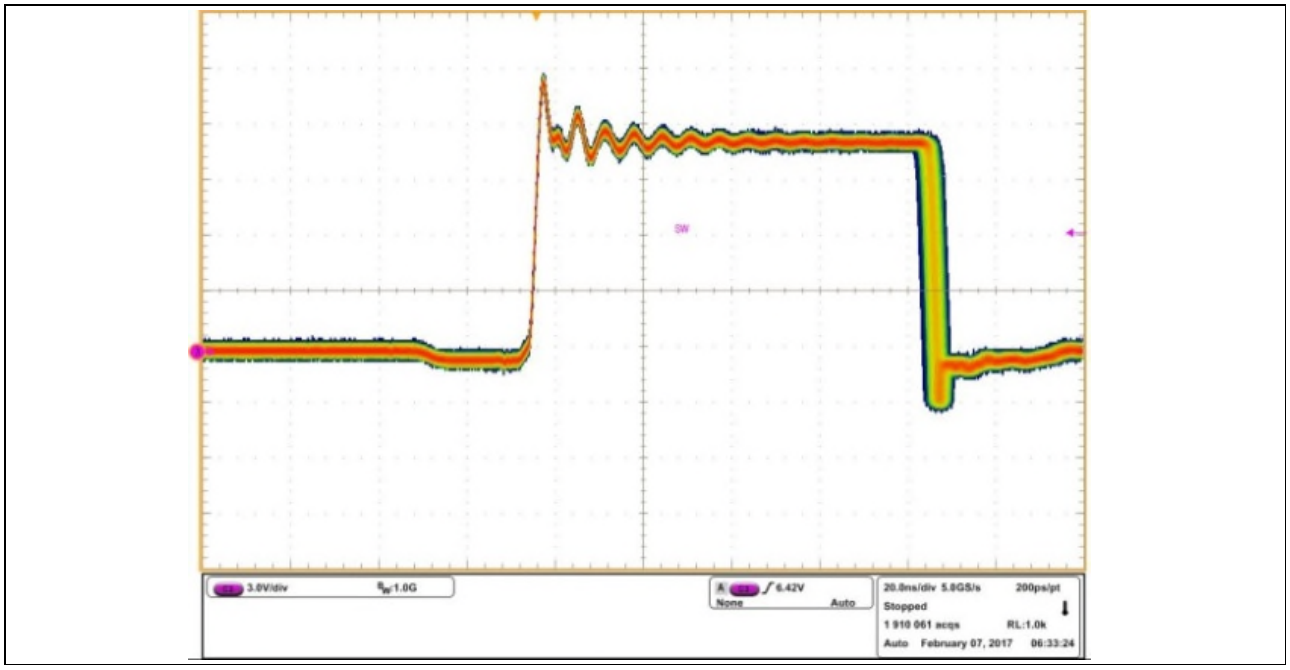

Figure 10 Sw node jitter at 19 A load, Ch_2:V_{out}

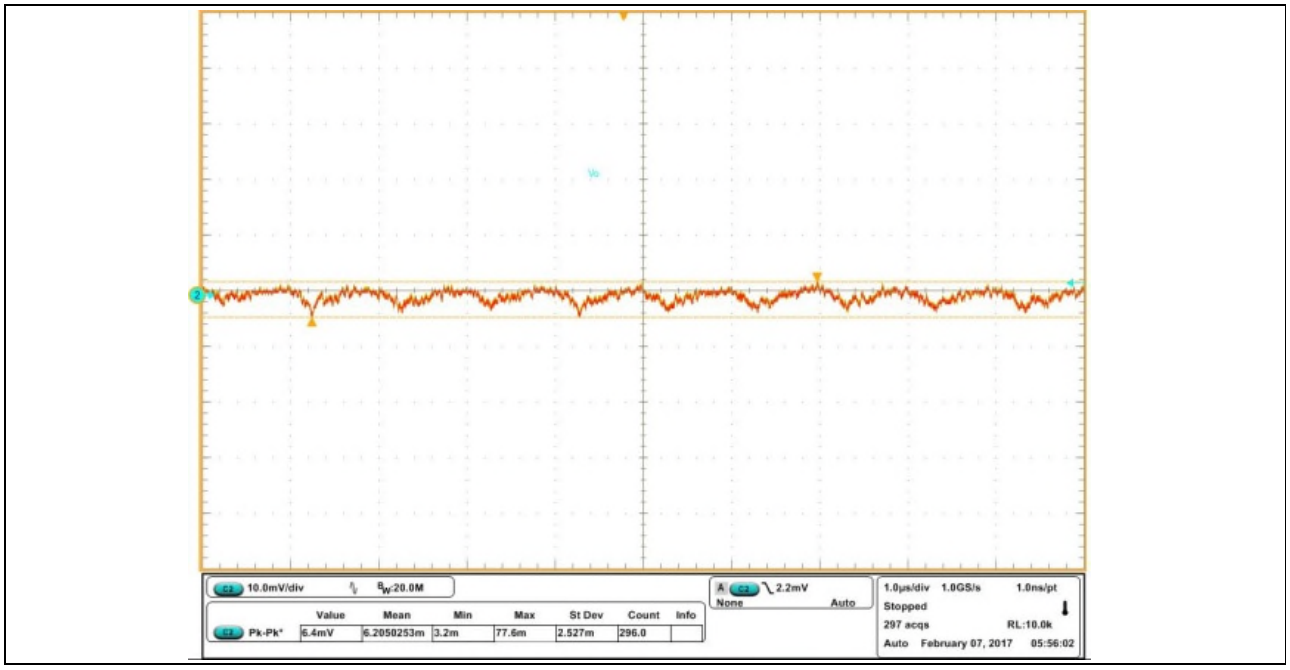

Figure 11 V_{out} ripple at 19 A load, Ch_2:V_{out}

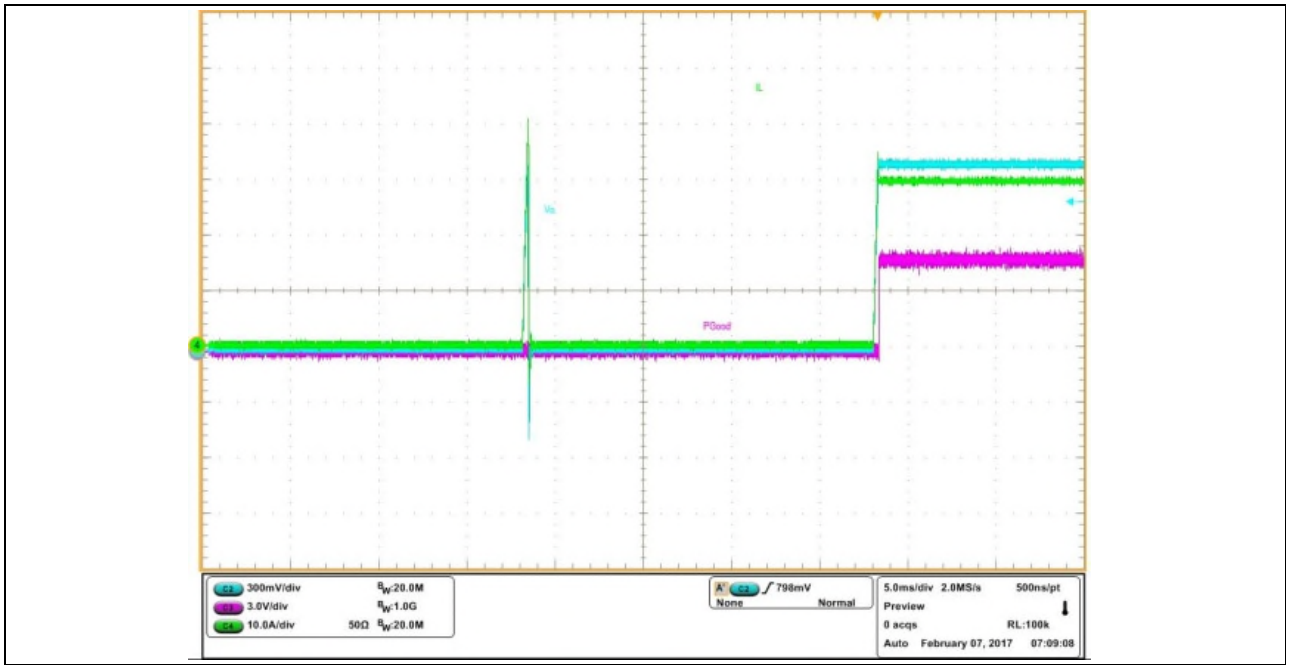

Figure 12 **Hiccup recovery at 19 A load, Ch_2:V_{out}, Ch_3:P_{Good}, Ch_4:I_{out}**

4.2 Bode plots

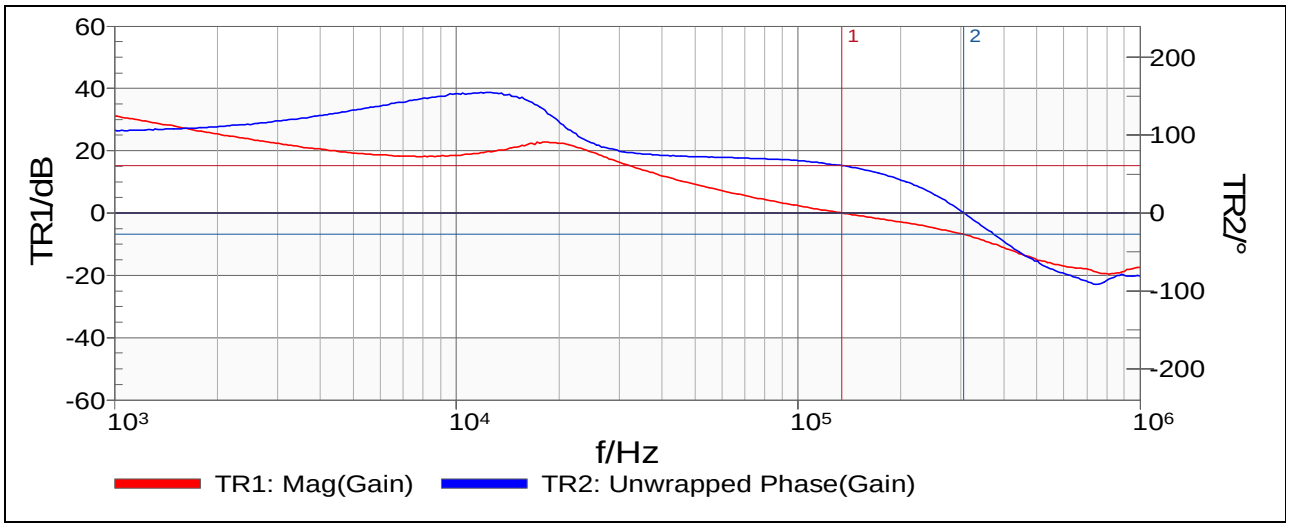

Figure 13 Bode plot at 19 A load, BW = 134 kHz, phase margin = 61 degrees, gain margin = 7 dB

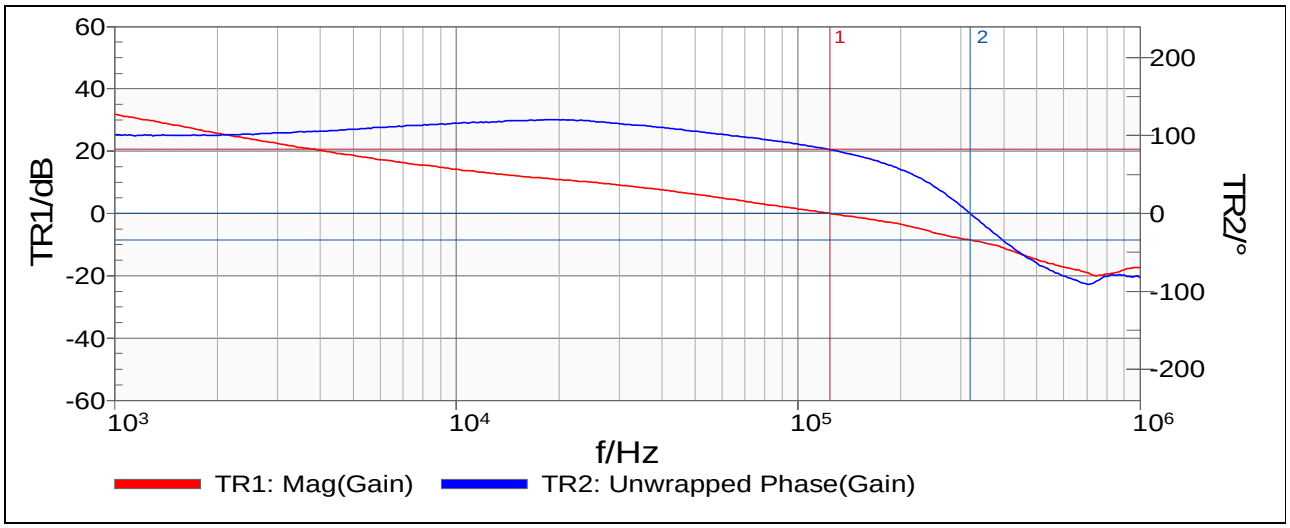

Figure 14 Bode plot at 0 A load, BW = 134 kHz, phase margin = 81 degrees, gain margin = 8.2 dB

4.3 Thermal image

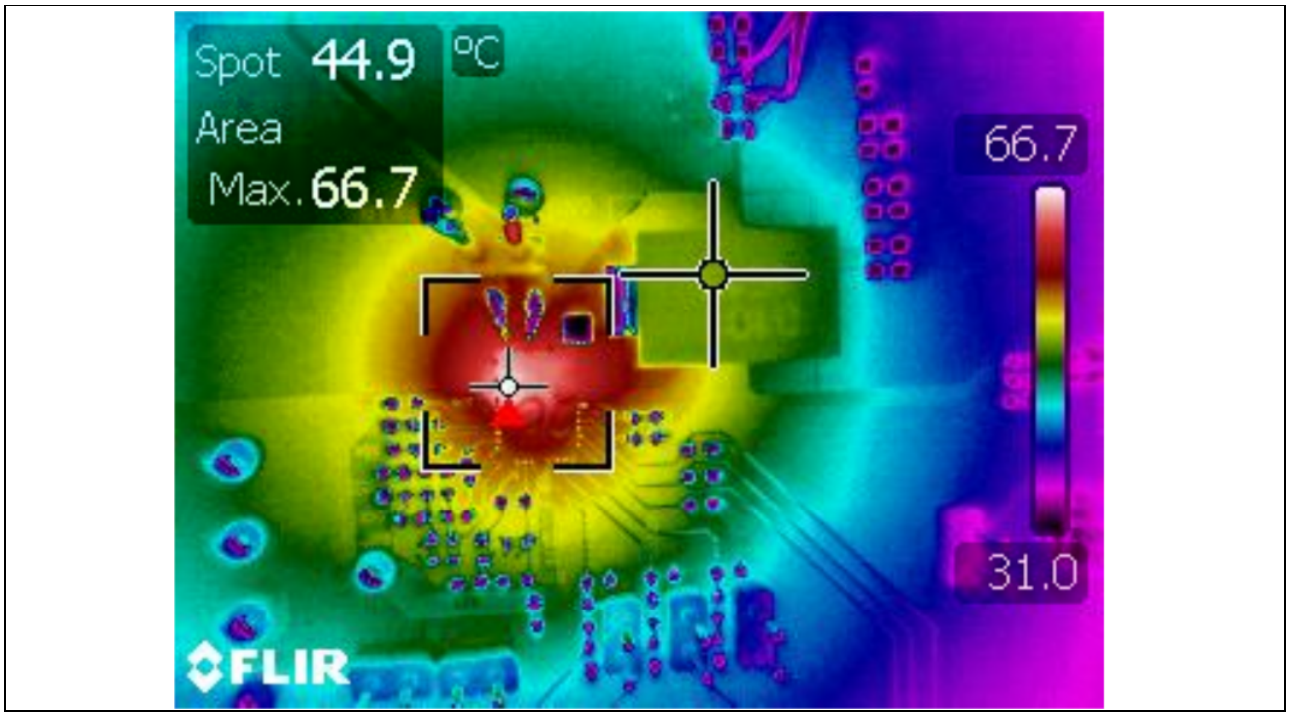

Figure 15 Thermal image of the board at 30 A load, IR38164: 66.7°C, inductor: 44.9°C

4.4 Efficiency and power loss

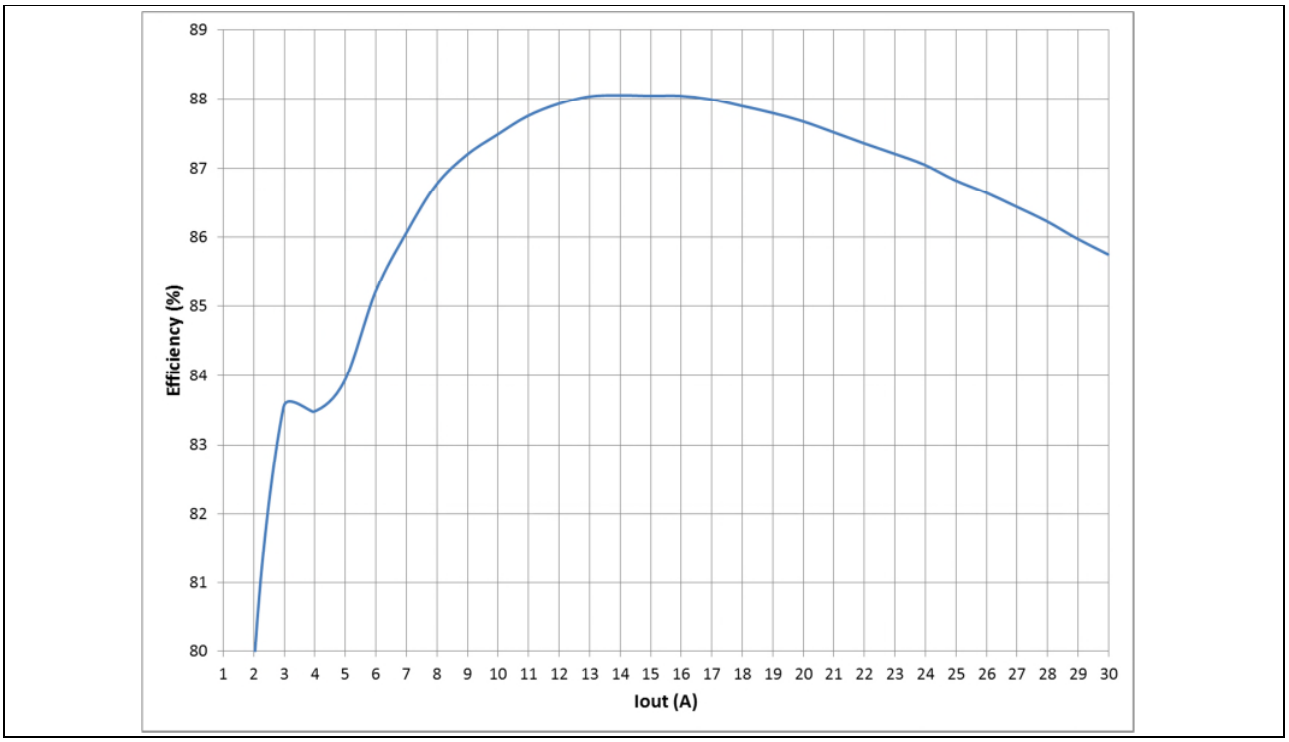

Figure 16 Efficiency vs load current

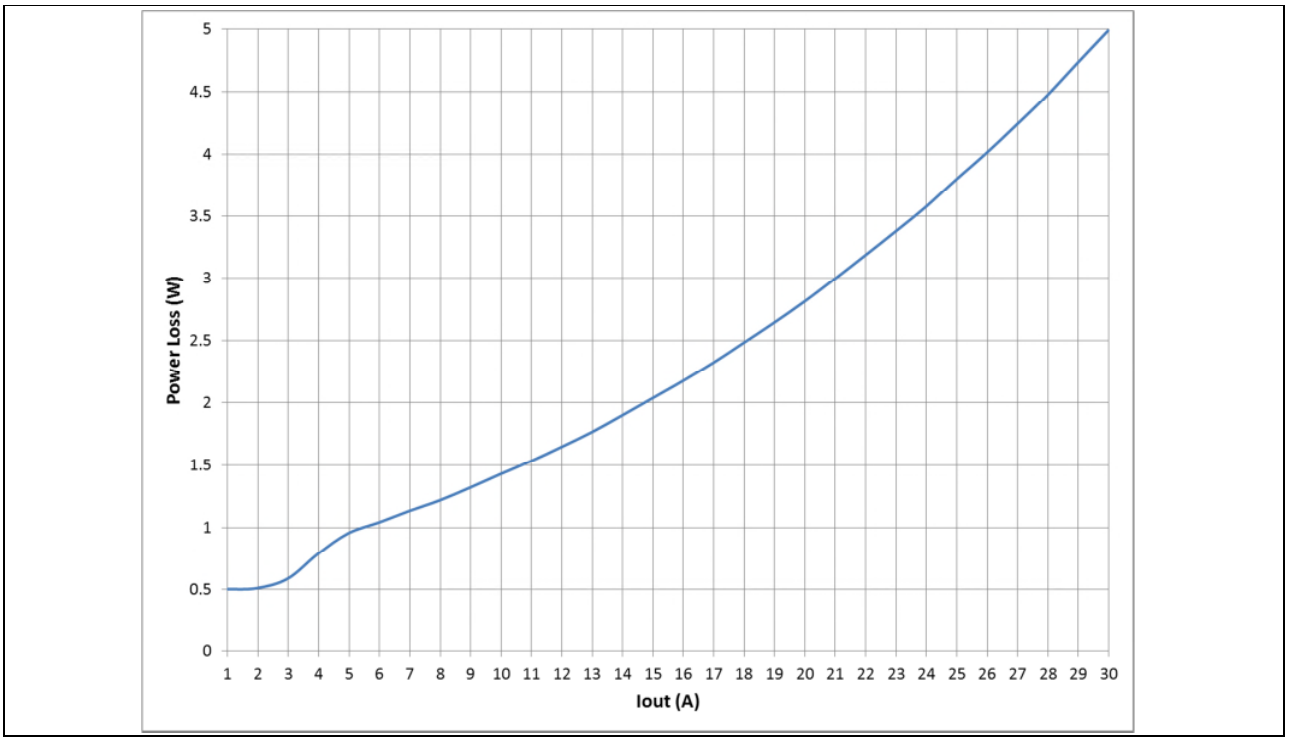

Figure 17 Power loss vs load current

Revision history

Major changes since the last revision

Page or reference	Description of change

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Edition <2018-03-12>
Published by
Infineon Technologies AG
81726 Munich, Germany

Do you have a question about this document?
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Document reference
UG_1803_PL12_1803_002658

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