Half-bridge evaluation board designed with CoolGaN™ GIT HEMTs and EiceDRIVER™ 2EDB8259Y

Ordering code: EVAL_2EDB_HB_GaN

About this document

Scope and purpose

This application note explains how to set up and use the CoolGaN™ gate injection transistor (GIT) HEMTs half-bridge evaluation board with EiceDRIVER™ 2EDB8259Y. The board allows testing of both Schottky and GIT HEMT GaN power switches in a DFN 8x8 package. The board includes a bias supply circuit for the gate driver that can be configured for unipolar and bipolar supply (with regulation on positive or negative rail) or non-isolated for operation in bootstrap. Using an external inductor, the board can be configured for buck- or boost-mode, double pulse testing or continuous PWM operation, hard- or soft-switching at power levels up to several kW and frequencies up to MHz range.

Intended audience

This document is intended for power electronic engineers who are interested in:

- comparing the performance of Schottky vs. GIT HEMT GaN power switches.
- looking at the performance of GaN when driven with a standard gate driver IC.
- comparing performance of GaN when using different gate driver supply approaches.

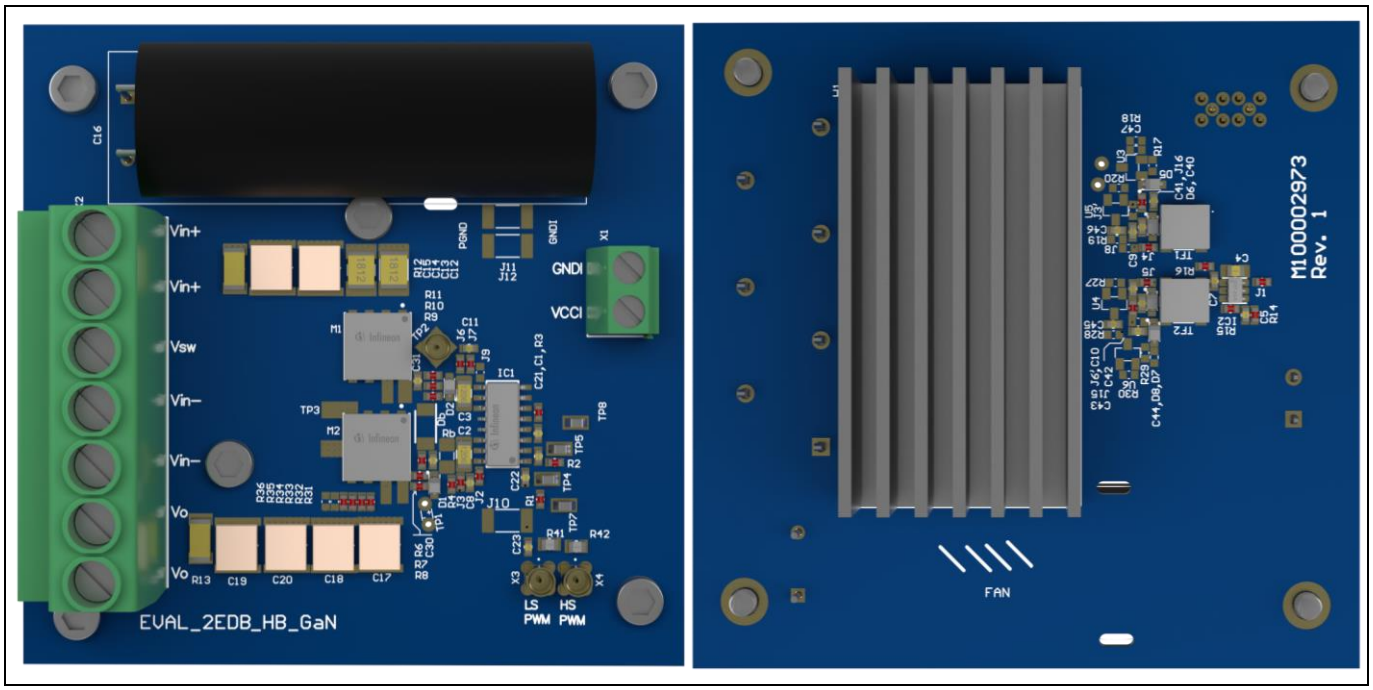

Figure 1 Front and back view of EVAL_2EDB_HB_GaN

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1 Introduction

This board enables testing of Infineon's CoolGaN™ GIT HEMTs (coming up, the testing of GaN power switches from other vendors will also be possible) along with the EiceDRIVER™ 2EDB8259Y isolated gate driver IC. The generic half-bridge topology is configurable for boost or buck operation, double pulse testing or continuous PWM operation at full power. Test points provide access to connect signals to an oscilloscope for measuring the switching performance of GaN power switches and gate driver IC.

PWM (see **section 2.3**): The half-bridge circuit board can be controlled by two PWM signals provided via a pulse generator. The half-bridge dead time is forced by the EiceDRIVER™ 2EDB8259Y only if the dead time between INA and INB is shorter than the minimum "safe dead time" configured on the gate driver via DTC pin.

Supply (see **section 2.2** and **2.2.1**): Gate-to-source voltages are generated if V_{CCI} supply is applied via DC power supply. V_{CCI} powers the gate driver primary side and eventually the on-board isolated bias supply. Several supply options (e.g., bipolar or unipolar, isolated or non-isolated) are possible for the driver secondary side without requiring an additional supply.

The output and bus voltage can range up to 450 V, limited by the capacitor rating. The half-bridge can switch currents of 12 A continuously, and peak currents of 35 A, in hard- or soft-switching. The operating frequency can be up to several MHz, depending on the thermal dissipation of the power switch.

1.1 Evaluation board specifications

Table 1 Evaluation board specifications

Parameter	Values			Unit	Note
	Min.	Typ.	Max		
V_{CCI} input voltage	9.5	12	15.8	V	conf. #A, B, C: supply via on-board bias circuit. Typical value depends on selected V_{pos}/V_{neg} (see **section 2.2**); by default, typical is 12 V.
	7.6	8	10.5	V	conf. # D: direct supply. Recommended 8-10 V
V_{CCI} input current	-	-	0.3	A	Max. considers potential operation at 2 MHz
INA, INB logic input levels	0	3.3	17	V	Typ. standard 3.3 V TTL levels
Vin+ to Vin-	0	400	450	V	Limited by capacitor voltage ratings
Vo to Vin-	0	-	450	V	(There may be ±30 V spikes appearing on Vo)
Transistor current, DC	-	-	12	A	Keep case temperature below 125°C
Transistor current, pulse	-	-	35	A	Keep case temperature below 125°C
Operating frequency	(DC)	-	2	MHz	Within thermal dissipation and temperature limits
PWM pulse width	18	-	∞	ns	Min. value set by the gate driver
Switching node V_{SW} speed	-	87	-	V/ns	20-80% for 0 A hard-switching, default config.
Gate drive voltage levels	[1]	3.3	-	V	[1] Min. is adjustable via supply configuration and C_c value
Dead time adjustment range	10	100	1000	ns	Typical value set by driver DTC resistance (R3)

Note: The PCB dimensions are 7.5 cm x 7.5 cm.

2 Board description and setup

2.1 Board test setup

EVAL_2EDB_HB_GaN is equipped with a 6-port terminal block allowing several connection options and testing in different configurations. A typical block diagram for double pulse (direct and reverse), buck-circuit and boost-circuit is shown in **Figure 2**, **Figure 3**, **Figure 4** and **Figure 5**.

A standard low-voltage power supply and pulse generator is needed to generate the gate-to-source signals for the GaN. For the switching of the half-bridge at high voltage, a 0 to 400 V DC power supply is required; this provides the DC bus voltage to the board. Finally, for testing at high power (in case of buck and boost-mode) a programmable DC electronic load is needed. An oscilloscope and probes (see recommendation in **chapter 2.5**) allow for signals monitoring on the main test points provided on the board.

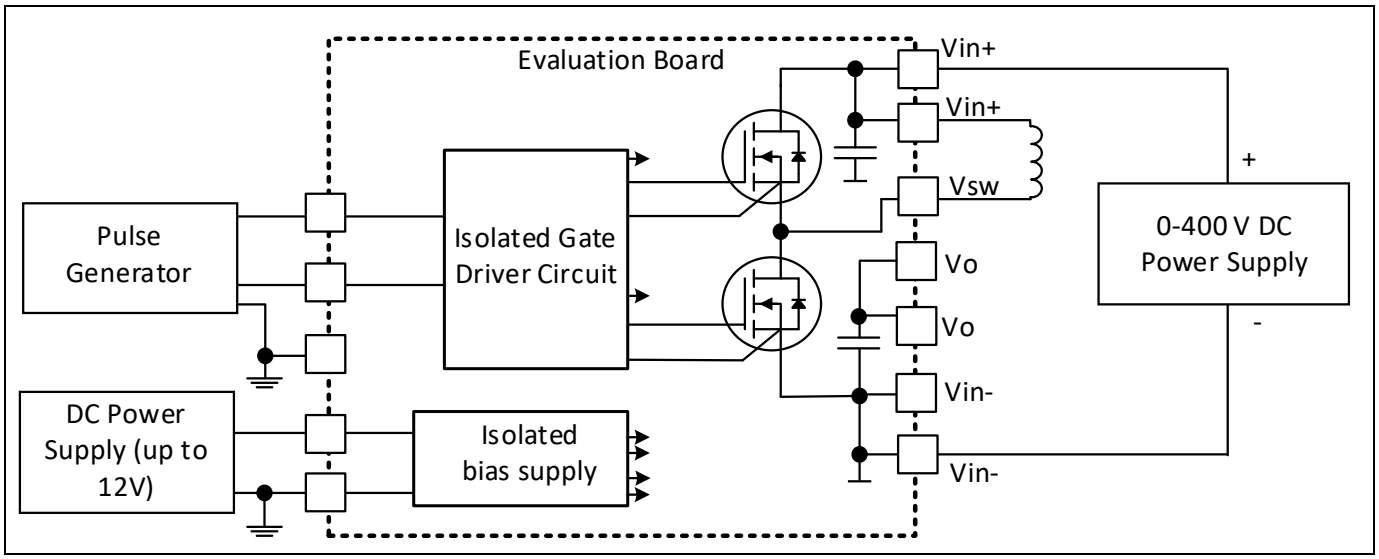

Figure 2 Evaluation board connected for direct double pulse test

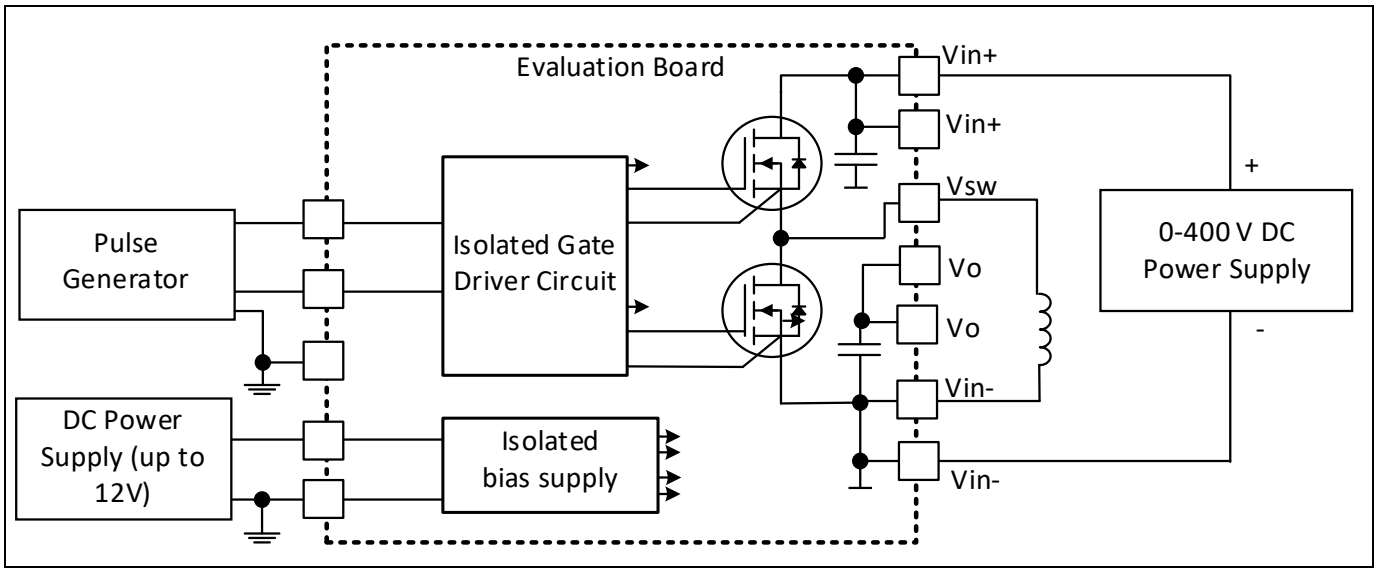

Figure 3 Evaluation board connected for reverse double pulse test

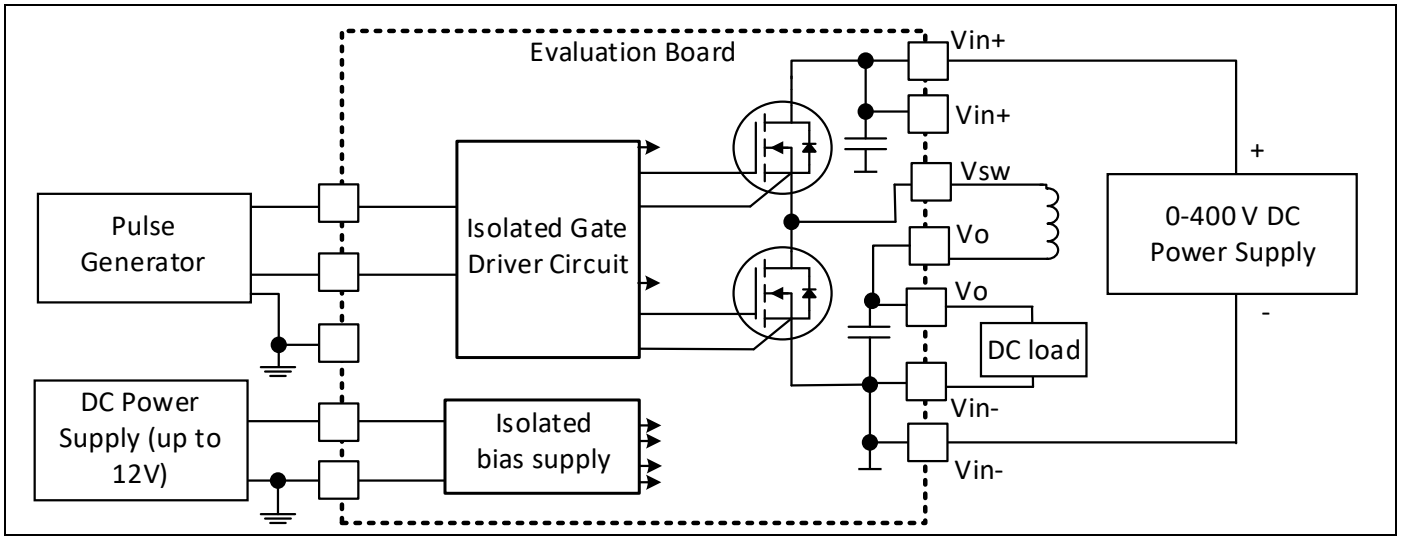

Figure 4 Evaluation board connected for buck-mode test

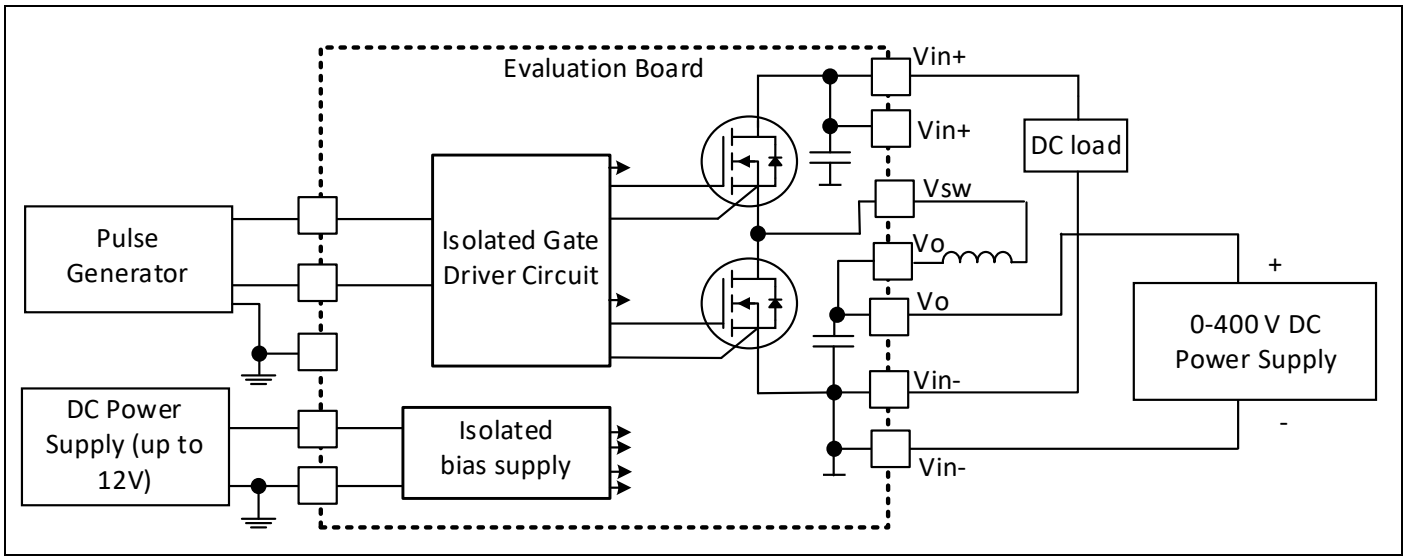

Figure 5 Evaluation board connected for boost-mode test

2.2 GaN driving setup

2.2.1 Selecting the driving setup: unipolar vs. bipolar, isolated vs. bootstrap

The board can be configured for GaN operation with unipolar or bipolar gate-to-source voltage, with isolated or non-isolated supply domains, with or without boostrap as shown in **Table 2**. The graphical explanation is shown in **Figure 6**.

Table 2 Bias supply configurations

Config. #	Unipolar vs. bipolar driving		Low-side supplied via		High-side supplied via		Pri-sec isolation
	Unipolar	Bipolar	V_{CCI}	Iso aux	bootstrap	Iso aux	
A (default)		x		x		x	x
B, B´	x			x		x	x
C, C´	x			x	x		x
D	x		x		x		

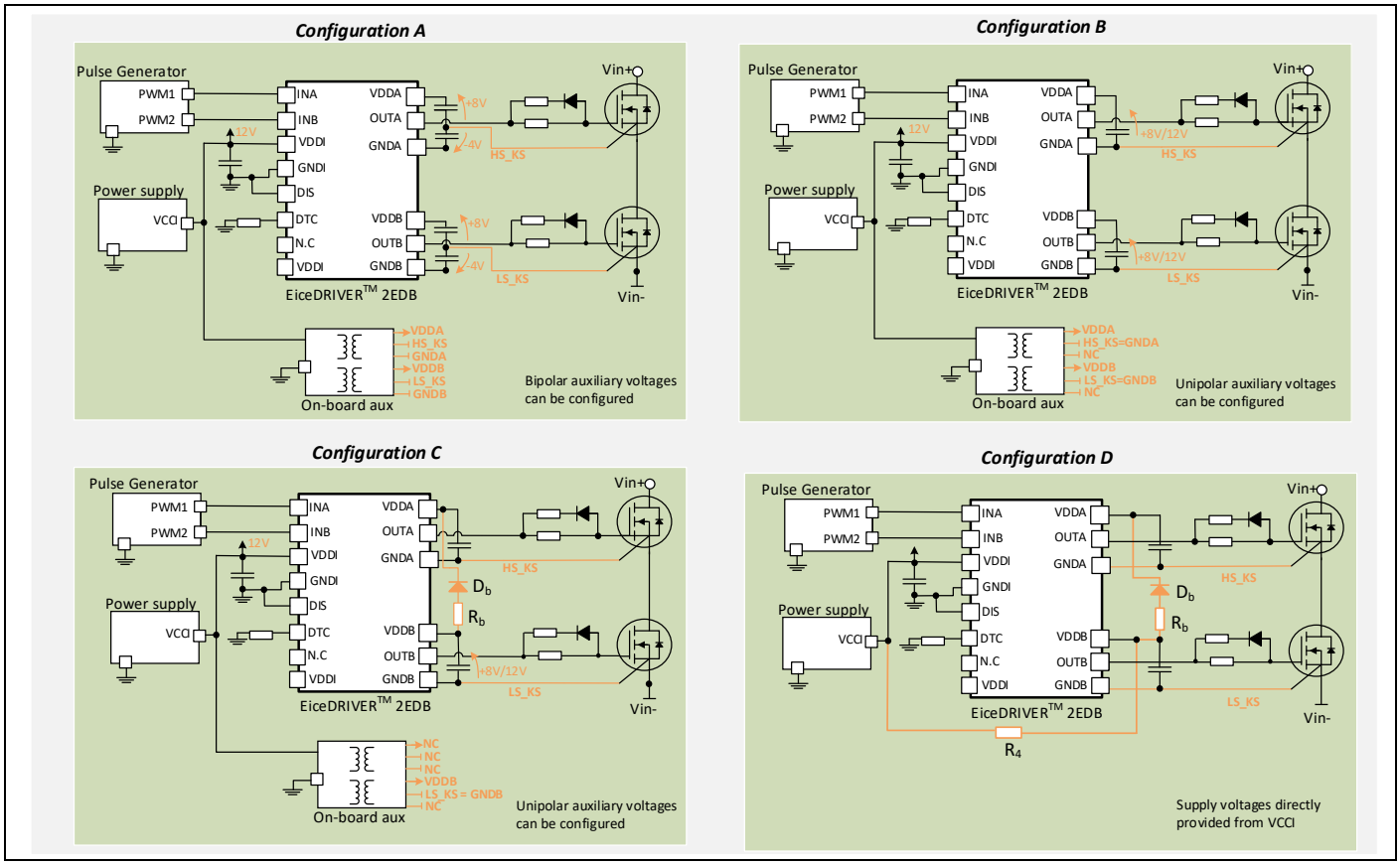

Figure 6 Bias supply configurations – graphical explanation

The desired bias supply configuration can be set by means of jumpers as shown in **Table 3**. The small footprint (0603) of the jumpers is intended for easy connection via solder dot and for low impedance, critical in particular for the jumpers sitting in the gate loop return paths (e.g., J3, J4, J6, J7,..).

Table 3 Jumper selection (“x” stands for 0 Ω resistor)

Configuration	J1	J2	J3, J3´	J4	J5	J6, J6´	J7	J8	J9	J10	J11	J12	Rb
A (default)	x	x	x	x	x	x	x						
B [1]	x	x	x		x	x		x	x				
B´ [1]	x	x		x	x		x	x	x				
C [1]	x	x	x					x	x				47Ω
C´ [1]	x	x		x				x	x				47Ω
D								x	x	x	x	x	47Ω

[1] In configuration B and C, the supply voltage ($V_{CCA/B}$ – $GND_{A/B}$) of the 2EDB driver is only the upper portion, also called “positive rail”, of the voltage generated by the bias supply (V_{C8}/ V_{C10}); in configuration B´, C´ instead it is the full voltage (V_{C8}+V_{C9}) as shown in **Figure 8**. For more flexibility, in the default configuration e.g., it allows to test the GaN either with a unipolar 8 V or 12 V.

Figure 7 helps to identify the jumpers on the board and enable a faster setup change. Please short the jumpers highlighted in blue and open the ones in red.

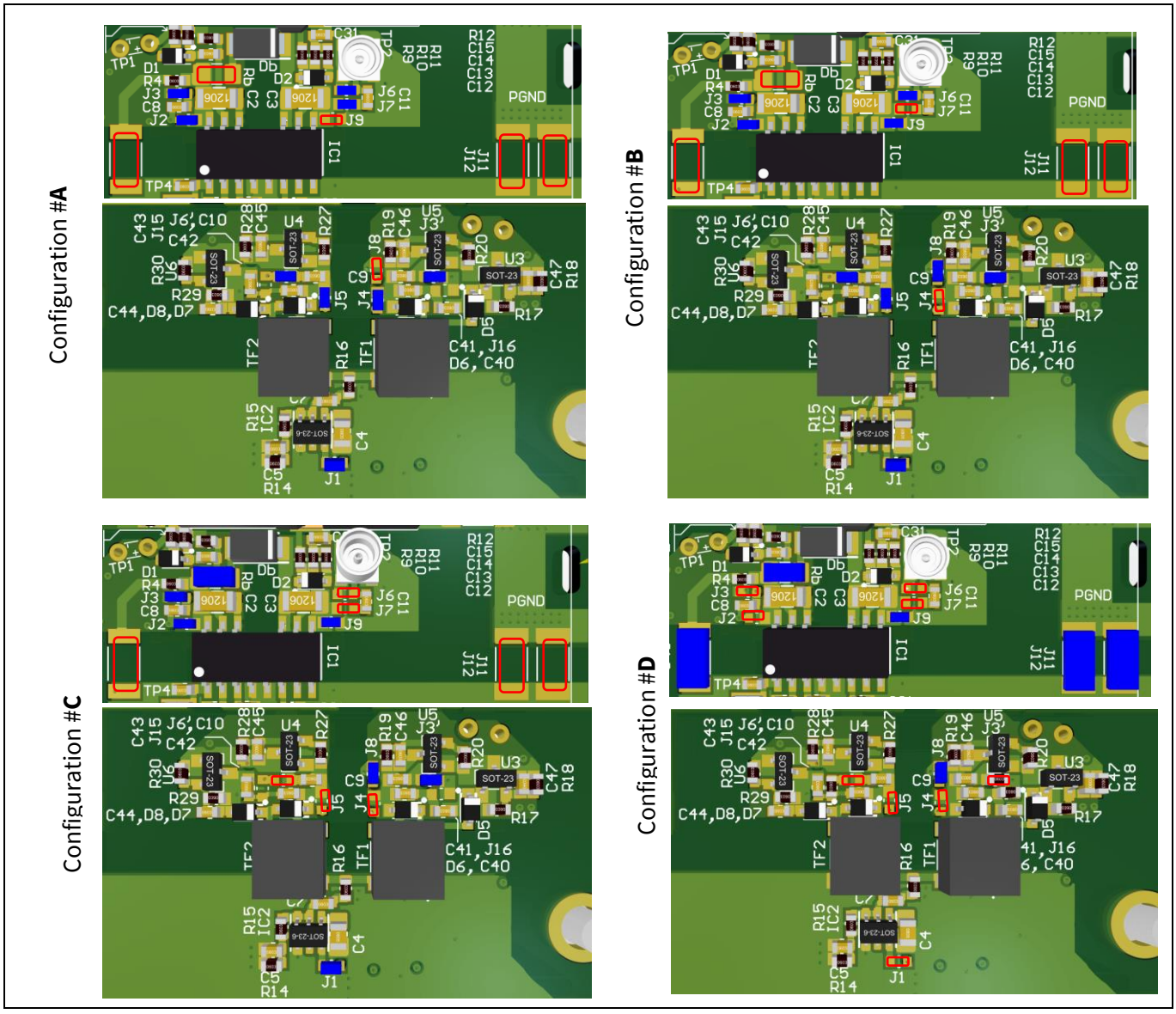

Figure 7 Jumpers position (short the jumpers highlighted in blue, open the ones in red)

2.2.2 Configure the bias supply voltage

This section describes how to tune the bias supply voltage split for the configurations A, B, C.

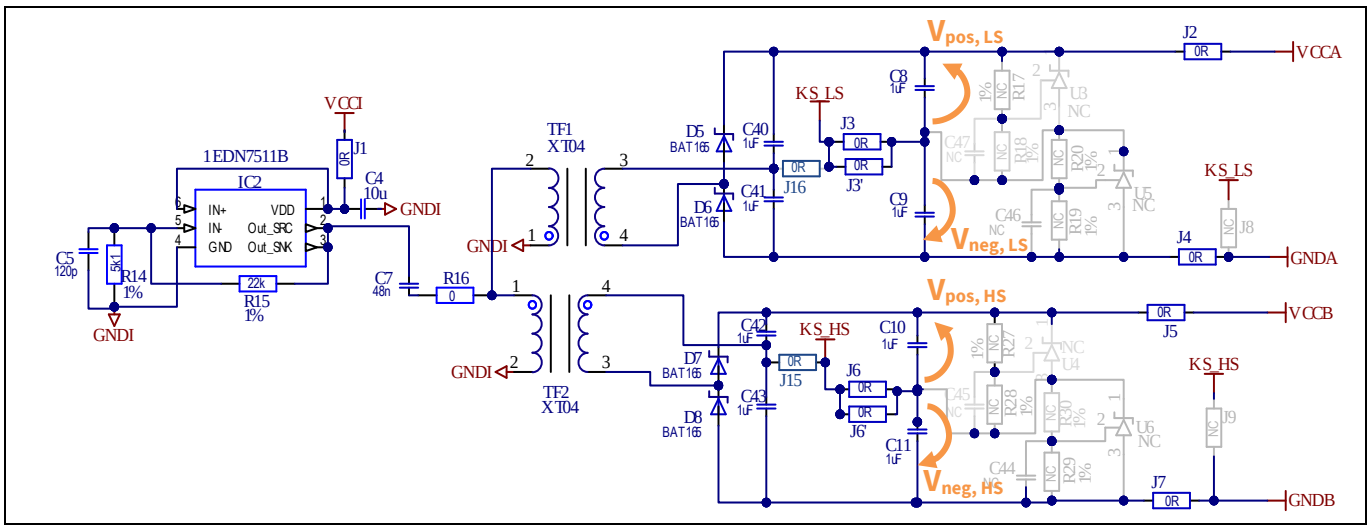

Figure 8 Bias supply dimensioned for V_{CCI} =12 V and for unregulated V_{pos}=8 V, V_{neg}= -4 V

The bias supply circuit realizes a simple and cost effective galvanic isolated DC-DC converter. A single-channel low-side gate driver (EiceDRIVER™ 1EDN7511B) is operated as an oscillator by connecting the output to its inverted input pin (IN-).

Isolation is achieved by the ICE XT04 transformer, which features an attractive small size and low input-to-output capacitance (< 4 pF) fundamental for driving of wide bandgap (WBG) power switches. Besides the reduced dimension, the device still guarantees 3 mm primary-to-secondary creepage.

By default, the output voltages of the bias supply circuit are both unregulated. This is the case because the isolated DC-DC converter shows a very good regulation over a wide range of output current that covers the application use-cases well. For example, when driving Infineon CoolGaN™ IGLD60R070D1 at 100 kHz and 2 MHz, the variation of positive and negative bias supply rails is limited to only 0.3 V. For detailed information about the bias supply circuit please refer to application note **[4]**; here efficiency, output voltage regulation, start-up, shut-down and output short circuit capability are widely analyzed.

The board also allows 1 percent regulation of the positive or negative rails by enabling the TL432 regulator U3/ U4 or U5/ U6 respectively. In particular, the regulation of the positive rail may be considered when testing Schottky gate GaN HEMTs where the gate voltage must not exceed a certain limit, typically close to 6 V.

The default configuration is bipolar unregulated with +7 V, -4 V bias voltage split that can be changed as recommended in **Table 4**.

Table 4 Recommended dimensioning for different unregulated bipolar V_{GS} driving levels

V_{pos}	V_{neg}	V_{CCI}	R14
+7 V	-4 V	12 V	5.1 kΩ
+9 V	-5 V	15 V	3.9 kΩ
+8 V	-6 V	15 V	4.3 kΩ
+5 V [1]	-4 V [1]	10 V	7.5 kΩ

[1] This configuration is included for testing of Schottky GaN HEMTs from different suppliers. Please also consider enabling the 1 percent positive rail regulation.

2.3 Dead time setup

EiceDRIVER™ 2EDB8259Y includes a dead time control (DTC) and shoot-through protection (STP) that can be activated by means of the resistance R3. The driver dead time is set according to formula 1:

$$t_{DT}(ns) = 10 \times R_3(k\Omega)$$

A standard 0 to 10 V pulse generator can be used to generate the logic PWM signals; 50 Ω load setting should be considered. The PWMs signals can be applied to INA, INB board connectors via coaxial cables.

The half-bridge dead time replicates INA, INB dead time unless this is shorter than the “safe dead time” set on the driver via R3. For example, in **Figure 9** the dead time set on the driver is 100 ns (R3 = 10 kΩ); being INA, INB dead time longer (220 ns), the last one is replicated on the gate-to-source signals. In **Figure 10** instead, complementary INA, INB are considered with no dead time; therefore, the driver dead time of 46 ns (R3= 4.6 kΩ) is forced.

2EDB dead time therefore implements a “first level of protection against half-bridge shoot-through” ensuring no logic overlap due to wrong programming or noise on the input traces. It is important to highlight that half-bridge shoot-through could still happen due to induced noise on the gate-to-source voltage when the switching node commutates (Miller effect); this can be controlled by proper dimensioning of the negative V_{GS} in off-state.

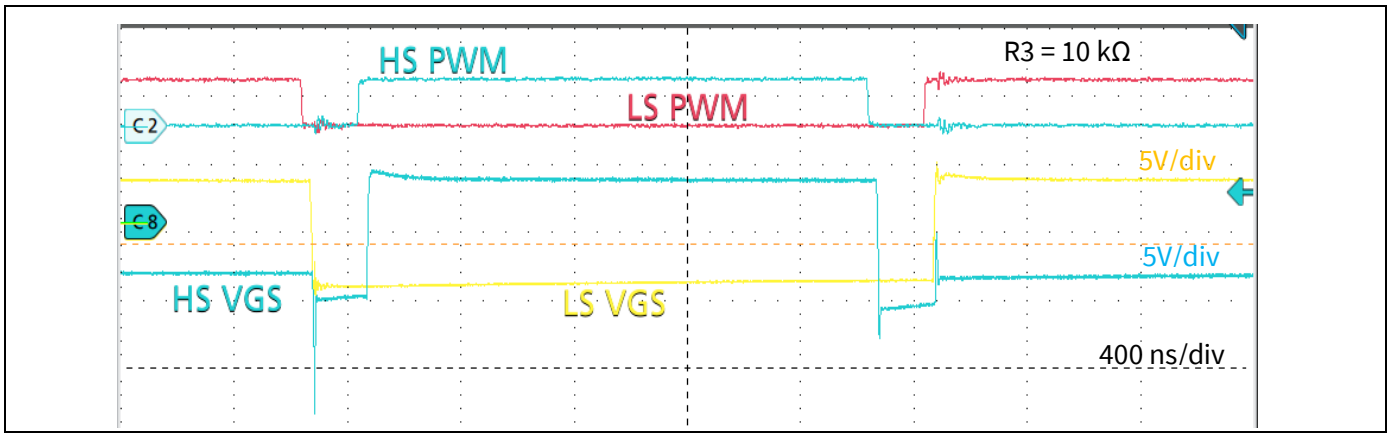

Figure 9 Example of gate-to-source voltage dead time set by PWM signals (R3=10 kΩ, PWM signals with 220 ns dead time)

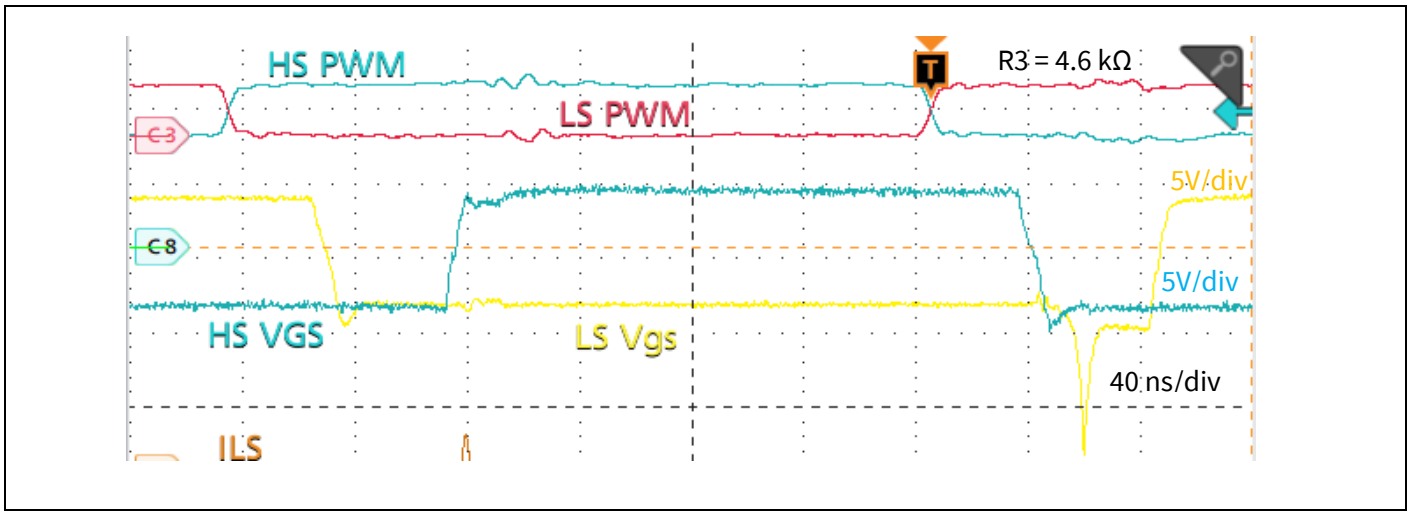

Figure 10 Example of gate-to-source voltage dead time forced by the 2EDB driver (R3 = 4.6 kΩ, complementary PWM with no dead time)

2.4 Gate driver circuit

Figure 11 shows the gate driver circuit based on the EiceDRIVER™ 2EDB8259Y including the configuration of dead time control, bypass capacitors, and also the RC interface for the CoolGAN™ GIT HEMTs

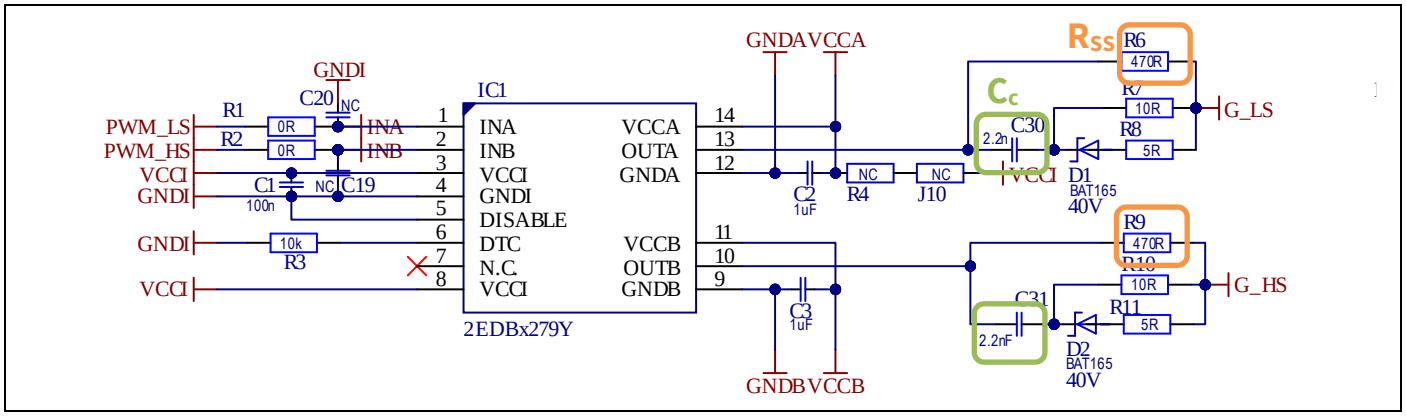

Figure 11 Gate driver circuit based on the EiceDRIVER™ 2EDB8259Y

In addition to the usual turn-on and turn-off resistance, Infineon's CoolGAN™ GIT HEMT requires few additional components as described below.

- **Static resistance R_{ss}** (R6/ R9): fixes the gate current feed into the CoolGAN™ during ON-state and therefore its $R_{DS(ON)}$; recommended gate current is in the 5 to 10 mA range.
- **Dynamic capacitance C_c** (C30, C31): decouples the static current from dynamic current. In addition, by storing charge during turn-on, forces a negative gate-to-source voltage at turn-off.

For sake of simplicity, when changing bias supply levels as per **Table 4** in the bipolar configuration (A), those parameters can be left unchanged at first glance without risk of return-on; see **Figure 12**. In case of unipolar driving (B, C configurations) a proper size of C_c is necessary because the negative $V_{GS,off}$ is only given by the charge stored on C_c; an exhaustive overview about driving Infineon's CoolGAN™ GIT HEMT can be found in application note **[1]**.

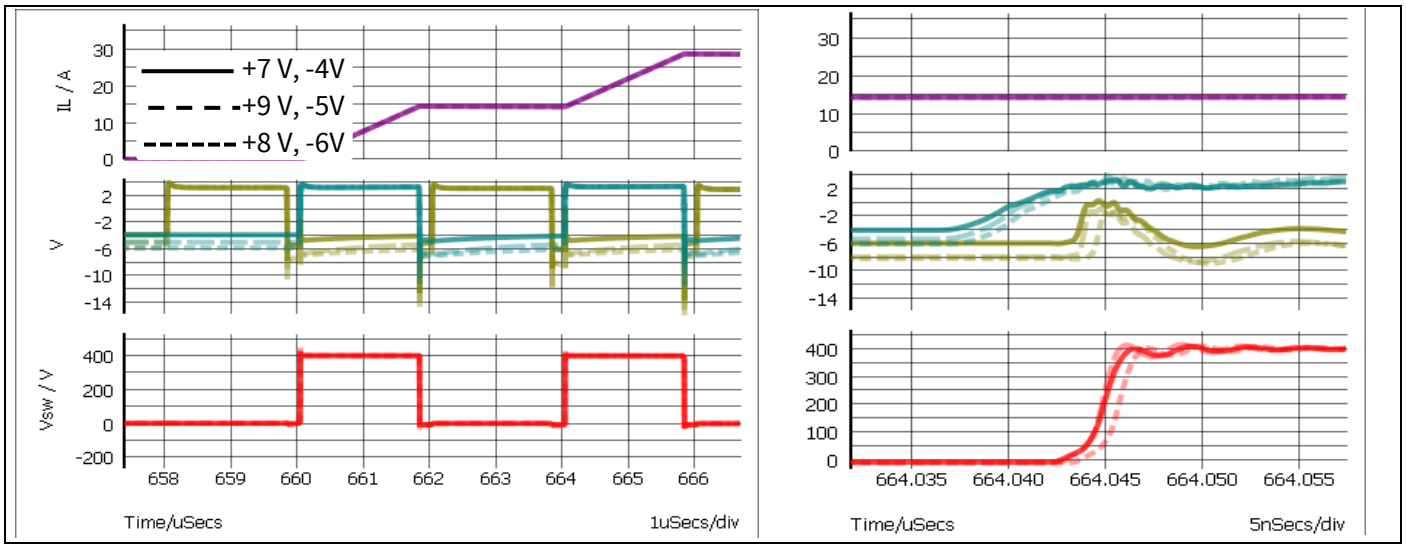

Figure 12 Overview on gate-to-source signals when driving IGLD60R070D1 in Conf. A with different bipolar supply voltages; this shows that even if, for simplicity, gate driver circuit parameters are not changed the operation is still safe

2.5 Measuring points

There are five test points on the board for connection to the oscilloscope to observe the signals of interest. **Table 5** includes the description of the test point and recommendation of probes and accessories.

Table 5 Test points and required probe

Test point label	Description	Referred to	Probe	Accessories
TP1	Low-side gate-to-source voltage	LS Kelvin source	1 GHz passive probe with low capacitance (e.g. TPP1000) [1]	short ground spring (016-2034-xx)
TP2	High-side gate-to-source voltage	HS Kelvin source	IsoVu (e.g., TIVP1) with TIVPMX10X (+-50V) sensor tip [2]	-
TP3	Switching node	LS Kelvin source	High-voltage passive probe (e.g., PHV 1000)	BCN adapter soldered to exposed pads
TP4, TP7	INA input to GNDI	GNDI	Passive 500 MHz [3]	Hook tip(013-0363-xx) for INA, alligator clip(196-3521-xx) for GNDI
			Standard differential probe	-
TP5, TP8	INB input to GNDI	GNDI	Passive 500 MHz [3]	Hook tip(013-0363-xx) for INA, alligator clip(196-3521-xx) for GNDI
			standard dif probe	-
-	Low-side MOSFET current	PGND or LS Source	ISoVu (e.g., TIVP1 with TIVPMX10X (+-50V) sensor tip	MMCX to be soldered on the 1 Ω shunt resistors (see **section 3.2.1**)

[1] Do not use a standard differential probe for GaN gate-to-source signals due to high capacitance that distorces the waveforms
[2] Do not use a standard differential probe for high-side measurements due to limited CMRR
[3] Passive probe can be used when GNDI = PGND, then in configuration D or in the other configurations when there is no bulk voltage applied. Otherwise please use differential probe.

3 Double pulse

3.1 Overview

Figure 13 and **Figure 14** show the results of respectively a direct double pulse test (setup in **Figure 2**) and a reverse double pulse test (setup in **Figure 3**) with 50 µH external inductor up to 35 A test current. In the direct double pulse test, with the inductor placed across the high-side device, the low-side GaN behaves as the active switch and the high-side device as the freewheeling transistor; vice versa for the reverse double pulse.

For more details on double pulse testing refer to section 4.8 in reference **[3]**.

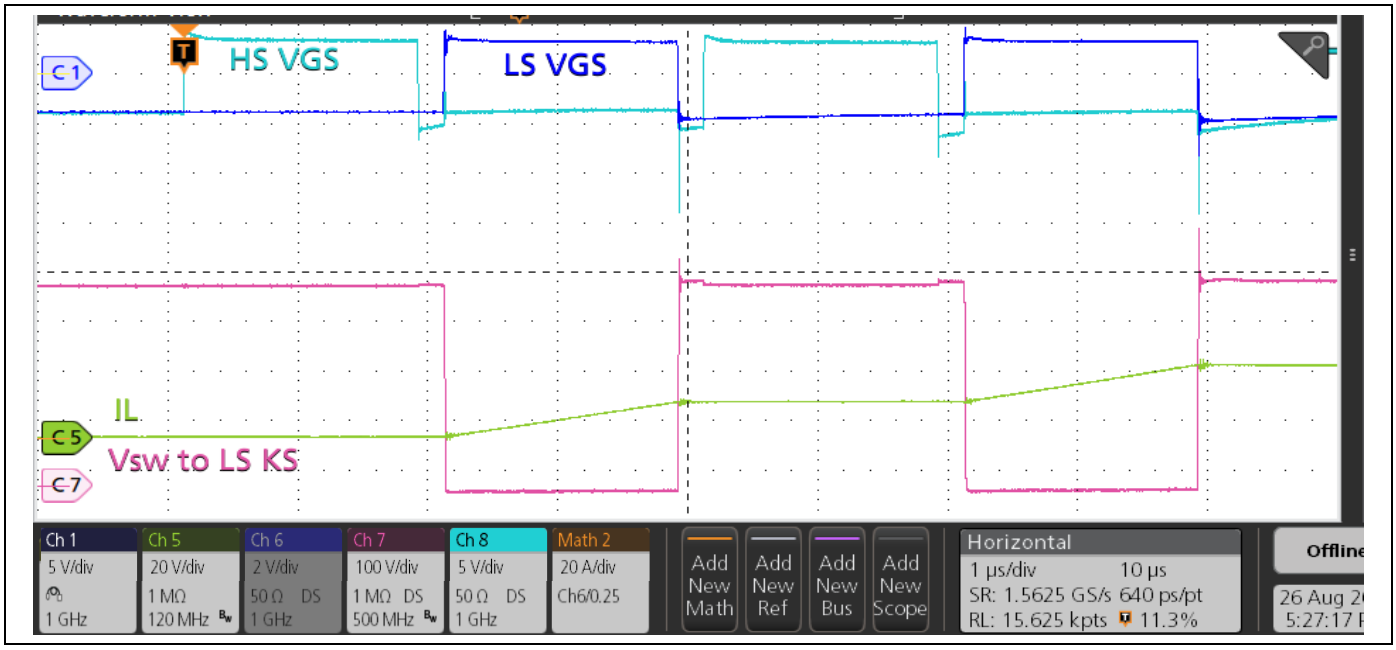

Figure 13 Direct double pulse test with 50 µH inductor

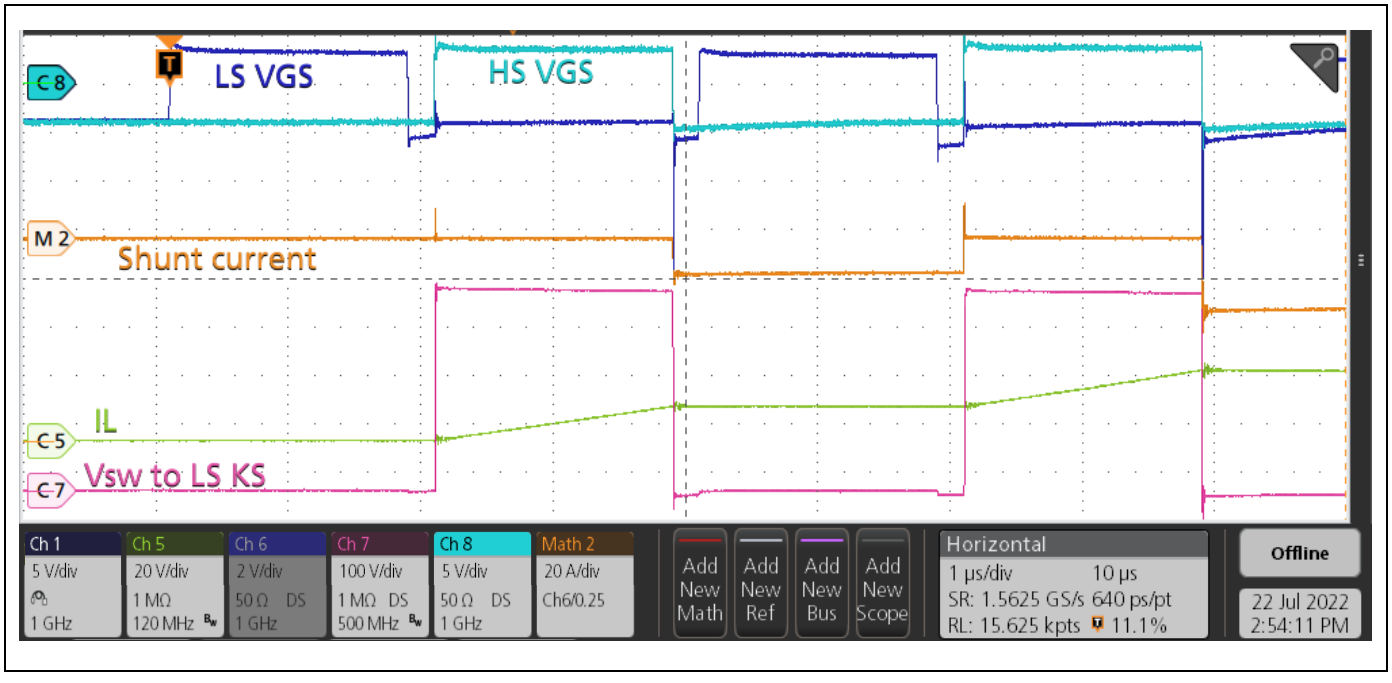

Figure 14 Reverse double pulse test with 50 µH inductor

Figure 15 shows in detail the four transitions for the reverse double pulse test, allowing a closer look at the switching node (see magenta, waveform C7) and to the GaN low-side current (in orange, waveform M2). The switching node transition speed is given from 20 percent to 80 percent of the full voltage swing.

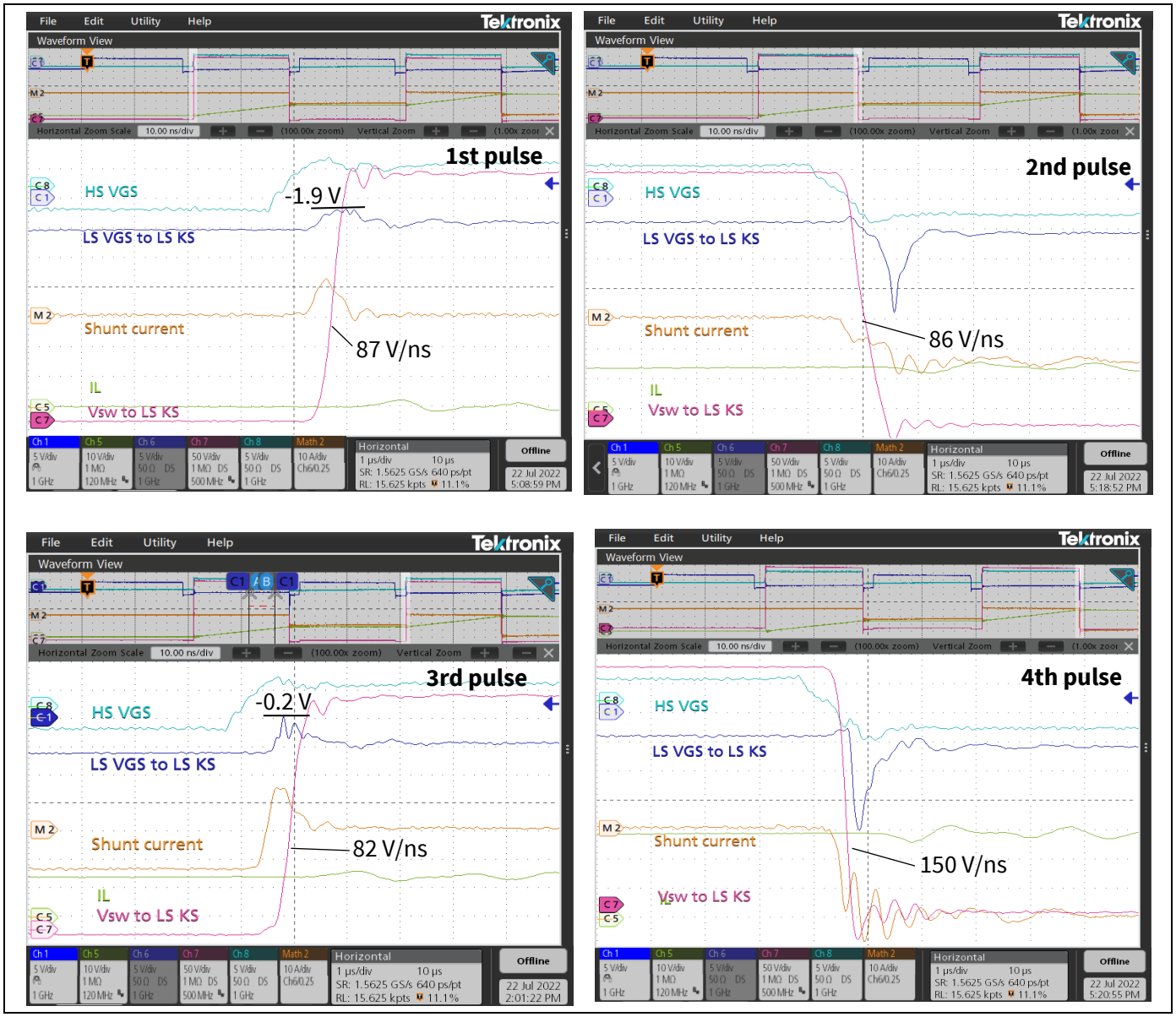

Figure 15 Reverse double pulse with 50 µH test inductor – zoom on the transitions

Clearly in the reverse double pulse the high-side GaN is the one experiencing hard-switching turn-on (active switch). At the same time the low-side GaN, that is the “diode device”, experiences an increase of its gate-to-source voltage (in dark blue, waveform C1) during high-side turn-on due to the well-known Miller current charge induced by the fast change of the switching node. It is important to dimension the gate components in order to ensure that the low-side V_{GS} stays well below the gate threshold at the rated current to avoid unwanted return-on; indication on return-on free transition is also provided by the low-side current measurement (see **chapter 3.2.3**).

3.2 Measuring the half-bridge current

3.2.1 Mounting of MMCX connector for minimum inductance measurement

The board allows the possibility to deeply look into the switch commutation current, e.g., during double pulse test. R31, R32, ... R40 can accommodate simple 1 Ω resistors in 0603 footprint to create a low-inductance shunt to measure the low-side switch current.

To ensure that a negligible inductance is added to the power loop and towards the oscilloscope, the following two measures can be implemented:

- Solder the resistors upside down
- Solder an MMCX connector directly on top of the resistors in the middle of the queue to create a “star connection”. The MMCX connector is provided together with the board.

Those measures allow a clean and fair measurement when the commutation current is not 0 A as fast commutating di/dt could induce a voltage drop and delay on the parasitic inductances and distorce the measurement.

3.2.2 Measuring the commutation and Q_{oss} current

Figure 16 shows the 2nd high-side turn-on pulse at 16 A load current during reverse double test. At the beginning of the turn-on (phase b) S1 channel starts opening and the current, which was flowing through the low-side body diode (phase a), starts to flow into its channel. After, the 2nd phase (c) starts during which the switching node commutates; C_{oss1} discharged through S1 channel and C_{oss2} is charged via S1 channel. The current visible on the low-side shunt is the commutating current during phase B and the Q_{oss2} charge is the commutating current during phase C.

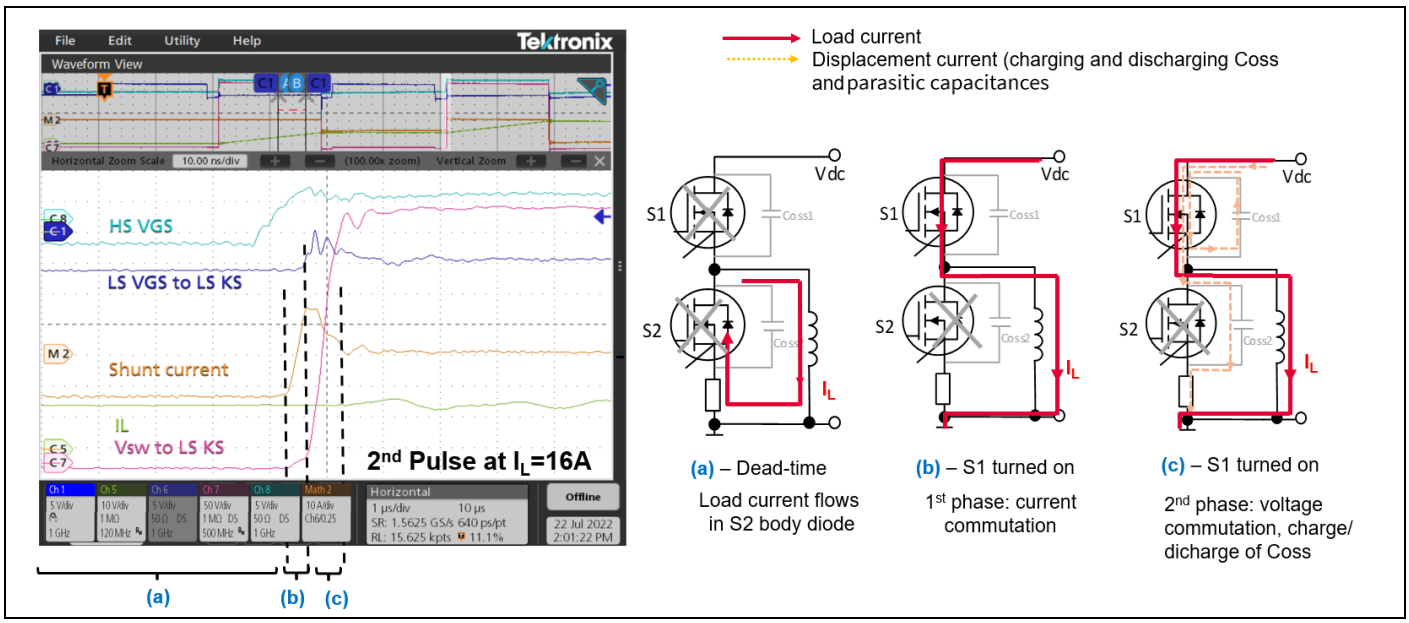

Figure 16 Half-bridge current during high-side hard-switching turn-on

Q_{oss} charge can be measured during phase (c) via oscilloscope with the “Area” option between the cursor. Measured Q_{oss} is around 60 nC, which is realistically slightly higher than ideal $Q_{oss,\,ideal}$ =47 nC specified in the IGLD60R070D1 datasheet. The additional contribution comes from the charge of the parasitic capacitances as

the one related to PCB switching node – GND plane overlap, the one of the external inductor and the load capacitances of the probes.

The measured Q_{oss} can also be double checked by back calculation from the soft-switching transition as shown in **Figure 17**. During soft-switching, the load-current is responsible for the switching-node transition; high-side C_{oss1} and low-side C_{oss2} respectively charges and discharges via the inductor path with I_L current.

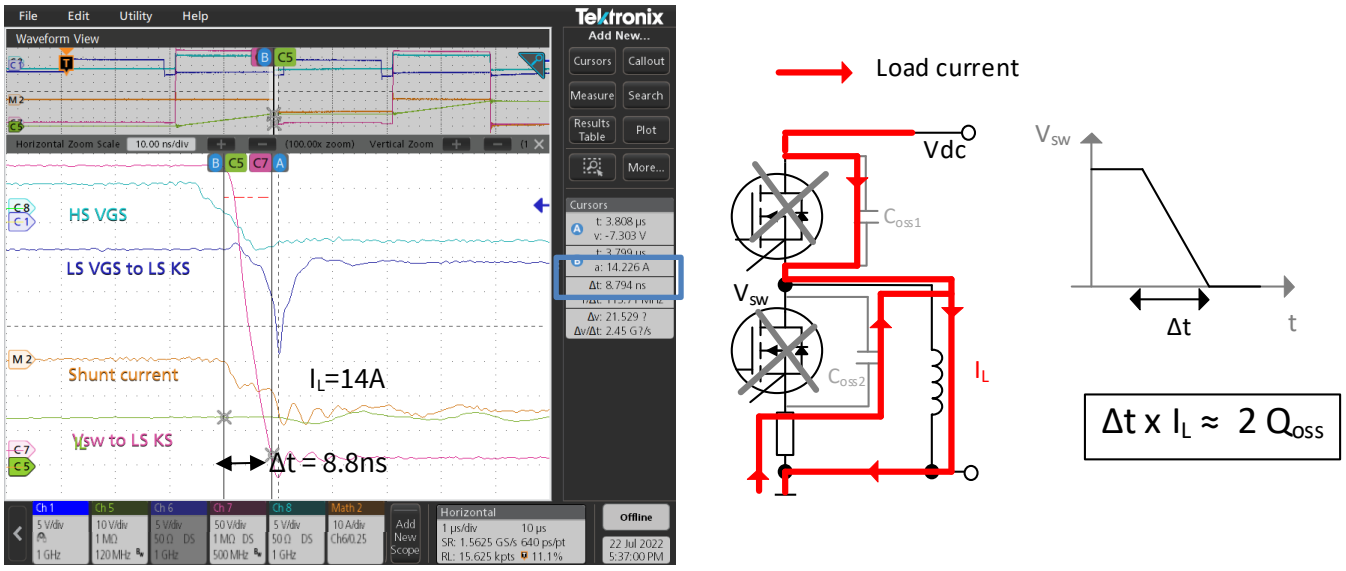

Figure 17 Soft-switching – estimation of real Q_{oss} also including parasitics

3.2.3 Detecting shooth-through

The gate-to-source voltages provide a first way to look at possible return-on. During hard-switching of one device, the gate-to-source voltage of the complementary device could increase due to coupling through its gate-to-source capacitance (C_{GS}) and gate-to-drain capacitance (C_{GD}). If the V_{GS} is above the threshold, then there is clearly a return-on with a shoot-through in the half-bridge. However, the accessible gate-to-source voltage is the one measured outside the GaN device, after its $R_{G,int}$ gate resistance and bond-wire inductances; therefore, the internal V_{GS} can be higher than the one measured across the gate-source pins.

Looking at the half-bridge current and charge during hard-switching turn-on is an alternative way to detect a potential shooth-through condition. For this reason, an accurate current measurement is very important.

Bipolar driving, Conf A. (+7.5 V, -4 V)

Unipolar driving, Conf B. (+7.5 V) without C_c adaptation (using 2EDB7259Y)

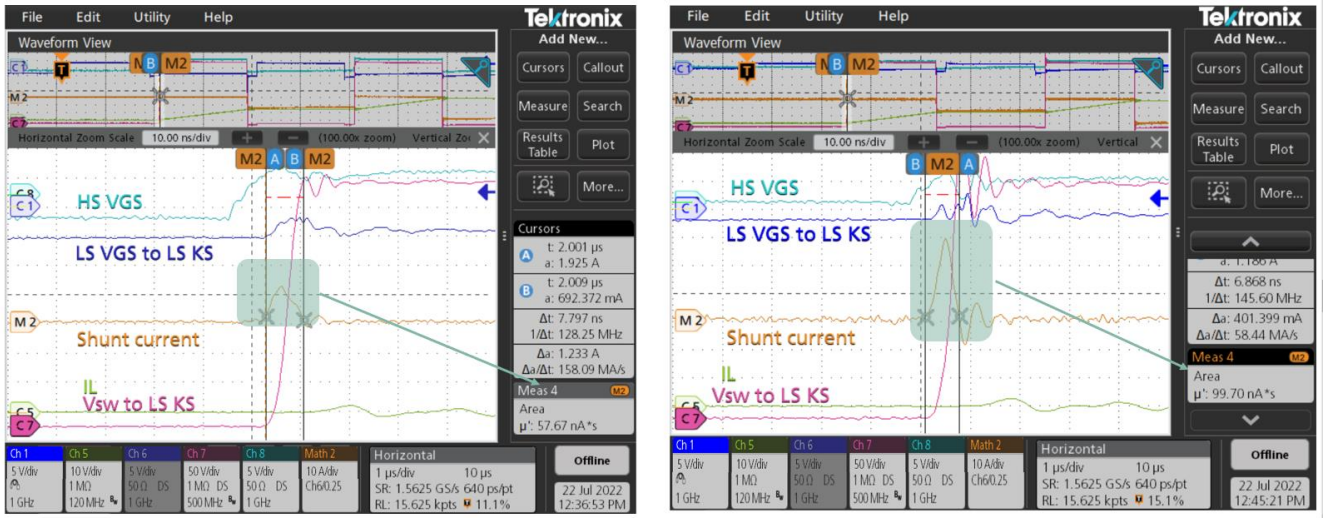

Figure 18 Right-side shows clear return-on with almost two times higher turn-on charge at 0 A

For a demonstration, a return-on has been easily forced by switching from Conf. A (bipolar) to Conf. B (unipolar) without adapting the gate coupling capacitance C_c; in this case, the negative $V_{GS,off}$ is only -2 V instead of -4 V leading V_{GS} to go above the threshold and creating a shoot-through in the half-bridge.

Figure 18 clearly shows that the right-side turn-on transition is affected by return-on being the measured charge almost two times higher. Also, the ringing on the switching node and on the high-side V_{GS} are a clear indication of a shoot-through condition in the half-bridge.

4 Buck mode

When the external inductor is connected between V_{sw} and V_o terminals (see **Figure 4**), the circuit is configured as a buck converter. The buck output voltage (Vo to Vin-) will be proportional to the buck input voltage (VIN+ to Vin-) times the high-side MOSFET duty-cycle. With the appropriate inductor, the PWMs frequency can be set low (tens of kHz), or up to 2 MHz. The circuit can be operated continuously in this mode, provided that the temperature of the transistors is kept to a safe level. The circuit is entirely open-loop since there is no feedback control, so the output voltage will not be regulated and it will vary with the load. When operating at high frequencies, ensure that the inductor ripple-current always changes polarity each half-cycle, so that the circuit operates in zero voltage switching (ZVS) mode; otherwise, operation in hard-switching at high-frequency will result in large power dissipation due to the switching loss.

Attention: Make sure to first turn-on the low-voltage bias supply (V_{CCI}), then the PWM generator and only after the high-voltage DC source. Otherwise, if no proper start-up sequence is implemented, high current would flow into the circuit leading to destruction of the power switches. See section 6.1.2 for an example of simple start-up sequence.

4.1 Buck mode without DC load – complete soft-switching

Without DC load connected to the evaluation board, a complete soft-switching performance can be observed. **Figure 19** shows the test performed on the board using 50 µH inductor and a function generator set at 100 kHz with duty-cycle of 50 percent. With 400 V DC bus, the output settles at 200 V and the peak-to-peak current will be about 20 A. Both high- and low-side GaN transistors are operating in ZVS mode with 29 V/ns. The negative spikes on the gate voltages is due to the non-linear capacitance of C_{rss} (related to the GaN device); for more information refer to section 4.2.2 in reference **[3]**. **Figure 19** also include thermal image of the switches operating at around 61°C without FAN.

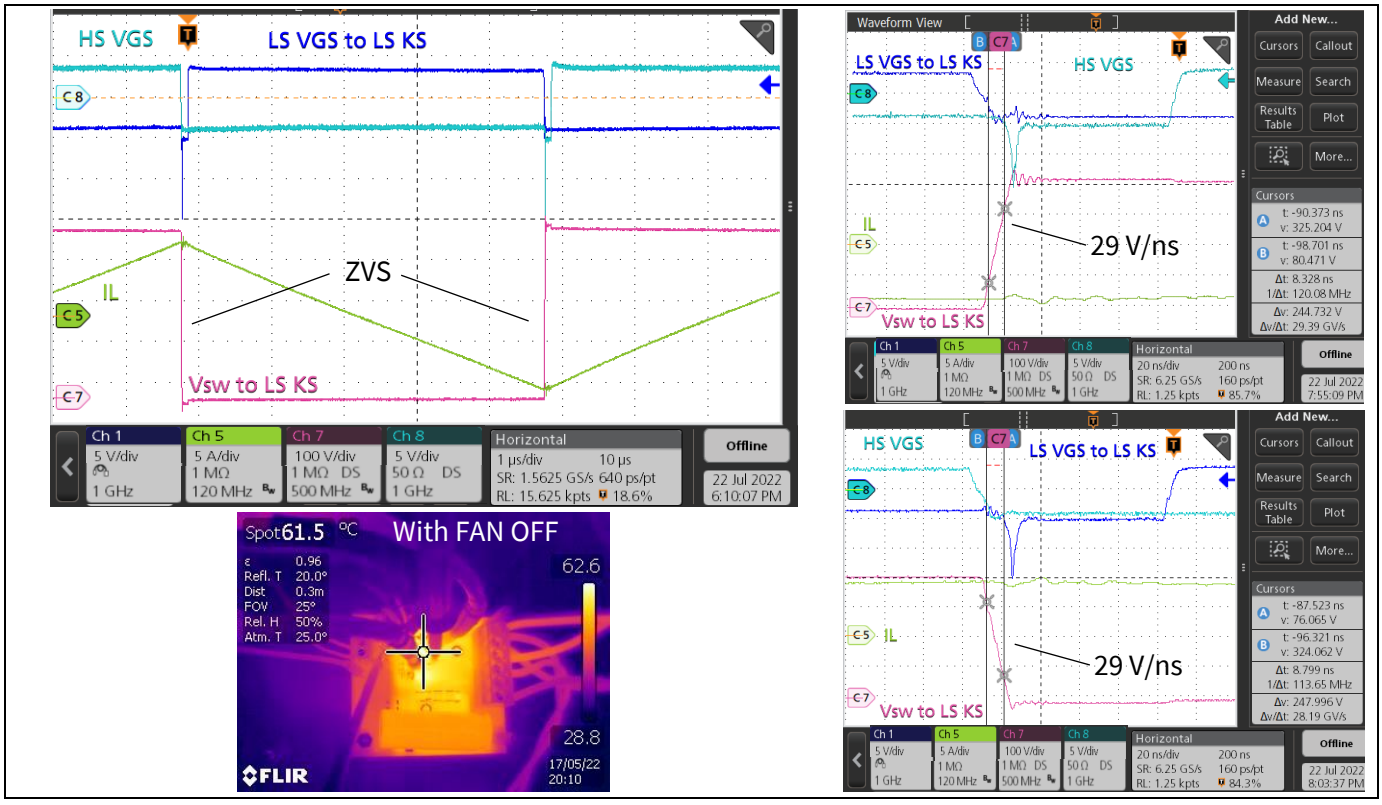

Figure 19 Buck-mode witout DC load with 50 µF inductor, 100 kHz frequency, 50 percent duty-cycle and 100 ns dead time

Figure 20 shows the use-case with 5 µH inductor and a function generator set at 2 MHz with duty-cycle of 50 percent. With 400 V DC bus, the output settles at 200 V and the peak-to-peak current will be about 10 A. The GaN switches operate at around 60°C with FAN on.

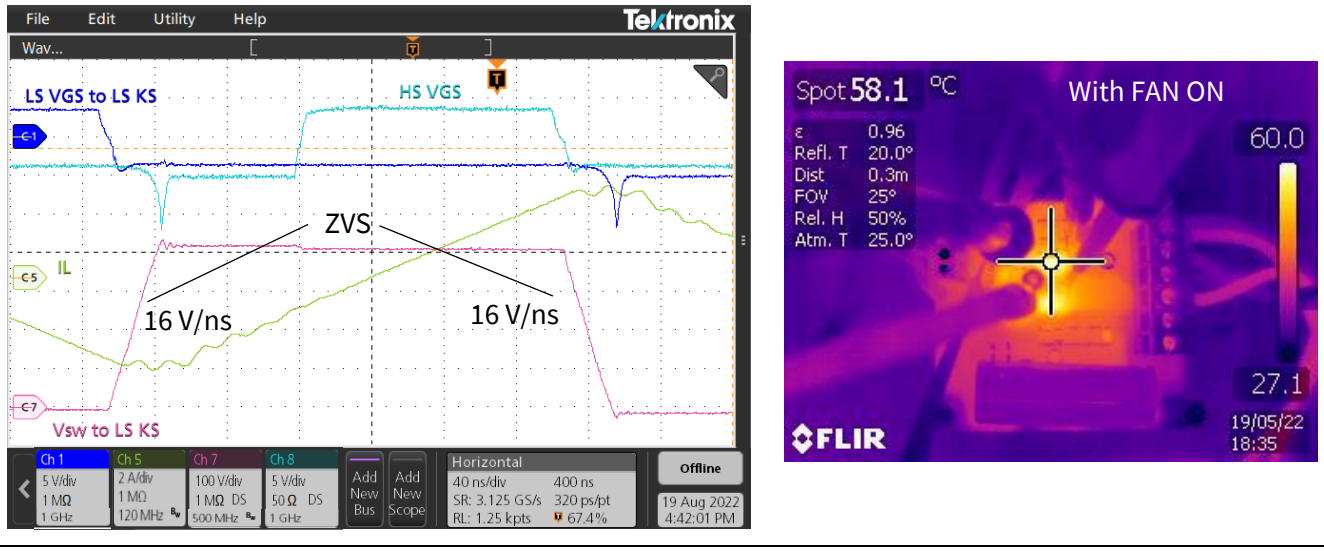

Figure 20 **Buck-mode without DC load with 5 µF inductor, 2 MHz frequency, 50 percent duty-cycle and 100 ns dead time**

Due to higher frequency the dead time can be reduced to 46 ns by change of R3 (10 kΩ → 4.6 kΩ). This also brings down the temperature on the GaN devices due to reduced reverse conduction losses (see **Figure 21**).

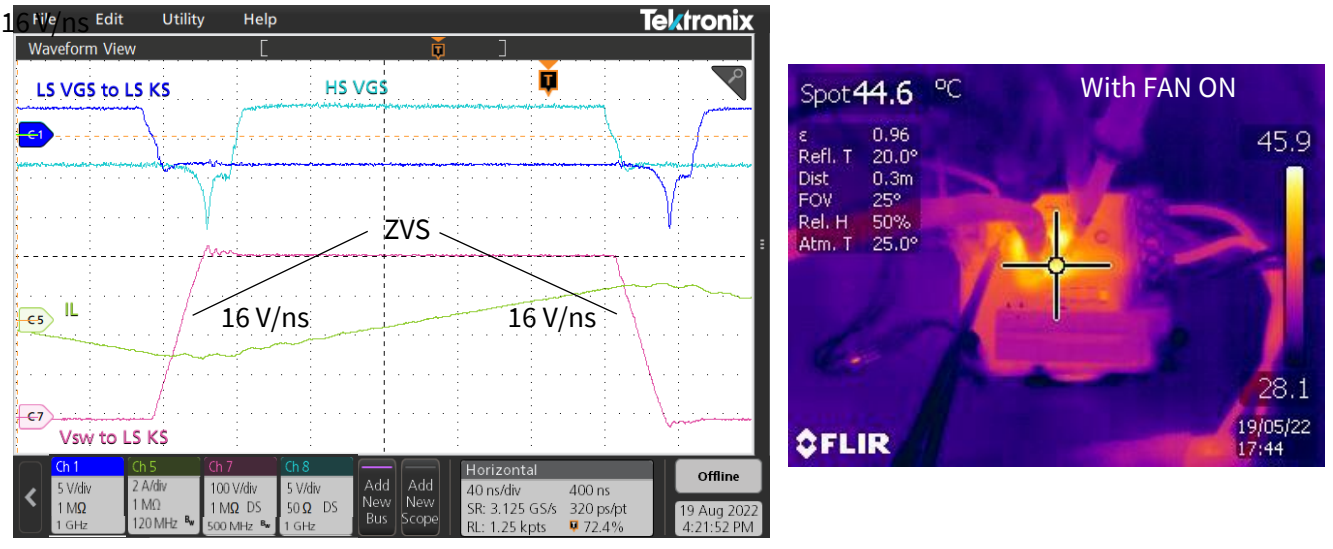

Figure 21 **Buck-mode without DC load with 5 µF inductor, 2 MHz frequency, ~50 percent duty-cycle and 46 ns dead time**

4.2 Buck mode with DC load

When a DC load is connected to the evaluation board, the high-side and low-side GaN transistors turn-on (or off) with a different switching current. **Figure 22** shows an example with 10 A positive output load applied via a programmable DC electronic load; the setup still uses 50 µH inductor and 100 kHz logic signals with duty-cycle of 50 percent. In this case, the low-side switch still operates in ZVS whilst the high-side switch experiences a

hard-switching turn-on. Being the soft-switching current level very high (20 A), the speed of the soft-switching transition (70 V/ns) is comparable with the speed of the hard-switching transition (76 V/ns).

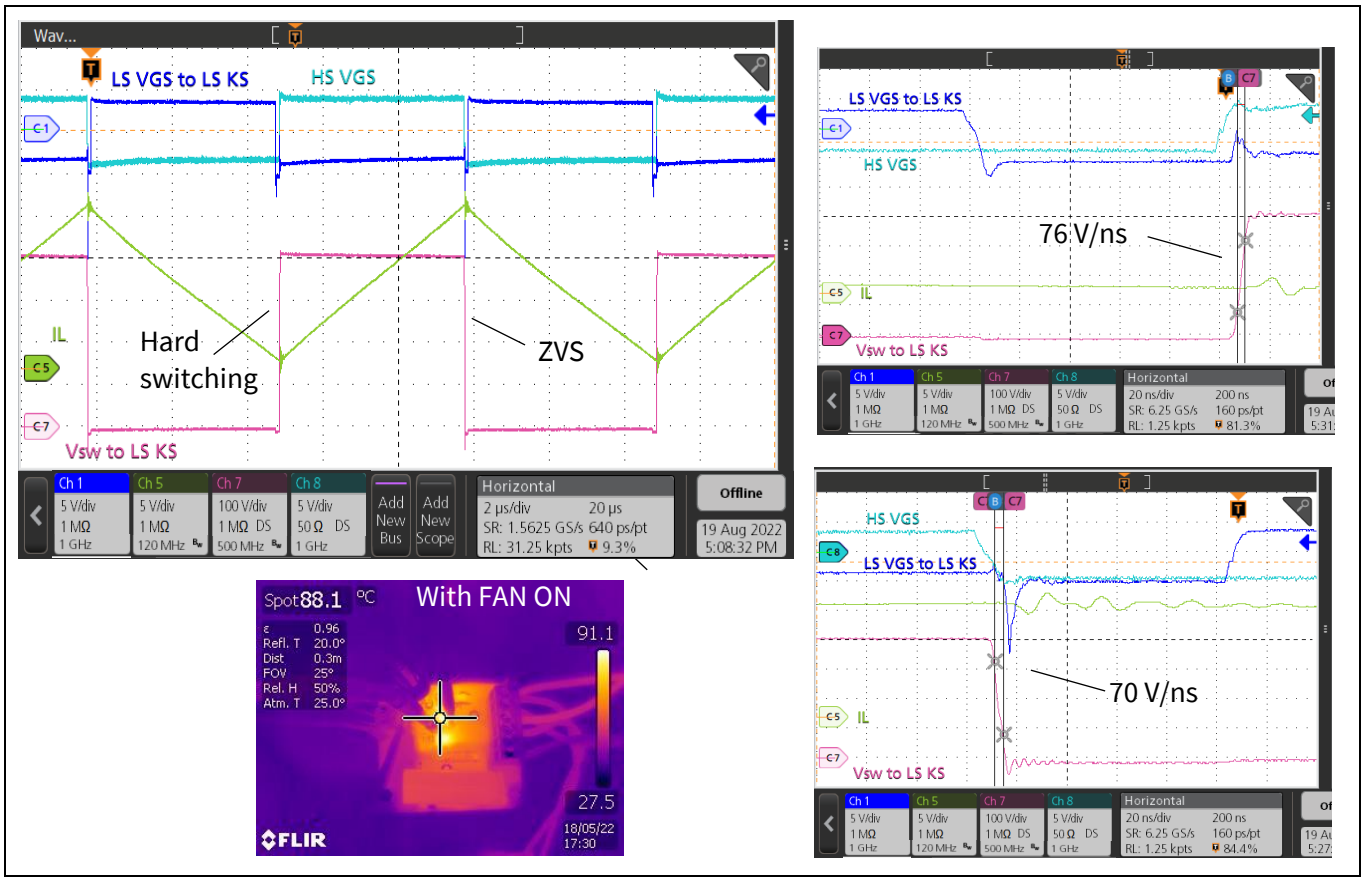

Figure 22 **Buck-mode at 10 A DC load (2 KW) with 50 uF inductor, 100 kHz frequency, ~50 percent duty-cycle and 100 ns dead time – hard-switching for high-side and soft-switching for low-side**

Figure 23 instead shows the use-case with 2 MHz switching frequency, 50 percent duty-cycle, 5 µH inductor and 3 A output current applied via a programmable DC electronic load. Here, the low-side GaN switch is still operating in ZVS with 8 A current whilst the high-side experiences a partial hard-switching.

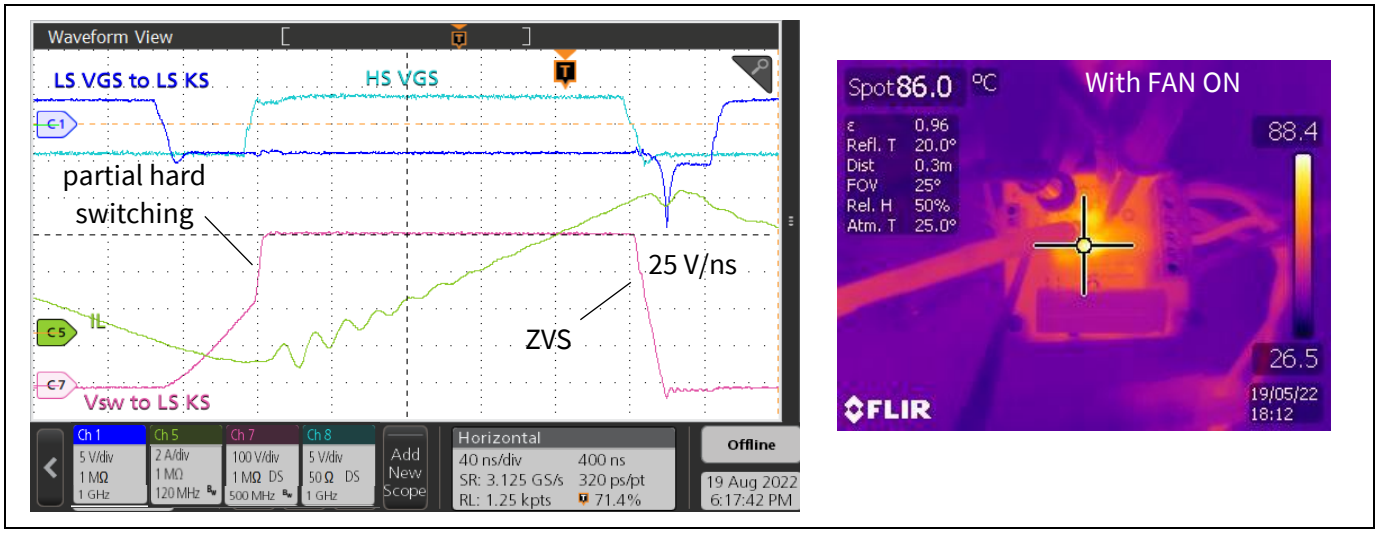

Figure 23 **Buck-mode at 3 A DC load (600 W) with 5 µF inductor, 2 MHz frequency, ~50% duty-cycle and 48 ns dead time – soft-switching for low-side and partial hard-switching for high-side**

5 Boost mode

The board can be configured in boost-mode with the setup shown in **Figure 5**. The boost output voltage (Vin+ to Vin-) will be proportional to the boost input voltage (Vo to Vin-) times D/(1-D) where D is the duty-cycle of the low-side GaN switch. With an input voltage of 320 V and a low-side duty-cycle of 20 percent, an output voltage of 400 V is achieved.

Attention: Make sure to first turn-on the low-voltage bias supply (V_{CCI}), then the PWM generator and only after the high-voltage DC source. Otherwise, if no proper start-up sequence is implemented, high-current would flow into the circuit leading to destruction of the devices.

5.1 Boost mode without DC load

Without DC load connected to the evaluation board, a complete or partial soft-switching performance can be observed depending on the value of the external inductor.**Figure 24** shows the test performed on the board using 650 µH inductor and a function generator set at 100 kHz with duty-cycle of 20 percent for the low-side and 80 percent for the high-side GaN switch. The peak-to-peak current is about 1 A and both high- and low-side GaN transistors are operating in partial ZVS mode due to low current. The negative spikes on the gate voltages is due to the non-linear capacitance of C_{rss} (related to the GaN device); for more information refer to section 4.2.2 in reference **[3]**. **Figure 24** also includes a thermal image of the switches operating at around 29°C without FAN.

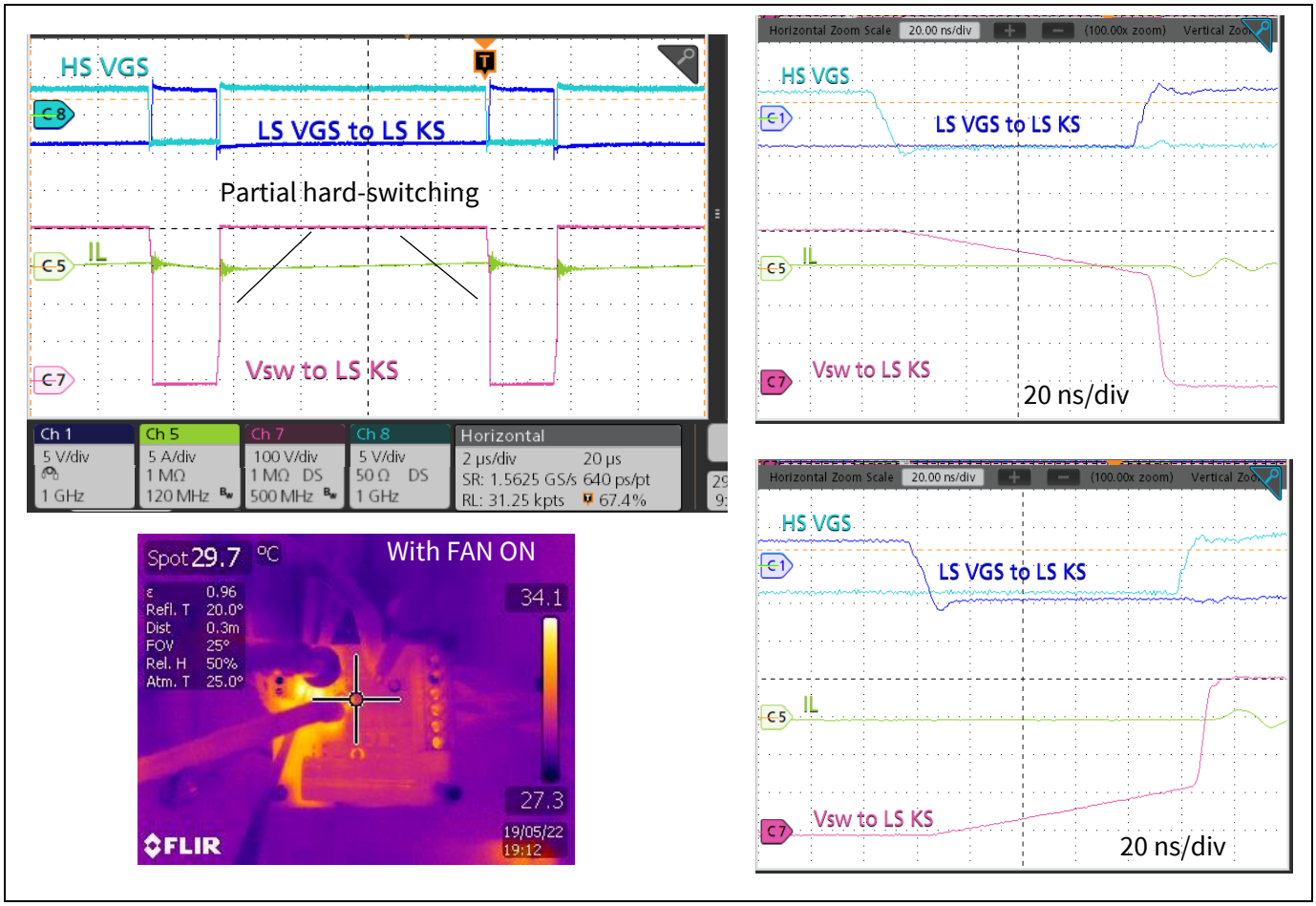

Figure 24 Boost-mode without DC load with 650 µH inductor, 100 kHz frequency, ~20 percent duty-cycle on the low-side GaN switch and 100 ns dead time

5.2 Boost mode with DC load

When a DC load is connected to the evaluation board, the high-side and low-side GaN transistors experience a different turn-on (or -off) behavior. **Figure 25** shows an example with 6.2 A positive output load current applied via a programmable DC electronic load; the setup still uses 650 µH inductor and 100 kHz logic signals with duty-cycle of 20 percent for the low-side GaN. With 650 µH inductor, the peak-to-peak current is only limited to 1 A and therefore the switching current for both low-side and high-side transition is always positive. Therefore, the low-side switch operates in full ZVS mode whilst the high-side switch experiences a hard-switching turn-on.

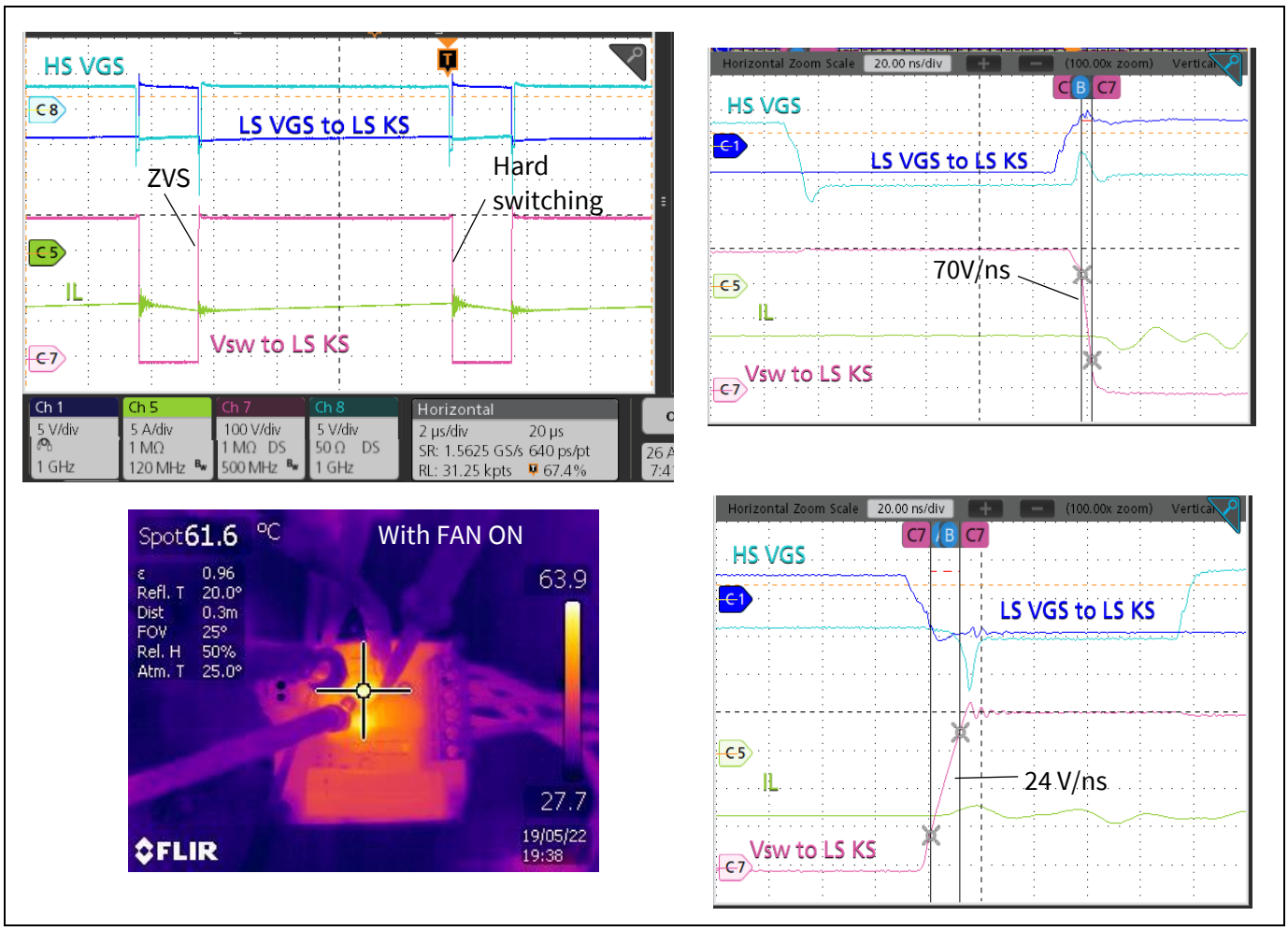

Figure 25 Boost-mode at 6.2 A DC load (2500 W) load with 650 µH inductor, 100 kHz frequency, ~20 percent duty-cycle on the low-side GaN switch and 100 ns dead time

6 Unipolar supply

6.1.1 General considerations

As explained in **section 2.2**, the board can be configured to operate with unipolar supply. **Figure 26** shows a gate-to-source voltage comparison between bipolar and unipolar operation; the default Conf. A (-7.5 V, -4 V) is compared with Conf. D (bootstrap). For simplicity, the RC interface parameters (R_{ss}, C_c) have been left unchanged.

With a supply voltage VCCI of 12 V for Conf. D, similar negative gate-to-source voltage (around -4 V in soft-switching) is achieved at the beginning of the turn-off, when the switching node transition happens. For the bipolar configuration, the V_{GS} keeps at -4 V during the entire turn-off due to imposed negative voltage from the bias supply. Instead, for the unipolar case the gate capacitances C_c discharges, here completely to 0 V; therefore, the next turn-on transition starts at 0 V. Clearly for unipolar case, the ending point of the discharge changes with switching frequency and duty-cycle and therefore the initial level of V_{GS} at the beginning of the next turn-on changes with the operating point. Therefore, in some topologies such as totem pole PFC where the duty-cycle is not constant, the V_{GS} changes and with it the turn-on losses also vary unless a higher C_c is considered.

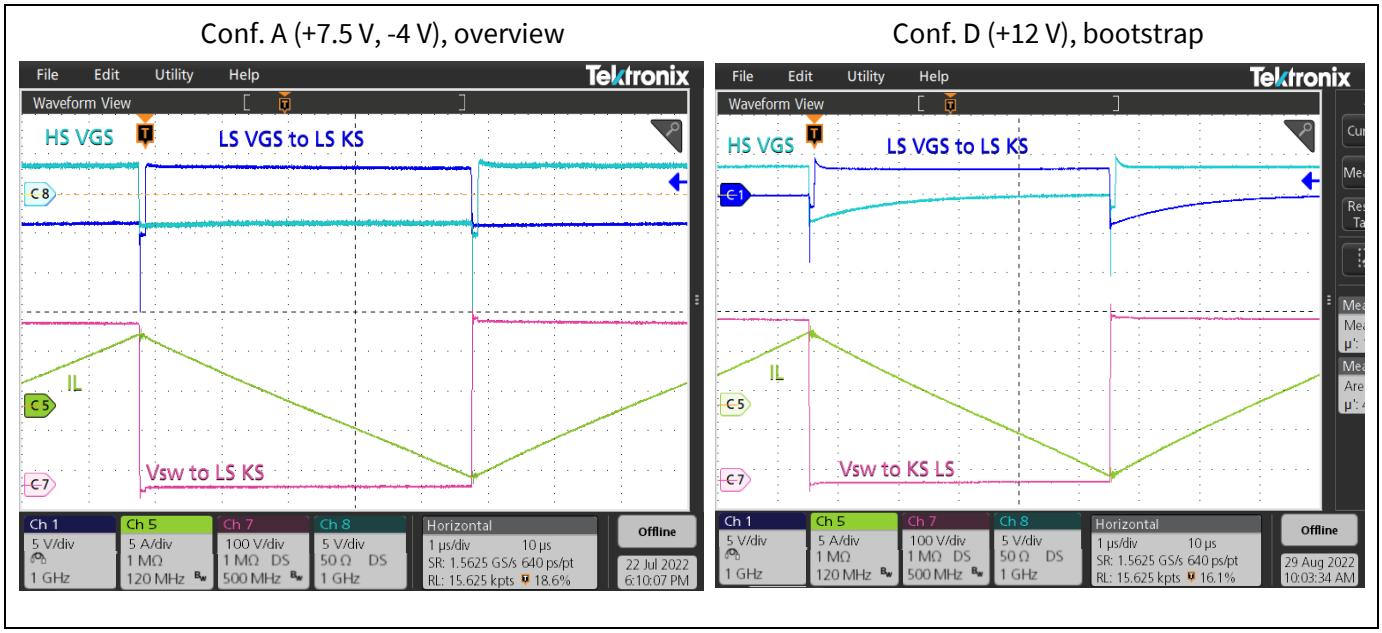

Figure 26 Buck-mode at no load with 50 µF inductor, 100 kHz frequency and 50 percent duty-cycle – overview of bipolar vs. unipolar supply driving

Unipolar and bipolar supply show different pros and cons and the selection is left to the user. The bipolar supply driving is the most reliable solution, as it always ensures a safe negative V_{GS} even when the gate capacitance C_c is discharged; this can happen at the “first pulse” in start-up or in special system conditions (e.g., burst mode). However, it requires additional circuitry for the bipolar bias supply. This application note also includes a recommendation for the bias supply circuit which benefits of high CMTI, compact size and attractive price; more information can be found also in **[4]**.

6.1.2 Start-up in buck-mode with boostrap

When bootstrap is used (Conf. D), start-up or recovery conditions must be carefully checked because for some time, until the boostrap capacitor is charged, only the low-side GaN is able to switch; this can create critical unbalances and induced noise.

As mentioned in **section 4**, also when using bipolar supply, it is always recommended to first turn-on the bias, after the PWMs and at the end the DC bulk. However, in case the user wants to check a start-up condition by first applying the DC bus, please take care of applying a proper PWMs start-up sequence to avoid excessive current into the circuit. **Figure 27** shows a very simple start-up in buck-mode with 50 µH external inductor. With 500 kHz PWMs and 20 percent duty-cycle on the high-side GaN device, the current stays below 10 A. Here Conf. D with RSFKL boostrap diode, R_b = 47 Ω and V_{CCI} = 12V is considered; the high-side gate signals (light blue, waveform C8) only appears after ~ 50 µs, when the boostrap supply approaches the driver UVLO. Before, no noise is visible on the high-side V_{GS} due to switching node movement thanks to the “fast output clamping” of the EceDRIVER™ 2EDB8259Y gate driver, which is active below UVLO already from ~1 V supply.

The zoom in **Figure 27** also shows that hard-switching occurs during start-up on the low-side V_{GS}; however, it can be taken under control with proper selection of the negative voltage and boostrap diode as in this example.

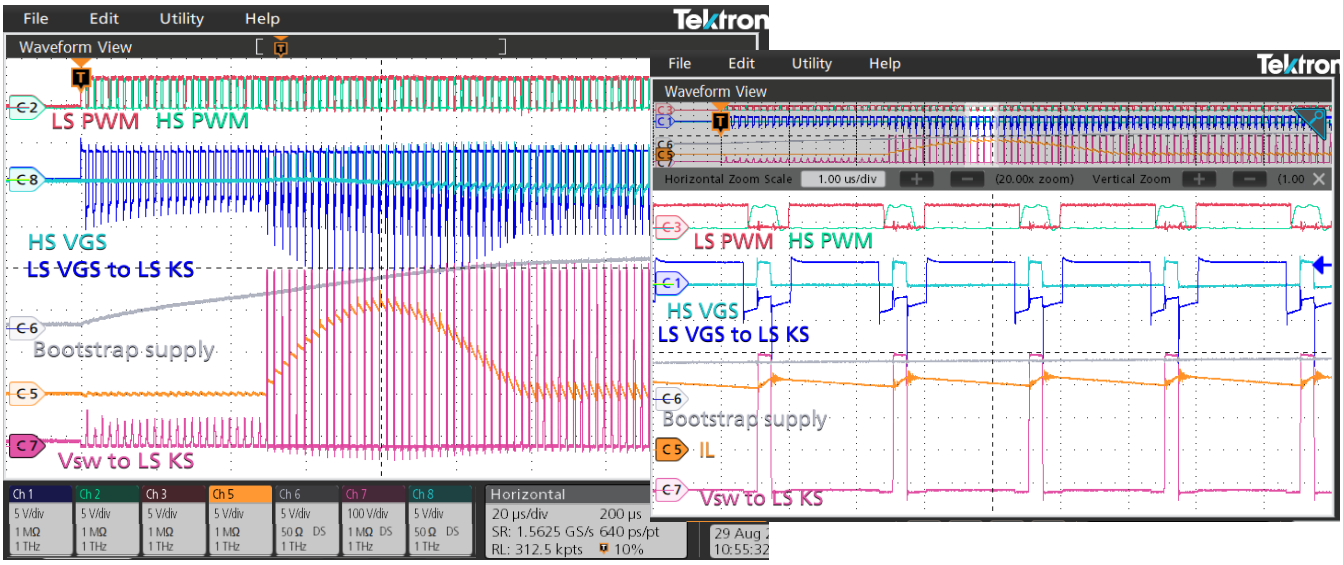

Figure 27 Buck-mode without DC load with 50 µF inductor, 500 kHz PWMs and 20 percent duty-cycle on the high-side GaN device – start-up in Conf. D with 12 V V_{CCI}

7 Board files: Schematic, Layout, BOM

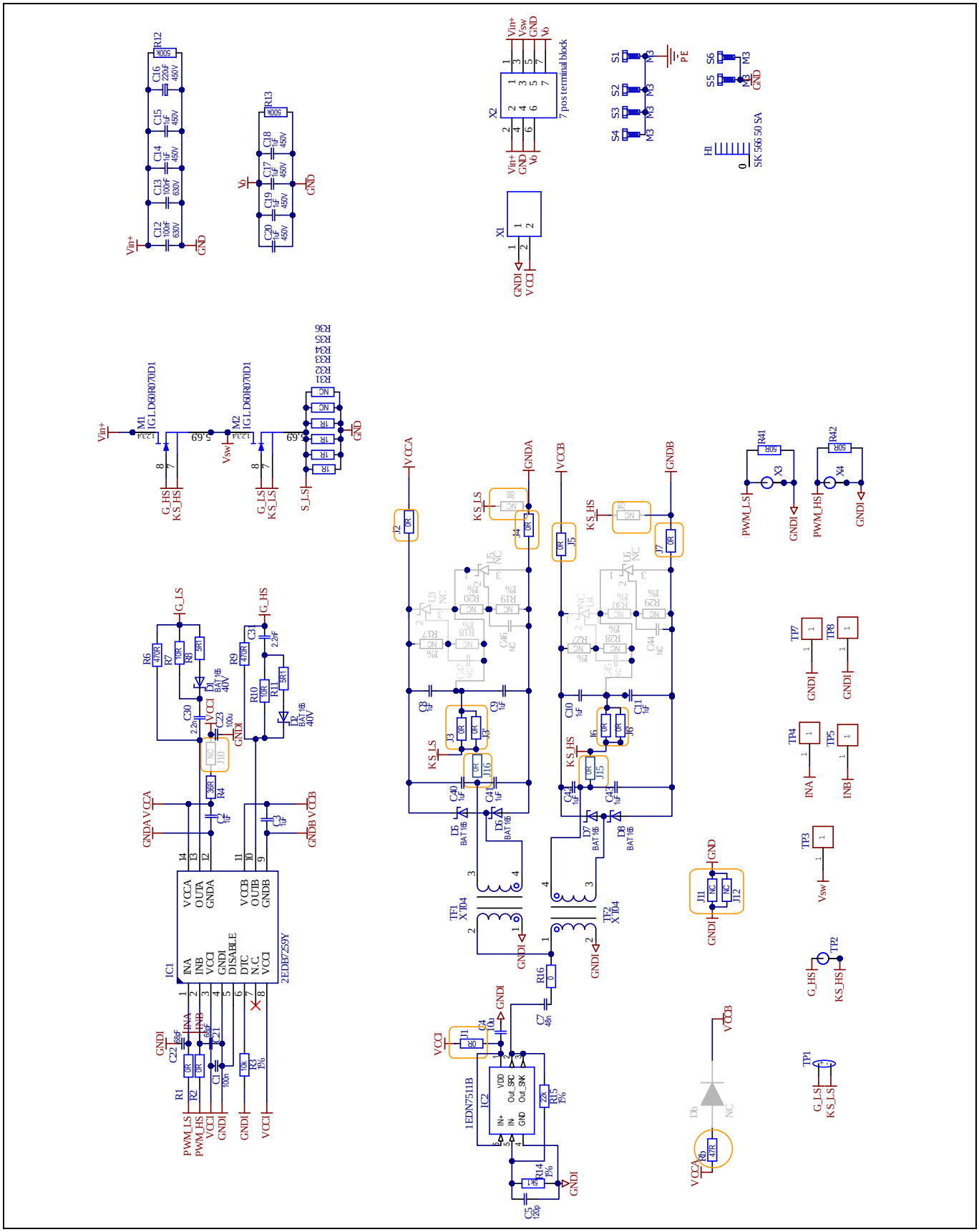

Figure 28 Schematic of EVAL_2EDB_HB_GaN evaluation board

The evaluation board is 1.6 mm thick, with 4 evenly-spaced copper layers 70 µm thick. The layer stackup is depicted below.

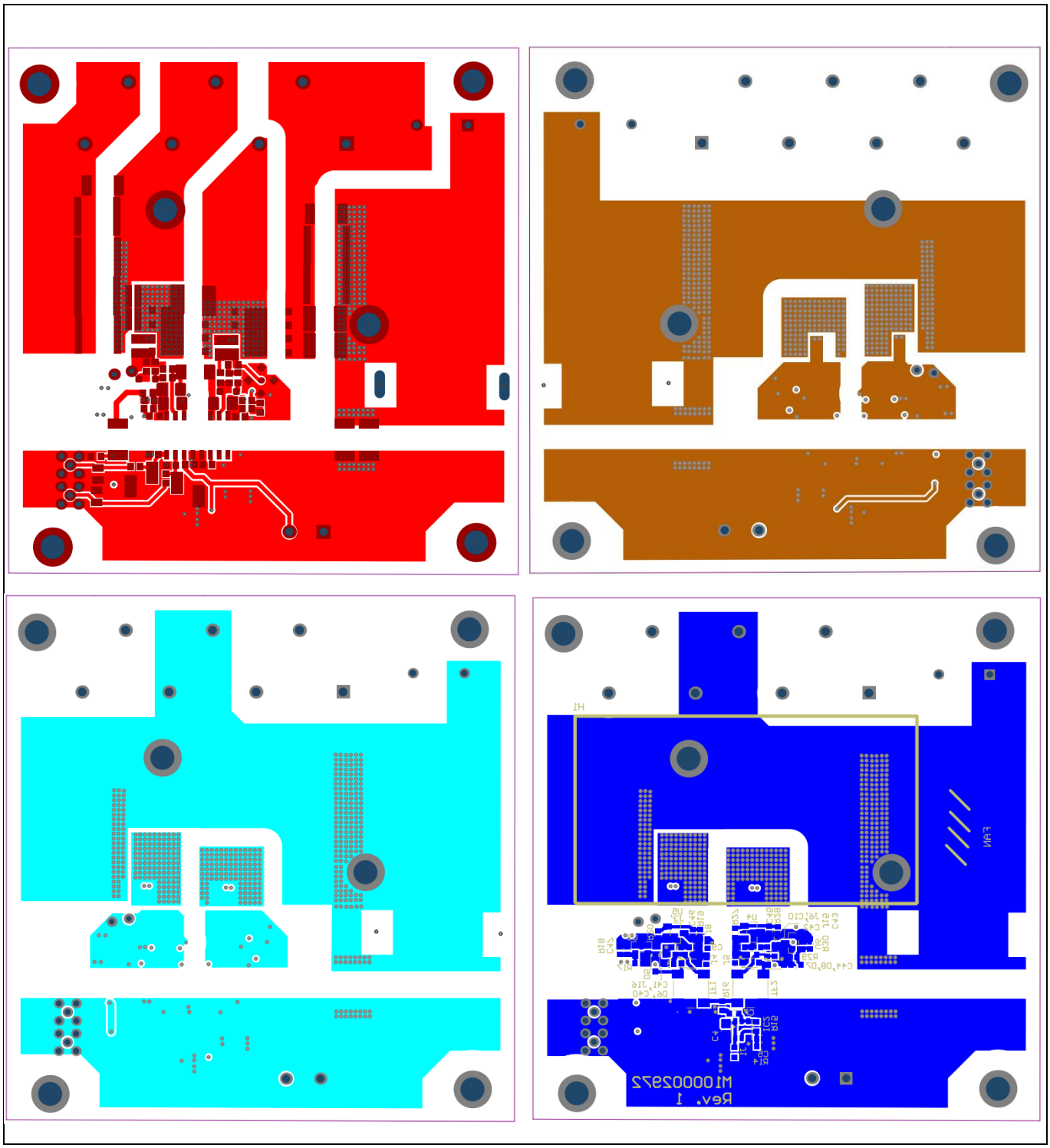

Figure 29 **Layout of EVAL_2EDB_HB_GaN evaluation board: top layer (in red), mid-layer1 (in brown), mid-layer2 (in cyan), bottom layer (in blue)**

8 References

[1] B. Zojer, “Driving 600 V CoolGaN™ high electron mobility transistors,” Infineon Technologies AG, Application Note **AN_201702_PL52_012**, 2018

[2] Infineon Technologies AG, “GaN EiceDRIVER™ single-channel isolated gate driver ICs for high voltage GaN HEMTs,” 2019. [Online]. **Available online**.

[3] Eric Persson, Yalcin Haksoz, “600 V CoolGaN™ half-bridge evaluation platform featuring GaN EiceDRIVER™,” Infineon Technologies AG, Application Note **AN_1811_PL52_1811_234307**, 2019

[4] Carmen Menditti Matrisciano, “KIT_1EDB_AUX_GaN”, Infineon Technologies AG, upcoming Application Note, 2022

[5] E. Persson, “CoolGaN™ application note,” Infineon Technologies AG, Application Note **AN_201702_PL52_010**, 2018

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[7] D. Varajao, T. Ferianz, V. Zhang, and C. Matrisciano, “Driving GaN HEMT High-Voltage Half-Bridge with a Single-Channel Non-Isolated Gate Driver with Truly Differential Inputs,” PCIM Europe 2020; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management, Nuremberg, Germany, 2020, pp. 1-8.

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