

# ESDF200-B1-W0201

Bi-directional ESD protection and EMI filter device, 3.3 V, 65 pF

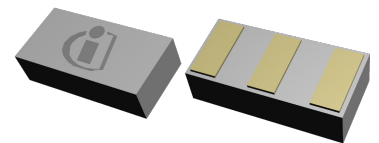


## Product description

This Infineon ESD (electrostatic discharge) protection and EMI (electromagnetic interference) low pass filtering device has a bi-directional and symmetric  $I/V$  characteristic and excellent clamping performance.

## Feature list

- ESD / transient protection according to:
  - IEC61000-4-2 (ESD):  $\pm 20$  kV (air) /  $\pm 20$  kV (contact)
  - IEC61000-4-4 (EFT):  $\pm 4$  kV /  $\pm 80$  A (5/50 ns)
  - IEC61000-4-5 (Surge):  $\pm 11$  A (8/20  $\mu$ s)
- Bi-directional maximum working voltage:  $V_{WM} = \pm 3.3$  V
- Line capacitance and line resistance:  $C_L = 65$  pF at  $f = 1$  MHz and  $R_L = 100 \Omega$
- Clamping voltage:  $V_{cl} = 5.4$  V at  $I_{TLP} = 16$  A with  $R_{dyn} = 0.05 \Omega$
- Very low leakage current:  $I_L = 1$  nA
- Small form factor SMD size 0201, low profile (0.73 x 0.28 x 0.15 mm<sup>3</sup>)



## Potential applications

- EMI sensitive lines in mobile devices (low speed data, audio, buttons, GPIO)

## Product validation

Qualified for industrial applications according to the relevant tests of JEDEC47/20/22.

## Device information

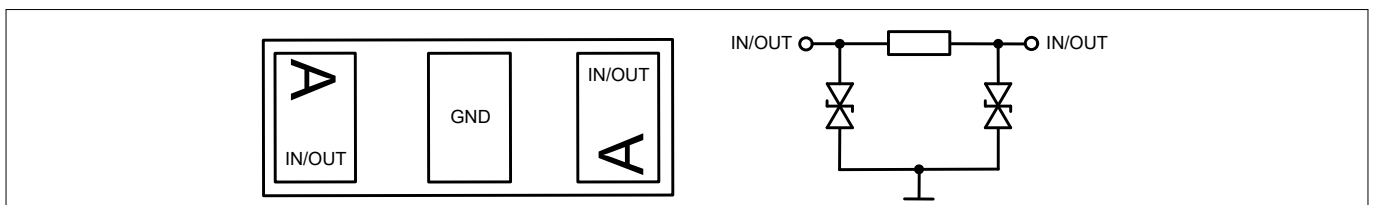


Figure 1 Pin configuration and schematic diagram

Table 1 Part information

Product name / Ordering code	Package	Pin configuration	Marking	Pieces / Reel
ESDF200-B1-W0201 / ESDF200B1W0201E6327XTSA1	WLL-3-2	1-line, bi-directional	A	15 k

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## 1 Absolute maximum ratings

### 1 Absolute maximum ratings

**Table 2** Absolute maximum ratings at  $T_A = 25^\circ\text{C}$ , unless otherwise specified

Parameter	Symbol	Values		Unit	Note or test condition
		Min.	Max.		
Working voltage	$V_{WM}$	-3.3	+3.3	V	
Working current	$I_{WM}$	-2	+2	mA	From IN to OUT
ESD discharge voltage	$V_{ESD}$ (contact)	-20	+20	kV	Discharge network: $R = 330 \Omega$ , $C = 150 \text{ pF}$ <sup>1)</sup>
	$V_{ESD}$ (air)	-20	+20		
Peak pulse power	$P_{PK}$	-	66	W	Stress pulse: 8/20 $\mu\text{s}$ current waveform <sup>2)</sup>
Peak pulse current	$I_{PP}$	-11	+11	A	
Operating temperature	$T_{op}$	-55	+125	$^\circ\text{C}$	
Storage temperature	$T_{stg}$	-65	+150		

**Attention:** *Stresses above the maximum values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings. Exceeding only one of these values may cause irreversible damage to the component.*

<sup>1)</sup> Based on IEC61000-4-2.

<sup>2)</sup> Based on IEC61000-4-5.

2 Electrical characteristics

2 Electrical characteristics

Note:  $T_A = 25^\circ\text{C}$ , unless otherwise specified. Device is electrically symmetrical.  
 All electrical parameters and all maximum ratings valid with middle pad (pin 2) connected to ground.

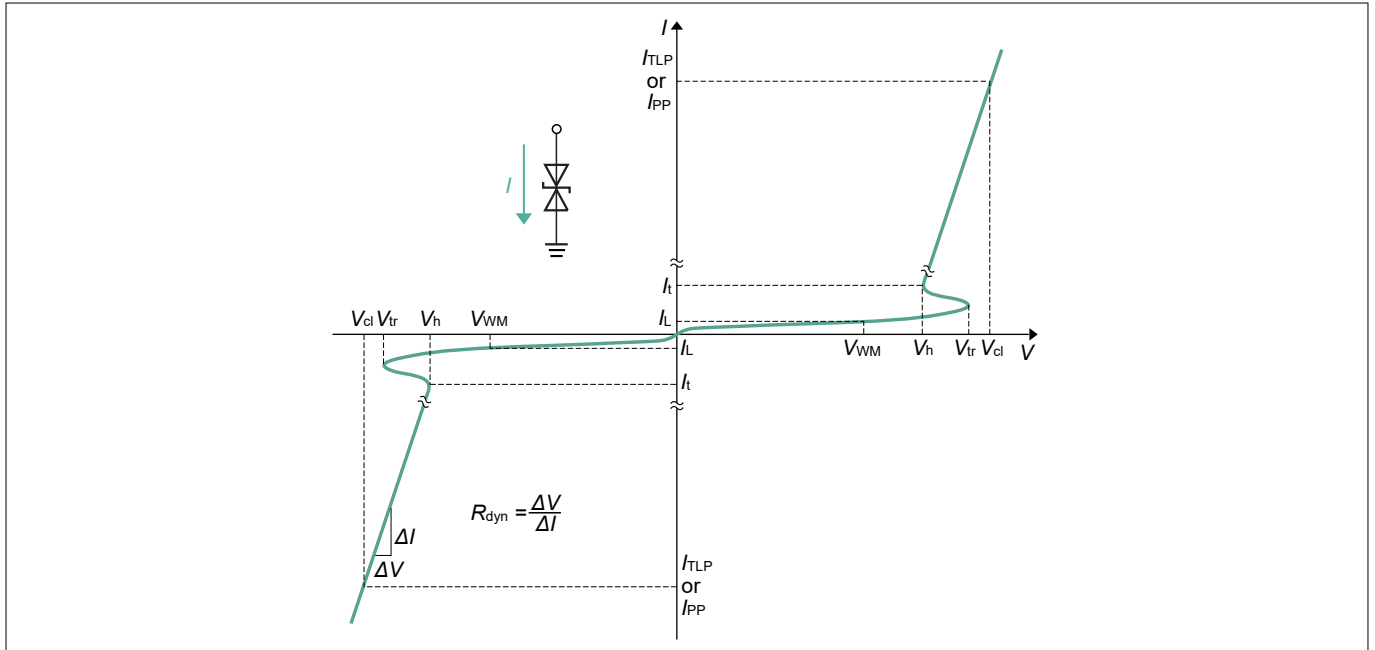


Figure 2 I/V characteristic curve

Table 3 I/V characteristic parameters

Symbol	Parameter
$I_h$	Holding current
$I_L$	Leakage current
$I_{PP}$	Peak pulse current, based on IEC61000-4-5
$I_t$	Test current
$I_{TLP}$	TLP current
$R_{dyn}$	Dynamic resistance
$V_{cl}$	Clamping voltage
$V_h$	Holding voltage
$V_t$	Test voltage
$V_{tr}$	Trigger voltage
$V_{WM}$	Maximum working voltage

## 2 Electrical characteristics

**Table 4 DC characteristics**

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
Trigger voltage <sup>3)</sup>	$V_{tr}$	–	6.5	–	V	
Holding voltage	$V_h$	4.9	6	7.2		$I_t = 1 \text{ mA}$
Leakage current	$I_L$	–	1	100	nA	$V_{WM} = 3.3 \text{ V}$
Line resistance	$R_L$	–	100	–	$\Omega$	

**Table 5 AC characteristics**

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
Line capacitance <sup>4)</sup>	$C_L$	–	65	–	pF	$V = 0 \text{ V}, f = 1 \text{ MHz}$
		–	52	–		$V = 3.3 \text{ V}, f = 1 \text{ MHz}$
Insertion loss <sup>5)</sup>	$S_{21}$	–	-6	–	dB	Pass band, $f < 10 \text{ MHz}$
		–	-23	–		Stop band, $f = 600 \text{ MHz}$
Series inductance	$L_S$	–	<0.1	–	nH	Extracted from S-parameters

**Table 6 Protection characteristics**

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
Clamping voltage (TLP) <sup>6) 7)</sup>	$V_{cl}$	–	4.9	–	V	$I_{TLP} = 4 \text{ A}$
		–	5.1	–		$I_{TLP} = 8 \text{ A}$
		–	5.4	–		$I_{TLP} = 16 \text{ A}$
		–	6.1	–		$I_{TLP} = 30 \text{ A}$
Clamping voltage (8/20 $\mu\text{s}$ ) <sup>8)</sup>		–	5.1	–		$I_{PP} = 6 \text{ A}$
		–	5.6	–		$I_{PP} = 9 \text{ A}$
		–	6	–		$I_{PP} = 11 \text{ A}$
Dynamic resistance <sup>6)</sup>	$R_{dyn}$	–	0.05	–	$\Omega$	

<sup>3)</sup> Verified by design.

<sup>4)</sup> IN and OUT in parallel versus ground

<sup>5)</sup>  $Z_0 = 50 \Omega$

<sup>6)</sup> TLP parameters:  $Z_0 = 50 \Omega$ ,  $t_p = 100 \text{ ns}$ ,  $t_r = 0.6 \text{ ns}$ , averaging window 30-60 ns.

<sup>7)</sup> Refer to application note AN210. [2]

<sup>8)</sup>  $t_p = 8/20 \mu\text{s}$ . Stress pulse based on IEC61000-4-5.

3 Typical characteristic diagrams

### 3 Typical characteristic diagrams

Note:  $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise specified.

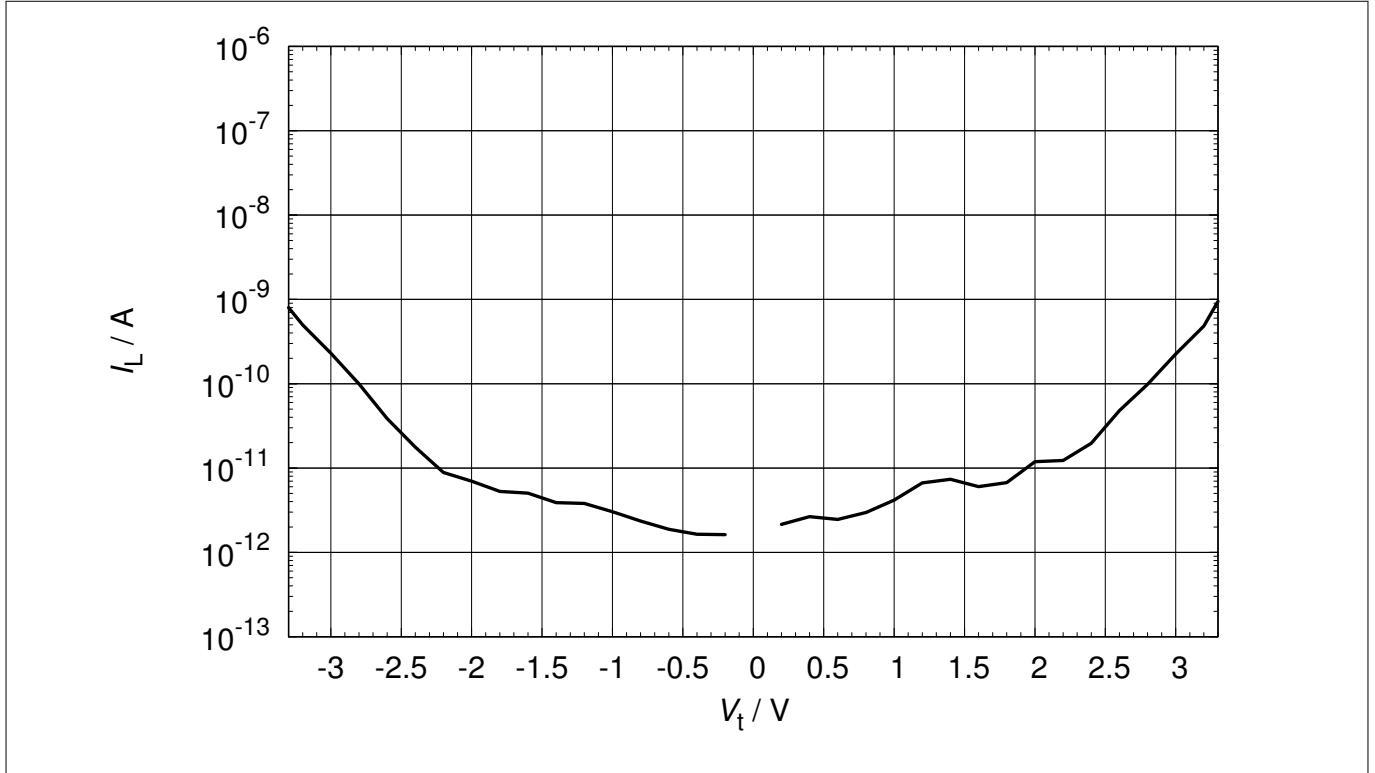


Figure 3 Leakage current:  $I_L = f(V_t)$

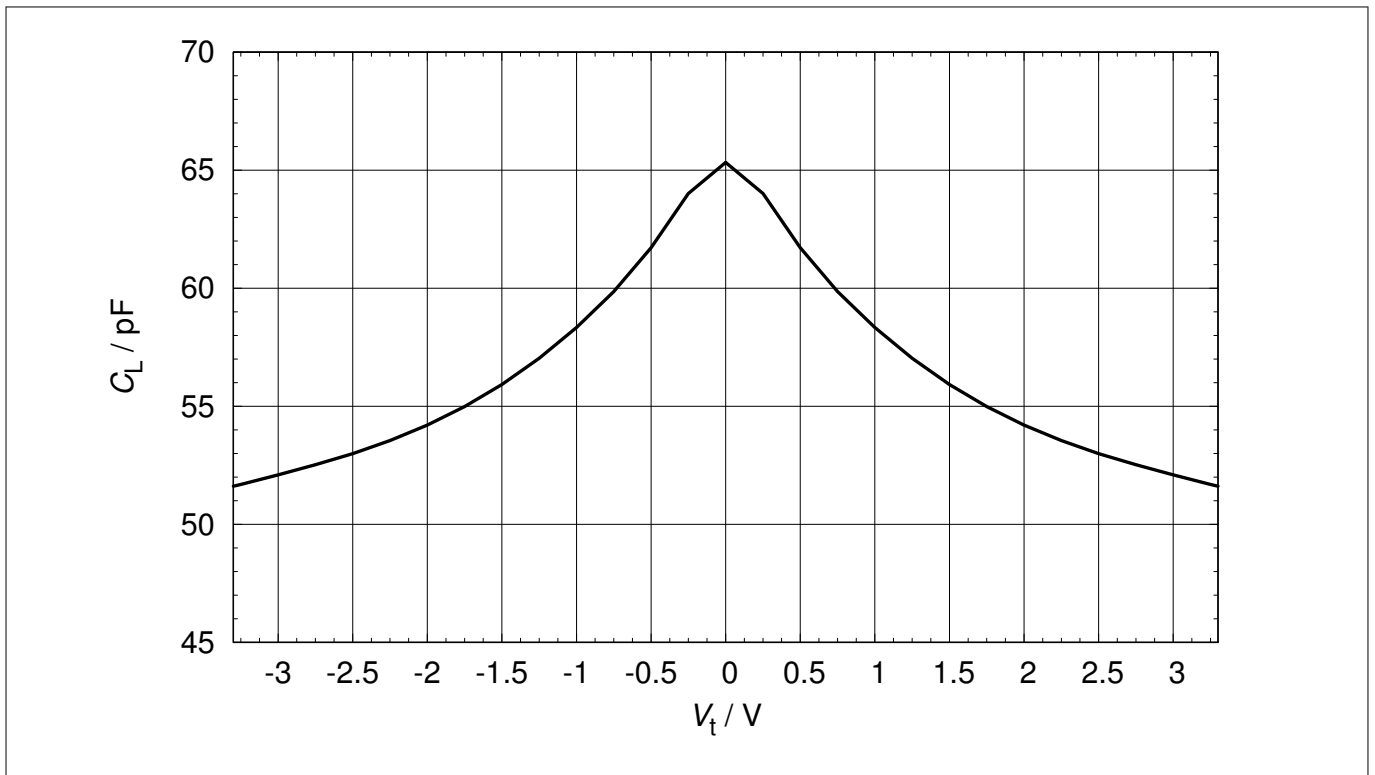


Figure 4 Line capacitance:  $C_L = f(V_t)$ ,  $f = 1\text{ MHz}$

3 Typical characteristic diagrams

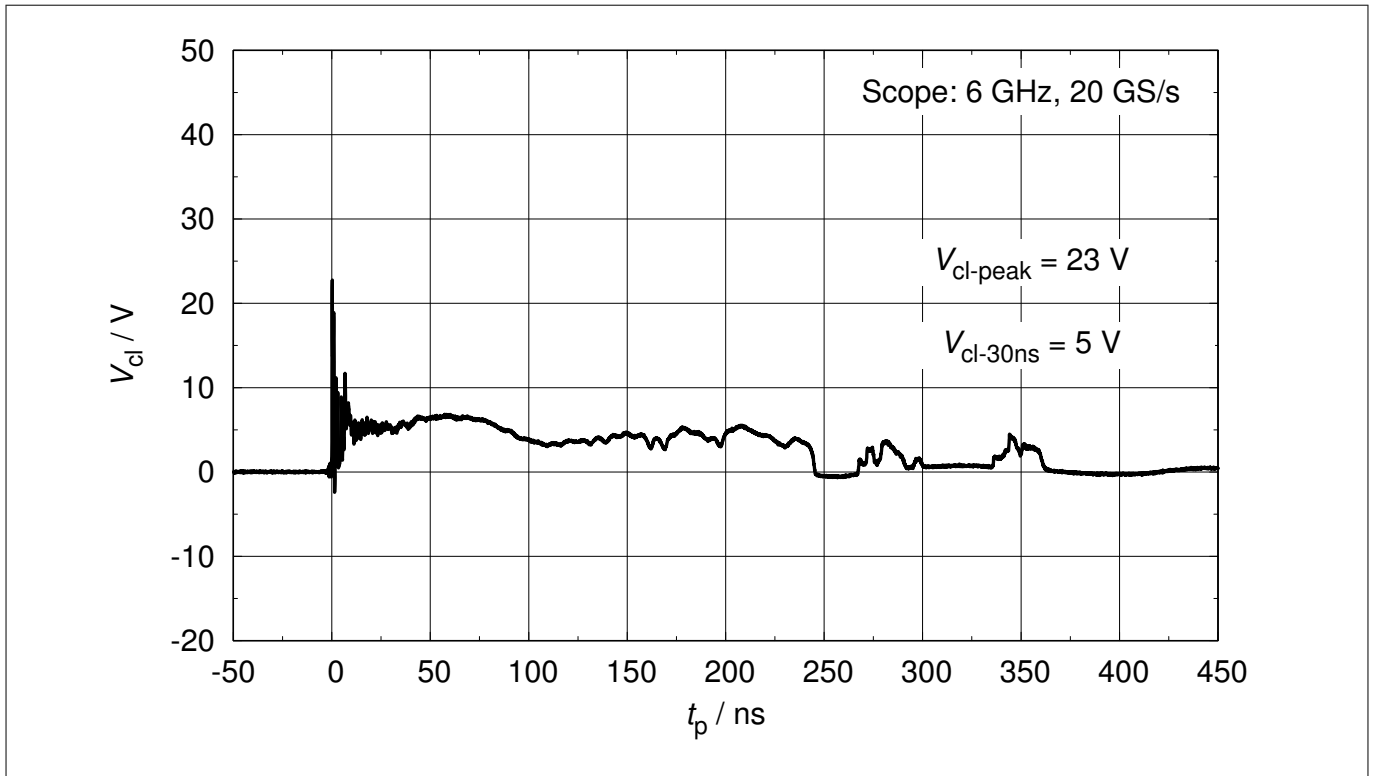


Figure 5 Clamping voltage (ESD):  $V_{cl} = f(t_p)$ , 8 kV positive pulse based on IEC61000-4-2

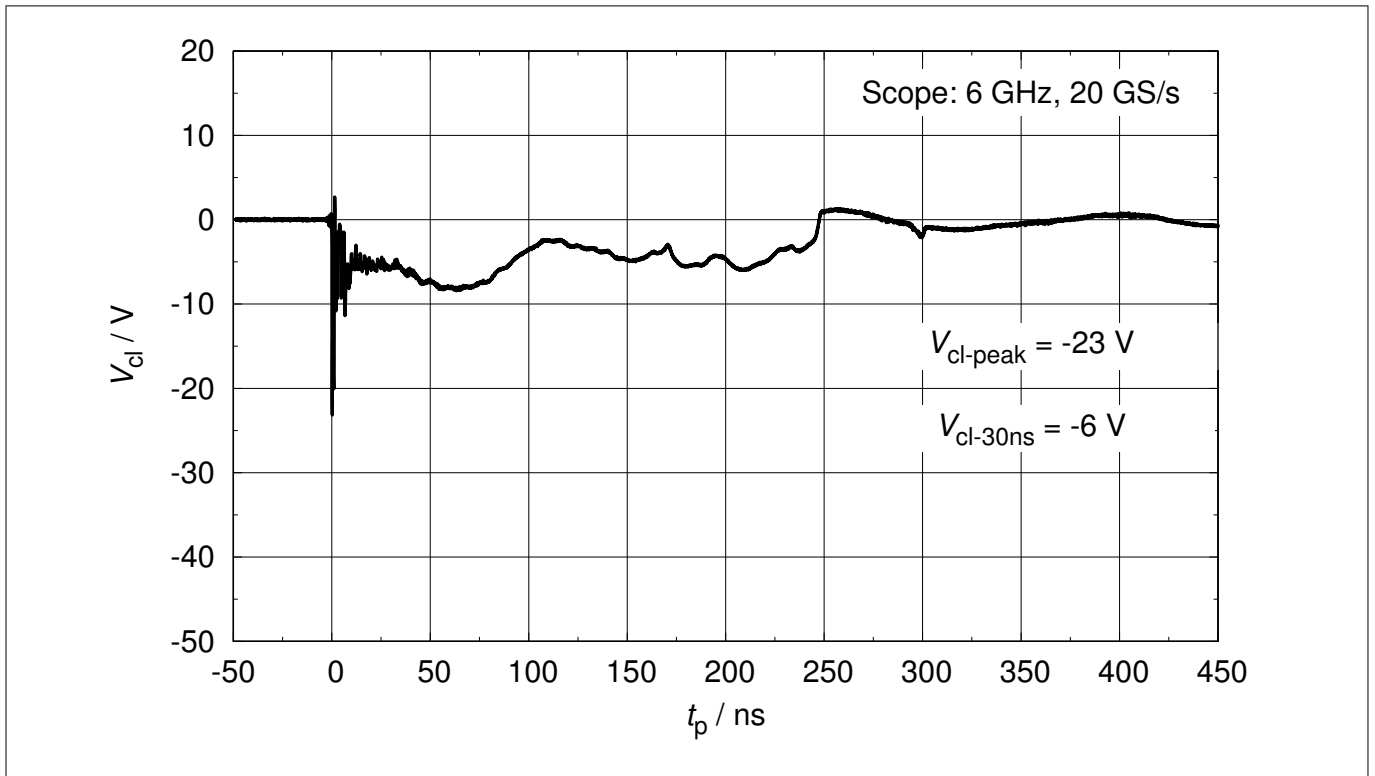


Figure 6 Clamping voltage (ESD):  $V_{cl} = f(t_p)$ , 8 kV negative pulse based on IEC61000-4-2

3 Typical characteristic diagrams

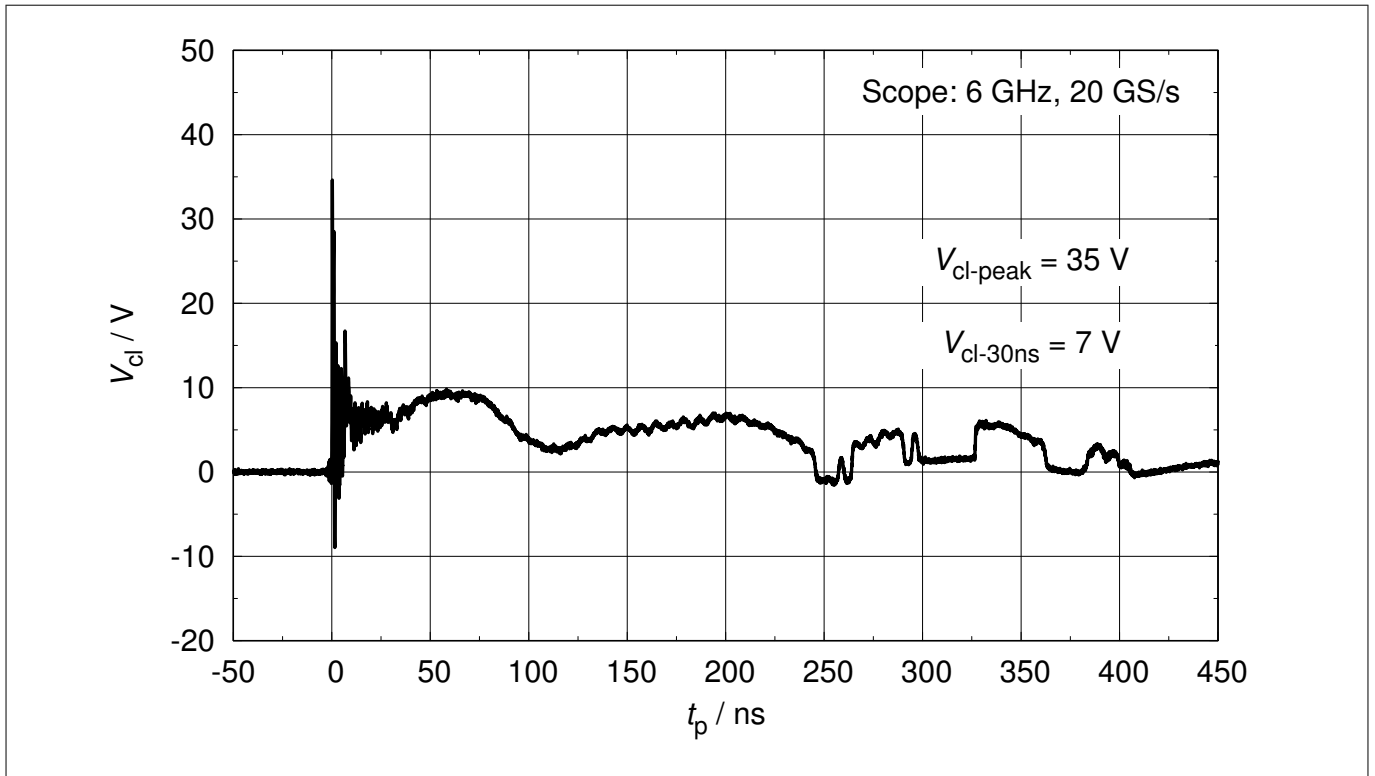


Figure 7 Clamping voltage (ESD):  $V_{cl} = f(t_p)$ , 15 kV positive pulse based on IEC61000-4-2

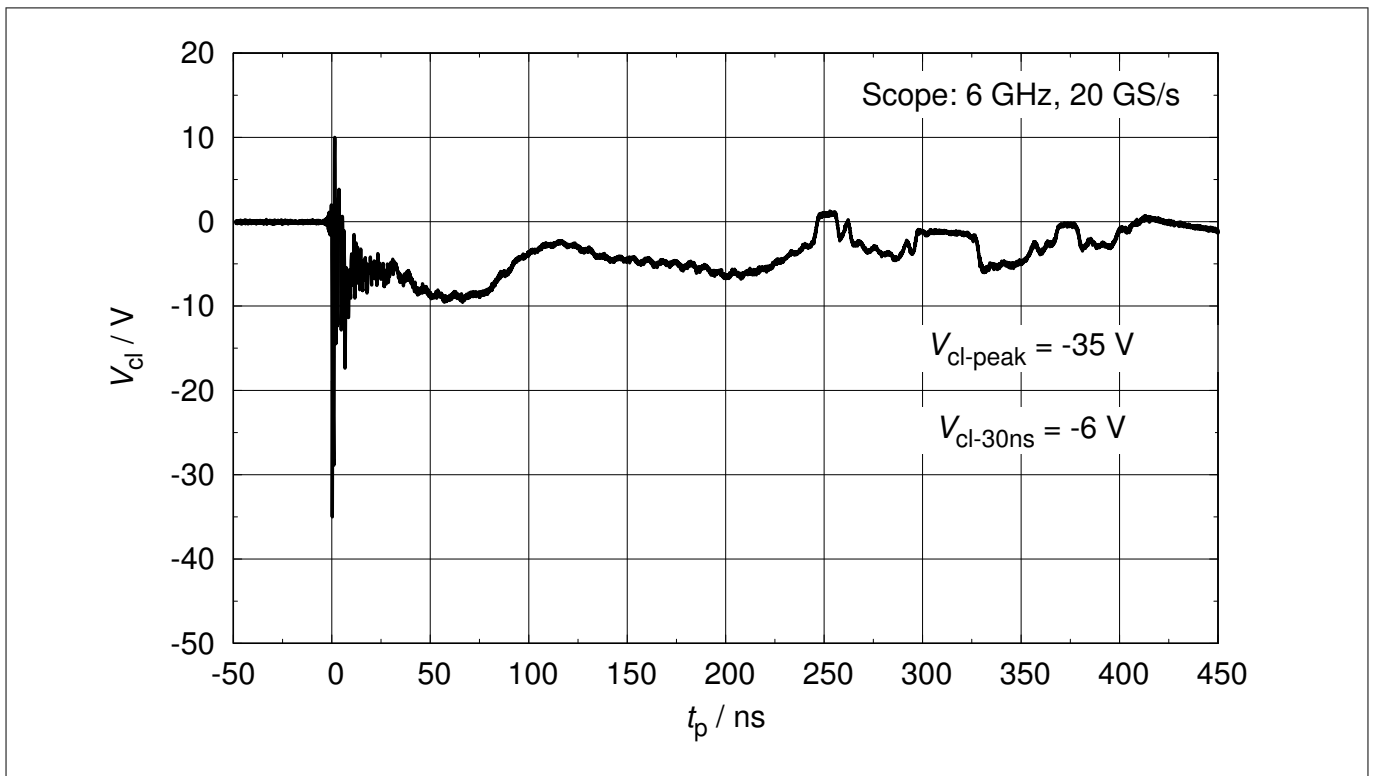


Figure 8 Clamping voltage (ESD):  $V_{cl} = f(t_p)$ , 15 kV negative pulse based on IEC61000-4-2



3 Typical characteristic diagrams

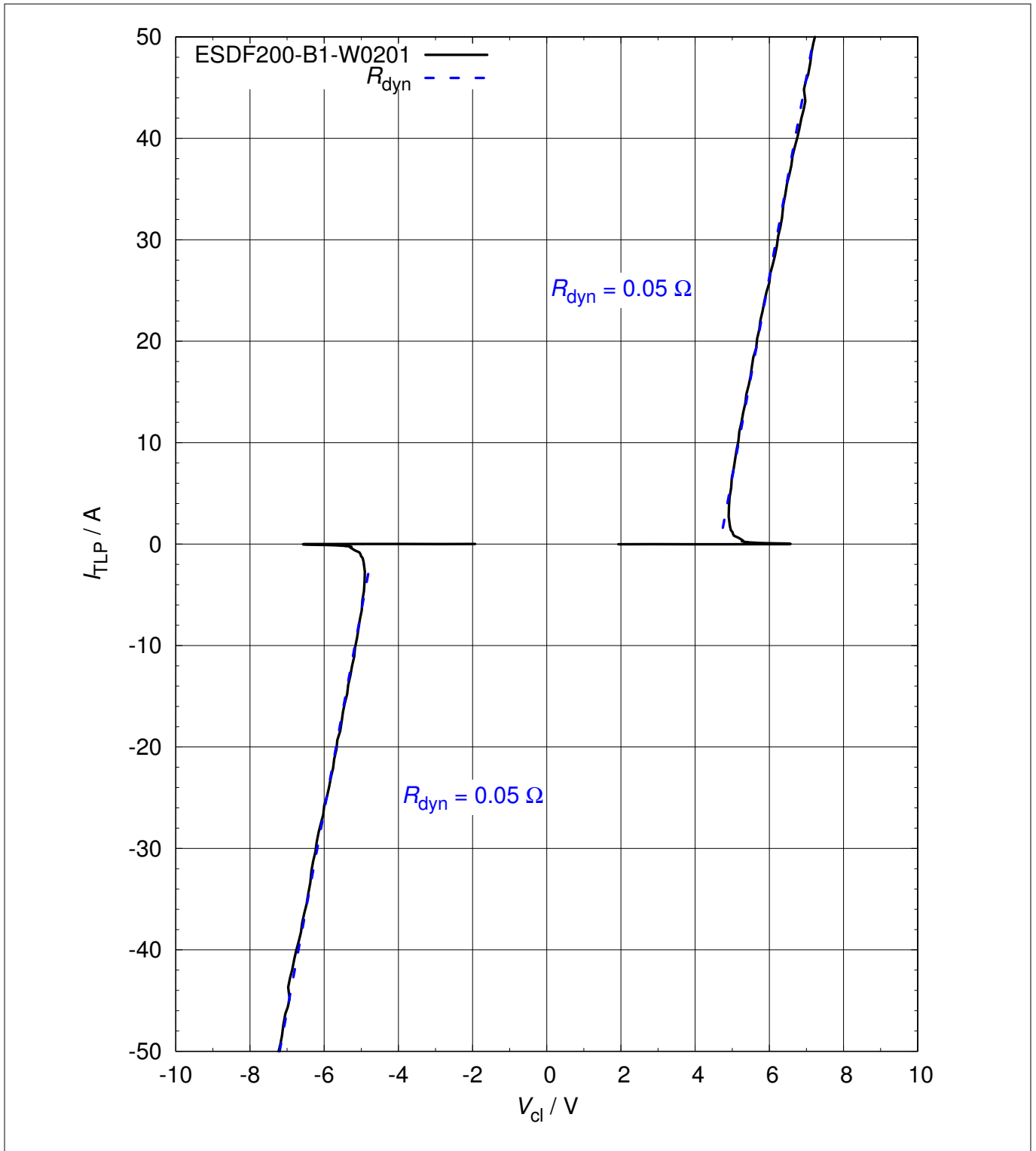


Figure 9 Clamping voltage (TLP):  $I_{TLP} = f(V_{cl})$

3 Typical characteristic diagrams

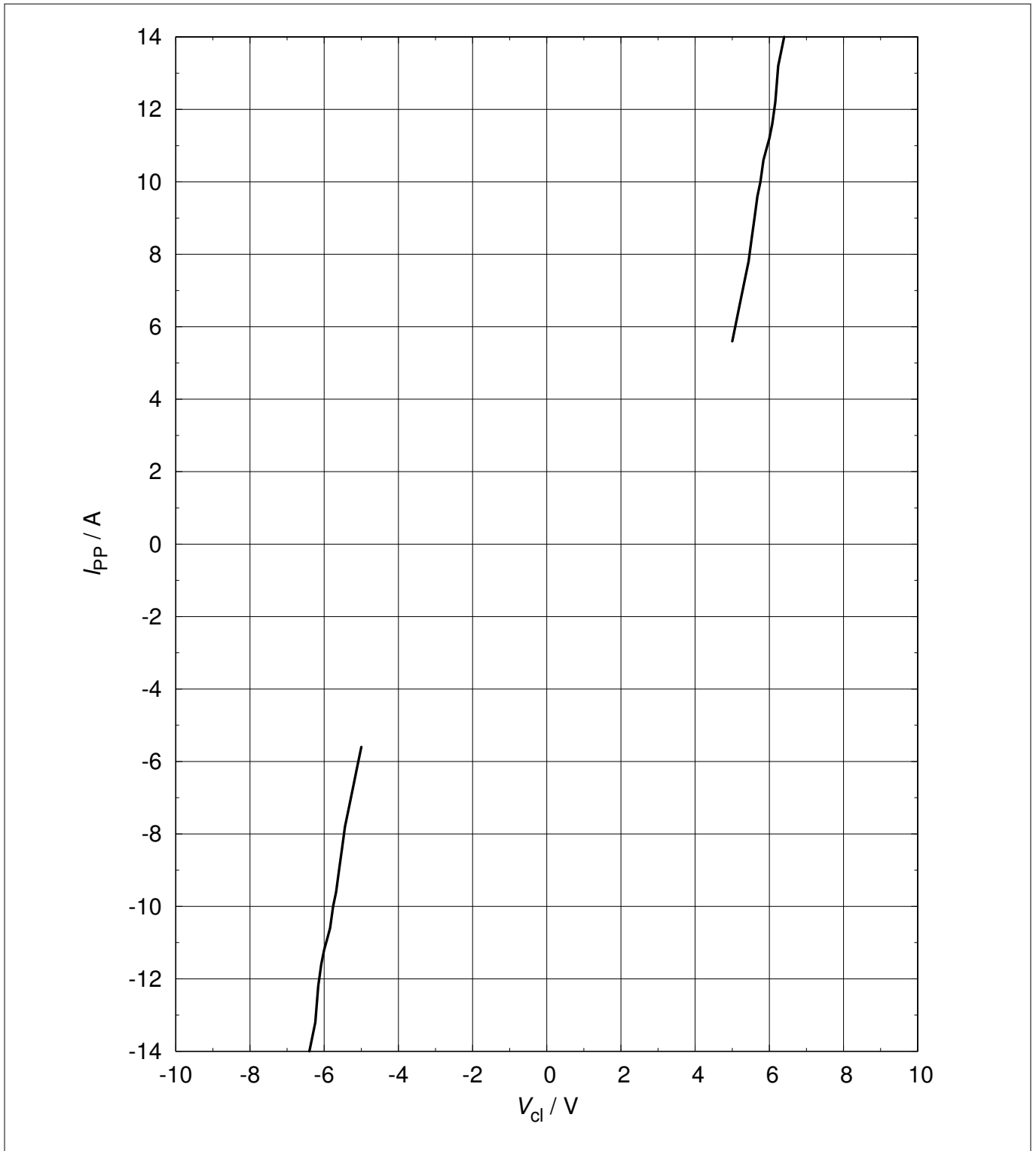
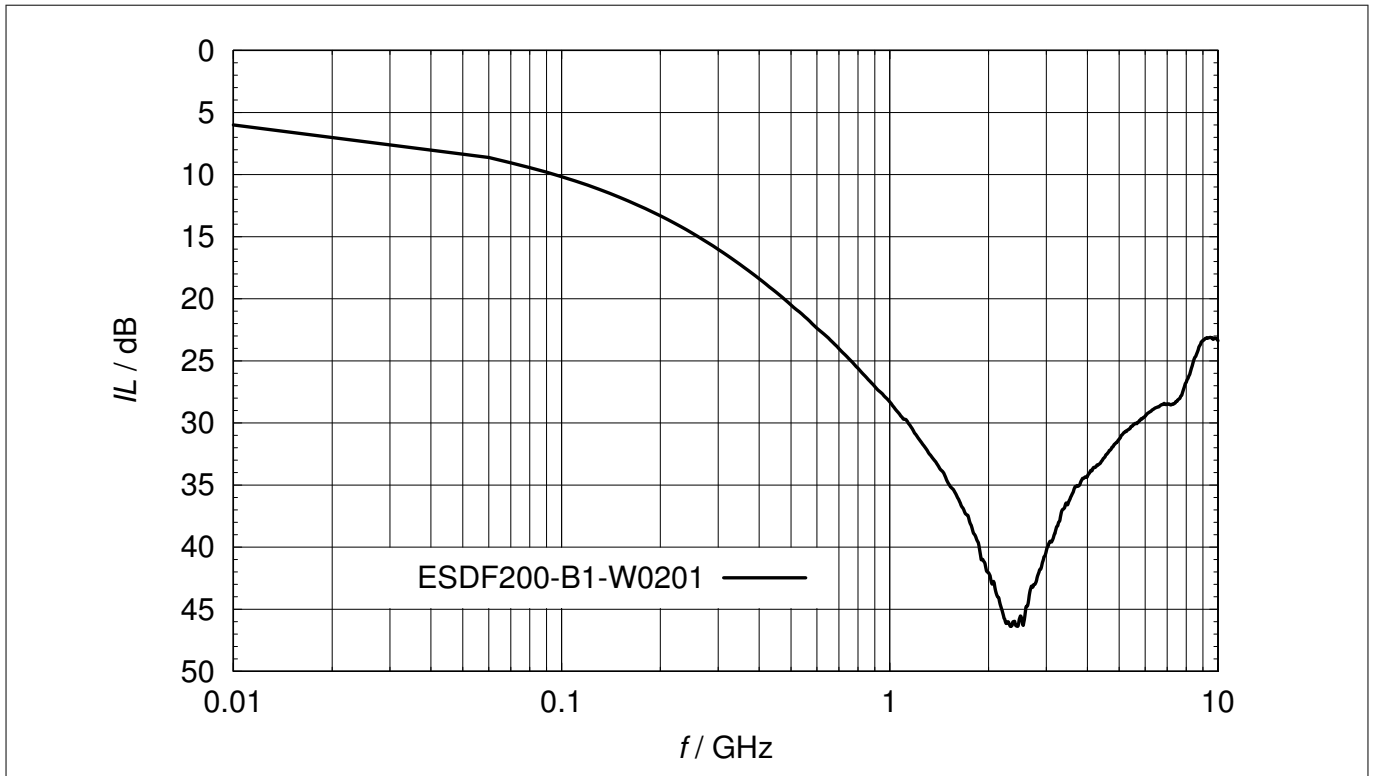


Figure 10 Clamping voltage (Surge):  $I_{PP} = f(V_{cl})$ , based on IEC61000-4-5

**3 Typical characteristic diagrams**



**Figure 11** Insertion loss  $IL = f(f)$ , measured in a 50  $\Omega$  system

4 Package information WLL-3-2

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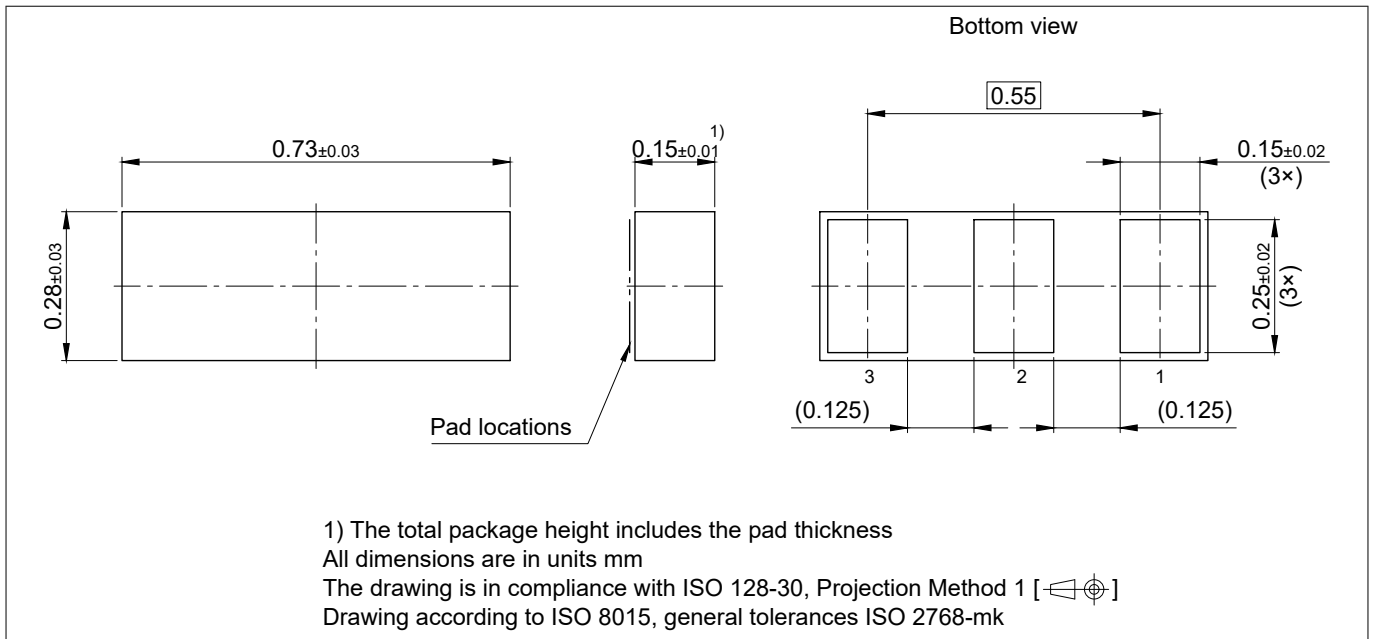


Figure 12 WLL-3-2 package

Note: For package information including footprint, packing and assembly recommendation refer to:

<https://www.infineon.com/cms/en/product/packages/SG-WLL/SG-WLL-3-2/>

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**5 References****5 References**

[1]	Infineon AG - Understanding ESD protection device characteristics
[2]	Infineon AG - <b>Application note AN210</b> : Effective ESD Protection Design at System Level Using VF-TLP Characterization Methodology

**6 Revision history**

Document version	Date of release	Description of changes
v1.0	2020-06-07	<ul style="list-style-type: none"><li>First final datasheet version</li></ul>

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