ESD5V5U5ULC

Ultra-low capacitance ESD / transient / surge protection array

TVS (transient voltage suppressor)
5.5 V, 0.45 pF, RoHS compliant

Feature list

- ESD/transient protection of high speed data lines exceeding:
  - IEC61000-4-2 (ESD): ±25 kV (air/contact)
  - IEC61000-4-4 (EFT): ±2.5 kV/±50 A (5/50 ns)
  - IEC61000-4-5 (Surge): ±6 A (8/20 μs)
- Maximum working voltage: $V_{RWM} = 5.5$ V
- Extremely low capacitance: $C_L = 0.45$ pF I/O to GND (typical)
- Very low dynamic resistance: $R_{DYN} = 0.2$ Ω (typical) I/O to GND
- Very low reverse clamping voltage: $V_{CL} = 9$ V (typical) at $I_{PP} = 16$ A
- Protection of $V_{BUS}$ with one line freely selectable

Potential applications

- Protection of all I/O and $V_{BUS}$ lines in dual USB2.0 ports
- 10/100/1000 Ethernet
- DVI, HDMI, FireWire

Product validation

Qualified for industrial applications according to the relevant tests of JEDEC47/20/22

Device information

Table 1 Part information

<table>
<thead>
<tr>
<th>Type</th>
<th>Package</th>
<th>Configuration</th>
<th>Marking code</th>
</tr>
</thead>
<tbody>
<tr>
<td>ESD5V5U5ULC</td>
<td>PG-SC74-6-2</td>
<td>5 lines, uni-directional</td>
<td>20</td>
</tr>
</tbody>
</table>

Figure 1 Pin configuration and schematic diagram

Datasheet Please read the Important Notice and Warnings at the end of this document Revision 1.5
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Maximum ratings

1 Maximum ratings

Note: $T_A = 25$ °C, unless otherwise specified.

Table 2 Maximum ratings

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Values</th>
<th>Unit</th>
<th>Note or test condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>ESD contact discharge $^1$</td>
<td>$V_{ESD}$</td>
<td>±25</td>
<td>kV</td>
<td></td>
</tr>
<tr>
<td>Peak pulse current $^2$</td>
<td>$I_{pp}$</td>
<td>±6</td>
<td>A</td>
<td>$t_p = 8/20$ µs</td>
</tr>
<tr>
<td>Operating temperature range</td>
<td>$T_{OP}$</td>
<td>-40 to 125</td>
<td>°C</td>
<td></td>
</tr>
<tr>
<td>Storage temperature</td>
<td>$T_{stg}$</td>
<td>-65 to 150</td>
<td>°C</td>
<td></td>
</tr>
</tbody>
</table>

Attention: Stresses above the maximum values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings. Exceeding only one of these values may cause irreversible damage to the component.

$^1$ $V_{ESD}$ according to IEC61000-4-2

$^2$ $I_{pp}$ according to IEC61000-4-5
2 Electrical characteristics

Note: $T_A = 25 \, ^\circ\text{C}$, unless otherwise specified.

![Diode_Characteristic_Curve_with_snapback_Uni-directional.svg](Diode_Characteristic_Curve_with_snapback_Uni-directional.svg)

**Figure 2** Definitions of electrical characteristics

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Values</th>
<th>Unit</th>
<th>Note or test condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>Reverse working voltage</td>
<td>$V_{RWM}$</td>
<td>–</td>
<td>5.5</td>
<td>V</td>
</tr>
<tr>
<td>Reverse current</td>
<td>$I_R$</td>
<td>–</td>
<td>&lt;1</td>
<td>100</td>
</tr>
</tbody>
</table>

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## Electrical characteristics

### Table 4  RF characteristics

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Values</th>
<th>Unit</th>
<th>Note or test condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>Line capacitance</td>
<td>$C_L$</td>
<td></td>
<td>pF</td>
<td>$V_R = 0 , V, , f = 1 , MHz, , I/O , \rightarrow , GND$</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0.45</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>0.23</td>
<td>0.5</td>
<td></td>
</tr>
<tr>
<td>Line capacitance</td>
<td>$C_L$</td>
<td></td>
<td>pF</td>
<td>$V_R = 0 , V, , f = 825 , MHz, , I/O , \rightarrow , I/O$</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0.25</td>
<td>–</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>0.13</td>
<td>–</td>
<td></td>
</tr>
<tr>
<td>Capacitance variation between I/O and GND</td>
<td>$\Delta C_{i/o-GND}$</td>
<td>–</td>
<td>0.02</td>
<td>$V_R = 0 , V, , f = 1 , MHz, , I/O , \rightarrow , GND$</td>
</tr>
<tr>
<td>Capacitance variation between I/O</td>
<td>$\Delta C_{i/o-i/o}$</td>
<td>–</td>
<td>0.01</td>
<td>$V_R = 0 , V, , f = 1 , MHz, , I/O , \rightarrow , I/O$</td>
</tr>
</tbody>
</table>

### Table 5  ESD and surge characteristics

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Values</th>
<th>Unit</th>
<th>Note or test condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>Reverse clamping voltage $^1$</td>
<td>$V_{CL}$</td>
<td>–</td>
<td>V</td>
<td>$I_{pp} = 1 , A, , t_p = 8/20 , \mu s, , I/O , \rightarrow , GND$</td>
</tr>
<tr>
<td></td>
<td></td>
<td>9</td>
<td>–</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>12</td>
<td>–</td>
<td></td>
</tr>
<tr>
<td>Reverse clamping voltage $^1$</td>
<td>$V_{CL}$</td>
<td>–</td>
<td>V</td>
<td>$I_{pp} = 3 , A, , t_p = 8/20 , \mu s, , I/O , \rightarrow , GND$</td>
</tr>
<tr>
<td></td>
<td></td>
<td>8.9</td>
<td>–</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>11.5</td>
<td>–</td>
<td></td>
</tr>
<tr>
<td>Forward clamping voltage $^2$</td>
<td>$V_{FC}$</td>
<td>–</td>
<td>V</td>
<td>$I_{pp} = 1 , A, , t_p = 8/20 , \mu s, , GND , \rightarrow , I/O$</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1.75</td>
<td>–</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>2.5</td>
<td>–</td>
<td></td>
</tr>
<tr>
<td>Forward clamping voltage $^2$</td>
<td>$V_{FC}$</td>
<td>–</td>
<td>V</td>
<td>$I_{pp} = 3 , A, , t_p = 8/20 , \mu s, , GND , \rightarrow , I/O$</td>
</tr>
<tr>
<td></td>
<td></td>
<td>5.4</td>
<td>–</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>9.2</td>
<td>–</td>
<td></td>
</tr>
<tr>
<td>Dynamic resistance $^2$</td>
<td>$R_{DYN}$</td>
<td>–</td>
<td>$\Omega$</td>
<td>$I/O , \rightarrow , GND$</td>
</tr>
<tr>
<td>Dynamic resistance $^2$</td>
<td>$R_{DYN}$</td>
<td>–</td>
<td>$\Omega$</td>
<td>$GND , \rightarrow , I/O$</td>
</tr>
</tbody>
</table>

---

1  $I_{pp}$ according to IEC61000-4-5
2  Please refer to application note AN210, TLP parameters: $Z_0 = 50 \, \Omega$, $t_p = 100 \, \mu s$, $t_r = 300 \, ps$, averaging window: $t_1 = 30 \, ns$ to $t_2 = 60 \, ns$, extraction of dynamic resistance using least squares fit of TLP characteristic between $I_{pp1} = 10 \, A$ and $I_{pp2} = 40 \, A$.  

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3 Typical characteristic diagrams

Note: \( T_A = 25 \, ^\circ C, \) unless otherwise specified.

Figure 3 Line capacitance \( C_L = f(V_R) \) at \( f = 825 \, MHz \)

Figure 4 Line capacitance \( C_L = f(f) \), \( V_R = 0 \, V \)
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Typical characteristic diagrams

Figure 5  Insertion loss $I_L = f(f), \ V_R = 0 \ \text{V}$

Figure 6  Forward characteristic, $I_F = f(V_F), \ \text{current forced}$
Figure 7 Reverse current $I_R = f(T_A)$, $V_R = 5.5$ V (typical)

Figure 8 Reverse characteristic, $I_R = (V_R)$, voltage forced
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Typical characteristic diagrams

Figure 9  TLP characteristic I/O to GND

![Figure 9 TLP characteristic I/O to GND](image)

Figure 10  TLP characteristic GND to I/O

![Figure 10 TLP characteristic GND to I/O](image)

1) TLP parameter: \( Z_0 = 50 \, \Omega \), \( t_p = 100 \, \text{ns} \), \( t_r = 300 \, \text{ps} \), averaging window: \( t_1 = 30 \, \text{ns} \) to \( t_2 = 60 \, \text{ns} \), extraction of dynamic resistance using least squares fit of TLP characteristic between \( I_{PP1} = 10 \, \text{A} \) and \( I_{PP2} = 40 \, \text{A} \). The equivalent stress level \( V_{IEC} \) according IEC61000-4-2 \( (R = 330 \, \Omega , C = 150 \, \text{pF}) \) is calculated at the broad peak of the IEC waveform at \( t = 30 \, \text{ns} \) with \( 2 \, \text{A/kV} \).
4 Application information

**Figure 11** Ethernet

**Figure 12** USB2.0
5 Package information

Note: Dimensions in mm.

5.1 PG-SC74-6-2 package

Figure 13 PG-SC74-6-2 package overview

Figure 14 PG-SC74-6-2 footprint

Figure 15 PG-SC74-6-2 packing

Figure 16 PG-SC74-6-2 marking example (see Device information)
References

[1] Infineon AG - Application Note AN210: Effective ESD protection design at system level using VF-TLP characterization methodology

Revision history

Revision history: Rev. 1.4. 2016-04-21

Page or Item | Subjects (major changes since previous revision)
--- | ---
Revision 1.5, 2018-06-12 | Data sheet layout changed, references updated, ordering information scheme deleted
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