ESD3V3U4ULC
Ultra-low Capacitance ESD / Transient Protection Array

ESD3V3U4ULC
1 Ultra-low Capacitance ESD / Transient Protection Array

1.1 Features

- ESD / transient protection of high speed data lines exceeding:
  - IEC61000-4-2 (ESD): ±20 kV (air/contact)
  - IEC61000-4-4 (EFT): ±2.5 kV (5/50ns)
  - IEC61000-4-5 (Surge): ±3 A (8/20 μs)
- Maximum working voltage: \( V_{RWM} = 3.3 \text{ V} \)
- Ultra low capacitance \( C_L = 0.4 \text{ pF} \) I/O to GND (typical)
- Very low clamping voltage: \( V_{CL} = 8 \text{ V} \) (typical) at \( I_{PP} = 16 \text{ A} \)
- Very low dynamic resistance: \( R_{DYN} = 0.19 \text{ Ω} \) (typical)
- TSLP-9-1 package with pad pitch 0.5 mm, optimized pad design to simplify PCB layout
- Pb-free and halogen free package (RoHS compliant)

1.2 Application Examples

- USB 3.0, 10/100/1000 Ethernet, Firewire
- DVI, HDMI, S-ATA, DisplayPort
- Mobile HDMI Link, MDDI, MIPI, etc.

1.3 Product Description

![Pin Configuration and Schematic Diagram](PG-TSLP-9-1_PinConf_and_SchematicDiag.png)

Figure 1 Pin Configuration and Schematic Diagram

<table>
<thead>
<tr>
<th>Table 1</th>
<th>Ordering Information</th>
</tr>
</thead>
<tbody>
<tr>
<td>Type</td>
<td>Package</td>
</tr>
<tr>
<td>ESD3V3U4ULC</td>
<td>TSLP-9-1</td>
</tr>
</tbody>
</table>
2 Characteristics

Table 2 Maximum Rating at $T_A = 25 \, ^\circ\mathrm{C}$, unless otherwise specified

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Values</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>ESD contact discharge$^{1)}$</td>
<td>$V_{ESD}$</td>
<td>-20 – 20</td>
<td>kV</td>
</tr>
<tr>
<td>Peak pulse current ($t_p = 8/20 , \mu\text{s})$</td>
<td>$I_{PP}$</td>
<td>-3 – 3</td>
<td>A</td>
</tr>
<tr>
<td>Operating temperature</td>
<td>$T_{OP}$</td>
<td>-40 – 125</td>
<td>°C</td>
</tr>
<tr>
<td>Storage temperature</td>
<td>$T_{stg}$</td>
<td>-65 – 150</td>
<td>°C</td>
</tr>
</tbody>
</table>

1) $V_{ESD}$ according to IEC61000-4-2
2) $I_{PP}$ according to IEC61000-4-5

2.1 Electrical Characteristics at $T_A = 25 \, ^\circ\mathrm{C}$, unless otherwise specified

![Figure 2 Definitions of electrical characteristics](image-url)
### Table 3  DC Characteristics at $T_A = 25 \, ^\circ\text{C}$, unless otherwise specified

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Values</th>
<th>Unit</th>
<th>Note / Test Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>Reverse working voltage$^1$</td>
<td>$V_{RWM}$</td>
<td>–</td>
<td>3.3</td>
<td>V I/O to GND</td>
</tr>
<tr>
<td>Reverse current$^1$</td>
<td>$I_R$</td>
<td>1</td>
<td>50</td>
<td>nA I/O to GND, $V_R = 3.3 , \text{V}$</td>
</tr>
<tr>
<td>Breakdown voltage$^1$</td>
<td>$V_{BR}$</td>
<td>6.2</td>
<td>–</td>
<td>V I/O to GND</td>
</tr>
<tr>
<td>Reverse trigger voltage$^2$</td>
<td>$V_{t1}$</td>
<td>6.2</td>
<td>–</td>
<td>V I/O to GND</td>
</tr>
<tr>
<td>Reverse holding voltage$^2$</td>
<td>$V_h$</td>
<td>3.35</td>
<td>4</td>
<td>4.4 V I/O to GND, $I_R = 10 , \text{mA}$</td>
</tr>
</tbody>
</table>

$^1$ Voltage forced
$^2$ Current forced

### Table 4  RF Characteristics at $T_A = 25 \, ^\circ\text{C}$, unless otherwise specified

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Values</th>
<th>Unit</th>
<th>Note / Test Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>Line capacitance$^1$</td>
<td>$C_L$</td>
<td>–</td>
<td>0.65</td>
<td>pF $V_R = 0 , \text{V}, f = 1 , \text{MHz}$, I/O to GND</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0.2</td>
<td>0.35</td>
<td>pF $V_R = 0 , \text{V}, f = 1 , \text{MHz}$, I/O to I/O</td>
</tr>
<tr>
<td>Channel capacitance matching between I/O to GND</td>
<td>$\Delta C_{i/o-GND}$</td>
<td>0.035</td>
<td>–</td>
<td>pF $V_R = 0 , \text{V}, f = 1 , \text{MHz}$, I/O to GND</td>
</tr>
<tr>
<td>Channel capacitance matching between I/O to I/O</td>
<td>$\Delta C_{i/o-i/o}$</td>
<td>0.017</td>
<td>–</td>
<td>pF $V_R = 0 , \text{V}, f = 1 , \text{MHz}$, I/O to I/O</td>
</tr>
</tbody>
</table>

$^1$ Total capacitance line to ground
Table 5  ESD Characteristics at $T_A = 25^\circ$C, unless otherwise specified

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Values</th>
<th>Unit</th>
<th>Note / Test Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>Clamping voltage$^{1)}$</td>
<td>$V_{CL}$</td>
<td>$- 4.8$</td>
<td>$V$</td>
<td>$I_{pp} = 1$ A, $t_p = 8/20\mu$s from I/O to GND</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$- 6.2$</td>
<td></td>
<td>$I_{pp} = 3$ A, $t_p = 8/20\mu$s from I/O to GND</td>
</tr>
<tr>
<td>Clamping voltage$^{2)}$</td>
<td>$V_{CL}$</td>
<td>$- 8$</td>
<td></td>
<td>$I_{TLP} = 16$ A, from I/O to GND</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$- 11$</td>
<td></td>
<td>$I_{TLP} = 30$ A, from I/O to GND</td>
</tr>
<tr>
<td>Forward clamping voltage$^{1)}$</td>
<td>$V_{FC}$</td>
<td>$- 1.4$</td>
<td></td>
<td>$I_{pp} = 1$ A, $t_p = 8/20\mu$s from GND to I/O</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$- 2.3$</td>
<td></td>
<td>$I_{pp} = 3$ A, $t_p = 8/20\mu$s from GND to I/O</td>
</tr>
<tr>
<td>Forward clamping voltage$^{2)}$</td>
<td>$V_{FC}$</td>
<td>$- 6$</td>
<td></td>
<td>$I_{TLP} = 16$ A, from GND to I/O</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$- 9$</td>
<td></td>
<td>$I_{TLP} = 30$ A, from GND to I/O</td>
</tr>
<tr>
<td>Dynamic resistance$^{2)}$</td>
<td>$R_{DYN}$</td>
<td>$- 0.19$</td>
<td>$\Omega$</td>
<td>I/O to GND</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$- 0.23$</td>
<td>$\Omega$</td>
<td>GND to any I/O</td>
</tr>
</tbody>
</table>

1) $I_{pp}$ according to IEC61000-4-5

2) Please refer to Application Note AN210. TLP parameter: $Z_0 = 50$ Ω , $t_p = 100$ns, $t_i = 300$ps, averaging window: $t_1 = 30$ ns to $t_2 = 60$ ns, extraction of dynamic resistance using least squares fit of TLP characteristic between $I_{pp1} = 10$ A and $I_{pp2} = 40$ A [2].
3 **Typical Characteristics** at $T_A = 25 \, ^\circ C$, unless otherwise specified

![Figure 3](#)  
**Reverse current**, $I_R = (V_R)$

![Figure 4](#)  
**Reverse current**: $I_R = f(T_A)$, $V_R = 3.3 \, V$
Typical Characteristics at $T_A = 25 \, ^\circ\text{C}$, unless otherwise specified

Figure 5  Line capacitance: $C_L = f(V_R)$, $f = 1$MHz, from I/O to GND
Figure 6  Clamping voltage (TLP): $I_{TLP} = f(V_{TLP})$ according ANSI/ESD STM5.5.1- Electrostatic Discharge Sensitivity Testing using Transmission Line Pulse (TLP) Model. TLP conditions: $Z_0 = 50 \Omega$, $t_p = 100$ ns, $t_r = 0.6$ ns, $I_{TLP}$ and $V_{TLP}$ averaging window: $t_1 = 30$ ns to $t_2 = 60$ ns, extraction of dynamic resistance using squares fit to TLP characteristics between $I_{TLP1} = 10$ A and $I_{TLP2} = 40$ A. Please refer to Application Note AN210[2]
Figure 7  Pulse current (IEC61000-4-5) versus clamping voltage: $I_{pp} = f(V_{CL})$

$R_{DYN} = 0.70 \, \Omega$

$R_{DYN} = 0.44 \, \Omega$
Typical Characteristics at $T_A = 25 \, ^\circ\text{C}$, unless otherwise specified

Figure 8  Clamping voltage at $+8 \, \text{kV}$ discharge according IEC61000-4-2 ($R = 330 \, \Omega, C = 150 \, \text{pF}$)

Figure 9  Clamping voltage at $-8 \, \text{kV}$ discharge according IEC61000-4-2 ($R = 330 \, \Omega, C = 150 \, \text{pF}$)
Typical Characteristics at $T_A = 25 \, ^\circ\text{C}$, unless otherwise specified

Figure 10  Clamping voltage at $+15 \, \text{kV}$ discharge according IEC61000-4-2 ($R = 330 \, \text{Ohm}, \ C = 150 \, \text{pF}$)

Figure 11  Clamping voltage at $-15 \, \text{kV}$ discharge according IEC61000-4-2 ($R = 330 \, \Omega, \ C = 150 \, \text{pF}$)
4 Application Information

To design USB3.0 link for best system level ESD performance and error free Signal Integrity is mandatory. To bring both requirements together, the ESD protection devices has to provide excellent ESD and a very low device capacitance. The Infineon ESD3V3U4ULC in “array” configuration, combined with a clear and straightforward “full through” layout fulfills these requirements in the best way.

Figure 12 USB3.0 structure with ESD protection devices [3]
5 Ordering Information Scheme

ESD 0P1 RF - XX YY

- Package
  XX = Pin number (i.e.: 02 = 2 pins; 03 = 3 pins)
  YY = Package family:
  LS = TSSLP
  LRH = TSLP

- For Radio Frequency Applications

- Line Capacitance \( C_L \) in pF: (i.e.: 0P1 = 0.1pF)

ESD 5V3 UN U - XX YY

- Package or Application
  XX = Pin number (i.e.: 02 = 2 pins; 03 = 3 pins)
  YY = Package family:
  LS = TSSLP
  LRH = TSLP
  S = SOT363
  U = SC74

  XX = Application family:
  LC = Low Clamp
  HDMI

- UNi- / Bi-directional or Rail to Rail protection

- Number of protected lines (i.e.: 1 = 1 line; 4 = 4 lines)

- Capacitance: Standard (>10pF), Low (<10pF), Ultra-low (<1pF)

- Maximum working voltage \( V_{RWM} \) in V: (i.e.: 5V3 = 5.3V)

Figure 13 Ordering information scheme
6 Package Information

6.1 TSLP-9-1 (mm)

Figure 14 TSLP-9-1: Package overview

Figure 15 TSLP-9-1: Footprint

Figure 16 TSLP-9-1: Packing

Figure 17 TSLP-9-1: Marking

1) Dimension applies to plated terminals
References


[3] Infineon Technologie AG - Application Note AN240: Effective ESD Protection for USB3.0, combined with perfect Signal Integrity.