Protection Device
TVS (Transient Voltage Suppressor)

ESD217-B1-02EL
Bi-directional, +14 / -8 V, 9 pF, 0402, RoHS and Halogen Free compliant
Information

For further information on technology, delivery terms and conditions and prices, please contact the nearest Infineon Technologies Office (www.infineon.com)

Warnings

Due to technical requirements, components may contain dangerous substances. For information on the types in question, please contact the nearest Infineon Technologies Office.

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1 Product Overview

1.1 Features

- ESD / transient protection according to:
  - IEC61000-4-2 (ESD): ±30 kV (air), ±25 kV (contact)
  - IEC61000-4-4 (EFT): ±3 kV / ±60 A (5/50 ns)
  - IEC61000-4-5 (Surge): ±3 A (8/20 µs)
- Asymmetrical, bi-directional working voltage up to $V_{\text{RWM}} = +14 \text{ V} / -8 \text{ V}$
- Low capacitance: $C_L = 9 \text{ pF (typical)}$
- Low clamping voltage: $V_{\text{CL}} = 26 \text{ V (typical)}$ at $I_{\text{TLR}} = 16 \text{ A}$
- Very low reverse current: $I_R < 1 \text{ nA (typical)}$
- Ultra low dynamic resistance: $R_{\text{DYN}} = 0.2 \Omega$ (typical)
- Pb-free (RoHS compliant) and halogen free package

1.2 Application Examples

- USB 2.0, 10/100 Ethernet, Firewire, DVI
- Mobile communication
- Consumer products (STD, MP3, DVD, DSC...)
- LCD display, camera
- Notebooks and desktop computers, peripherals

1.3 Product Description

![Pin Configuration and Schematic Diagram](PinConf_and_SchematicDiag.vsd)

**Table 1-1  Part Information**

<table>
<thead>
<tr>
<th>Type</th>
<th>Package</th>
<th>Configuration</th>
<th>Marking code</th>
</tr>
</thead>
<tbody>
<tr>
<td>ESD217-B1-02EL</td>
<td>TSLP-2-19</td>
<td>1 line, bi-directional</td>
<td>B</td>
</tr>
</tbody>
</table>

RoHS
2 Characteristics

Table 2-1 Maximum Ratings at $T_A = 25 \, ^\circ\text{C}$, unless otherwise specified

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Values</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>ESD air discharge</td>
<td>$V_{\text{ESD}}$</td>
<td>±30</td>
<td>kV</td>
</tr>
<tr>
<td>ESD contact discharge</td>
<td>$V_{\text{ESD}}$</td>
<td>±25</td>
<td>kV</td>
</tr>
<tr>
<td>Peak pulse power</td>
<td>$P_{\text{PK}}$</td>
<td>85</td>
<td>W</td>
</tr>
<tr>
<td>Peak pulse current</td>
<td>$I_{\text{PP}}$</td>
<td>±3</td>
<td>A</td>
</tr>
<tr>
<td>Operating temperature range</td>
<td>$T_{\text{OP}}$</td>
<td>-55 to 125</td>
<td>°C</td>
</tr>
<tr>
<td>Storage temperature</td>
<td>$T_{\text{stg}}$</td>
<td>-65 to 150</td>
<td>°C</td>
</tr>
</tbody>
</table>

1) $V_{\text{ESD}}$ according to IEC61000-4-2
2) Non-repetitive current pulse 8/20µs exponential decay waveform according to IEC61000-4-5

Attention: Stresses above the max. values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

2.1 Electrical Characteristics at $T_A = 25 \, ^\circ\text{C}$, unless otherwise specified

![Figure 2-1 Definitions of electrical characteristics](Image)
### Table 2-2  DC Characteristics at $T_A = 25$ °C, unless otherwise specified

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Values</th>
<th>Unit</th>
<th>Note / Test Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>Reverse working voltage</td>
<td>$V_{RWM}$</td>
<td>-8</td>
<td>14</td>
<td>V Pin 2 to Pin1</td>
</tr>
<tr>
<td>Breakdown voltage</td>
<td>$V_{BR}$</td>
<td>14.5</td>
<td>8.5</td>
<td>17</td>
</tr>
<tr>
<td></td>
<td></td>
<td>11.5</td>
<td>14</td>
<td>20</td>
</tr>
<tr>
<td>Reverse current</td>
<td>$I_R$</td>
<td>-</td>
<td>&lt;1</td>
<td>50</td>
</tr>
</tbody>
</table>

### Table 2-3  AC Characteristics at $T_A = 25$ °C, unless otherwise specified

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Values</th>
<th>Unit</th>
<th>Note / Test Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>Line capacitance</td>
<td>$C_L$</td>
<td>9</td>
<td>13</td>
<td>pF $V_{R} = 0 \text{ V}, f = 1 \text{ MHz}$</td>
</tr>
<tr>
<td>Series inductance</td>
<td>$L_S$</td>
<td>0.4</td>
<td></td>
<td>nH</td>
</tr>
</tbody>
</table>

### Table 2-4  ESD and Surge Characteristics at $T_A = 25$ °C, unless otherwise specified

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Values</th>
<th>Unit</th>
<th>Note / Test Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>Clamping voltage$^1)$</td>
<td>$V_{CL}$</td>
<td>-</td>
<td>26</td>
<td>V $I_{TLP} = 16 \text{ A}, t_p = 100 \text{ ns}$</td>
</tr>
<tr>
<td></td>
<td></td>
<td>-</td>
<td>29</td>
<td>$I_{TLP} = 30 \text{ A}, t_p = 100 \text{ ns}$</td>
</tr>
<tr>
<td></td>
<td></td>
<td>-</td>
<td>25.5</td>
<td>$I_{PP} = 3 \text{ A}, t_p = 8/20 \mu\text{s}, Pin2 to Pin1$</td>
</tr>
<tr>
<td></td>
<td></td>
<td>-</td>
<td>24</td>
<td>$I_{PP} = 3 \text{ A}, t_p = 8/20 \mu\text{s}, Pin1 to Pin2$</td>
</tr>
<tr>
<td>Dynamic resistance$^1)$</td>
<td>$R_{DYN}$</td>
<td>-</td>
<td>0.2</td>
<td>$t_p = 100 \text{ ns}, Pin2 to Pin1$</td>
</tr>
<tr>
<td></td>
<td></td>
<td>-</td>
<td>0.4</td>
<td>$t_p = 100 \text{ ns}, Pin1 to Pin2$</td>
</tr>
</tbody>
</table>

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1) Please refer to Application Note AN210[1]. TLP parameter: $Z_0 = 50 \Omega$, $t_p = 100\text{ns}$, $t_r = 300\text{ps}$.

2) Non-repetitive current pulse 8/20µs exponential decay waveform according to IEC61000-4-5
3 Typical Characteristics Diagrams

Typical characteristics diagrams at $T_A = 25^\circ$C, unless otherwise specified

**Figure 3-1** Reverse leakage current: $I_R = f(V_R)$, pin 2 to pin 1

**Figure 3-2** Line capacitance: $C_L = f(V_R)$, pin 2 to pin 1
Figure 3-3  Clamping voltage (TLP): $I_{\text{TLP}} = f(V_{\text{TLP}})$, pin 2 to pin 1
Figure 3-4  Clamping voltage(Surge): $I_{pp} = f(V_{CL})[1]$, pin 2 to pin 1
Figure 3-5  Insertion loss vs. frequency in a 50 Ω system
4 Package Information

4.1 TSLP-2-19

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**Figure 4-1** TSLP-2-19 Package outline

1) Dimension applies to plated terminals

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**Figure 4-2** TSLP-2-19 Footprint

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**Figure 4-3** TSLP-2-19 Packing

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**Figure 4-4** TSLP-2-19 Marking example, Type code see: Table 1-1 “Part Information” on Page 3
References

[1] Infineon AG - Application Note AN210: Effective ESD Protection design at System Level Using VF-TLP Characterization Methodology

[2] Infineon AG - Recommendations for PCB Assembly of Infineon TSLP and TSSLP Packages
Revision History Rev. 1.0, 2014-05-16
Page or Item | Subjects (major changes since previous revision)
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Revision 1.1, 2014-11-11
3 | Table 1-1) updated

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