

# ESD129-B1-W01005

## Protection Devices

TVS (Transient Voltage Suppressor)

Bi-directional, 18 V (AC), 13 V (DC), 0.3 pF, 01005, RoHS and Halogen Free compliant

## Features

- ESD / transient protection of high speed data lines according to:
  - IEC61000-4-2 (ESD):  $\pm 15$  kV (air / contact discharge)
  - IEC61000-4-4 (EFT):  $\pm 2$  kV /  $\pm 40$  A (5/50 ns)
  - IEC61000-4-5 (Surge):  $\pm 2$  A (8/20  $\mu$ s)
- Bi-directional working voltage up to:  $V_{RWM} = \pm 18$  V (AC),  $\pm 13$  V (DC)
- Line capacitance:  $C_L = 0.3$  pF (typical) at  $f = 1$  MHz
- Clamping voltage:  $V_{CL} = 32$  V (typical) at  $I_{TLP} = 16$  A with  $R_{DYN} = 0.82 \Omega$  (typical)
- Very low reverse current:  $I_R < 1$  nA (typical)
- Small form factor SMD size 01005 and low profile (0.43 mm x 0.23 mm x 0.15 mm); for further package information please refer to application note AN392 [\[3\]](#)
- Bi-directional and symmetric I/V characteristics for optimized design / assembly



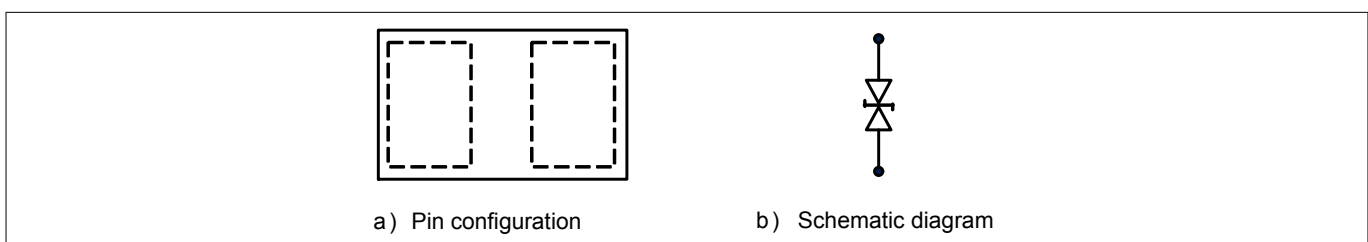
## Potential applications

- ESD protection of RF signal lines in Near Field Communication (NFC) applications

## Product validation

Qualified for industrial applications according to the relevant tests of JEDEC47/20/22

## Device information



**Figure 1** Pin configuration and schematic diagram

**Table 1** Part information

Type	Package	Configuration	Marking code
ESD129-B1-W01005	WLL-2-2	1 line, bi-directional	K <sup>1)</sup>

<sup>1)</sup> The device has no marking or date code on the device backside. The marking code is on pad side.

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**Maximum ratings**

**1 Maximum ratings**

Note:  $T_A = 25\text{ °C}$ , unless otherwise specified

**Table 2 Maximum ratings**

Parameter	Symbol	Values	Unit
Reverse working voltage	$V_{RWM}$	$\pm 18^{1)} \pm 13^{2)}$	V
ESD discharge <sup>3)</sup>	$V_{ESD}$ (contact)	$\pm 15$	kV
	$V_{ESD}$ (air)	$\pm 15$	
Peak pulse power <sup>4)</sup>	$P_{PK}$	53	W
Peak pulse current <sup>4)</sup>	$I_{PP}$	$\pm 2$	A
Operating temperature range	$T_{OP}$	-55 to 125	°C
Storage temperature	$T_{stg}$	-65 to 150	°C

**Attention:** *Stresses above the maximum values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings. Exceeding only one of these values may cause irreversible damage to the component.*

<sup>1</sup> For RF peak voltage (NFC)

<sup>2</sup> For DC voltage

<sup>3</sup>  $V_{ESD}$  according to IEC61000-4-2 (R = 330  $\Omega$ , C = 150 pF discharge network)

<sup>4</sup> Stress pulse: 8/20 $\mu$ s current waveform according to IEC61000-4-5

Electrical characteristics

## 2 Electrical characteristics

Note:  $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise specified. Device is electrically symmetrical.

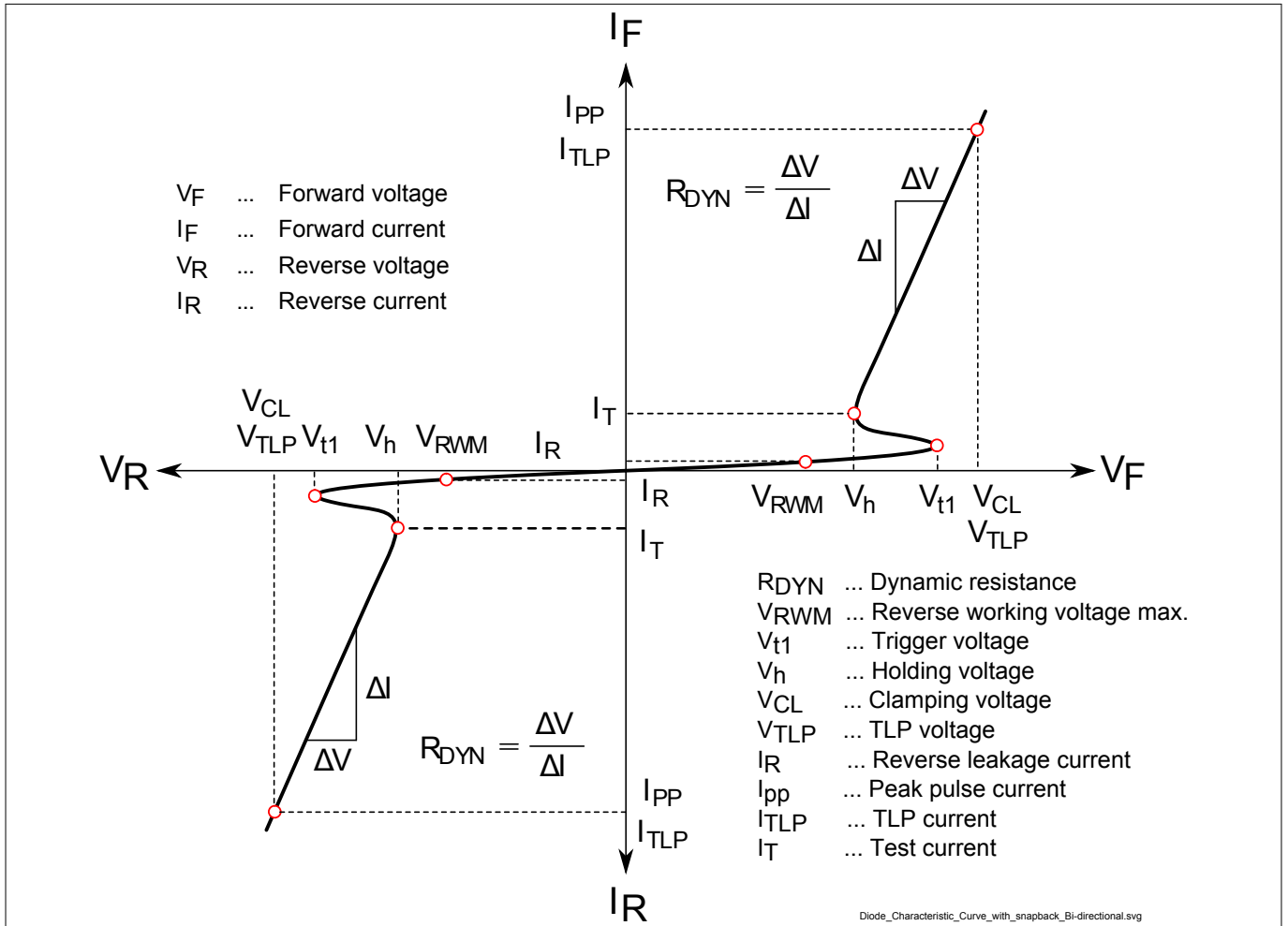


Figure 2 Definitions of electrical characteristics

**Electrical characteristics**

**Table 3 DC characteristics**

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Trigger Voltage <sup>1)</sup>	$V_{t1}$	19	22	–	V	–
Holding voltage	$V_h$	13	16	19	V	$I_T = 40 \text{ mA}$
Reverse current	$I_R$	–	<1	30	nA	$V_R = 18 \text{ V}$

**Table 4 AC characteristics**

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Line capacitance	$C_L$	–	0.30	0.5	pF	$V_R = 0 \text{ V}, f = 1 \text{ MHz}$
		–	0.22	–		$V_R = 0 \text{ V}, f = 1 \text{ GHz}$

**Table 5 ESD and Surge characteristics**

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Clamping voltage <sup>2)</sup>	$V_{CL}$	–	32	–	V	$I_{TLP} = 16 \text{ A}, t_p = 100 \text{ ns}$
Clamping voltage <sup>3)</sup>		–	17.5	–		$I_{PP} = 1 \text{ A}, t_p = 8/20 \mu\text{s}$
Dynamic resistance <sup>2)</sup>	$R_{DYN}$	–	0.82	–	$\Omega$	$t_p = 100 \text{ ns}$

<sup>1</sup> Verified by design

<sup>2</sup> Please refer to Application Note AN210 [1]. TLP parameters:  $Z_0 = 50 \Omega$ ,  $t_p = 100 \text{ ns}$ ,  $t_r = 0.6 \text{ ns}$ .

<sup>3</sup> Stress pulse: 8/20 $\mu\text{s}$  current waveform according to IEC61000-4-5

Typical characteristic diagrams

### 3 Typical characteristic diagrams

Note:  $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise specified

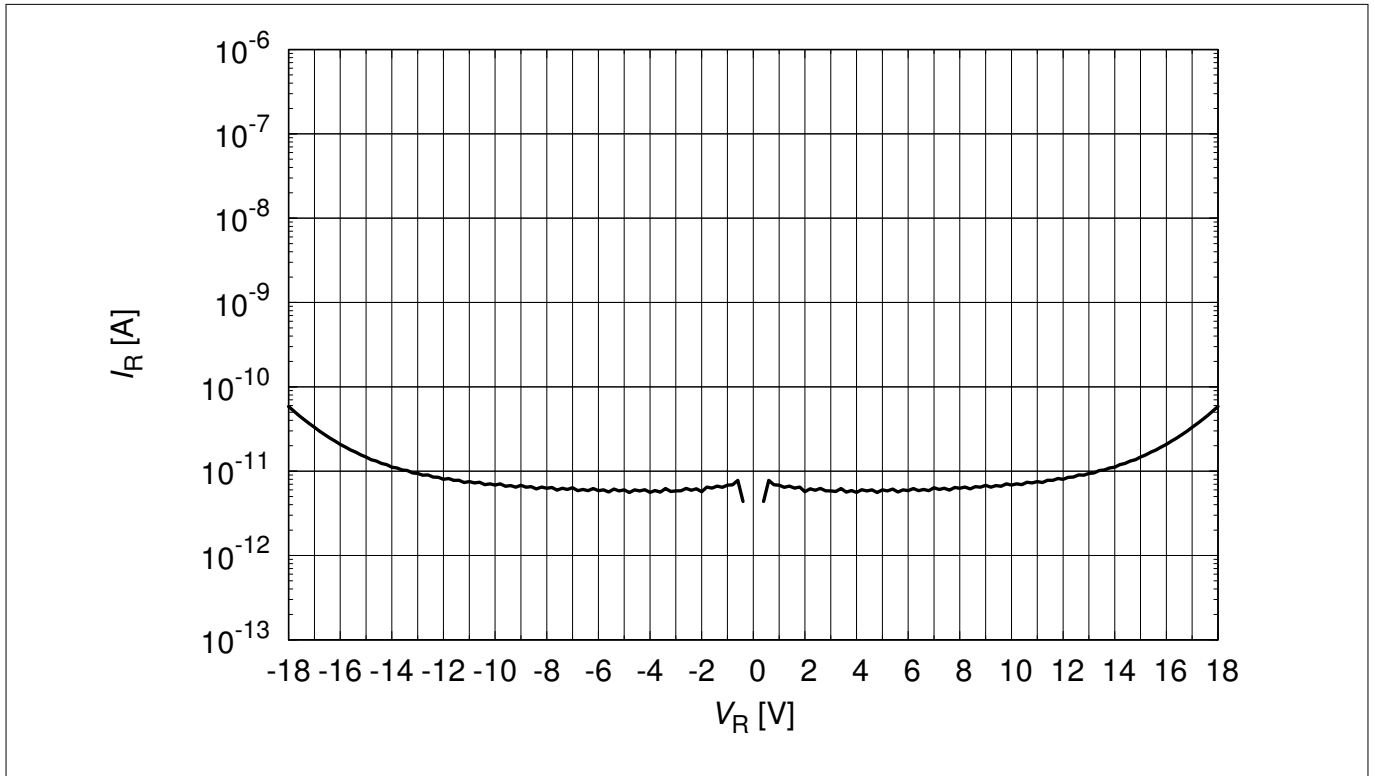


Figure 3 Reverse leakage current:  $I_R = f(V_R)$

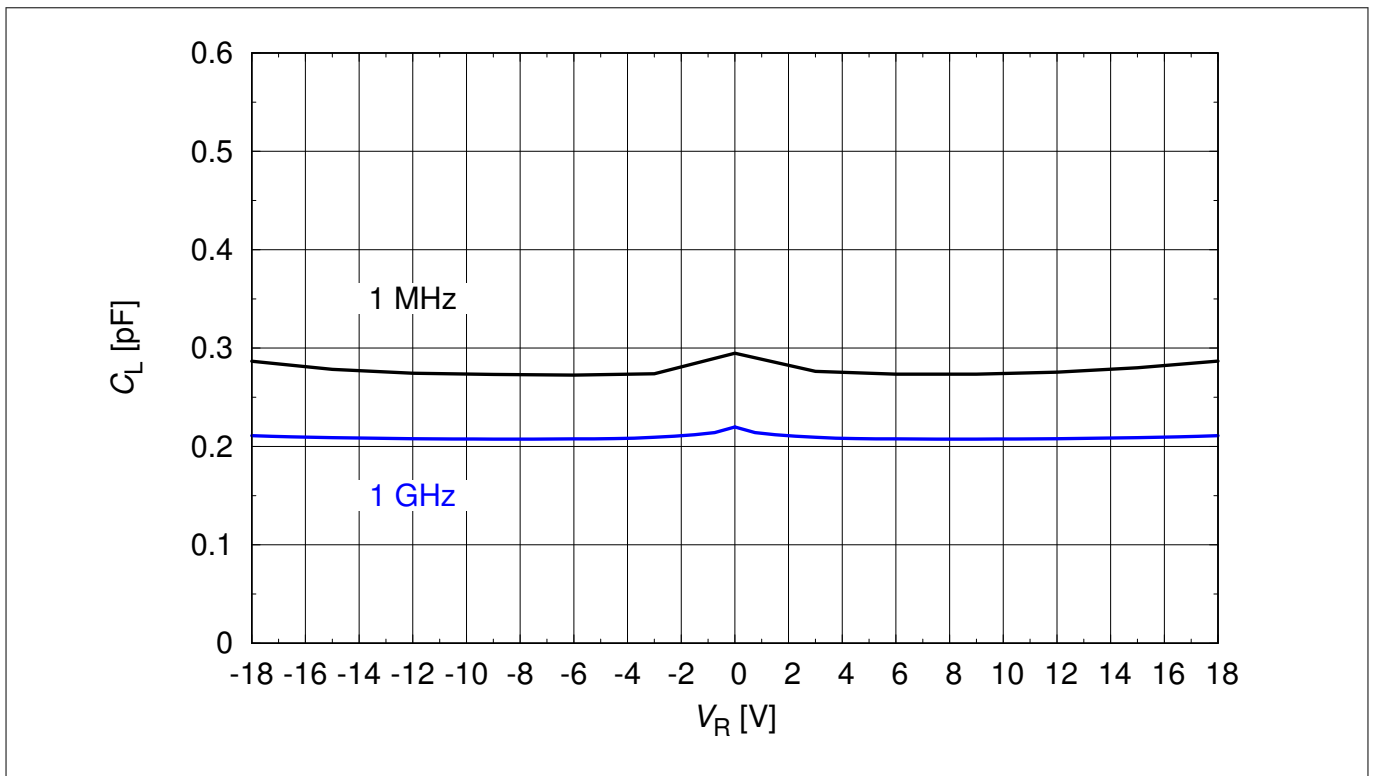


Figure 4 Line capacitance:  $C_L = f(V_R)$ ,  $f = 1\text{ MHz}$

Typical characteristic diagrams

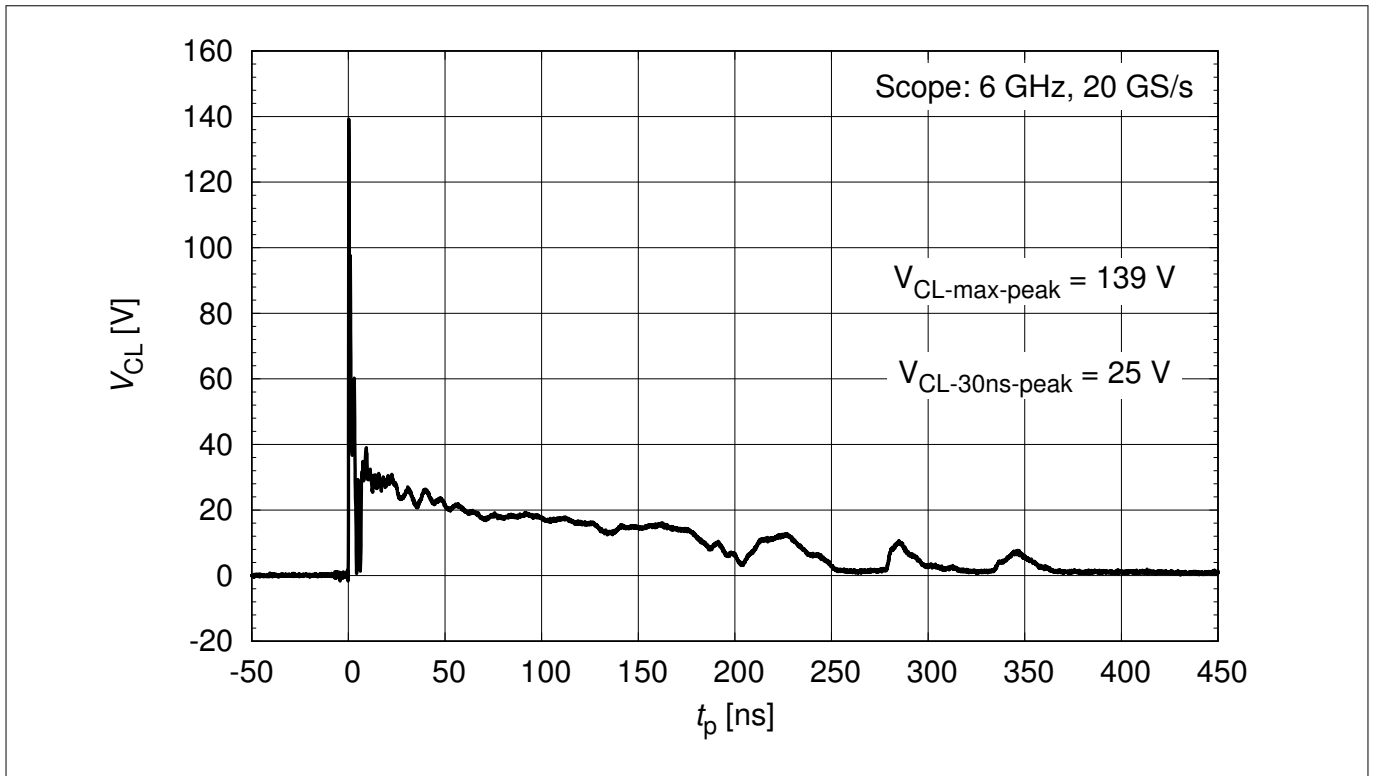


Figure 5 Clamping voltage (ESD):  $V_{CL} = f(t)$ , 8 kV positive pulse according to IEC 61000-4-2

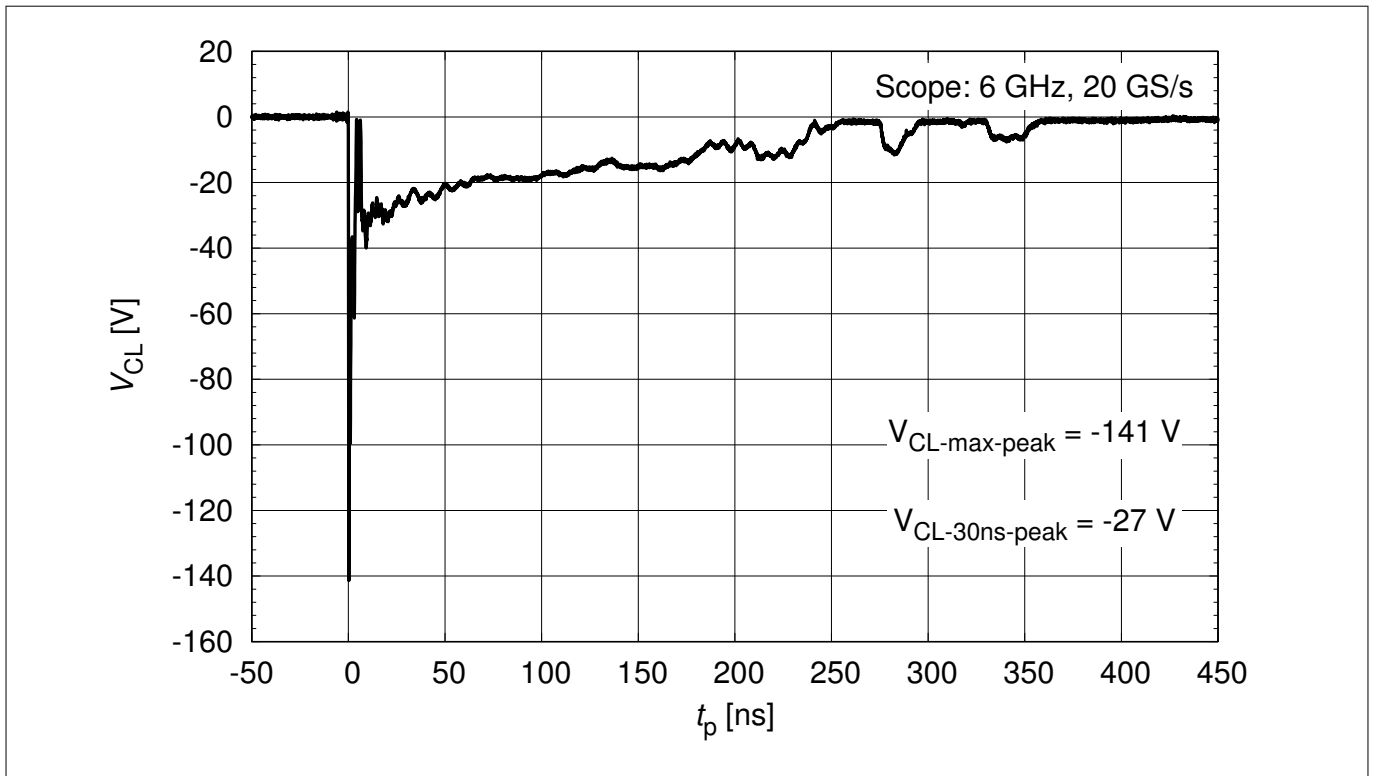


Figure 6 Clamping voltage (ESD):  $V_{CL} = f(t)$ , 8 kV negative pulse according to IEC 61000-4-2

Typical characteristic diagrams

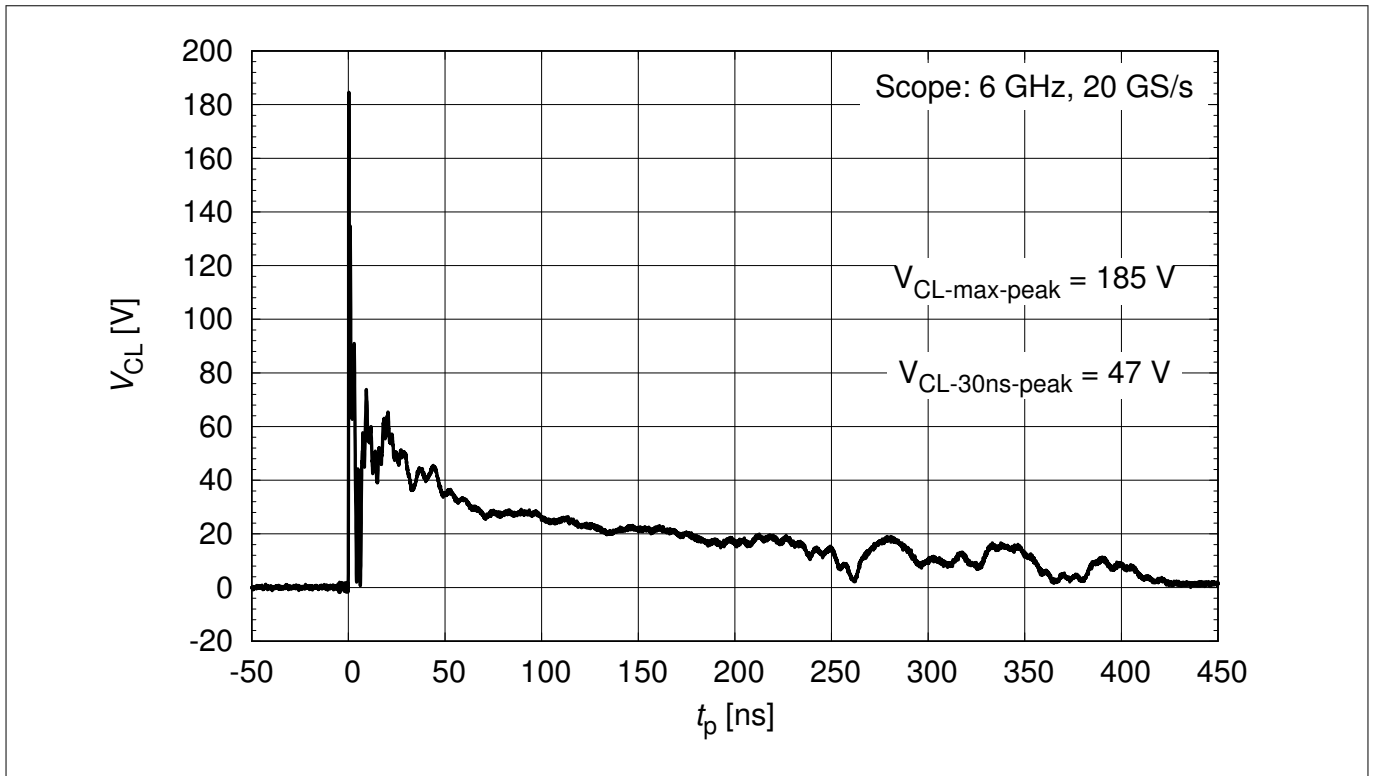


Figure 7 Clamping voltage (ESD):  $V_{CL} = f(t)$ , 15 kV positive pulse according to IEC 61000-4-2

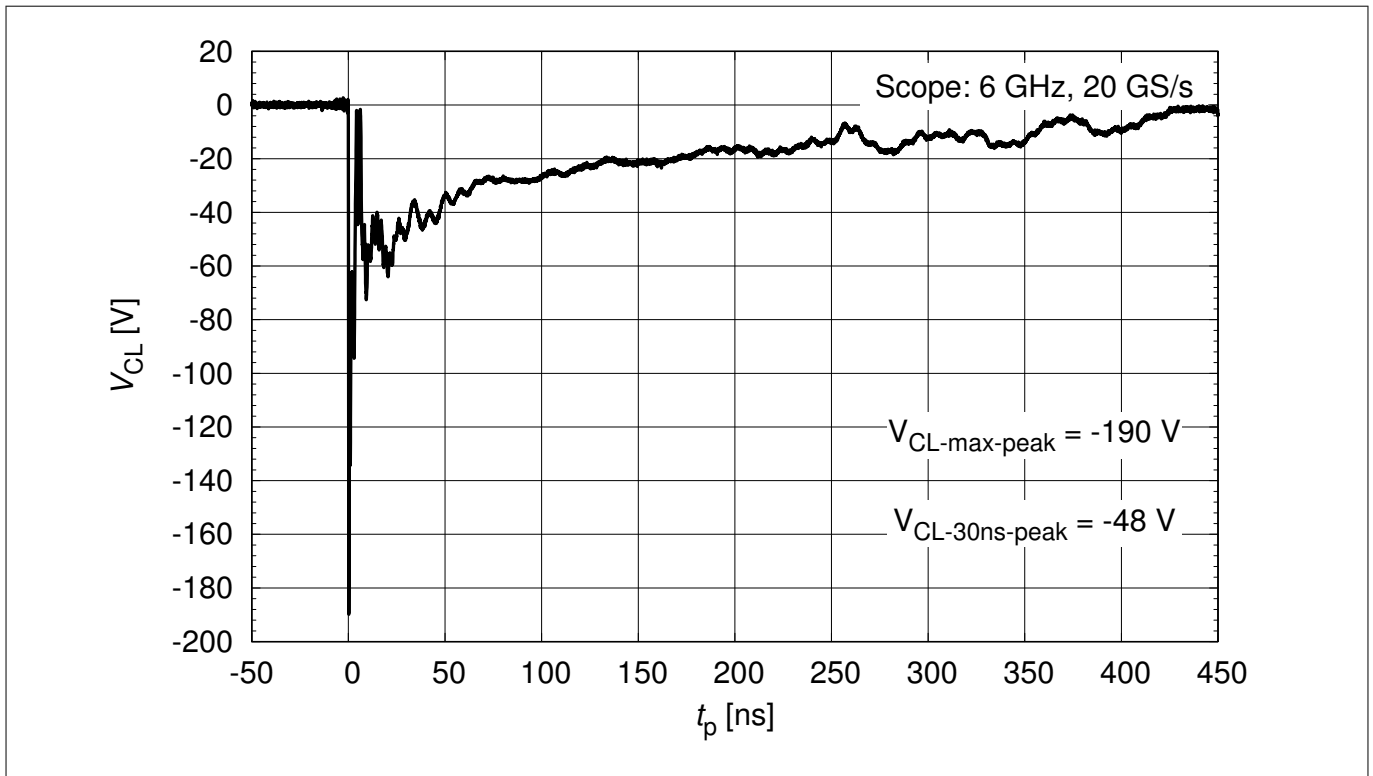
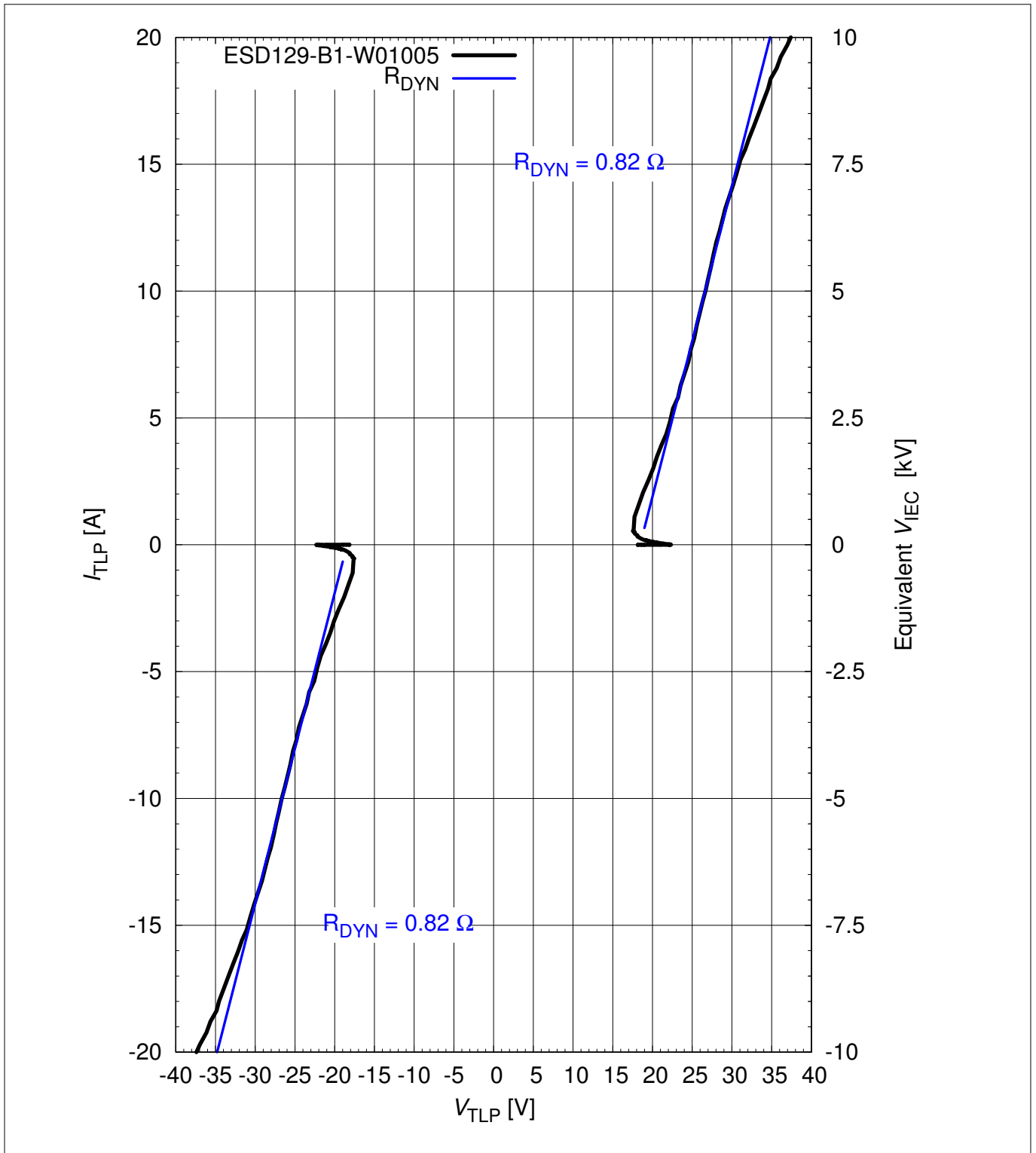


Figure 8 Clamping voltage (ESD):  $V_{CL} = f(t)$ , 15 kV negative pulse according to IEC 61000-4-2



**Typical characteristic diagrams**



**Figure 9 Clamping voltage (TLP):  $I_{TLP} = f(V_{TLP})$  [1]**

Typical characteristic diagrams

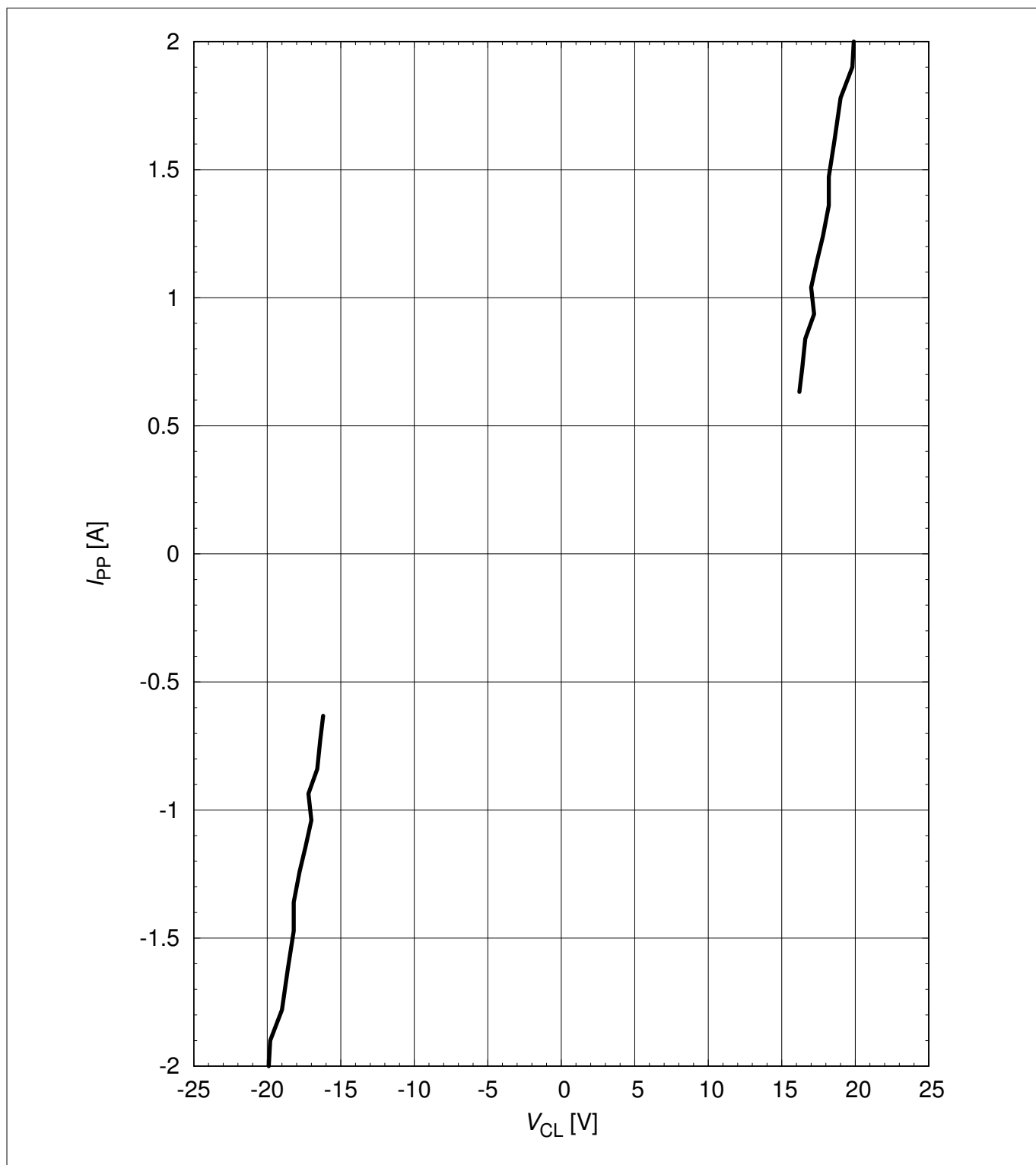
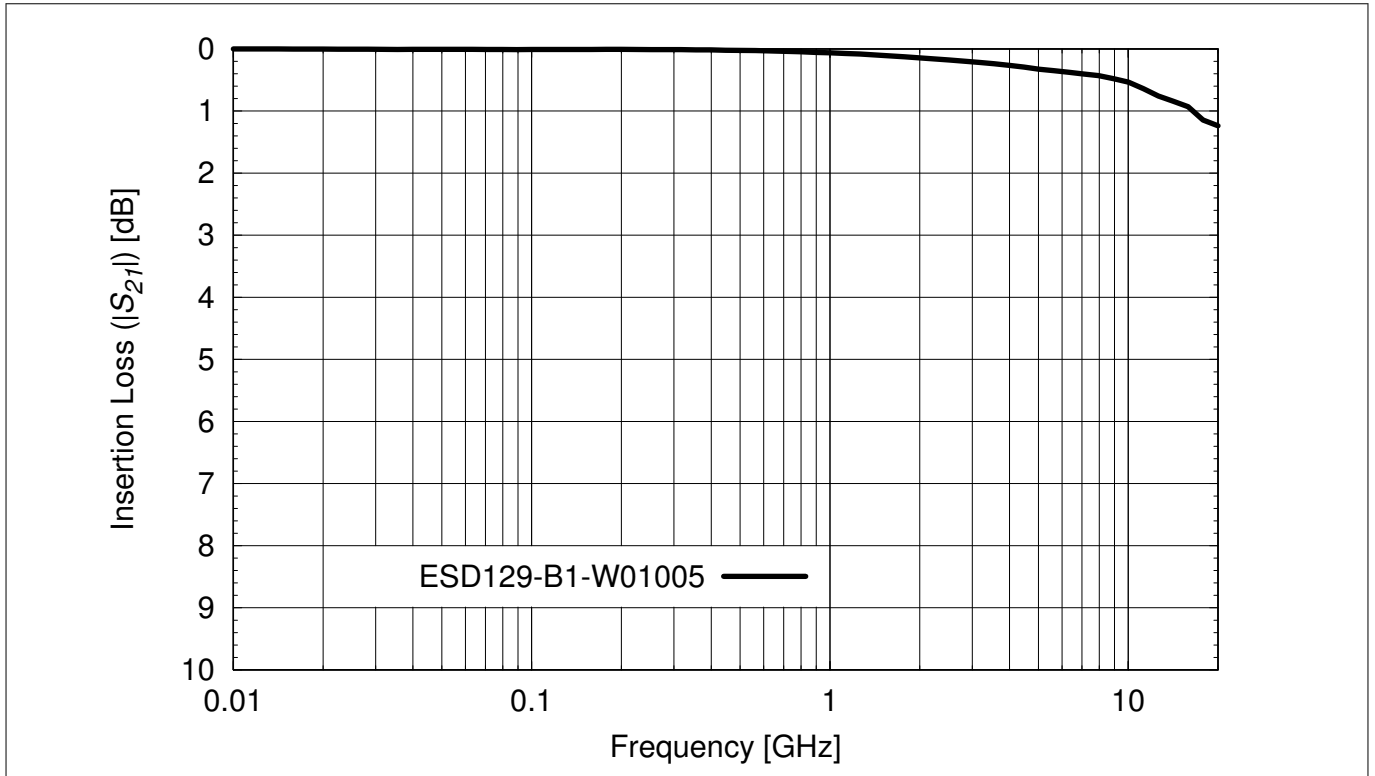


Figure 10 Clamping voltage (Surge):  $I_{PP} = f(V_{CL})$  according to IEC 61000-4-5 [1]

**Typical characteristic diagrams**



**Figure 11** Insertion loss vs. frequency in a 50 Ω system

Package information

## 4 Package information

### 4.1 WLL-2-2 package

Note: Dimensions in mm

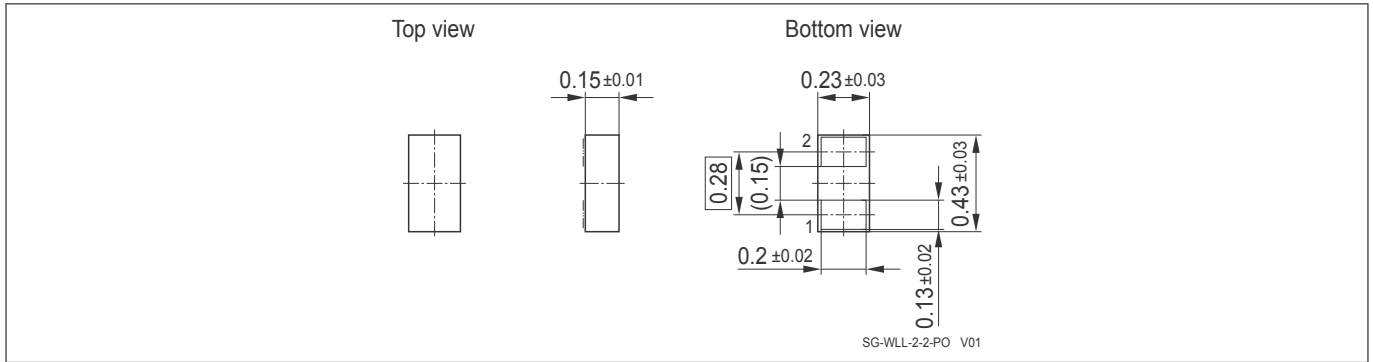


Figure 12 WLL-2-2 package outline

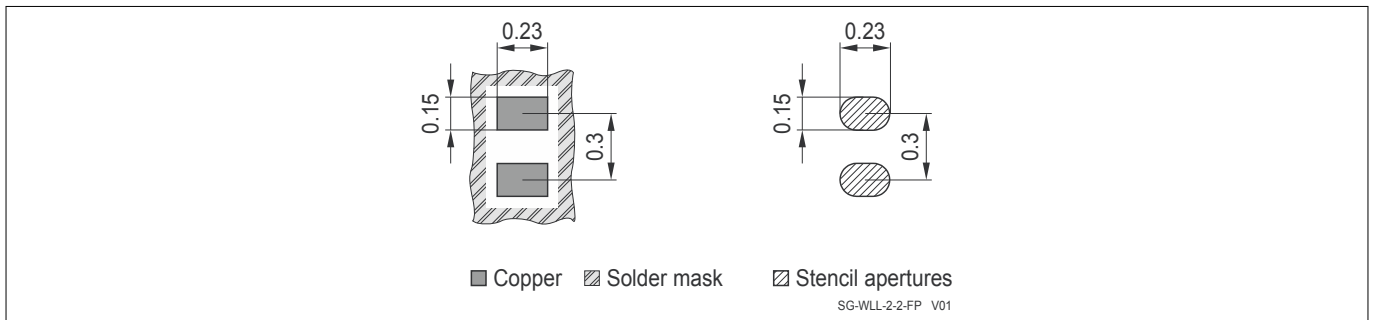


Figure 13 WLL-2-2 footprint (recommendation for Printed Circuit Board assembly see [2])

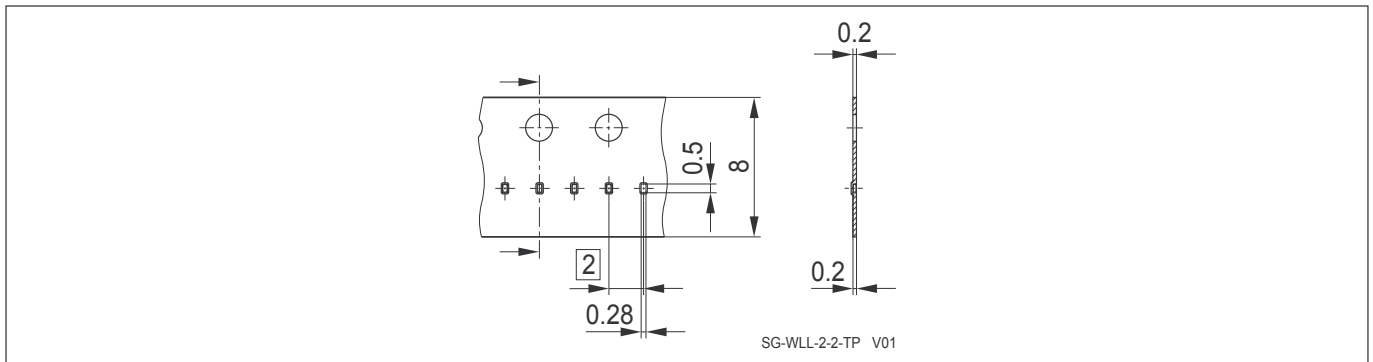


Figure 14 WLL-2-2 packing

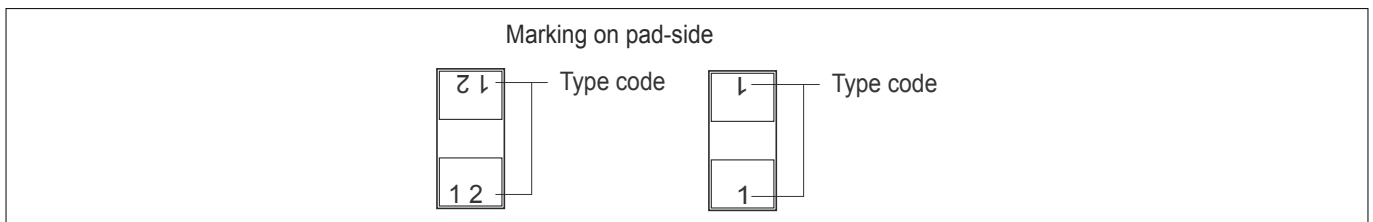


Figure 15 WLL-2-2 marking example (see [Device information](#))

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**References**

**5                      References**

- [1] Infineon AG - **Application Note AN210**: Effective ESD Protection design at System Level Using VF-TLP Characterization Methodology
- [2] Infineon AG - Recommendation for Printed Circuit Board Assembly of Infineon WLL Packages  
[http://www.infineon.com/Packageinformation\\_WLL](http://www.infineon.com/Packageinformation_WLL)
- [3] Infineon AG - **Application Note AN392**: TVS Diodes in ChipScalePackage reduce size and save cost
- [4] Infineon AG - **Application Note AN244**: ESD Protection in Chip Size Package (CSP) tailored for the NFC Frontend

**Revision history**

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**Revision history: Rev.1.0, 2017-05-08**

<b>Page or Item</b>	<b>Subjects (major changes since previous revision)</b>
Revision 1.1, 2017-10-27	
	Editorial changes
	Table 4 updated

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