Protection Device
TVS (Transient Voltage Suppressor)

ESD114-U1-02 Series
Uni-directional, 5.3 V, 0.4 pF, 0402, 0201, RoHS and Halogen Free compliant

ESD114-U1-02ELS
ESD114-U1-02EL

Data Sheet
Revision 1.0, 2014-10-30
Final
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1 Product Overview

1.1 Features

- ESD / Transient protection of high speed data lines exceeding
  - IEC61000-4-2 (ESD): ±20 kV (contact)
  - IEC61000-4-4 (EFT): ±2 kV / ±40 A (5/50 ns)
  - IEC61000-4-5 (surge): ±3 A (8/20 μs)
- Maximum working voltage: $V_{RWM} = ±5.3$ V
- Ultra low capacitance: $C_L = 0.4$ pF (typical)
- Very low clamping voltage $V_{CL} = +20 / -15$ V (typical) at $I_{TLP} = 16$ A
- Low dynamic resistance $R_{DYN} = 0.5$ Ω (typical)
- Very small form factor down to 0.62 x 0.32 x 0.31 mm$^3$
- Pb-free (RoHS compliant) and halogen free package

RoHS

1.2 Application Examples

- USB 2.0, Mobile HDMI Link, MDDI, MIPI, etc.
- HDMI, DisplayPort, DVI, Ethernet, Firewire, S-ATA

1.3 Product Description

![Pin Configuration and Schematic Diagram](Single_Die_diode_PinConf_and_SchematicDiag.vst.vsd)

**Figure 1** Pin Configuration and Schematic Diagram

<table>
<thead>
<tr>
<th>Table 1</th>
<th></th>
<th></th>
<th>Marking code</th>
</tr>
</thead>
<tbody>
<tr>
<td>Type</td>
<td>Package</td>
<td>Configuration</td>
<td></td>
</tr>
<tr>
<td>ESD114-U1-02ELS</td>
<td>TSSLP-2-3</td>
<td>1 line, uni-directional</td>
<td>K</td>
</tr>
<tr>
<td>ESD114-U1-02EL</td>
<td>TSLP-2-19</td>
<td>1 line, uni-directional</td>
<td>K</td>
</tr>
</tbody>
</table>
2 Maximum Ratings

Table 2 Maximum Ratings at $T_A = 25$ °C, unless otherwise specified

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Values</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>ESD contact discharge</td>
<td>$V_{ESD}$</td>
<td>±20</td>
<td>kV</td>
</tr>
<tr>
<td>Peak pulse current ($t_p = 8/20$ μs)</td>
<td>$I_{PP}$</td>
<td>±3</td>
<td>A</td>
</tr>
<tr>
<td>Operating temperature range</td>
<td>$T_{OP}$</td>
<td>-55 to 125</td>
<td>°C</td>
</tr>
<tr>
<td>Storage temperature</td>
<td>$T_{stg}$</td>
<td>-65 to 150</td>
<td>°C</td>
</tr>
</tbody>
</table>

1) $V_{ESD}$ according to IEC61000-4-2
2) Non-repetitive current pulse 8/20μs exponential decay waveform according to IEC61000-4-5

**Attention:** Stresses above the max. values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

3 Electrical Characteristics at $T_A = 25$ °C, unless otherwise specified
### Table 3  DC Characteristics at $T_A = 25 \, ^\circ\text{C}$, unless otherwise specified

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Values</th>
<th>Unit</th>
<th>Note / Test Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>Reverse working voltage</td>
<td>$V_{\text{RWM}}$</td>
<td>–</td>
<td>5.3  V</td>
<td>Pin 1 to Pin 2</td>
</tr>
<tr>
<td>Breakdown voltage</td>
<td>$V_{\text{BR}}$</td>
<td>6</td>
<td>–</td>
<td>$I_{\text{BR}} = 1 , \text{mA}$, from Pin 1 to Pin 2</td>
</tr>
<tr>
<td>Reverse current</td>
<td>$I_R$</td>
<td>–</td>
<td>10   nA</td>
<td>$V_R = 5.3 , \text{V}$, from Pin 1 to Pin 2</td>
</tr>
</tbody>
</table>

### Table 4  RF Characteristics at $T_A = 25 \, ^\circ\text{C}$, unless otherwise specified

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Values</th>
<th>Unit</th>
<th>Note / Test Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>Line capacitance</td>
<td>$C_L$</td>
<td>–</td>
<td>0.6  pF</td>
<td>$V_R = 0 , \text{V}$, $f = 1 , \text{MHz}$</td>
</tr>
<tr>
<td>Serie inductance</td>
<td>$L_S$</td>
<td>–</td>
<td>0.4  nH</td>
<td>ESD114-U1-02ELS</td>
</tr>
</tbody>
</table>

1) Total capacitance line to ground

### Table 5  ESD Characteristics at $T_A = 25 \, ^\circ\text{C}$, unless otherwise specified

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Values</th>
<th>Unit</th>
<th>Note / Test Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>Clamping voltage</td>
<td>$V_{\text{CL}}$</td>
<td>–</td>
<td>10   V</td>
<td>$I_{\text{TLP}} = 1 , \text{A}$, from Pin 1 to Pin 2</td>
</tr>
<tr>
<td></td>
<td></td>
<td>–</td>
<td>20</td>
<td>$I_{\text{TLP}} = 16 , \text{A}$, from Pin 1 to Pin 2</td>
</tr>
<tr>
<td></td>
<td></td>
<td>–</td>
<td>28</td>
<td>$I_{\text{TLP}} = 30 , \text{A}$, from Pin 1 to Pin 2</td>
</tr>
<tr>
<td></td>
<td></td>
<td>–</td>
<td>3</td>
<td>$I_{\text{TLP}} = 1 , \text{A}$, from Pin 2 to Pin 1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>–</td>
<td>15</td>
<td>$I_{\text{TLP}} = 16 , \text{A}$, from Pin 2 to Pin 1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>–</td>
<td>21</td>
<td>$I_{\text{TLP}} = 30 , \text{A}$, from Pin 2 to Pin 1</td>
</tr>
<tr>
<td>Dynamic resistance</td>
<td>$R_{\text{DYN}}$</td>
<td>–</td>
<td>0.56</td>
<td>Pin 1 to Pin 2</td>
</tr>
<tr>
<td></td>
<td></td>
<td>–</td>
<td>0.43</td>
<td>Pin 2 to Pin 1</td>
</tr>
</tbody>
</table>

1) Please refer to Application Note AN210[1]. TLP parameter: $Z_0 = 50 \, \Omega$, $t_p = 100\text{ns}$, $t_r = 300\text{ps}$, averaging window: $t_1 = 30 \, \text{ns}$ to $t_2 = 60 \, \text{ns}$, extraction of dynamic resistance using least squares fit of TLP characteristics between $I_{\text{PP1}} = 10 \, \text{A}$ and $I_{\text{PP2}} = 40 \, \text{A}$.
4 Typical Characteristics Diagrams

Typical characteristics diagrams at $T_a = 25^\circ C$, unless otherwise specified

**Figure 3** Reverse leakage current: $I_R = f(V_R)$

**Figure 4** Line capacitance: $C_L = f(V_R)$
Figure 5  IEC61000-4-2 : $V_{CL} = f(t)$, 8 kV positive pulse from pin 1 to pin 2

Figure 6  IEC61000-4-2 : $V_{CL} = f(t)$, 8 kV negative pulse from pin 1 to pin 2
Figure 7  IEC61000-4-2 : $V_{CL} = f(t)$, 15 kV positive pulse from pin 1 to pin 2

Figure 8  IEC61000-4-2 : $V_{CL} = f(t)$, 15 kV negative pulse from pin 1 to pin 2
Figure 9  Clamping voltage (TLP): $I_{TLP} = f(V_{TLP})$ [1], pin 1 to pin 2
5 Package Information

5.1 TSSLP-2-3 (mm)[3]

1) Dimension applies to plated terminals

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**Figure 10** TSSLP-2-3: Package overview

**Figure 11** TSSLP-2-3 Footprint

**Figure 12** TSSLP-2-3: Packing

**Figure 13** TSSLP-2-3: Marking (example)
5.2 TSLP-2-19 (mm)[3]

1) Dimension applies to plated terminals

Figure 14 TSLP-2-19: Package Overview

Figure 15 TSLP-2-19: Footprint

Figure 16 TSLP-2-19: Packing

Figure 17 TSLP-2-19: Marking (example)
References

[1] Infineon AG - Application Note AN210: Effective ESD Protection Design at System Level Using VF-TLP

[2] Infineon AG - Application Note AN140: ESD Protection for Digital High-Speed Interfaces (HDMI, FireWire, ...) using ESD5V3U1U)

[3] Infineon AG - Recommendations for PCB Assembly of Infineon TSLP and TSSLP Package
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