Dual-phase operation in multiphase buck applications

About this document

Scope and purpose

This document addresses the issue of driving multiple power stages from a single PWM signal. Even with high phase count power controllers (e.g., 16 phases), the need for current delivery has long surpassed the capability of having only one power stage per phase. Instead of deploying multiple controllers or controllers with greater phase count, this document discusses the feasibility of having power stages operating in parallel.

Intended audience

This document is written for design engineers of multiphase buck high current applications requiring a high phase count to support their respective loads.

Table of contents

1 Introduction

The current requirements for contemporary ASICs can be well beyond 1000 A. Power delivery is done with multiphase buck converters in which the phase number scales up with the current demand. For reasonable system efficiency, the thermal design current is in the vicinity of about 40 A. Scaling this number to 1000 A means a multiphase converter of 25 phases. For a 2000 A system, it would require 50 phases.

The issue at hand is that there are no controllers available for such a high phase count. However, that does not prevent from designing multiple phases per PWM output. In this paper, the different approaches will be discussed and compared. The dual-phase approach will be evaluated thoroughly.

2 Comparison of alternative solutions

The different solutions for delivering high current are shown in below table:

Table 1 Solutions for high current buck converter

Solution	Benefit	Drawback	Comment
Traditional	Small ripple, known topology	Requires master-slave controllers, extensive routing of signals	The layout will become unwieldy, therefore multiple controllers are required.
Phase doubler	Doubles the phase count for one controller PWM	Requires additional doubler ICs, dynamic current balance concern as impacted by 2nd power stage	The phase doubler ICs have to be routed in addition at twice the desired switching frequency.
Dual phases	Doubles phase count and simplifies routing	Higher steady-state ripple	Each PWM output drives two phases. Least hardware is required.

The multiphase buck converter for four output phases is depicted here:

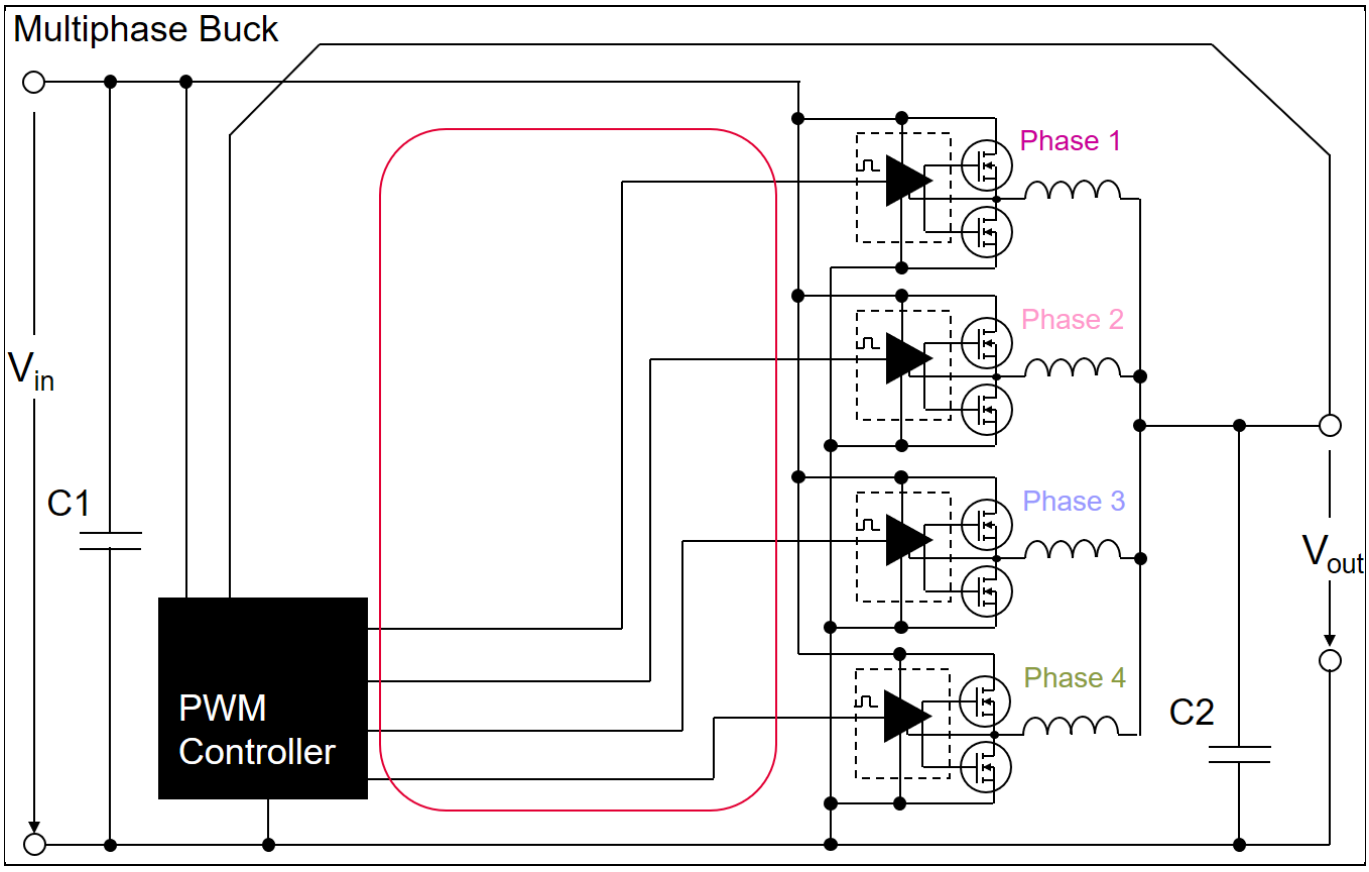

Figure 1 Traditional multiphase buck converter circuit

Comparison of alternative solutions

The figure below shows the implementation of the four phase buck with phase doublers.

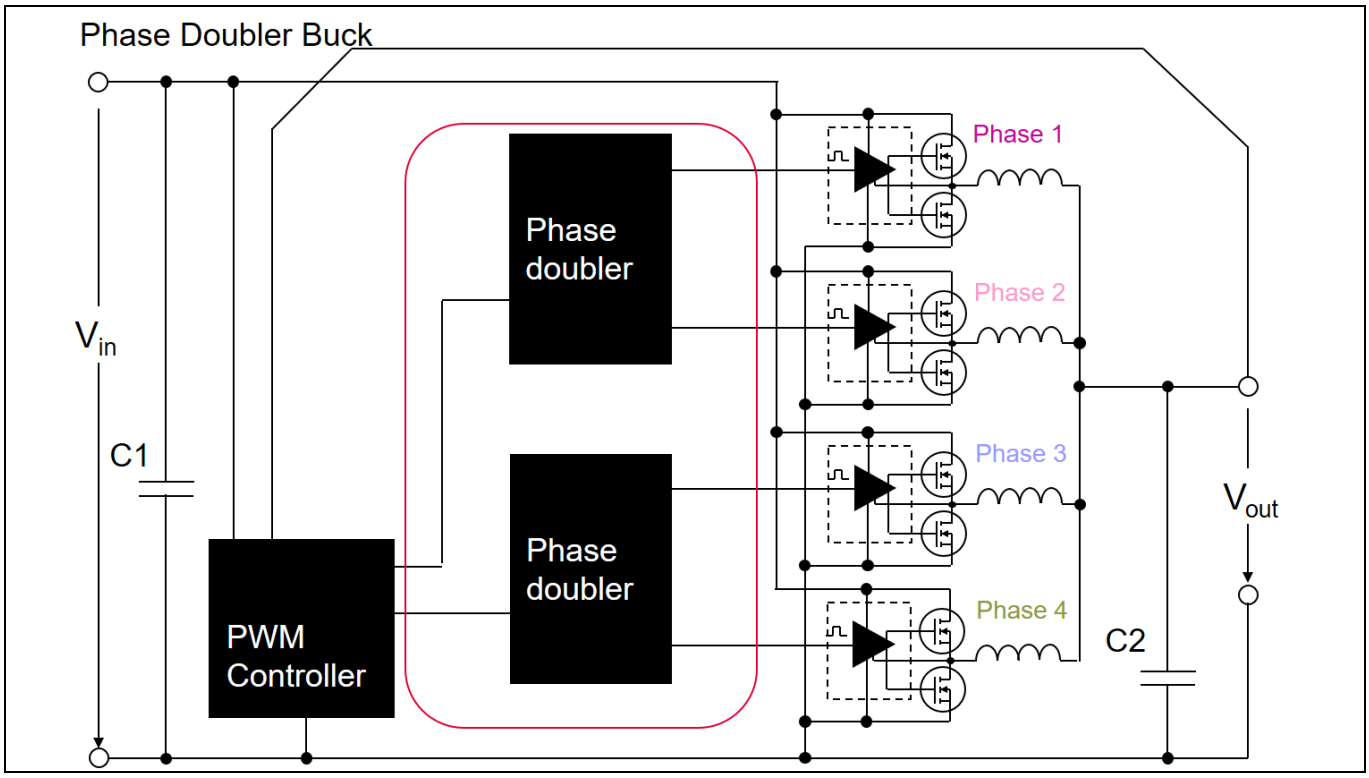

Figure 2 Multiphase buck converter circuit using phase doubler circuits

The dual-phase buck with four output phases is given as an example below.

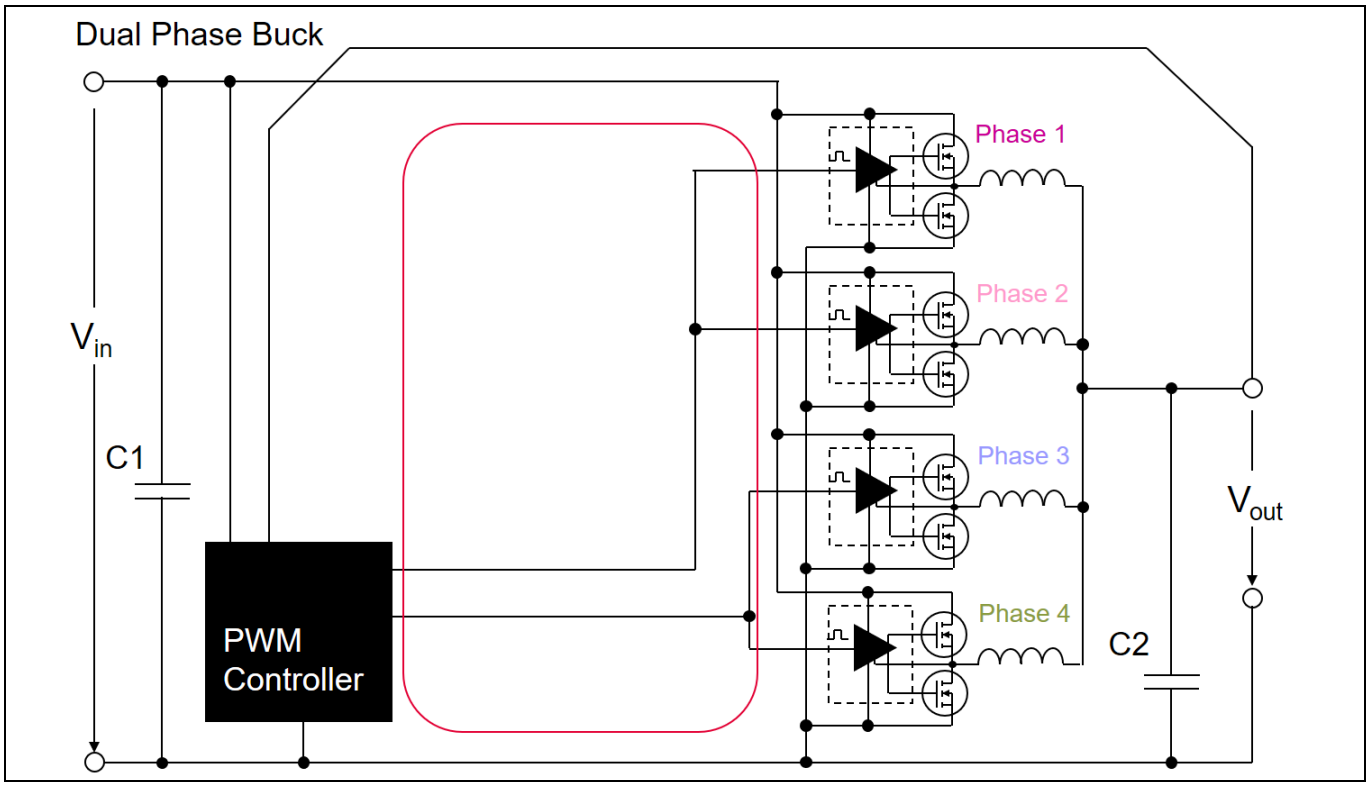

Figure 3 Multiphase buck converter circuit with dual-phase implementation

2.1 Steady-state ripple

When using a dual-phase approach, since only half of the phases are interleaved with each other, the steady-state worst case ripple current is increased compared to the traditional approach of the same phase count by a factor of four resulting from having half of the multiphase frequency and half of the effective phase inductance per switching event.

However, when quantifying the absolute value of ripple voltage for a minimum required output capacitance for any approach, it becomes clear that this is not a limitation.

Even in an eight-phase system this is not an issue:

Conditions:

V_{in} = 12 V, V_{out} = 1 V, L = 100 nH, fsw = 500 kHz, N = 8, C_{out} = 100 uF (a reference value to scale the total C_{out})

Calculation of the ripple current for that condition with 16 phases yields a current ripple of 3.33 A.

For the dual-phase approach the current ripple becomes 13.33 A.

The resulting output capacitance related voltage ripple for an ideal 100 uF capacitance is for the 16 phase traditional approach: 0.52 mV and for the dual-phase approach 4.15mV.

Considering the ESR of the output capacitors the ratio between the dual-phase approach ripple and the traditional approach becomes smaller.

The takeaway is that in high current systems where 16 phases are required, the transient support requires several Millifarad output capacitance, i.e. the calculated numbers will be reduced by over one order of magnitude.

Therefore, it becomes irrelevant, if the supply is done by a dual-phase system or a traditional one as the minimum required capacitance for the transient support is much larger than the requirements imposed on the voltage ripple. This trend gets stronger with higher phase count, so that it has no penalty on the circuit performance.

Calculation:

The output ripple current of a multiphase buck converter depends on the switching frequency, input and output voltages, the inductor values and the effective duty cycle of the combined phases.

Latter one can be calculated as:

$$D\_\text{eff} = 1 - ((1 - D) \cdot N - FLOOR\big((1 - D) \cdot N\big)) \quad (1)$$

An equivalent input voltage for multiphase calculation results from:

$$V_{IN\_multiphase} = \frac{V_{\text{out}}}{D_{\text{eff}}}$$

The ripple current per phase is given as:

$$\Delta \mathrm{I}_{ph} = \mathrm{D} \cdot \frac{Vin - Vout}{L \cdot f_{sw}} \quad (2)$$

The multiphase ripple current is then the result of all overlapping currents of all phases:

Assuming evenly spaced phase firing, the multiphase ripple current is:

Comparison of alternative solutions

$$N_{maxSimultaneousOn} = FLOOR(D \cdot N) + IF(D \cdot N - FLOOR(D \cdot N) = 0{,}0{,}1) \quad (3)$$

$$N_{minSimultaneousOn} = N_{maxSimultaneousOn} + IF(D \cdot N - FLOOR(D \cdot N) = 0{,}0{,}-1) \quad (4)$$

$$N_{maxSimultaneousOff} = N - N_{minSimultaneousOn} \quad (5)$$

Now the di/dt for the single-phase emulation can be obtained.

$$\left.\frac{di}{dt}\right|_{on} = \frac{Vin-Vout}{L} \quad (6)$$

$$\left.\frac{di}{dt}\right|_{off} = \frac{-Vout}{L} \quad (7)$$

$$\left.\frac{di}{dt}\right|_{eff\_off} = N_{minSimultaneousOn} \cdot \left.\frac{di}{dt}\right|_{on} + N_{maxSimultaneousOff} \cdot \left.\frac{di}{dt}\right|_{off} \quad (8)$$

$$I_{MultiphaseRipple} = \frac{(1-D\_\mathrm{eff})}{N \cdot fsw} \cdot \left|\left.\frac{di}{dt}\right|_{eff\_off}\right| \quad (9)$$

For the example parameters given, the multiphase output ripple current evaluates to be:

$$D = 1/12 \quad (10)$$

$$D_{\mathrm{eff}} = 1 - \left(\left(1 - \frac{1}{12}\right) \cdot 8 - FLOOR\left(\left(1 - \frac{1}{12}\right) \cdot 8\right)\right) = \frac{2}{3} \quad (11)$$

$$\Delta \mathrm{I}_{ph} = \frac{12\ \mathrm{V} - 1\ V}{12 \cdot 100\ nH \cdot 500\ kHz} = \frac{11\ kA}{600} = 18.3\ A \quad (12)$$

$$N_{maxSimultaneousOn} = 1 \quad (13)$$

$$N_{minSimultaneousOn} = 0 \quad (14)$$

$$N_{maxSimultaneousOff} = 8 \quad (15)$$

$$\left.\frac{di}{dt}\right|_{on} = \frac{11\ V}{100\ nH} \quad (16)$$

$$\left.\frac{di}{dt}\right|_{off} = \frac{-1\ V}{100\ nH} \quad (17)$$

$$\left.\frac{di}{dt}\right|_{eff\_off} = -0.08 \frac{A}{ns} \quad (18)$$

$$I_{MultiphaseRipple} = \frac{(1-2/3)}{4\ MHz} \cdot 0.08 \frac{A}{ns} = \frac{20}{3} A = 6.67\ A \quad (19)$$

For the aforementioned operating conditions the ripple current has been plotted against the phase count:

Comparison of alternative solutions

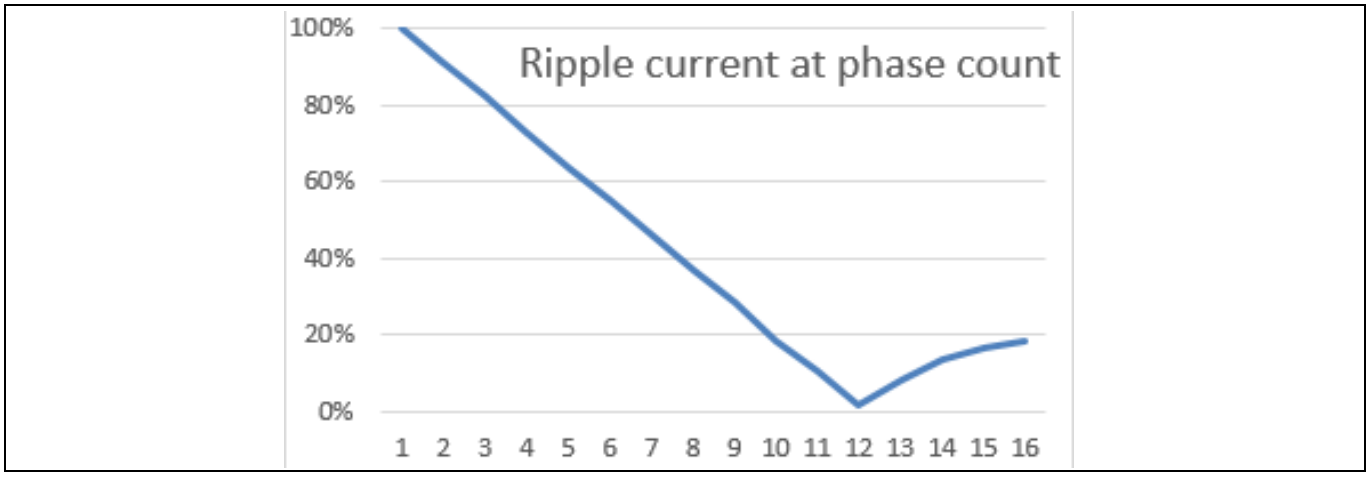

Figure 4 Output ripple current as function of phase count

In case of a dual-phase setup, the eight phases would result in 4 dual phases with 50nH resulting inductance per dual phase.

$$D\_eff\_dualPh = \frac{1}{3} \quad (20)$$

$$N_{maxSimultaneousOn} = 1 \quad (21)$$

$$N_{minSimultaneousOn} = 0 \quad (22)$$

$$N_{maxSimultaneousOff} = 4 \quad (23)$$

$$\left.\frac{di}{dt}\right|_{on} = \frac{11\,V}{50\,nH} \quad (24)$$

$$\left.\frac{di}{dt}\right|_{off} = \frac{-1\,V}{50\,nH} \quad (25)$$

$$\left.\frac{di}{dt}\right|_{eff\_off} = -\frac{4\,V}{50\,nH} \quad (26)$$

$$I_{MultiphaseRipple} = \frac{(1-1/3)}{2\,MHz} \cdot 0.08\frac{A}{ns} = \frac{0.16\,A}{6\,ns} = 26.67\,A \quad (27)$$

The calculation also shows a four times higher multiphase ripple current as expected. Note that this is the ripple current stemming from two simultaneously firing phases.

As the phase count increases to numbers where the dual-phase solution is needed, for example 32 phases, the ripple current for the given condition is then:

$$D\_eff\_32 = \frac{2}{3} \quad (28)$$

$$N_{maxSimultaneousOn\_32} = 3 \quad (29)$$

$$N_{minSimultaneousOn\_32} = 2 \quad (30)$$

$$N_{maxSimultaneousOff} = 30 \quad (31)$$

$$\left.\frac{di}{dt}\right|_{on\_32} = \frac{11\,V}{100\,nH} \quad (32)$$

Comparison of alternative solutions

$$\left.\frac{di}{dt}\right|_{off\_32} = \frac{-1\,V}{100\,nH} \tag{33}$$

$$\left.\frac{di}{dt}\right|_{eff\_off\_32} = -\frac{8\,V}{100\,nH} \tag{34}$$

$$I_{MultiphaseRipple\_32} = \frac{1/3}{32 \cdot 500\,\text{kHz}} \cdot \frac{8\,V}{100\,nH} = \frac{1}{600\,\text{Hz}} \cdot \frac{V}{H} = 1.67A \tag{35}$$

With a dual-phase approach this number will increase to:

$$D\_eff\_16 = \frac{1}{3} \tag{36}$$

$$N_{maxSimultaneousOn\_16} = 2 \tag{37}$$

$$N_{minSimultaneousOn\_16} = 1 \tag{38}$$

$$N_{maxSimultaneousOff\_16} = 15 \tag{39}$$

$$\left.\frac{di}{dt}\right|_{on\_16} = \frac{11\,V}{50\,nH} \tag{40}$$

$$\left.\frac{di}{dt}\right|_{off\_16} = \frac{-1\,V}{50\,nH} \tag{41}$$

$$\left.\frac{di}{dt}\right|_{eff_{off\_16}} = -\frac{4\,V}{50\,nH} \tag{42}$$

$$I_{MultiphaseRipple\_16} = \frac{1}{150\,MHz} \cdot \frac{1\,V}{1\,nH} = \frac{1\,\text{kA}}{150} = 6.67A \tag{43}$$

This is again four times the ripple of the 32 phase traditional approach and well within a reasonable range.

2.2 Transient performance

In a dual-phase fixed-frequency system the worst case delay to a transient is the time it take for the next switching pulse to be issued after the last pulse has become low. That time is half of the switching period, i.e. 1.25 us at 500 kHz switching frequency. However, during a transient event the non-linear transient support features of the controller are being enabled. They will drive the PWM outputs simultaneously by either increasing the switching frequency momentarily or by adding additional pulses before the next scheduled fixed frequency pulse and consequenctly enlarge the effective duty cycle. Therefore, the dual-phase arrangement will observe the same transient support as the conventional setup.

The phase doubler cannot drive all PWM outputs simultaneously as by hardware design, half of the phases are always in off-state. In addition, the phase doubler IC itself has some propagation delay (typically > 10ns), thus slightly reducing the phase margin of the phase doubler solution.

2.3 Current sharing

The controller handles current sharing based on the current information provided for each of its PWM outputs. Therefore, the traditional approach, a single-phase per PWM, is the benchmark.

In case of phase doubler and dual-phase setup, two power stages report a shared current information to the controller. Therefore, the accuracy of the OC-threshold set in the controller depends on the precision of current balancing between these two phases.

Comparison of alternative solutions

Having a phase doubler always requires to feed an average current signal of these two phases back to the controller. Otherwise it would be possible for one unmonitored phase to act on repetitive transients stronger than other phases and effectively run into a fault condition.

With the dual-phase approach, this is not possible because the connected phases are being driven simultaneously. Therefore, the current reported by one phase is approximately identical to the current in the other phase. It is still advisable to average the current information to improve accuracy in case of some small steady offset. For any design it is advisable to design with possible phase imbalance in mind, i.e. to set the design target for a dual-phase design lower by for example 5 A compared to a conventional design.

The current of the phases sharing the same PWM output is fed back to the controller as an averaged signal.

Here, the schematic of the current sharing connection on **TDA21472** power stages is shown.

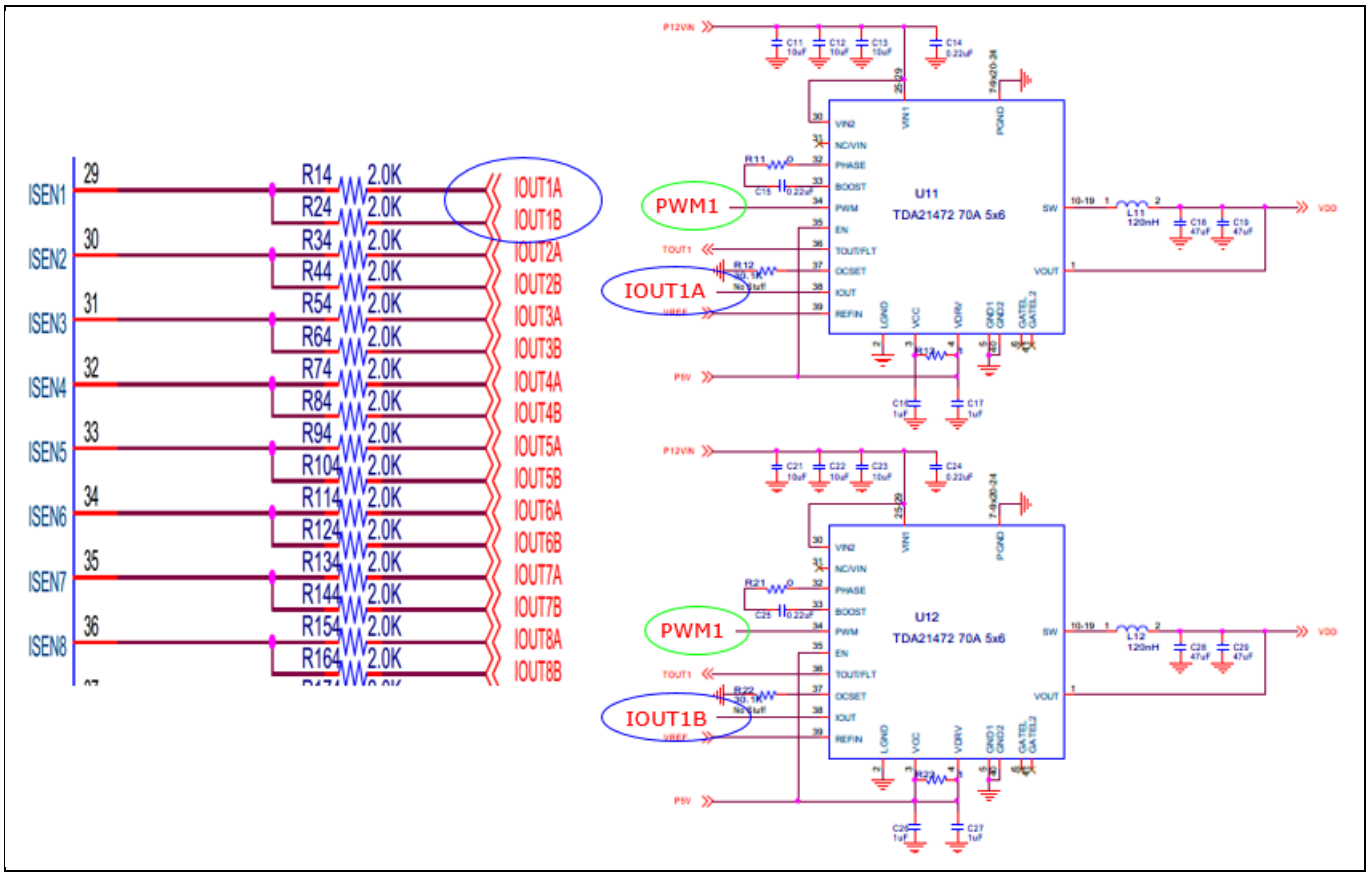

Figure 5 Dual-phase connection of power stages driven from the same PWM output

Since the controller gets an averaged signal of the two connected phases per PWM, it is receiving only half of the total current. Consequently, the controller has to be setup to scale the current information by a factor of two, or the system has to take into account that only half the current is being reported.

If the controller does not account for the doubling in current, this has to be considered when setting the loadline target value.

In theory, with identical power stages and controller defined minimum pulses, it is not possible to observe a runaway of current in one of the power stages compared to the other as the higher current will result in a higher dissipation for otherwise identical conditions and hence is self-limiting.

The current mismatch between power stages in dual-phase arrangement where both power stages have the same driving conditions and supply voltages results from the timing mismatch of the PWM to switching node.

Comparison of alternative solutions

The timing mismatch leads to different duty cycles for both phases and has the effect of having different average output voltages at the phase nodes. This voltage difference drives a current between the connected power stages. This current is an accumulated DC current and limited by the impedances between the power stage phase nodes (DCR of both inductors, pcb resistances, power stage switch node interconnect resistances). Additionally, the higher current leads to a bigger voltage drop for the input voltage to the power stages. This means that the actual voltage of the power stage with the bigger effective duty cycle also has a lower actual input voltage leading to an additional balancing effect.

The calculation for the integrated power stages **TDA21470**, **TDA21472** and **TDA21475**, for example, yields that, considering a worst case design mismatch for the on-time with a +/-3 sigma distribution, the current mismatch between the dual phases is limited to 6.9 A at 500 kHz switching frequency. The current imbalance increases linearly over switching frequency.

For the design target current the value should be chosen to be below the current value for the traditional approach by half of the calculated current imbalance value.

In the following, test results for current sharing among PWM connected phases are shown.

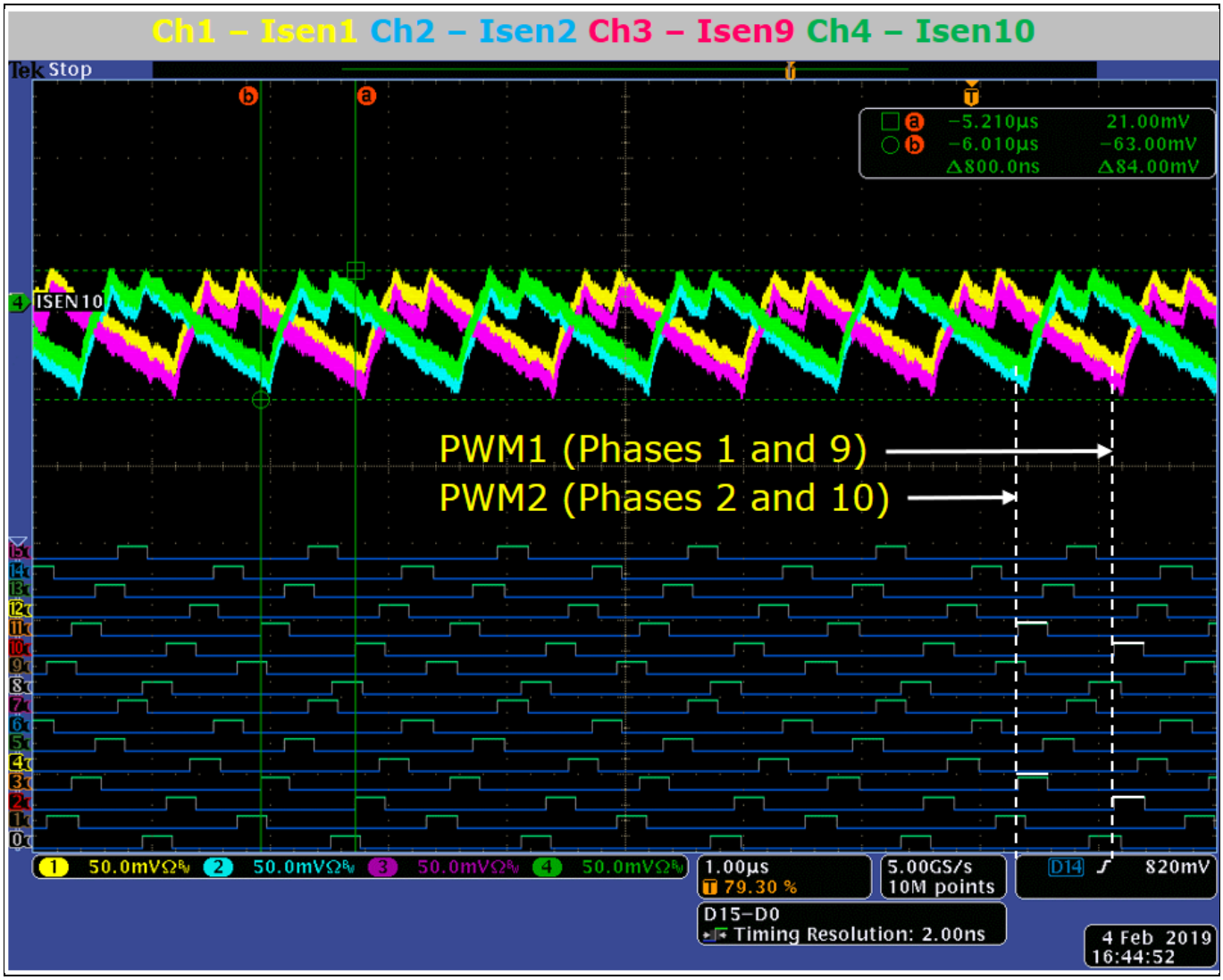

Figure 6 Phase current balance in steady-state for phases located on opposite sides of the load

It can be seen that there is very little difference between the connected phases. The imbalance here is about 2 A. The current relationship stays constant as every phase follows the same PWM pulse width.

Comparison of alternative solutions

This is expected when the power stages are of the same type and the operating conditions are identical, i.e. input and output voltage, inductance and board temperature are equal while the PWM signal is applied to both power stages.

In dynamic conditions the consideration does not change as everything is still the same for both connected power stages. A minimum pulse width at the PWM ensures that both power stages either issue a pulse to the switching node or they do not. Hence, the current is expected to also track nicely through any dynamic condition. In the following, a step load of 300 A has been applied repetitively at 300 Hz and the currents in the PWM connected phases at opposite sides of the load have been monitored.

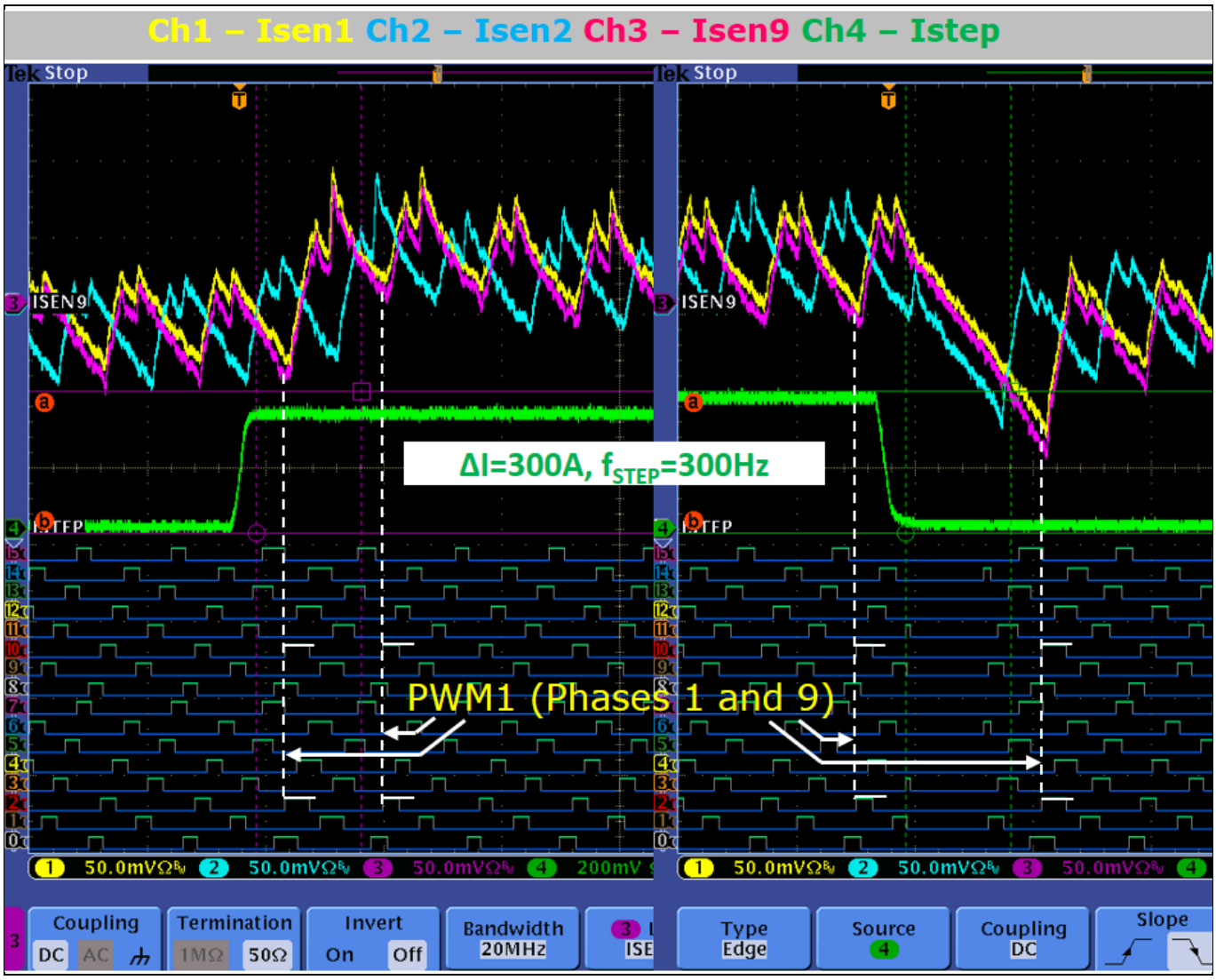

Figure 7 Phase current balance of opposite phases during a 300 A load step

It can be concluded that the dynamic phase sharing also works very well.

Comparison of alternative solutions

Investigations of dynamic situations at 10 kHz, 50 kHz, 100 kHz and 200 kHz load step frequencies have not shown any abnormal behavior as outlined in the following figures.

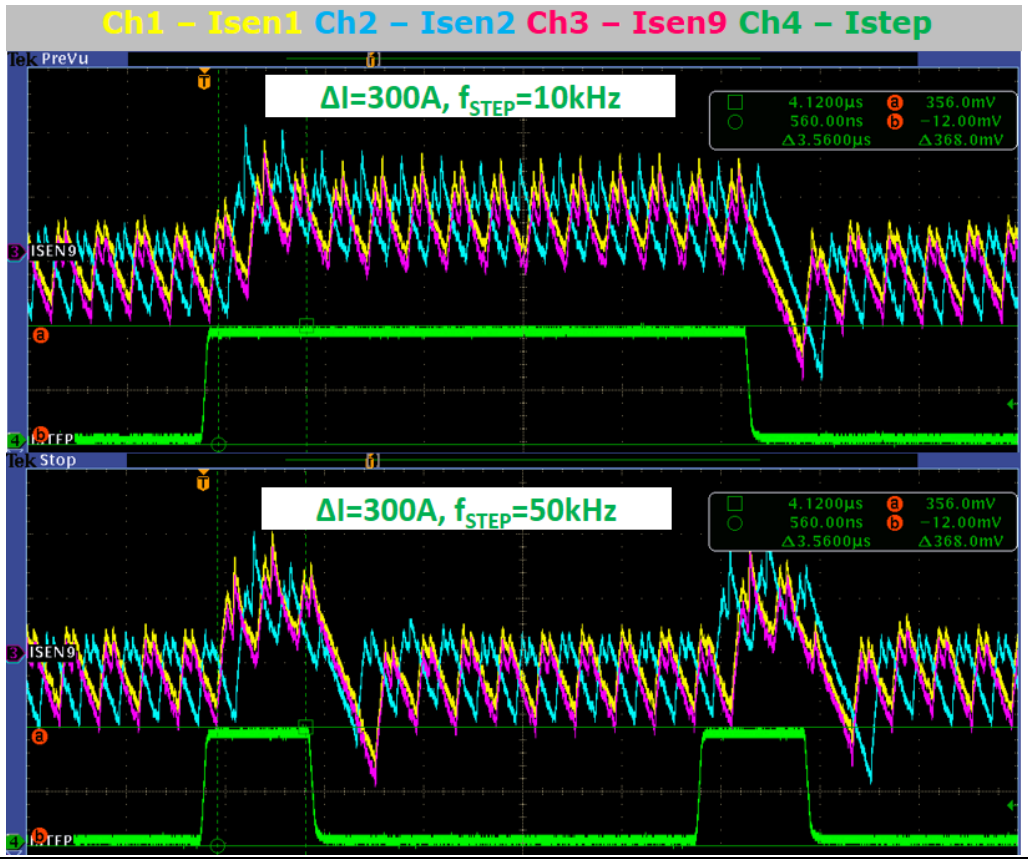

Figure 8 **Phase current balance of opposite phases during a 300 A load step at 10 kHz and 50 kHz**

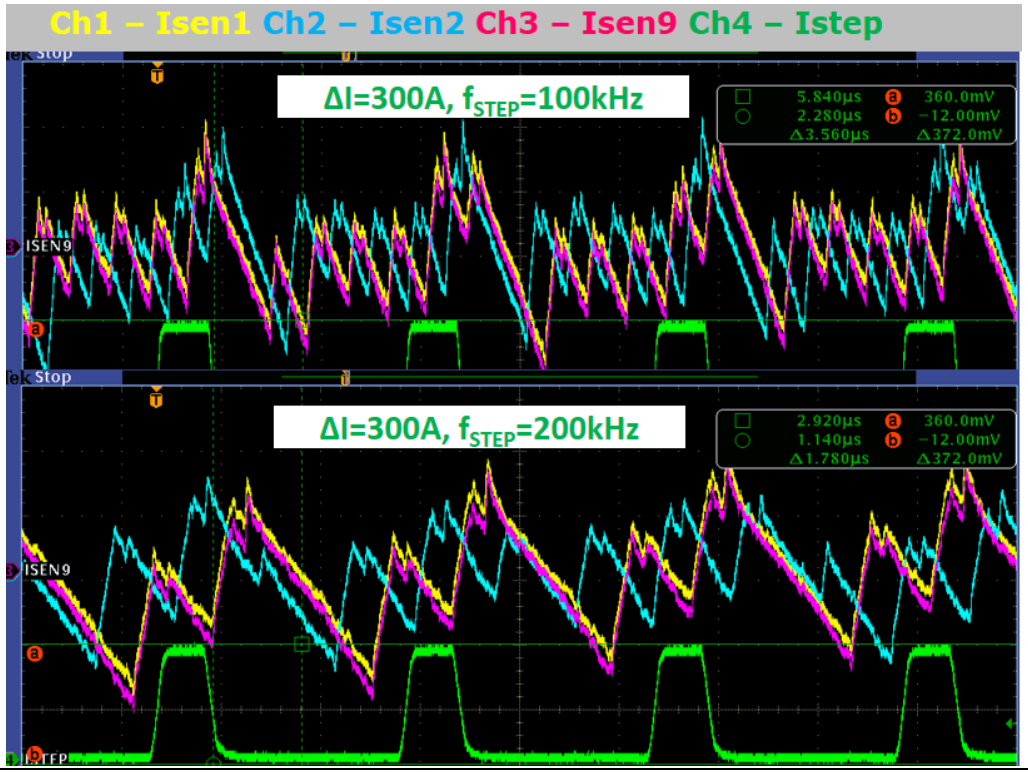

Figure 9 **Phase current balance of opposite phases during a 300 A load step at 100 kHz and 200 kHz**

Comparison of alternative solutions

The dynamic waveforms do not show any additional current imbalance that can be attributed to the transient events. Since it has been proven that current sharing is very good regardless of the phase locations, it is advisable to place the shared phases onto opposite ends to mitigate current commutations across the board.

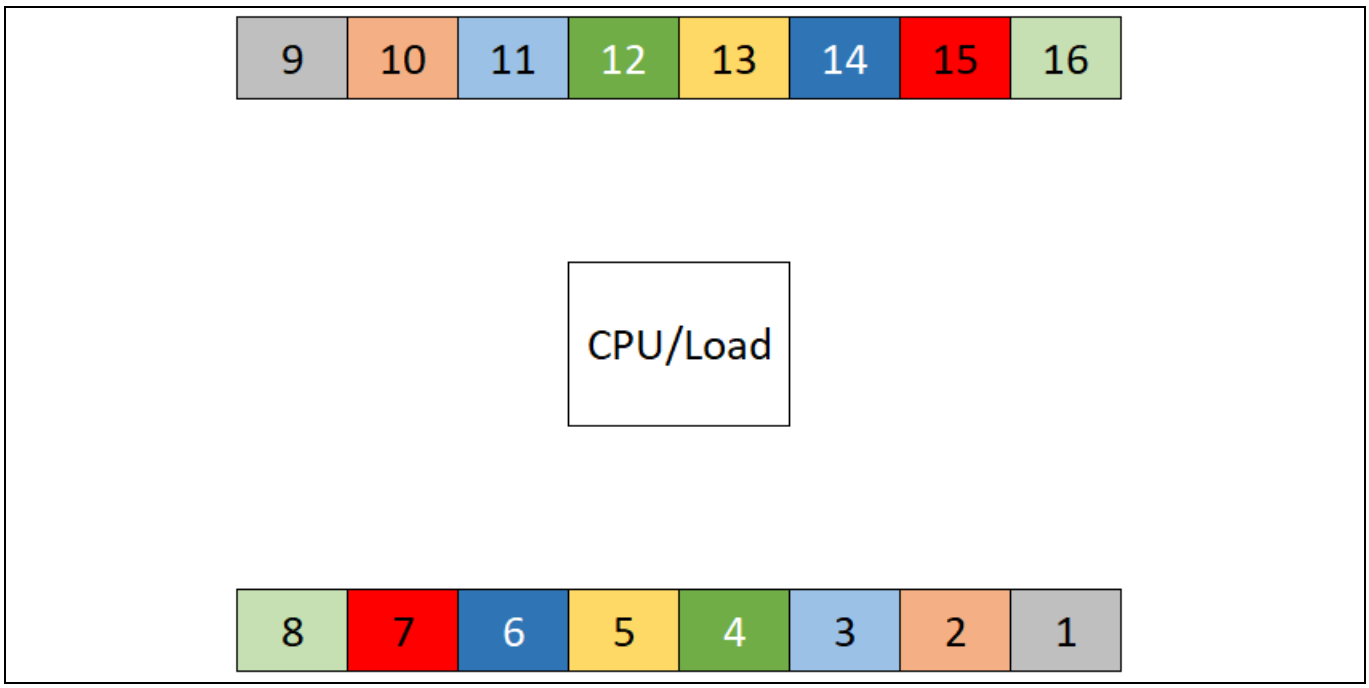

Figure 10 Proposed phase arrangement on an application board for best dynamic results

To understand this proposal, one can envision that the current at any given time is being delivered to the load from opposite locations, i.e. though separate copper planes. This means that each power stage has the maximum amount of copper for conduction available. This results in lowering the effective distribution impedance of the pcb.

If the design focus is on layout simplicity or for cases where a substantial input voltage difference across the pcb exists, then the dual phases can be treated as an equivalent single-phase and placed adjacent to each other. This will allow for routing with the least signal traces back to the controller at the expense of less balanced current between the dual phases.

2.4 Layout

The phase doubler has a controller with half the phases but requires external phase doubler ICs to drive the power stages individually. That adds to layout complexity.

The dual-phase approach is by far the easiest to design. It uses minimal hardware (controller with half the phases, no external doubler circuit).

In order to quantify the layout constraints that need to beimposed, tests on the demo board DB326 have been performed. The controller is an 8-phase device while the board was setup to switch 16 phases.

The following figure shows the board.

Comparison of alternative solutions

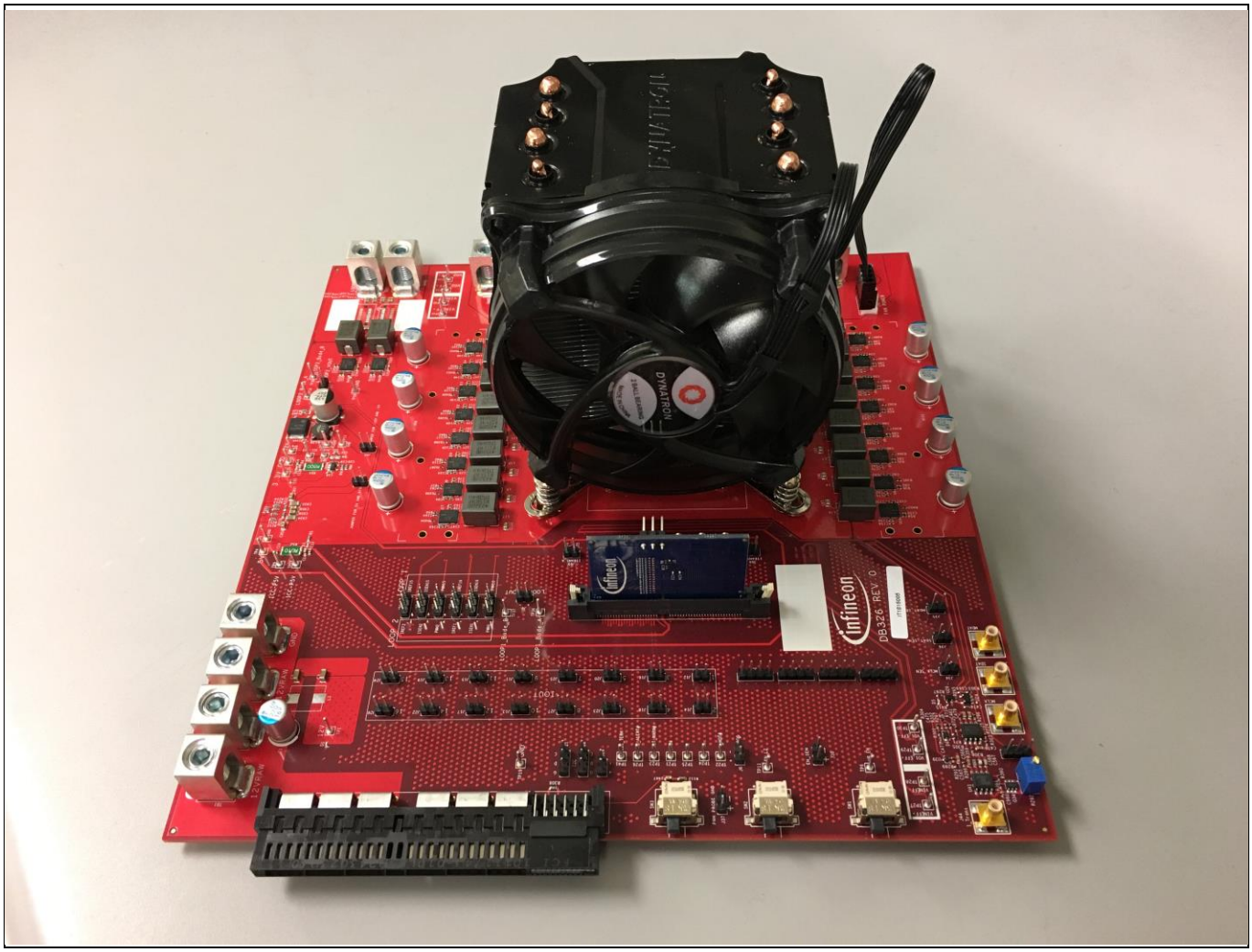

Figure 11 Demo board DB326

For the investigation the physical phase assignments are critical.

Table 2 Phase assignments

PWM output	1	2	3	4	5	6	7	8
Phases	1 and 9	2 and 10	3 and 11	4 and 12	5 and 13	6 and 14	7 and 15	8 and 16

Comparison of alternative solutions

The physical arrangement of the 16 phases around the load is shown in the figure below.

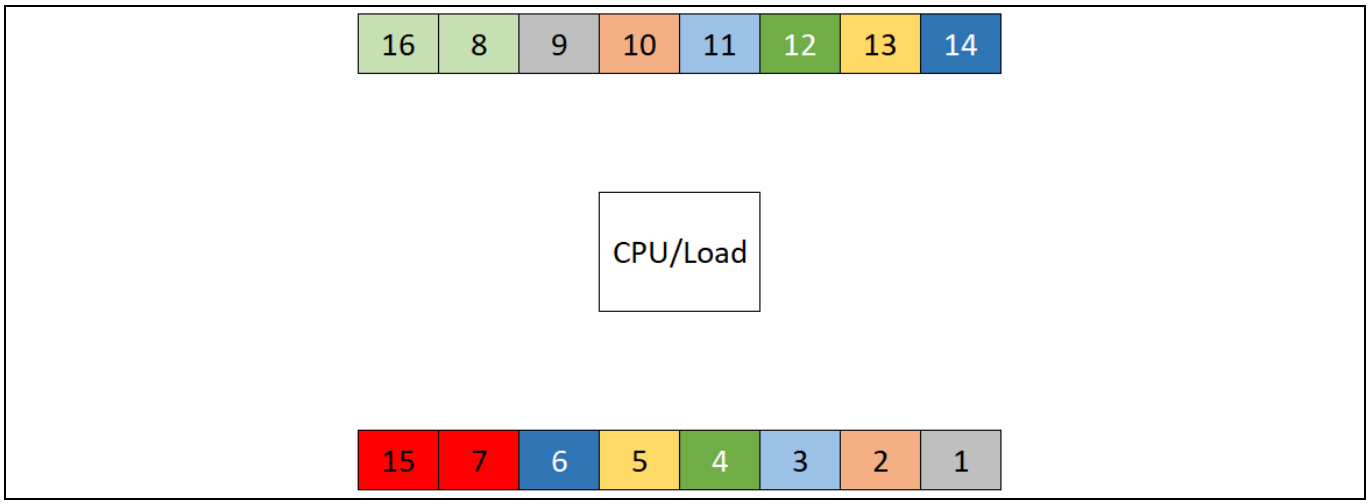

Figure 12 Phase arrangement on the 16-phase demo board DB326

It can be seen that phases 7/15 and 8/16 are adjacent to each other while all other phases are on opposite sides of the load. This provided an opportunity to study the phase imbalance caused by phase arrangements.

In conclusion, to achieve the best phase current balance among paralleled power stages, these power stages should have a maximum impedance between their outputs. With only one PWM signal driven and one common current reported, an inherent imbalance will manifest in different average voltages at their respective switching nodes, driving a DC current between these power stages. If they are placed side by side, the impedance is very small and the current due to imbalance is higher compared to power stages on opposite ends of the board.

The parasitics on the board between phases 7/15 and 8/16 are minimal, so that the potential worst case DC current imbalance is expected to be found in these phases.

Comparison of alternative solutions

Next, the power section of the board with phase assignments is shown.

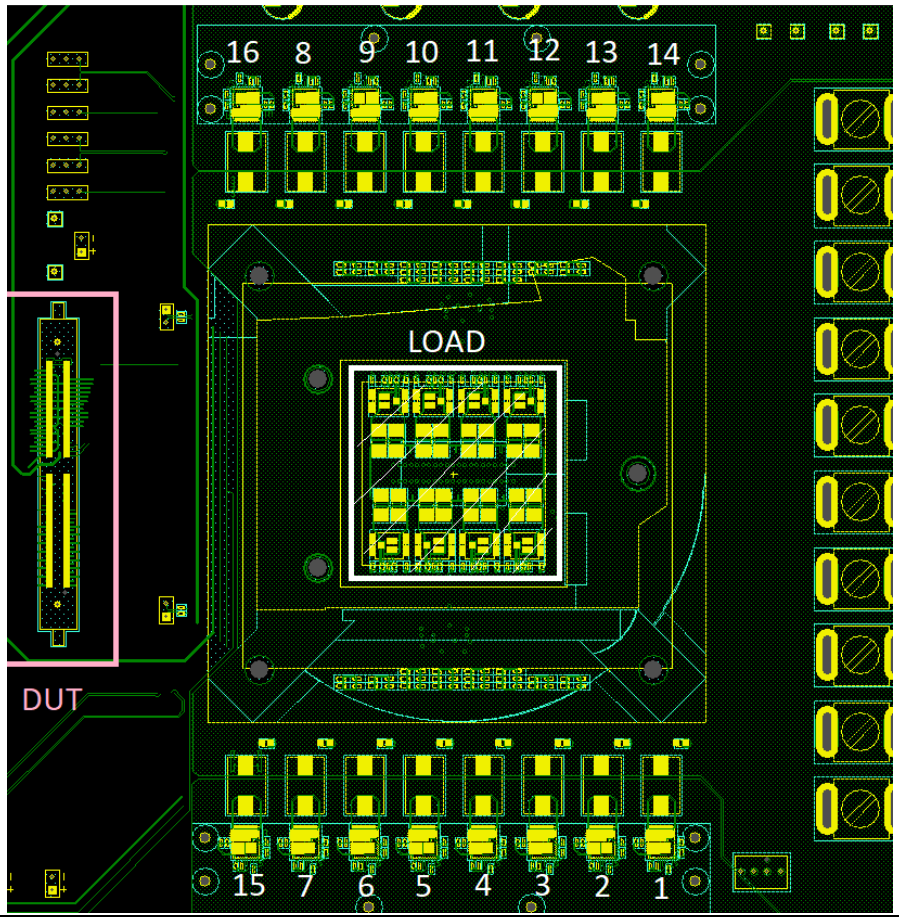

Figure 13 Demo board DB326, components and power layout

Based on these finding the recommendation for how to arrange dual phases for 16 PWM outputs on a double sided design is the following:

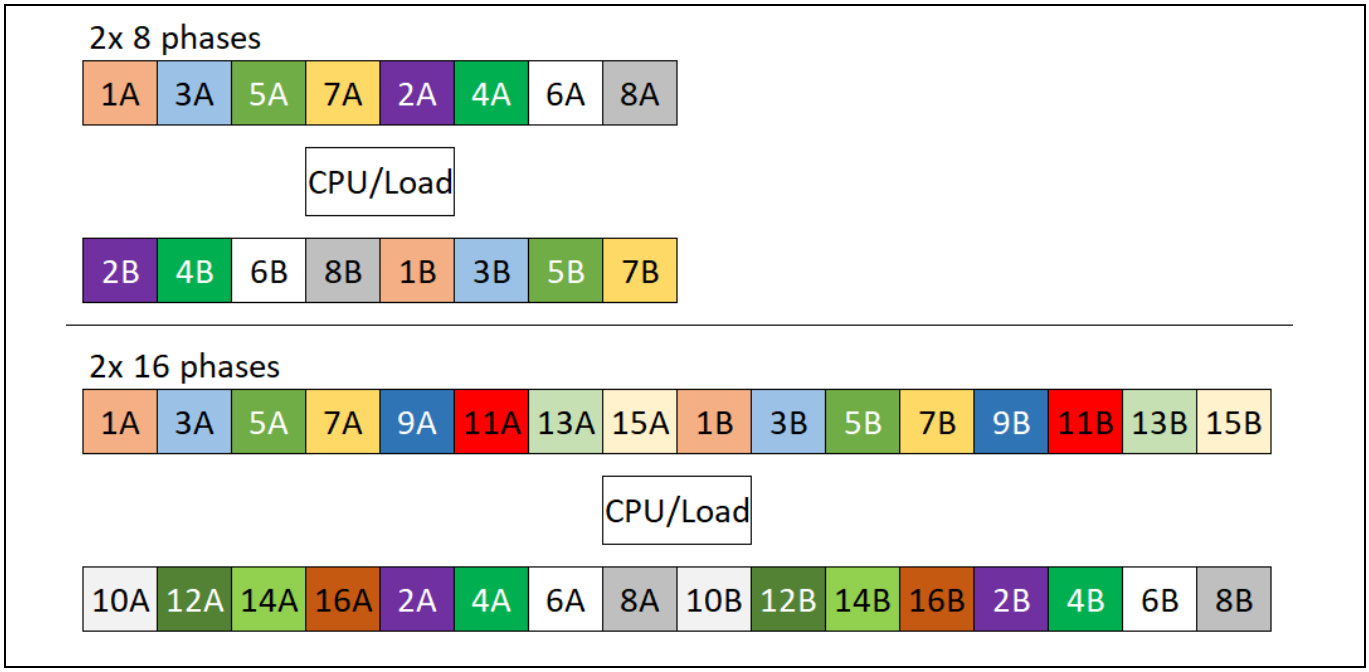

Figure 14 Recommendation for dual-phase layout in a double sided supply

Comparison of alternative solutions

Phases xA and xB are to be tied together into the dual-phase operation. The top phase alignment is for 16 phases controlled by an 8-phase controller and the bottom arrangement is for 32 phases driven by a 16-phase controller.

2.5 Efficiency

Efficiency differences can be explained by two aspects:

1: Bias power consumption

- The dual-phase setup requires the least bias power as it drives the least number of phases.
- The phase doubler uses the highest bias power because each doubler circuit needs to be supplied in addition to the controller.

2: Ripple current loss

- The ripple current is higher with the dual-phase approach compared to the alternatives. For the aforementioned example of a switching frequency of 500 kHz the output current ripple is 3.33 A in the traditional case and 13.33 A in the dual-phase setup. The ripple current related power loss of the dual-phase setup is therefore four time higher compared to the traditional setup. However, if quantified, it will be see that the value is still negligible compared to all other loss factors:

Assumption: ESR_effective = 1 mOhm (44)

$$P_{CoutESR} = ESR \cdot \frac{\Delta I_{ripple}^2}{12} \quad (45)$$

$$P_{CoutESR} = 1mOhm \cdot \frac{(13.33A)^2}{12} = 14.8\,mW \quad (46)$$

2.6 Fault handling

Each power stage reports faults onto a common fault input. This logic is in an OR logic configuration among the power stages. The additional power stages for dual phase will simply be added to that connection. If they encounter a failure, it still will be reported to the controller in the same way.

3 Summary

The document has shown a superior solution for high phase count multiphase buck converter to achive a very high output current with controllers of a much smaller phase count. The example here was given for a dual-phase PWM but the general concept can be enhanced to even more combined phases.

To sum up, below are the key takeaways:

- By using a dual-phase system additional complex hardware is not required.
- Transient performance equivalent to the traditional converter is maintained.
- Output voltage ripple performance is sacrificed but is by far not a limiting criterion.
- Cost benefits can be obtained by having a smaller controller, no additional phase doubler circuits, reduced board space and less complexity routing the design.
- Fault reporting is not impacted.
- Current sharing is very well maintained.
- In summary, for any multiphase application using more than 16 phases, the dual-phase design is a recommended solution for achieving great performance with reduced circuit complexity.

Revision history

Document version	Date of release	Description of changes
V 1.0	10-07-2020	First release

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