EVAL_ISO_2DIB0410F user manual

Evaluation board for Infineon ISOFACE™ dual-channel digital isolators

About this document

Scope and purpose

This document introduces the Infineon ISOFACE™ dual-channel digital isolators and describes how to evaluate their performance by using the evaluation board EVAL_ISO_2DIB0410F.

Intended audience

This document is intended for design engineers who want to design high-voltage (HV) applications with Infineon digital isolators for isolation purposes.

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1 Introduction of Infineon ISOFACE™ dual-channel digital isolators

Isolation provides safety in HV applications and improves electrical noise immunity. To meet the continually growing requirements for isolation products, Infineon Technologies offers ISOFACE™ dual-channel digital isolators with the highest robustness, most accurate timing performance and lowest power consumption. This product family, based on coreless transformer (CT) technology, uses two coils stacked on top of each other with SiO_2 as insulation material in between, and has the following features:

- RoHS-compliant PG-DSO-8 narrow-body 150 mil package
- High common-mode transient immunity greater than 100 kV/µs
- Wide supply voltage range, from 2.7 to 6.5 V (absolute maximum 7.5 V)
- Accurate timing, with 26 ns typical propagation delay and -4/+6 ns spread
- Low power consumption with maximum 3.3 mA at 3.3 V and 1 Mbps
- CMOS variable and TTL fixed input thresholds options available
- Pin-to-pin compatible with all dual-channel digital isolator products in SOIC-8 narrow-body package (150 mil) available on the market

This digital isolator family includes the following product variants:

Table 1 Product variants of Infineon ISOFACE™ dual-channel digital isolator family

Part number	Channel configuration	Input thresholds	Default output state	Isolation rating	Package
2DIB0400F	2 forward 0 reverse (2+0)	Variable (CMOS)	Low	V_{ISO} = 3000 V_{RMS} (UL1577 Ed. 5)	PG-DSO-8 150 mil 5 x 4 mm
2DIB0401F			High		
2DIB1400F	1 forward 1 reverse (1+1)		Low		
2DIB1401F			High		
2DIB0410F	2 forward 0 reverse (2+0)	Fixed (TTL)	Low		
2DIB0411F			High		
2DIB1410F	1 forward 1 reverse (1+1)		Low		
2DIB1411F			High		

The target applications are:

- DC-DC bricks in telecom and server power supply systems
- High-side floating PWM signal transfer for GaN with integrated power stage (GaN-IPS)
- Isolated UART and CAN communication

2 Evaluation board EVAL_ISO_2DIB0410F

To make the evaluation of ISOFACE™ dual-channel digital isolators easier, Infineon offers the evaluation board EVAL_ISO_2DIB0410F, as shown in **Figure 1**.

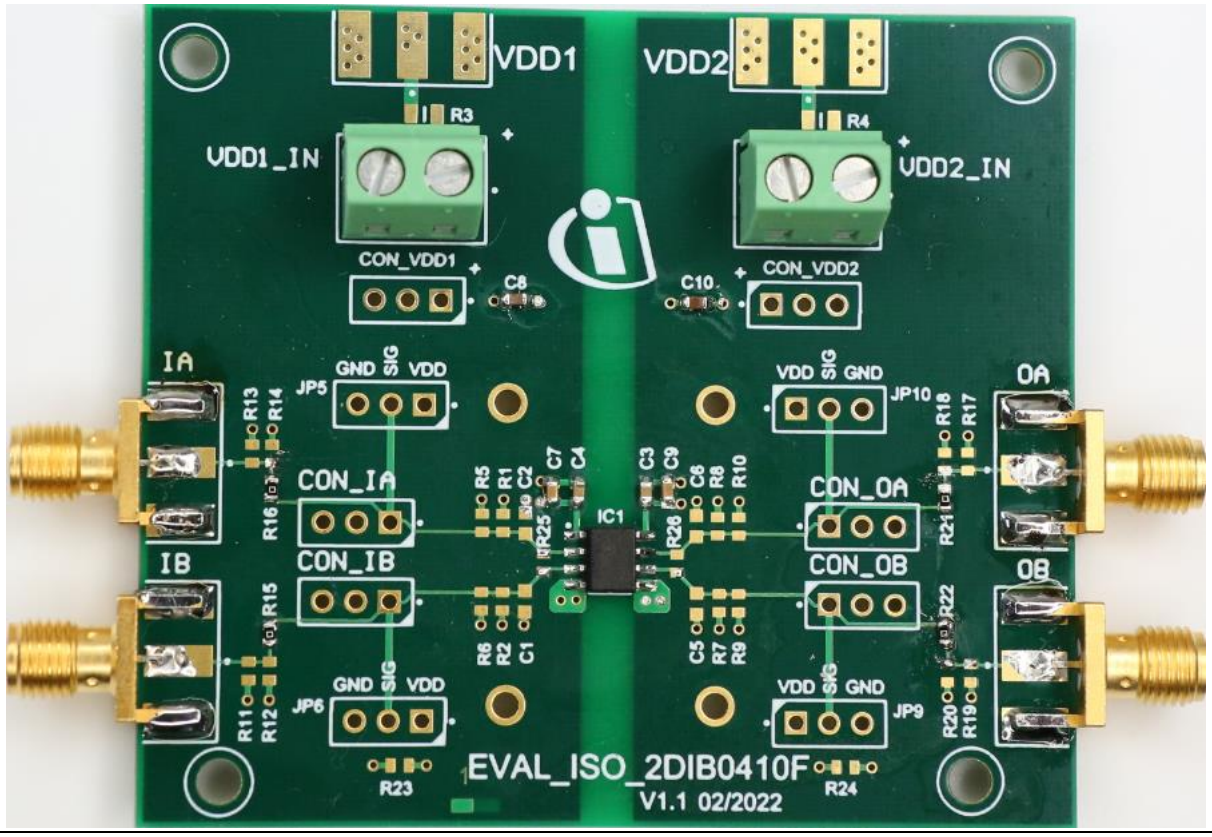


Figure 1 Evaluation board EVAL_ISO_2DIB0410F

This board is designed with a four-layer stack to achieve high EMC performance even at high data-speed operation. Standard FR-4 class epoxy is used as the PCB material. For a more detailed stack specification, please see **chapter 2.1**.

It comes with the digital isolator ISOFACE™ 2DIB0410F (2+0, TTL input threshold, default output low) variant assembled by default. But it can also be used to evaluate other product variants of the dual-channel digital isolator family. However, they are not supplied with the board and must be ordered separately. The evaluation board has the following features:

- Support for high-speed probes to measure all power supply, input and output signals. The connectors are not supplied with the board and must be assembled separately.
- Support for edge-mounted coaxial (SMA) connectors. The SMA connectors are not supplied with the board and must be assembled separately.
- Easy accessibility of input and output pins, e.g., connection of additional filters, load, and pull-up and pull-down resistors. The components must be assembled separately.

For a more detailed description of the features listed above, please see **chapter 3**.

2.1 Board layer stack

To achieve a low-EMI performance even at a high data rate of up to 40 Mbit/s, the board uses a four-layer PCB design:

- Layer 1: high-speed layer
  This layer is intended for high-speed signal traces, for example signal inputs and signal outputs.
- Layer 2: ground layer
  One ground layer is placed in between to provide the shielding effect.
- Layer 3: power layer
  This layer is intended for all power supply traces for the digital isolator.
- Layer 4: ground layer
  As there are no low-speed signal traces available, this layer is designed as the ground layer for better shielding.

The layer stacking is shown in **Figure 2**.

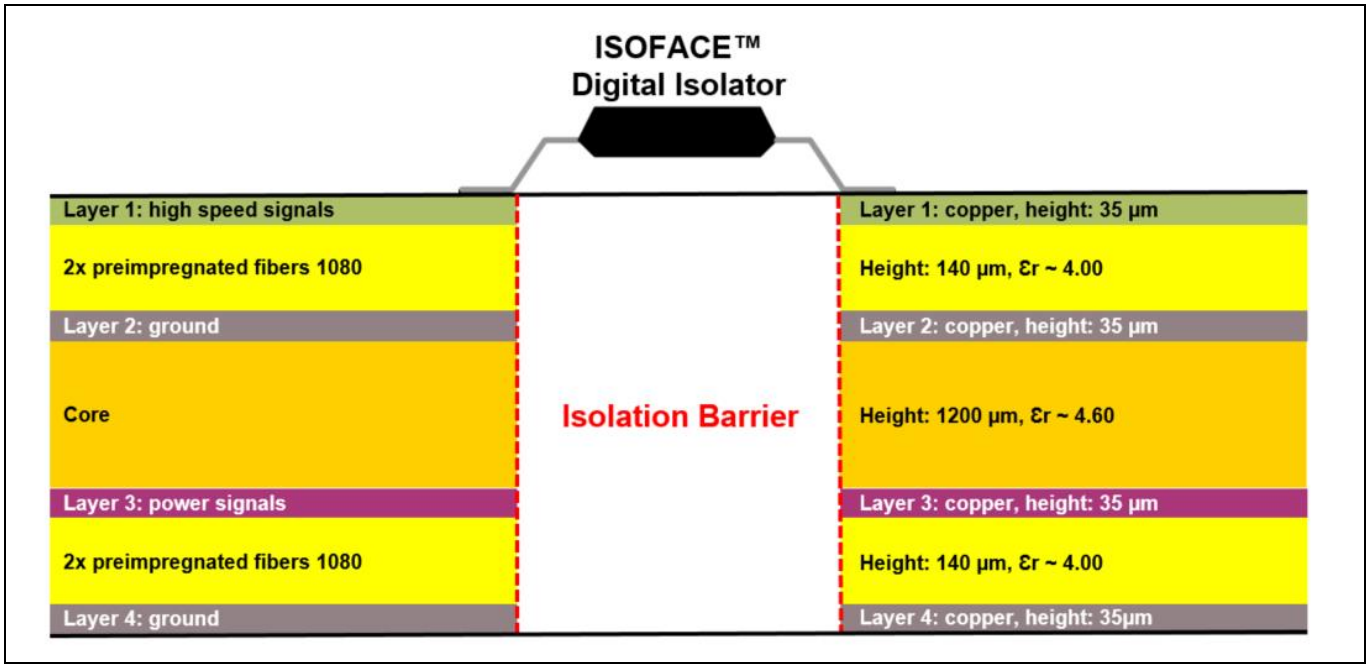


Figure 2 Layer stack of EVAL_ISO_2DIB0410F

2.2 Board schematic

The schematic of the evaluation board EVAL_ISO_2DIB0410F is provided in **Figure 3**.

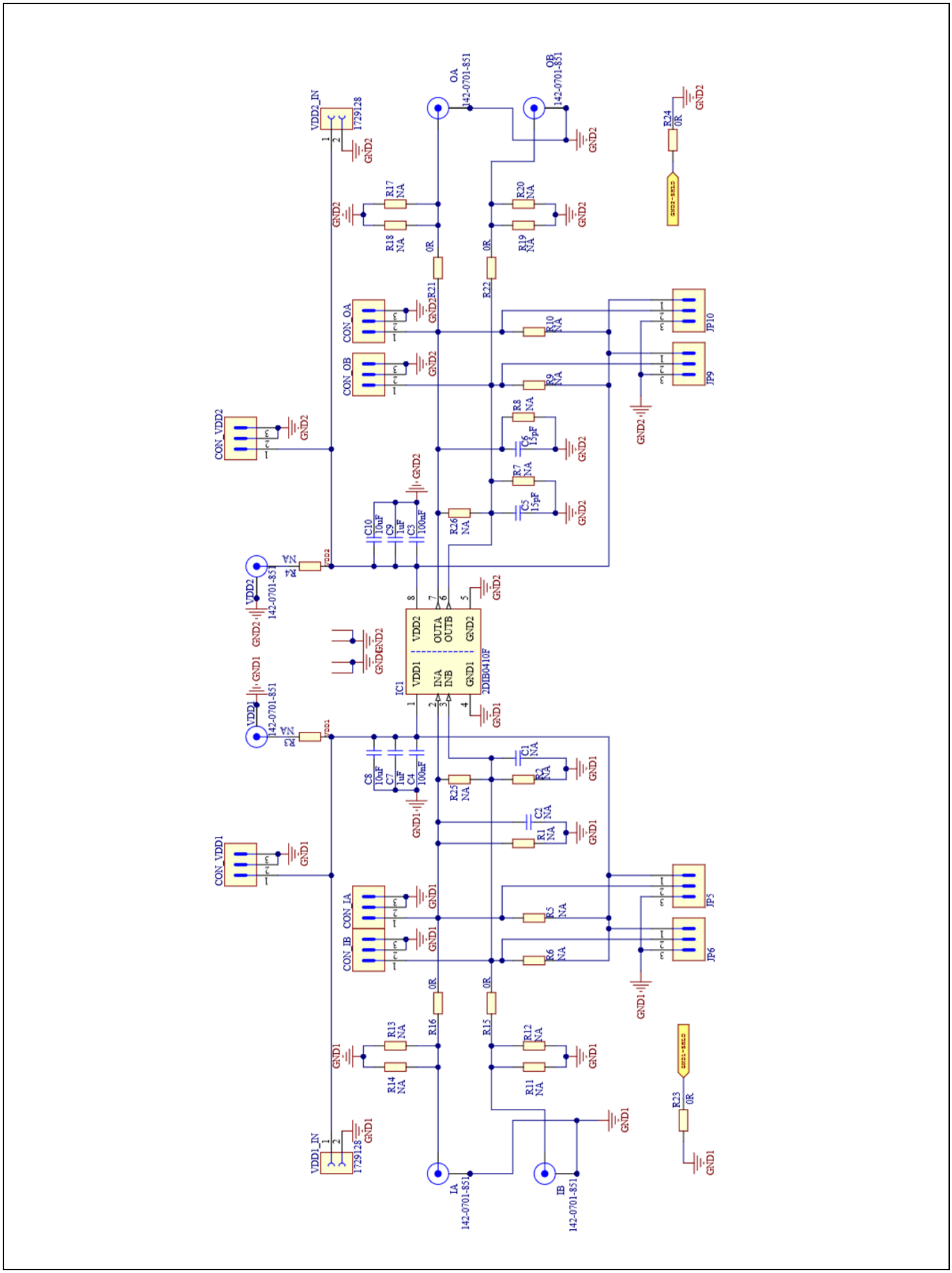
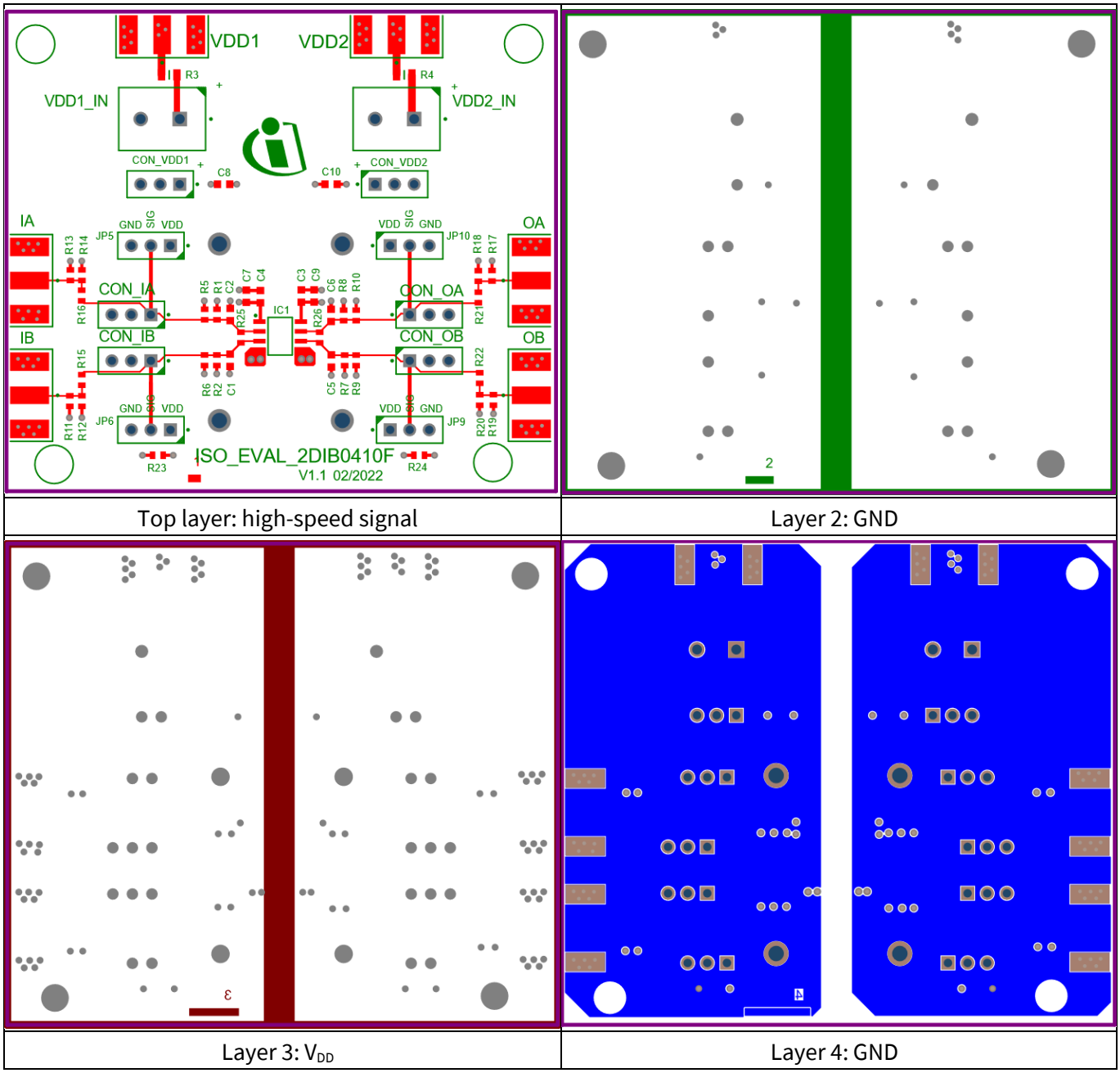


Figure 3 Schematic of EVAL_ISO_2DIB0410F

2.3 Board layout

The layout of the evaluation board EVAL_ISO_2DIB0410F is provided in **Figure 4**. Please note that the isolation barrier in the middle is placed in each layer and has a width of 4 mm. There are no traces, pads or vias placed within this isolation barrier.



Top layer: high-speed signal | Layer 2: GND

Layer 3: V_{DD} | Layer 4: GND

Figure 4 PCB layout of EVAL_ISO_2DIB0410F

3 Functional description

3.1 Connections

The board offers two power supply connections (VDD1 and VDD2) and four input/output connections for the dual-channel digital isolator 2DIB0410F.

3.1.1 Power connections

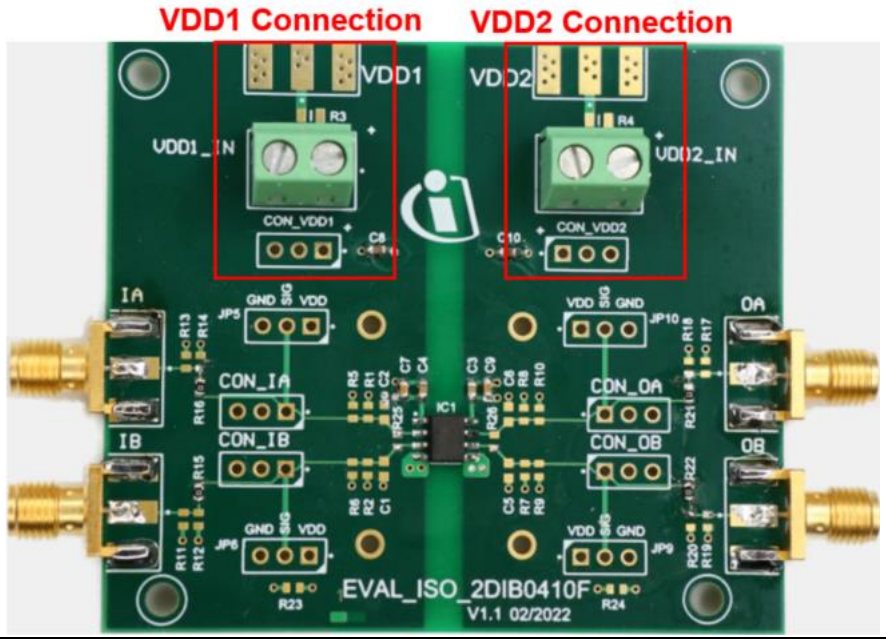


Figure 5 Power connections of EVAL_ISO_2DIB0410F

- **Power connection VDD1**

  This connection provides the V_{DD} supply for side 1 of the digital isolator. The operating supply voltage range is 2.7 to 6.5 V. For this connection, there is one edge-mounted SMA connector (VDD1) and one terminal block (VDD1_IN) available. To use the SMA connector, jumper R3 needs to be assembled. To measure the power supply signal on side 1 with a high-speed probe, there is a header block (CON_VDD1) designed.

- **Power connection VDD2**

  This connection provides the V_{DD} supply for side 2 of the digital isolator. The operating supply voltage range is 2.7 to 6.5 V. For this connection, there is one edge-mounted SMA connector (VDD2) and one terminal block (VDD2_IN) available. To use the SMA connector, jumper R4 needs to be assembled. To measure the power supply signal on side 2 with a high-speed probe, there is a header block (CON_VDD2) designed.

- **Bypass capacitors for power supply**

  There are three bypass capacitors designed on each side of the digital isolator to reduce noise on the power supply line. C8 and C10 (10 µF) are placed close to the terminal block to compensate for the long power supply cable. C4, C7 and C3, C9 (100 nF and 1 µF) are placed directly next to the digital isolator so that a stable V_{DD} supply is guaranteed.

3.1.2 Signal connections

There are two signal connections for each side of the digital isolator planned: two input and two output connections. Depending on which product variant is assembled on the board, there are different configurations of input and output connections. **Figure 6** gives an example using 2+0 digital isolator ISOFACE™ 2DIB0410F.

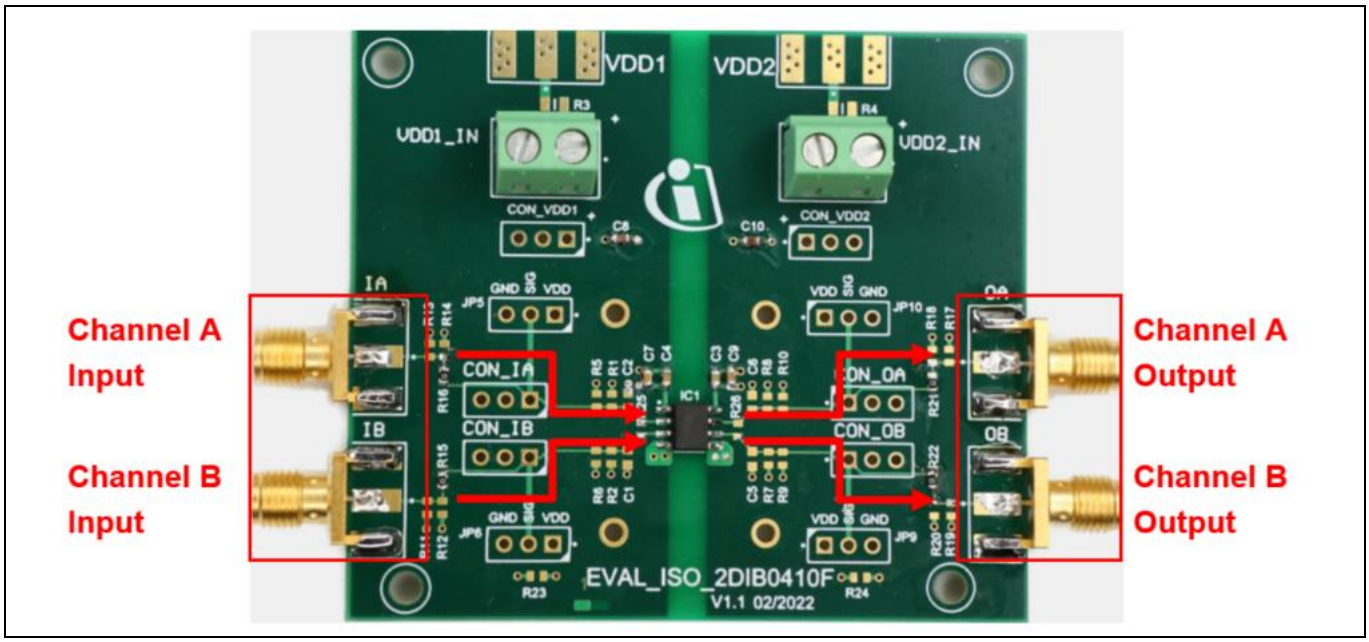


Figure 6 Signal connections of EVAL_ISO_2DIB0410F

- **Signal connection IA**

  For a 2+0 digital isolator this is the input of channel A; there is one edge-mounted SMA connector (IA) and one terminal block (CON_IA) available. To use the SMA connector, jumper R16 must be assembled. CON_IA can also be used to connect the high-speed probe for monitoring.

- **Signal connection IB**

  For a 2+0 digital isolator this is the input of channel B; there is one edge-mounted SMA connector (IB) and one terminal block (CON_IB) available. To use the SMA connector, jumper R15 must be assembled. CON_IB can also be used to connect the high-speed probe for monitoring.

- **Signal connection OA**

  For a 2+0 digital isolator this is the output of channel A; there is one edge-mounted SMA connector (OA) and one terminal block (CON_OA) available. To use the SMA connector, jumper R21 must be assembled. CON_OA can also be used to connect the high-speed probe for monitoring.

- **Signal connection OB**

  For a 2+0 digital isolator this is the output of channel B; there is one edge-mounted SMA connector (OB) and one terminal block (CON_OB) available. To use the SMA connector, jumper R22 must be assembled. CON_OB can also be used to connect the high-speed probe for monitoring.

To evaluate 1+1 digital isolator ISOFACE™ 2DIB1410F, **Figure 7** gives an example of the signal connection configurations.

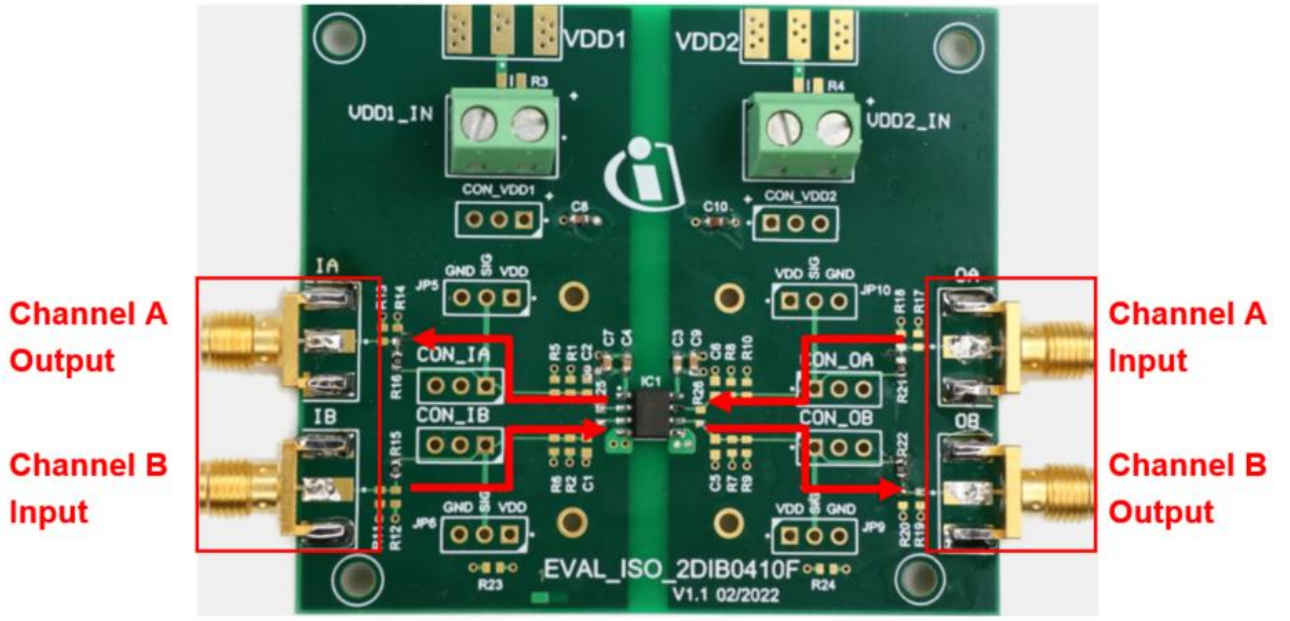


Figure 7 Signal connections of EVAL_ISO_2DIB0410F for 1+1 digital isolator

3.2 Configuration

As shown in **Figure 8**, to make the evaluation easier, the input and output connections of each data channel of the digital isolator can be configured individually: for example, impedance match, load, and pull-up/-down possibilities.

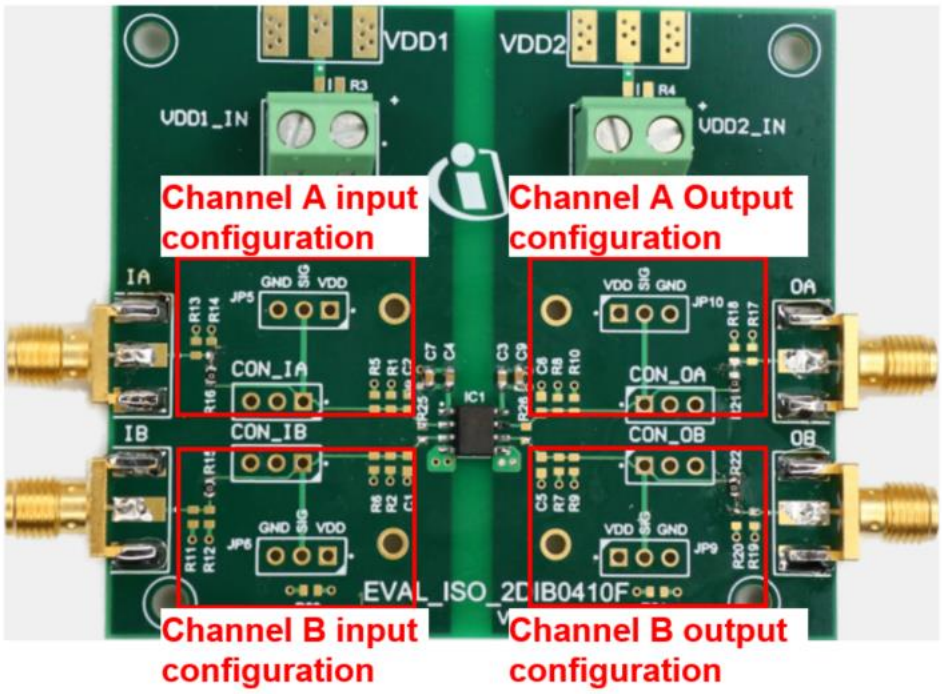


Figure 8 Additional configuration of EVAL_ISO_2DIB0410F

- Each data channel (A and B) has three pull-down resistors and one pull-up resistor on each side (input and output). Together with the jumpers for the SMA connectors (R15, R16, R21, R22), impedance matching can be performed individually for each input and each output.
- Input filter capacitors (C1 and C2) can be assembled for each input data channel.
- R25 is a jumper to short both the input data channels together if they share the same input.
- Output load capacitors (C5 and C6) can be assembled for each output data channel.
- Terminal blocks CON_IB, CON_IA, CON_OB and CON_OA are designed to conveniently short the input/output channels to V_{DD} or GND if required. They can also be used as signal input/output terminals.
- Jumper R23 and R24 are used to connect both ground layers 2 and 4.

3.3 Operation and typical waveforms

Figure 9 shows the typical configuration to operate the evaluation board EVAL_ISO_2DIB0410F using two isolated DC power supplies.

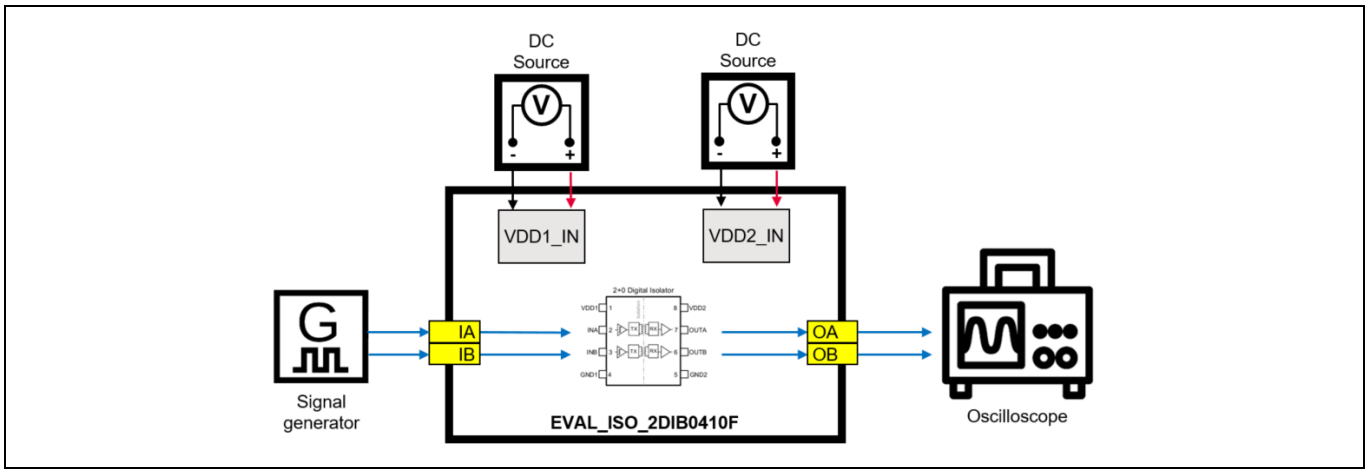
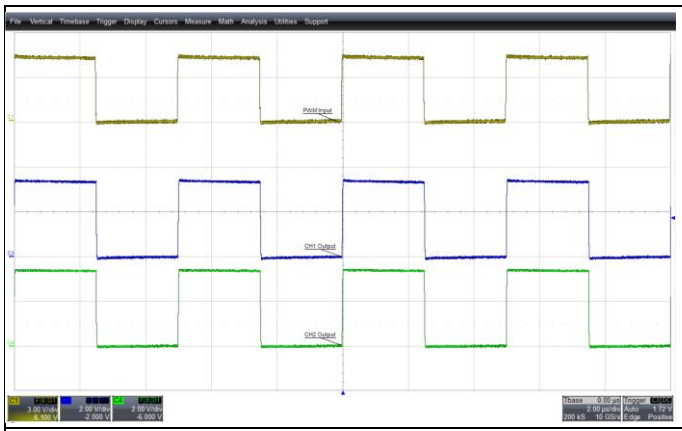
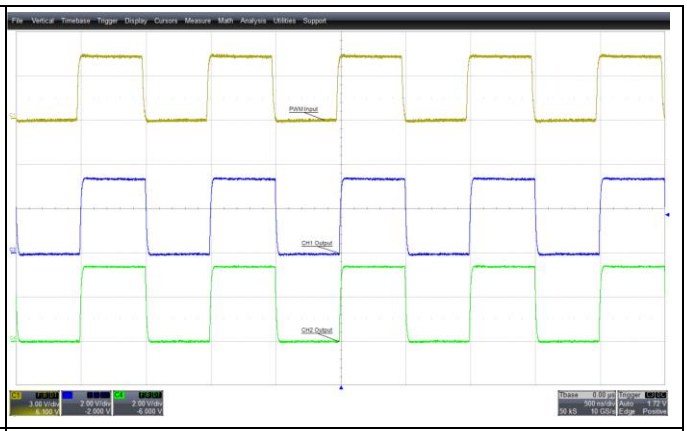


Figure 9 Typical operation of EVAL_ISO_2DIB0410F

Figure 10 shows the input and output waveforms of both channels measured at 200 kHz and 1 MHz PWM.



VDD1 = VDD2 = 3.3 V
Yellow: CH1 and CH2 input PWM at 200 kHz
Blue: CH1 output
Green: CH2 output
Time scale: 2 µs/div



VDD1 = VDD2 = 3.3 V
Yellow: CH1 and CH2 input PWM at 1 MHz
Blue: CH1 output
Green: CH2 output
Time scale: 500 ns/div

Figure 10 Typical input and output waveforms of EVAL_ISO_2DIB0410F

3.4 High-voltage capability

This evaluation board is designed to comply with 3000 V_{RMS} basic isolation practices. High-voltage testing over 3000 V_{RMS} is not recommended.

Warning: ***This board is not designed for evaluation of any high-voltage safety function. This could result in personal injury or death, or property damage.***

4 Bill of materials

Table 2 Bill of materials of EVAL_ISO_2DIB0410F

Quantity	Designator	Description	Part number	Manufacturer
2	C1, C2	Capacitor 15 pF/50 V/ 0603/C0G/5% Not assembled	885012006052	Würth Elektronik
2	C3, C4	Capacitor 100 nF/50 V/ 0603/X7R/5%	885012206095	Würth Elektronik
2	C5, C6	Capacitor 15 pF/50 V/ 0603/C0G/5%	885012006052	Würth Elektronik
2	C7, C9	Capacitor 1 µF/25 V/0603/X7R/10%	885012206076	Würth Elektronik
2	C8, C10	Capacitor 10 µF/16 V/ 0603/X5R/20%	885012106031	Würth Elektronik
1	IC1	2DIB0410F/SOIC-8	2DIB0410F	Infineon Technologies
6	R3, R4, R15, R16, R21, R22, R23, R24	Resistor 0 R/75 V/0603/0 R	CRCW06030000Z0	Vishay
2	R25, R26	Resistor 0 R/75 V/0603/0 R Not assembled	CRCW06030000Z0	Vishay
6	IA, IB, OA, OB, VDD1, VDD2	SMA PCB end launch jack flat tab for 1.6 mm PCB WR-SMA	60312202114514	Würth Elektronik
2	VDD1_IN, VDD2_IN	Connector 1729128/CON-TER-THT-MKDSN 1.5-2-5.08	691213510002	Würth Elektronik
4	CON_IA, CON_IB, CON_OA, CON_OB,	Connector HTSW-103-07-G-S/CON-THT-2.54-3-1-8.38	61300311121	Würth Elektronik
6	CON_VDD1, CON_VDD2, JP5, JP6, JP9, JP10	Connector HTSW-103-07-G-S/CON-THT-2.54-3-1-8.38 Not assembled	61300311121	Würth Elektronik
16	R1, R2, R5, R6, R7, R8, R9, R10, R11, R12, R13, R14, R17, R18, R19, R20	Not assembled	N.A.	N.A.

Revision history

Document version	Date of release	Description of changes
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