CYWBDVK002AB

West Bridge® Astoria™ Development Kit Guide

Doc. # 001-47358 Rev. *D

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Contents

1. Introduction

The West Bridge® Astoria™ Development Kit (DVK) introduces system designers to Astoria and demonstrates its capabilities and performance. The DVK is equipped with all components to integrate the Astoria software into the customer's platform. This document explains the DVK components. It describes the development board, explains the interconnection scheme, and also discusses signal integrity simulations and concepts for connectivity testing.

1.1 Components

1.1.1 Development Board

The development board is a platform for software development. The P-port connector provides interconnection to the controller. It contains an SD slot for SD or MMC storage devices, and two 8-bit NAND slots. West Bridge Astoria firmware does not support NAND flash memories anymore. The slots of the two 8-bit NAND will be unused.

1.1.2 Kit Contents

The Astoria Kit contains the following items

- CYWBDVK002AB DVK board
- Power supply
- USB A-B cable
- One SD card (4GB)
- CD with documents and software

1.1.3 Supported OS Platforms

The Astoria DVK supports the following operating systems: Windows XP (32- and 64-bit), Vista (32- and 64-bit) and Windows 7 (32- and 64-bit).

1.1.4 Product Documentation

Product documentation includes:

- Astoria datasheet
- Application notes:
  - Interfacing to West Bridge® Astoria's Pseudo-NAND Processor Port - AN46712
  - Schematic Review Checklist For West Bridge® Astoria™ - AN46860
  - High-speed USB PCB Layout Recommendations - AN1168
- User guide (this document)

1.1.5 Astoria Software Development Kit (SDK)

The Astoria software development kit provides Astoria API source code, firmware, API reference documentation, and example hardware abstraction layer (HAL) layers and drivers. The kit and all documentation are included with the SDK executable and are available at http://www.cypress.com/go/CYWBDVK002AB.

1.1.6 Diagnostics Modules for Linux

The diagnostic module is provided for Linux in the form of a loadable kernel module. The module goes through a series of tests to diagnose problems with register read and write, interrupt testing, firmware download, and storage connectivity. Chapter 4. Diagnostics Module on page 17 provides details on the implementation of this module and how to run it.

1.2 Document Revision History

Revision	PDF Creation Date	Origin of Change	Description of Change
**	10/21/2008	OSG/AESA	New reference design guide for West Bridge Astoria.
*A	04/19/2011	EYZ	Added Appendix chapter.
*B	06/02/2011	ROSM	Added ‘Handling TSOP Packets’ section in the Appendix chapter.
*C	03/05/2012	NMMA	Content updates throughout the document
*D	10/31/2012	NMMA	No change; sunset review

1.3 Documentation Conventions

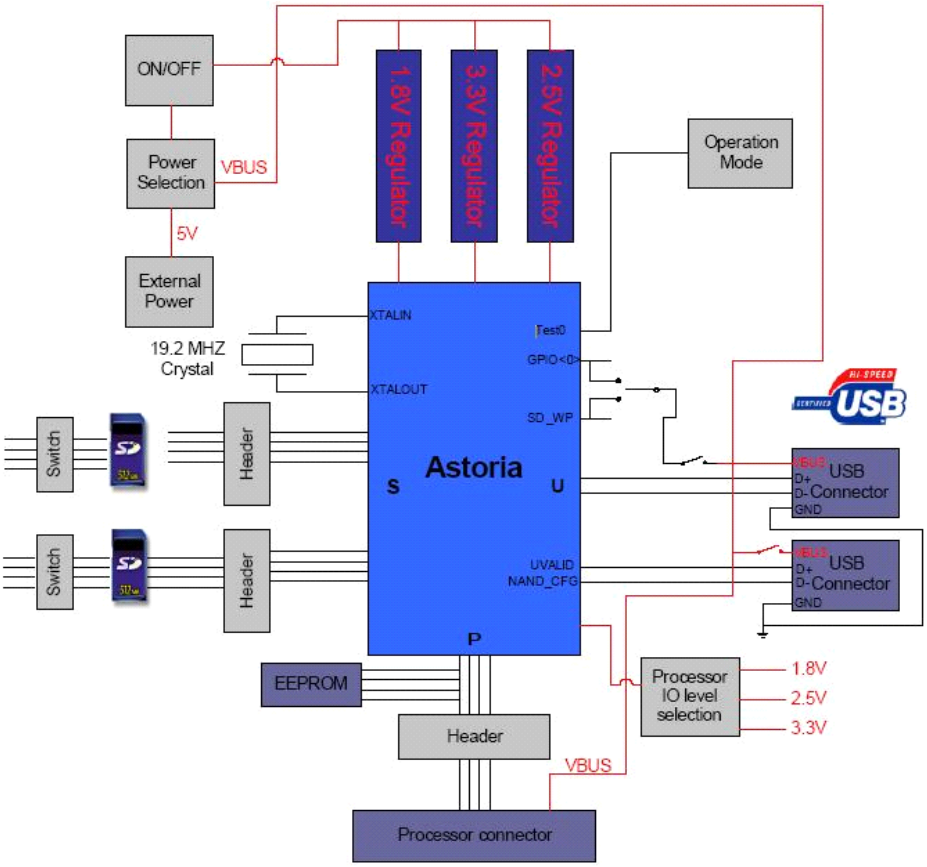
Table 1-1. Documentation Conventions for User Guides

Convention	Usage
Courier New	Displays file locations, user entered text, and source code: `C:\ ...cd\icc\`
Italics	Displays file names and reference documentation: Read about the *sourcefile.hex* file in the *PSoC Designer User Guide*.
[**Bracketed, Bold**]	Displays keyboard commands in procedures: [**Enter**] or [**Ctrl**] [**C**]
File > Open	Represents menu paths: File > Open > New Project
Bold	Displays commands, menu paths, and icon names in procedures: Click the **File** icon and then click **Open**.
Times New Roman	Displays an equation: 2 + 2 = 4
No text, gray table cell	Represents a reserved bit in register tables.

2. Astoria Board

2.1 Development Board

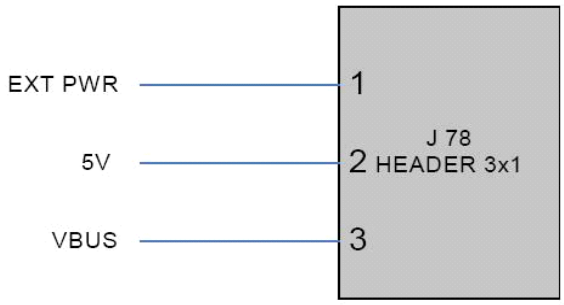
Figure 2-1. Block Diagram



2.1.1 Power Supply

The hardware can be powered from the USB host or from an external 5-V power supply. Use J78 to select the mode. Select 1-2 for an external power supply and 2-3 for power from the VBUS.

Figure 2-2. Power Supply



The 5-V supply is regulated by three regulators connected to the Astoria and storage devices. The following table shows how Astoria power domains are configured.

Table 2-1. Power Supply Routing

Power Domain	Description	Supply Level
V_{DD}	Core supply	1.8 V
AVDDQ	Analog supply	1.8 V
GVDDQ	General purpose I/Os	1.8 V
XVDDQ	Clocks supply	3.3 V
UVDDQ	USB supply	3.3 V
SSVDDQ	SD supply	3.3 V
SNVDDQ	GPIF supply	3.3 V
PVDDQ	Processor supply	1.8, 2.5, 3.3 V

Astoria processor interface I/Os are configurable and are capable of handling 1.8, 2.5, or 3.3 V supply levels. The SD device is powered by 3.3 V supply.

2.1.2 Crystal Oscillator

A 19.2 MHz crystal oscillator is connected to the crystal input of Astoria. The internal PLL produces the core, as well as SD and USB clocks. Crystal select pins are configured to support the frequency input.

2.1.3 USB Connector

A standard B type USB connector is provided to attach a USB cable. VBUS is passed to J78 to enable powering the board from the USB host. It is also connected to Astoria and the processor connector for host connectivity detection. GPIO<0> or SD_WP can be used to detect VBUS. Load J55 and then select J12 1-2 to connect VBUS to GPIO<0>, or 2- 3 to connect to SD_WP.

A standard A type USB connector is provided to allow access to the internal USB switch D+/D–.

2.1.4 P-Port Interfaces

Astoria supports multiple interfaces on the processor for easy connectivity. The P-Port on the Astoria DVK provides different interface options. To set up the required configurations on the development kit, use switches SW6 and SW4. When the switch is ON, the corresponding line is tied to ground. When the switch is OFF, the line is pulled up to PVDDQ with a 10-KΩ resistor. Table 2-2 and Table 2-3 show the pins connected to each of the switches. Table 2-4 shows the pin logic required for the interface modes.

Table 2-2. SW6 P-port Interface Control Switch

Switch	Pin
1	WAKE
2	TEST[0]
3	TEST[1]
4	TEST[2]

Note Wake must always be in the OFF position unless you want to force Astoria into standby mode.

Table 2-3. SW4 P-port Extended Interface Control Switch

Switch	Pin
1	A[2]
2	A[3]
3	A[7]
4	NULL

Table 2-4. P-port Configuration

Interface Modes								
TEST[2]	**TEST[1]**	**TEST[0]**	**VMTYPE**	**A[7]**	**A[3]**	**A[2]**	**Modes**	
0	0	1	x	x	x	x	Debug mode	
0	1	1	x	Use Extended Interface Mode (EIM)			Debug mode with EIM (Required for EEPROM)	
0	0	0	101	x	x	x	Normal (Non ADM Pseudo CRAM Mode)	
0	0	0	111	x	x	x	Normal (SRAM Mode)	
0	1	0	x	1	0	0	PNAND Mode - Small Block Device	EIM
0	1	0	x	0	0	0	PNAND Mode - Large Block Device	
0	1	0	x	1	1	0	PSPI Mode	
0	1	0	x	1	0	1	ADM Mode	

The Debug mode is a helpful tool that works with the CyConsole and Cypress download utility to allow firmware download from USB. In the Debug mode, Astoria automatically enumerates when connected to a USB host and Cypress USB driver is installed.

To install a driver:

1. Configure Astoria DVK board in Debug mode.
2. Connect a USB cable to the board and a USB host. Put J18 in ON position.
3. After the Hardware Update Wizard comes up, select **Yes, this time only**.
4. Select **Install Hardware** from `<Install_Directory>:\Cypress\West Bridge Astoria\<version>\USB Drivers` depending on the operating system and architecture (32/64-bit)**.** The device enumerates as “Cypress Astoria – DEBUG MODE PID=0x00A2”.

Use the browser to find the folder containing *cyusb.inf*. It is available on the DVK CD in the USB `Drivers` folder. Select the INF file for the operating system platform being used. The wxp folder has the drivers for Windows-XP (32- and 64-bit); wlh-wv folder has the drivers for Windows-Vista (32- and 64-bit); wlh-ws folder has the drivers for Windows-7 (32- and 64-bit).

2.1.5 EEPROM Boot Mode

An additional features of Astoria is the ability to boot without the assistance of the processor, by loading its firmware from an EEPROM. The EEPROM boot mode cannot work if the processor voltage is set to 1.8 V. If J13 is in position 2-3, the EEPROM mode cannot function; therefore, set J13 in position 1-2. To program the EEPROM, route A[5] and A[6] to the I^2C pins on the EEPROM, by switching SW5 to the OFF position.

2.1.5.1 EEPROM Firmware

All tools and firmware required to program the EEPROM are included in the EEPROM directory of the DVK CD.

2.1.5.2 Flashing Procedure for EEPROM

1. Set P-port Interface to debug mode with EIM. The EIM selected has no impact on the EEPROM functionality, but EEPROM cannot function outside of EIM. See Table 2-4 on page 9.
2. Launch the CyConsole utility from <Install_Directory>`:\Cypress\West Bridge Astoria\<version>\EEPROM`.
3. CyConsole uses the internal SIE to boot and enumerate in Debug mode. If EEPROM is preprogrammed with a boot code, the EEPROM booting must be disabled to allow SIE boot in Debug mode. To disable EEPROM boot, set SW5 to ON.
4. Power the DVK board and connect the USB cable to the host PC. Windows must recognize the Cypress USB device connection. CYConsole must show Astoria enumeration. If Astoria does not enumerate, then recheck all board settings. If the EEPROM is disconnected after enumeration, it can be reconnected now by switching SW5.
5. From the Options menu in CYConsole, select **EZ USB Interface**.
6. Press the **LgEEPROM** button. A file browser opens.
7. Navigate to the location of the .iic file (`<Install_Directory>:\\Cypress\West Bridge Astoria\<version>\EEPROM`). Select the file based on memory configuration. See S-port Memory Interfaces on page 10.

Now, the board can be set to nondebug EIM, but this is not required. After the EEPROM is programmed, power cycle the board. When powering up, the Astoria now loads its firmware from the EEPROM.

2.1.6 S-port Memory Interfaces

Astoria is designed to accept multiple types of memory configurations. The development kit supports most of the possible configurations. This section describes the memory configurations supported by the development board and how each memory configuration is implemented.

There are two SD slots and two NAND sockets on the development board. The following table shows how the memory sockets are designated.

Table 2-5. Memory Socket Designations

Name	Location	Board label
SD1	SD slot on the top of the board	J2
SD2	SD slot on the bottom of the board	J37
NAND1[a]	Closest NAND socket to the power switch	U2
NAND2[a]	Closest NAND socket to the serial port	U5

a. NAND flash sockets are unused because the Astoria firmware no longer supports the NAND flash memories.

Three switch arrays are provided to separate the NAND bus and the SD Card bus. Because the NAND flash memories are no longer supported by Astoria firmware, these switches must always be in OFF position. The three switch arrays on the development board are labeled SW2, SW3, and SW7. The following table lists the switch array controls.

Table 2-6. Switch Array Designation

Switch Array		Function	Relates
SW2	Off	Disconnects SD_IO[7:0] from NAND_IO[15:8]	SD1, NAND2
	On	Connects SD_IO[7:0] to NAND_IO[15:8]	
SW3	Off	Disconnects NAND_SD2_IO[7:0] from NAND_IO[7:0]	SD2, NAND1
	On	Connects NAND_SD2_IO[7:0] to NAND_IO[7:0]	
SW7	Off	Disconnects SD2 control from NAND control	SD2, NAND1, NAND2
	On	Connects SD2 control to NAND control	

The S-Port of the Astoria development kit supports the following memory interfaces.

- Single SD/MMC
- Dual SD/MMC
- Single SD/MMC and GPIF
- Single SD/MMC and GPIO
- GPIF and GPIO

Following is the demonstration of the first two types of memory configuration listed. For other memory interfaces, contact Cypress Support at http://www.cypress.com/support.

2.1.6.1 Single SD

When implementing a single SD, use only J2. When running demo firmware, the card detection is done using SD_IO[3]. However, if running other firmware that use GPIO detection, J75 must be connected. To configure the board for single SD operation, turn off SW2.

Firmware: *cyastfw_sd_mmc_rel_nopport*

2.1.6.2 Dual SD

Use SD1 and SD2 when implementing the dual SD configuration. When you run firmware that uses GPIO card detection, connect J75 and J30. To configure the board for dual SD operation, turn off SW2, SW3, and SW7, and install a jumper on J29.

Firmware: *cyastfw_dual_sdio_sd_mmc_rel_nopport.hex*

2.1.7 Astoria Processor Port

The Astoria processor port is connected to J15, a Samtec QSH06001LDA connector, for interconnection with the controller. Samtec QTH06001LDA is the matting connector. See the Astoria datasheet for expected controller timing. J14 and J16 contain the entire processor port interface for interconnection and debugging purposes.

Figure 2-3. J16 Debug Header

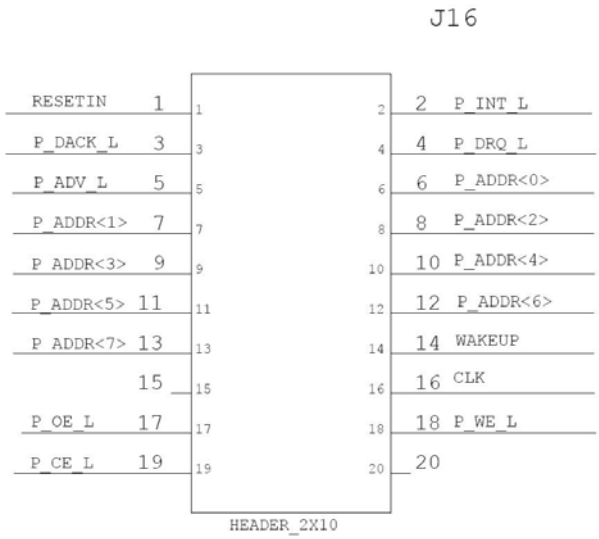


Figure 2-4. J14 Debug Header

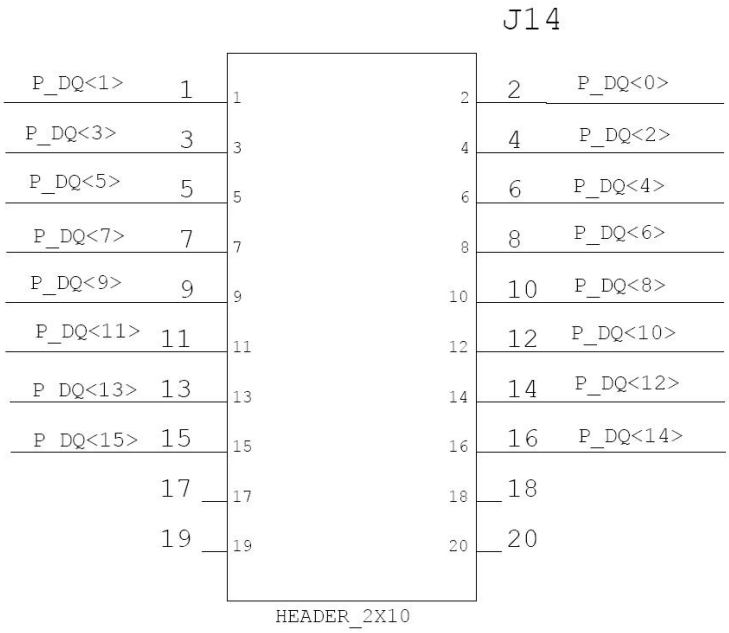
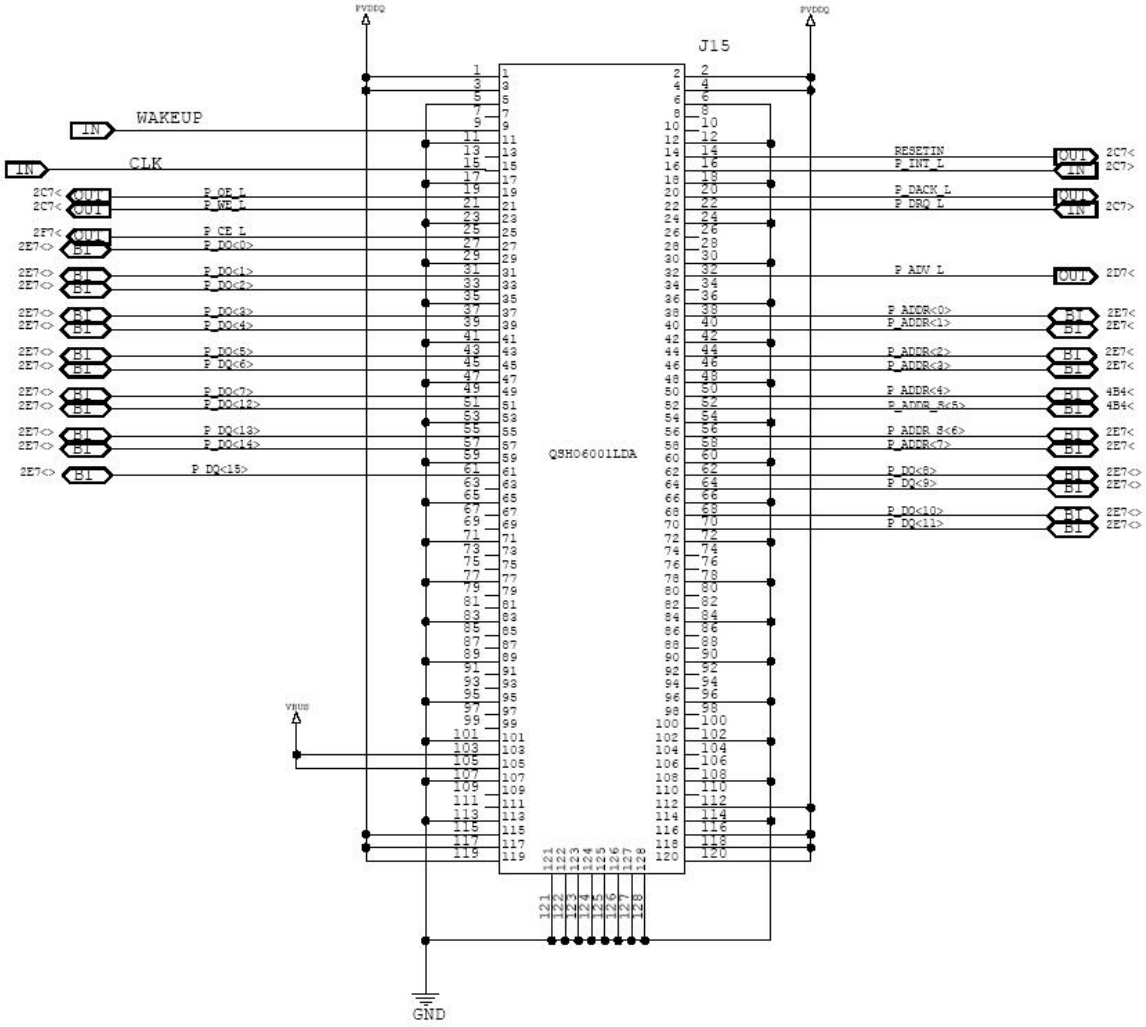


Figure 2-5. J15 Processor Connector



2.1.8 Astoria Storage Port

Figure 2-6. J16 NAND Debug Connector

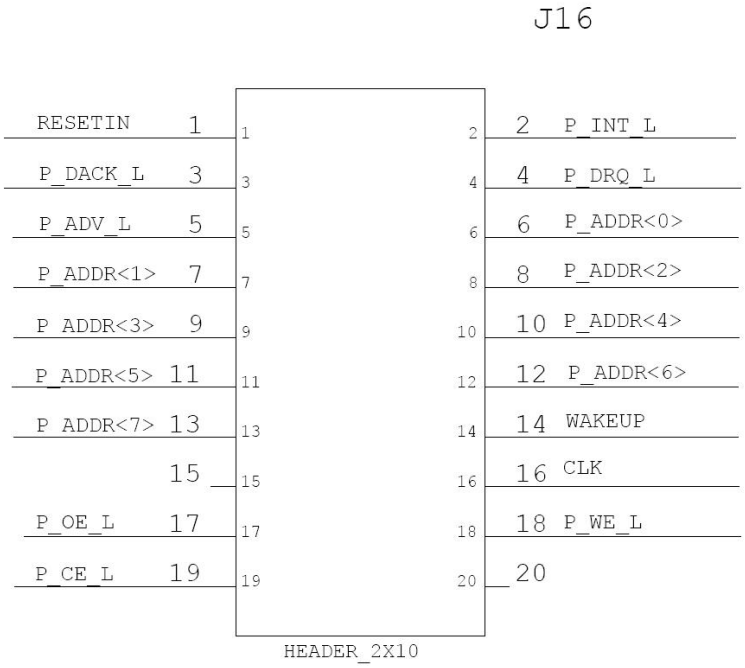
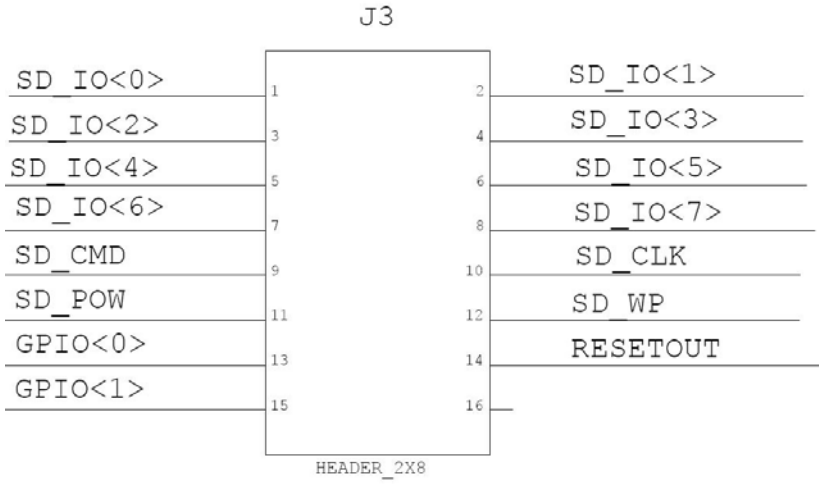


Figure 2-7. J3 SD Debug Connector



2.1.9 Reset Switch

SW1 is the main reset circuit for Astoria. To reset the NAND or SD, recycle the board power.

3. Interconnection to Astoria Board

The Astoria DVK hardware is designed to interconnect to a processor development platform. The optimal method to work with Astoria is to create a board with Astoria directly next to the processor.

The interconnection scheme uses the DVK board with a small adapter board to bring the processor interface to a connector that matches the controller platform expansion connector. Flex cables can be used to connect the two boards. If there are no flex cables available to match the connector at the controller side, use two adapter boards for the interconnection. Cypress recommends using Samtec HFEM020T05.00-SE flex cables with the QSH06001LDA connector on one adapter board and the QTH06001LDA on the other adapter board.

Interconnection causes signal integrity challenges. Cypress recommends simulating the interconnection topology before manufacturing the adapter boards. In most cases, adding termination resistors at the controller and selecting the correct termination value at Astoria can resolve reflections caused by mismatches. In some cases, buffering is required.

To run the signal integrity (SI) simulation, Cypress provides:

- Astoria IBIS model
- Trace information for the Astoria development board

To run the SI simulation, customers require:

- Processor IBIS model
- The I/Os type used for interconnection with Astoria
- Trace information on the controller board

The combination of these components can be used to simulate signal integrity. Simulation software, such as Hyperlynx from Mentor Graphics or SigXplorer from Cadence, can be used with the previous information to determine how to improve signal integrity. These tools provide pass/fail results to the simulation. In addition, the system designer must judge which scheme provides the optimal solution.

To demonstrate the importance of this simulation, two example simulations are provided. One example is with termination and another without.

In the first simulation, the waveform in black is the signal at the receiver side and blue is the transmitter side. As shown in Figure 3-1, there is minimal reflection and no glitches. In this simulation, proper termination resistors are used to arrive to this form. In the second simulation, shown in Figure 3-2, the same termination resistors are removed. The red waveform is the signal at the receiver. The reflection is much higher and there are glitches near the VIH level. This is an unacceptable waveform and can cause many system glitches.

Figure 3-1. SI Simulation with Termination

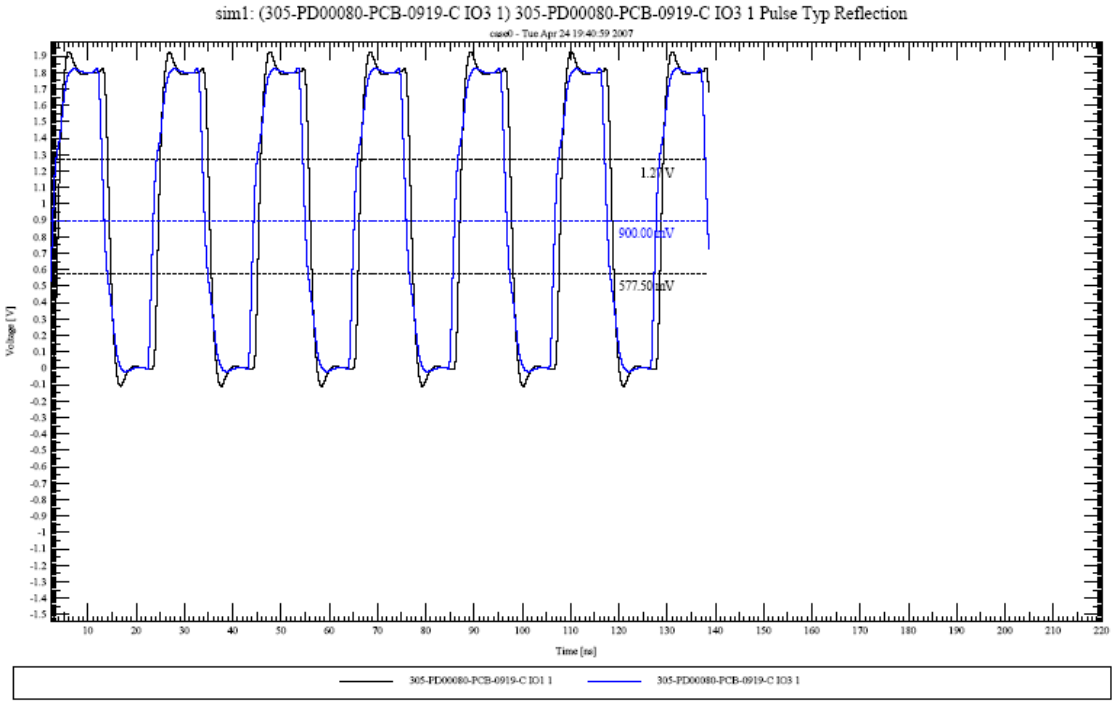
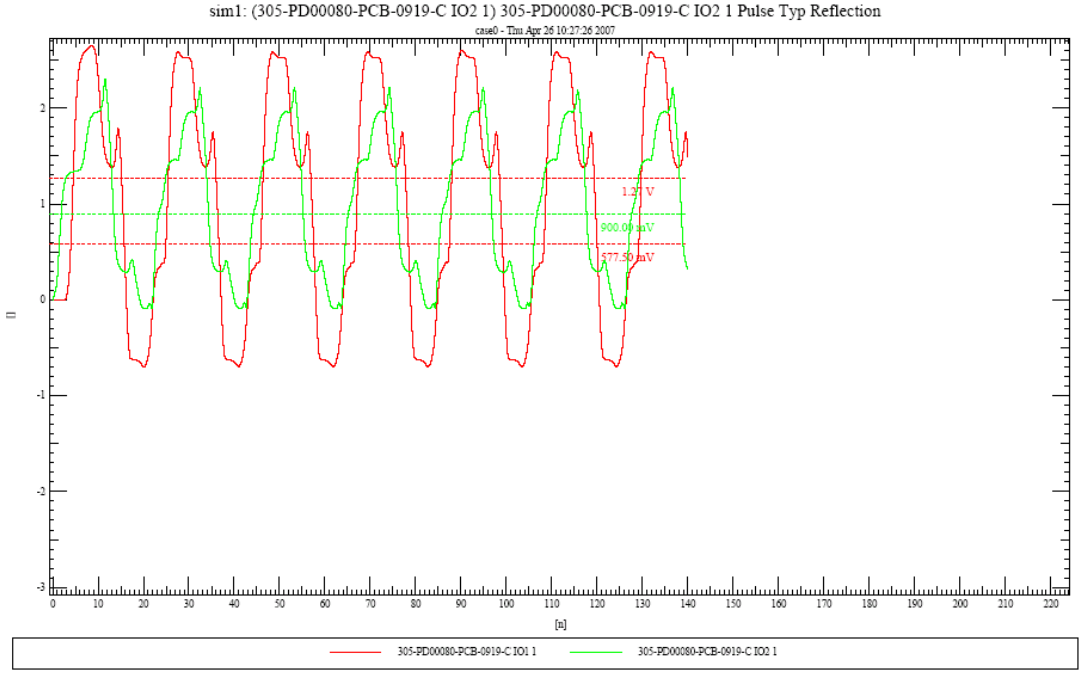


Figure 3-2. Simulation with no Termination



4. Diagnostics Module

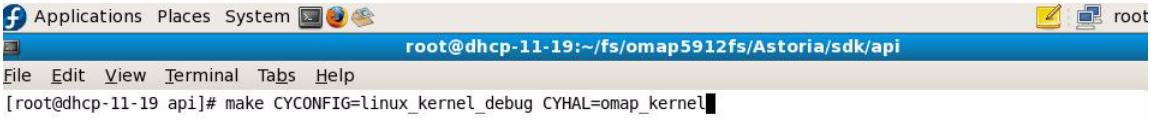
After implementing the hardware abstraction layer (HAL), ensure there is hardware access to Astoria. The primary goal of the diagnostics module is to test and verify HAL functionality and hardware connectivity for various interfaces of Astoria. This helps diagnose any problems that are identified.

4.1 Compiling Linux Diagnostics Module

Compile the diagnostics source file that generates the diagnostics loadable kernel module. The testing must be bundled in this format for the tests to acquire access to the platform hardware. The HAL functions required to run the diagnostics module are described in Additional HAL Functions Required on page 21.

Compilation can be done on the target platform or on a Linux PC using a cross-tool compiler. In Figure 4-1, the command `make CYCONFIG=linux_kernel_debug CYHAL=platform_hal` is used to execute the cross-tool compiler. In this case, `linux_kernel_debug` is the configuration used and `platform_hal` is replaced with `omap_kernel` to indicate the specific HAL implementation used. Figure 4-1 to Figure 4-4 uses the TI OMAP processor as an example.

Figure 4-1. Compile Linux Diagnostics Module



4.1.1 Running the Linux Diagnostics Test

Navigate to the directory where the diagnostics module is saved, usually *(*`ASTORIA SDK ROOT)\sdk\drivers\diag\(CYCONFIG)`. In the following example, the directory is `Astoria/sdk/drivers/diag/linux_kernel_debug`.

Enter the Linux command `klogd -c 8` to execute the klogd system daemon that intercepts and logs Linux kernel messages, allowing them to be printed to the console.

Figure 4-2. Run Linux Diagnostics Test

Enter the Linux command `insmod cyasdiag_module.ko`. This loads and runs the diagnostics module and displays the resulting messages to the console through the klogd daemon. Figure 4-3

and Figure 4-4 show an example of the diagnostics module output.

Figure 4-3. Linux Diagnostics Output

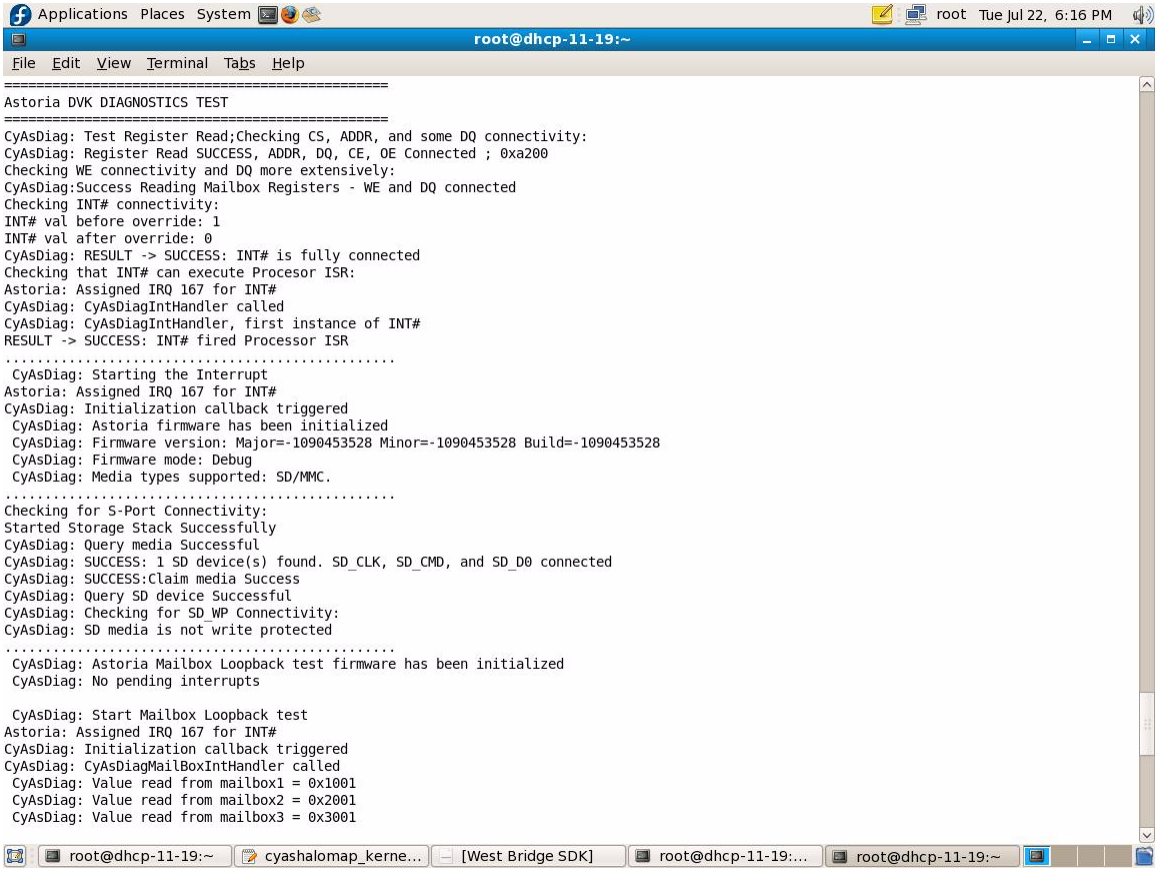
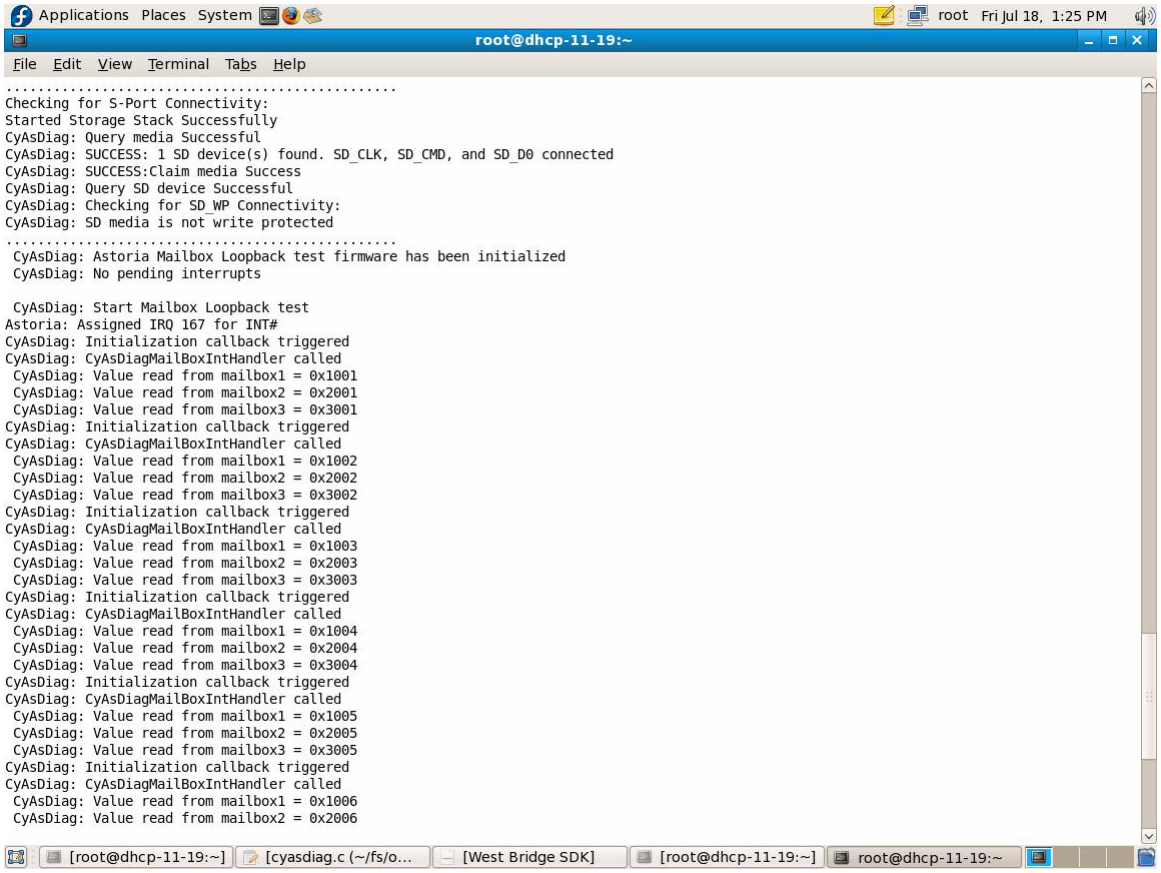


Figure 4-4. Linux Diagnostics Output (continued)



4.2 Test Description and Troubleshooting

This section describes the basic tests performed in diagnostics and what it means if they fail.

4.2.1 Register Read and Write

This test checks whether the CRAM control signals and address and data buses are correctly connected. The processor memory interface configuration and the memory range assigned to Astoria are also checked.

This test is done by reading the silicon ID of the attached West Bridge chip and comparing it to the known, default value. It also writes and reads back several writable registers (mailboxes) on the attached chip to do additional verification of the data buses, and ensure that writes are succeeding. To troubleshoot these failures, it is usually necessary to monitor the P-Port interface using a logic analyzer. For example, if the memory range assigned to Astoria is incorrect, CS is not asserted. If the processor memory interface is incorrectly configured, the timing of the control signals being generated by the processor is incorrect.

Possible error outputs:

- ERROR: ADDR, DQ, CE, OE, ADV, or TEST pins are not correctly connected. The read values are:
  - RESULT -> ERROR: exp 3, act
  - RESULT -> ERROR: exp 2, act

- RESULT -> ERROR: exp 1, act
- RESULT -> ERROR: WE not connected or DQ not fully connected

4.2.2 Interrupt Testing

This test checks if the INT# line is physically connected and if its assertion triggers the execution of an ISR. It is done by forcing the assertion of the interrupt signals through writing an override register within Astoria. The level of the INT line is pulled through an access similar to the GPIO before and after the forced assertion, to determine the presence of a physical connection. After this connection is verified, a diagnostics local ISR is registered and the module verifies that the assertion of the INT# line causes the execution of the ISR.

Possible error outputs:

- RESULT -> ERROR: INT# is not connected or incorrectly mapped
- RESULT -> ERROR: INT# did not fire processor ISR

4.2.3 Firmware Download

This test ensures that the DMA functionality of the HAL layer is correctly implemented. Firmware is downloaded through a series of DMA transactions. If the DMA handling for these transactions is not correct, the firmware download fails and outputs an error code.

Possible error outputs:

- <1> CyAsDiag: Cannot Start Interrupt Monitor. Reason code:
- <1> CyAsDiag: Cannot download the astoria firmware. Reason code:

4.2.4 Storage Connectivity

This test ensures that the applicable signals between Astoria and the attached storage are correctly connected. This is done by executing some basic storage queries through the Astoria API.

Possible error outputs:

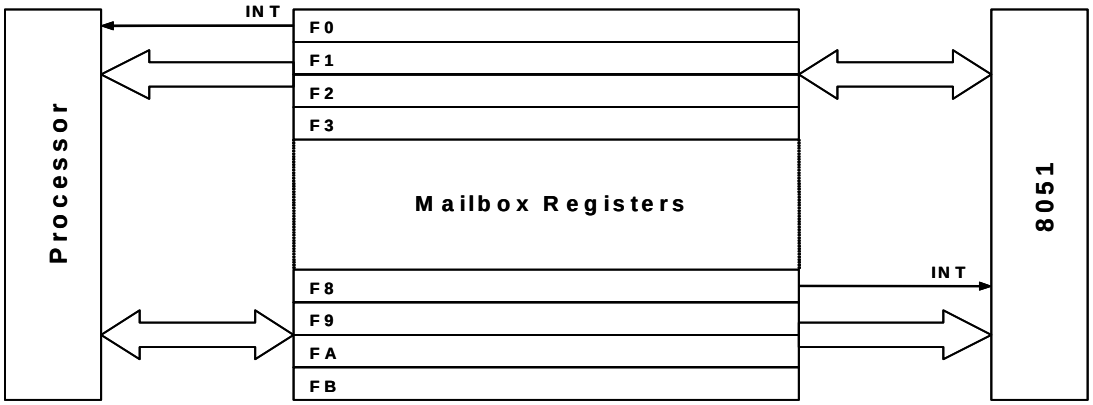
- <1>CyAsDiag: SD storage media was not found
- <1>CyAsDiag: Nand storage media was not found

4.2.5 Mailbox Loopback

This test ensures that mailbox interactions between the processor and Astoria are reliable. To run this test, a custom firmware image is downloaded to Astoria that provides mailbox loopback functionality.

A message is written by the processor through the diagnostics to the MCU Mailbox registers (F8-FB), which is then read by the 8051 and written back to the P0 Mailbox registers (F0 -F3). This is again read by the processor and verified.

Figure 4-5. Mailbox Loopback Diagram



4.3 Additional HAL Functions Required

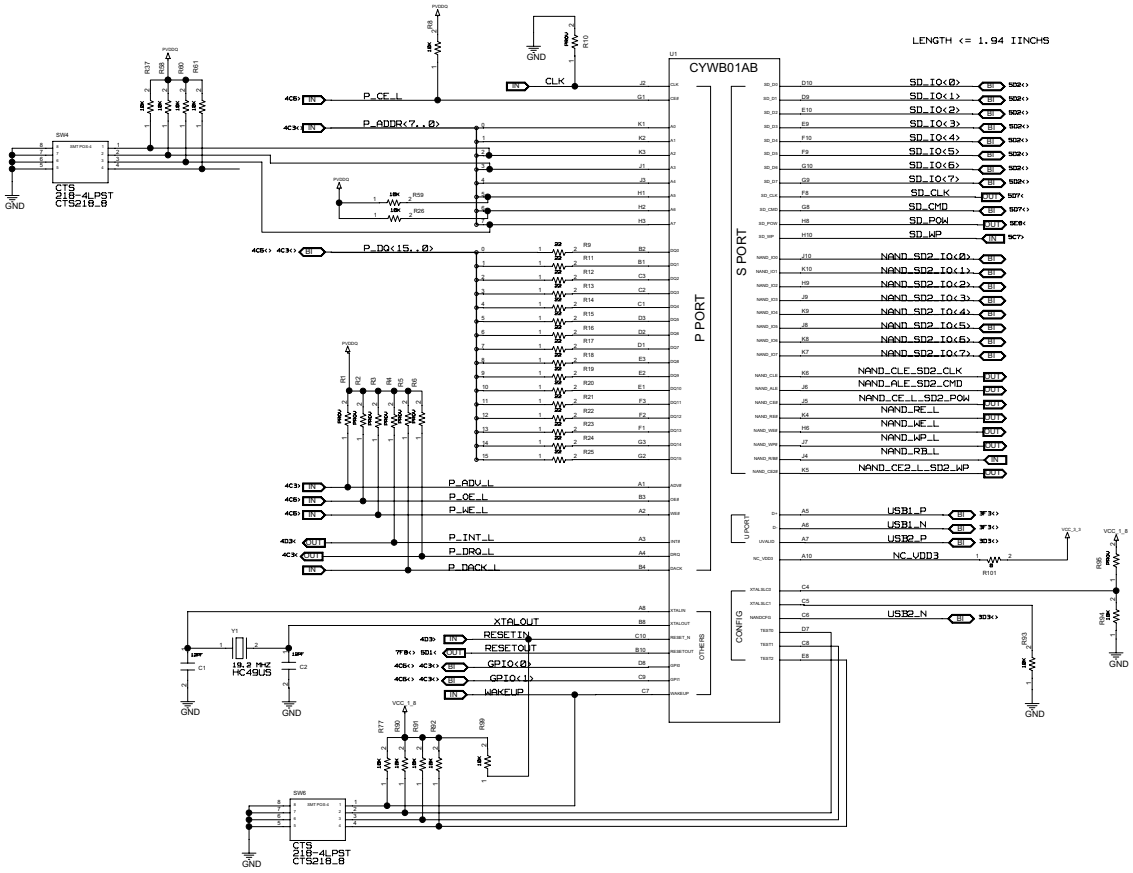
The diagnostics module relies on implementing a set of HAL functions in a specific way with a predefined naming convention. This can be changed, but the corresponding diagnostics test must also change accordingly.

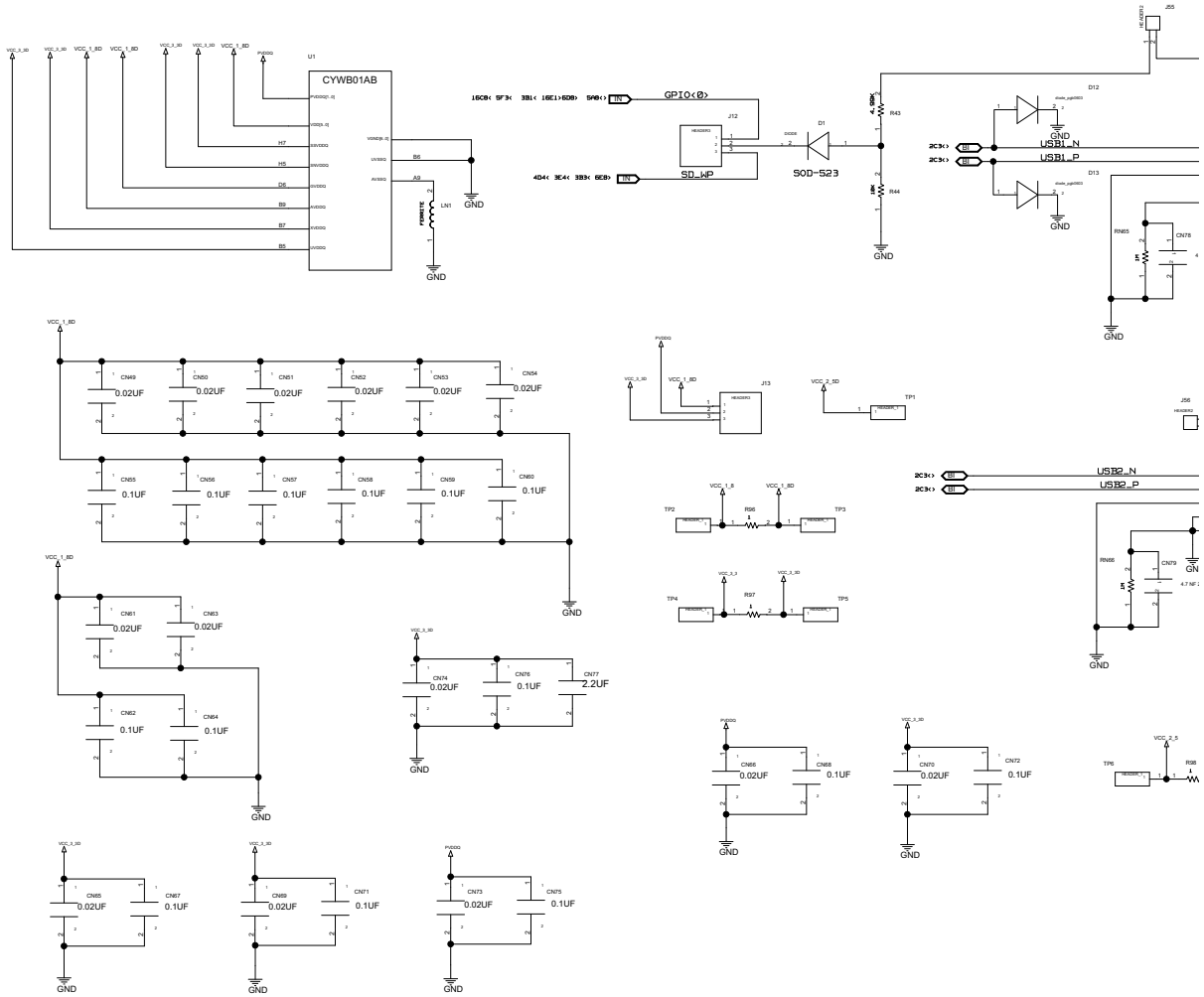
- `int CyAnHalStart (`CyAsHalDeviceTag *tag`)` - This function makes the call to start the HAL layer in a system agnostic fashion and passes back any necessary pointers.
- `int CyAnHalStop (`CyAsHalDeviceTag *tag`)` - This function makes the call to stop the HAL layer system agnostic, so that a standard function can be called.
- `int CyAsHalGetIntVal(void)` - Returns the current value of INT# signal using GPIO-like access.
- `int` CyAsStartInterruptHandler(CyAsHalDeviceTag tag) - Registers standard HAL interrupt routines.
- `int` CyAsHalDiagConfigInt(int asInterrupt,void *dev_p, CyAsInthandlers inthandler) - Allows local diagnostic ISR to be registered with the HAL.
- `int` CyAsHalDiagReleaseInt(int asInterrupt,void *dev_p) - Releases the IRQs, unregisters the ISR.

A. Appendix

A.1 Schematic

A.1.1 Board Overview

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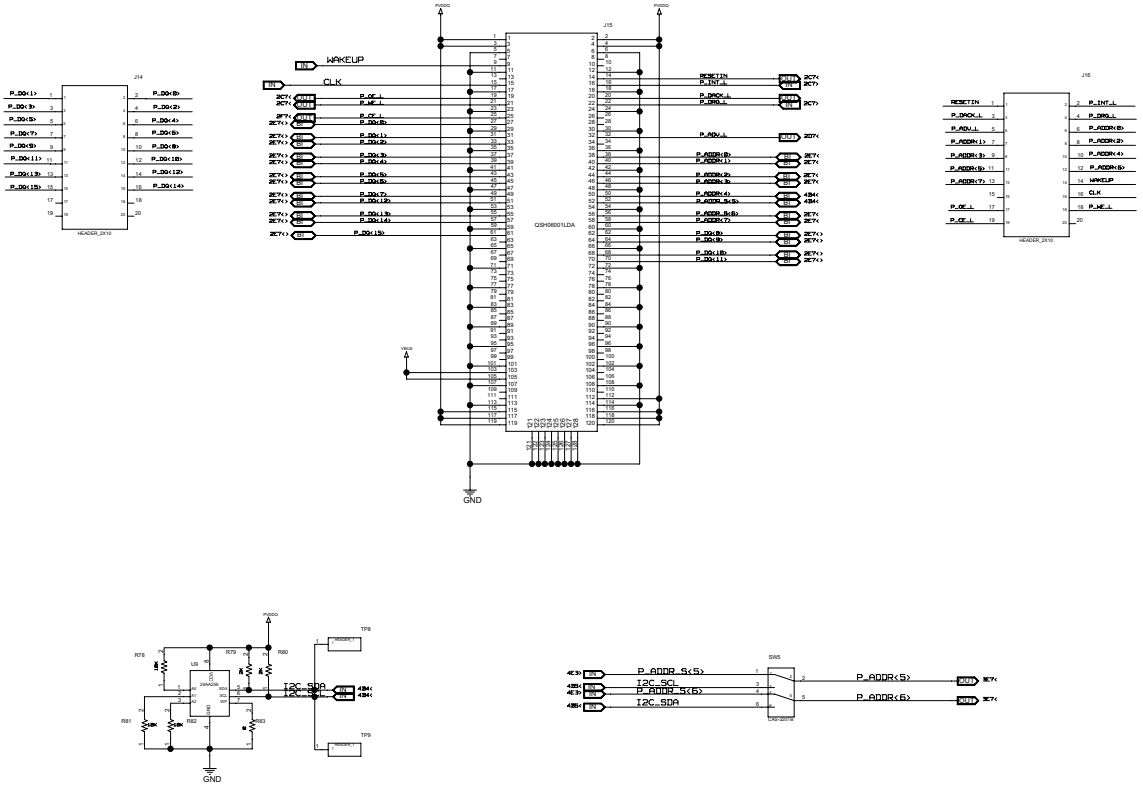
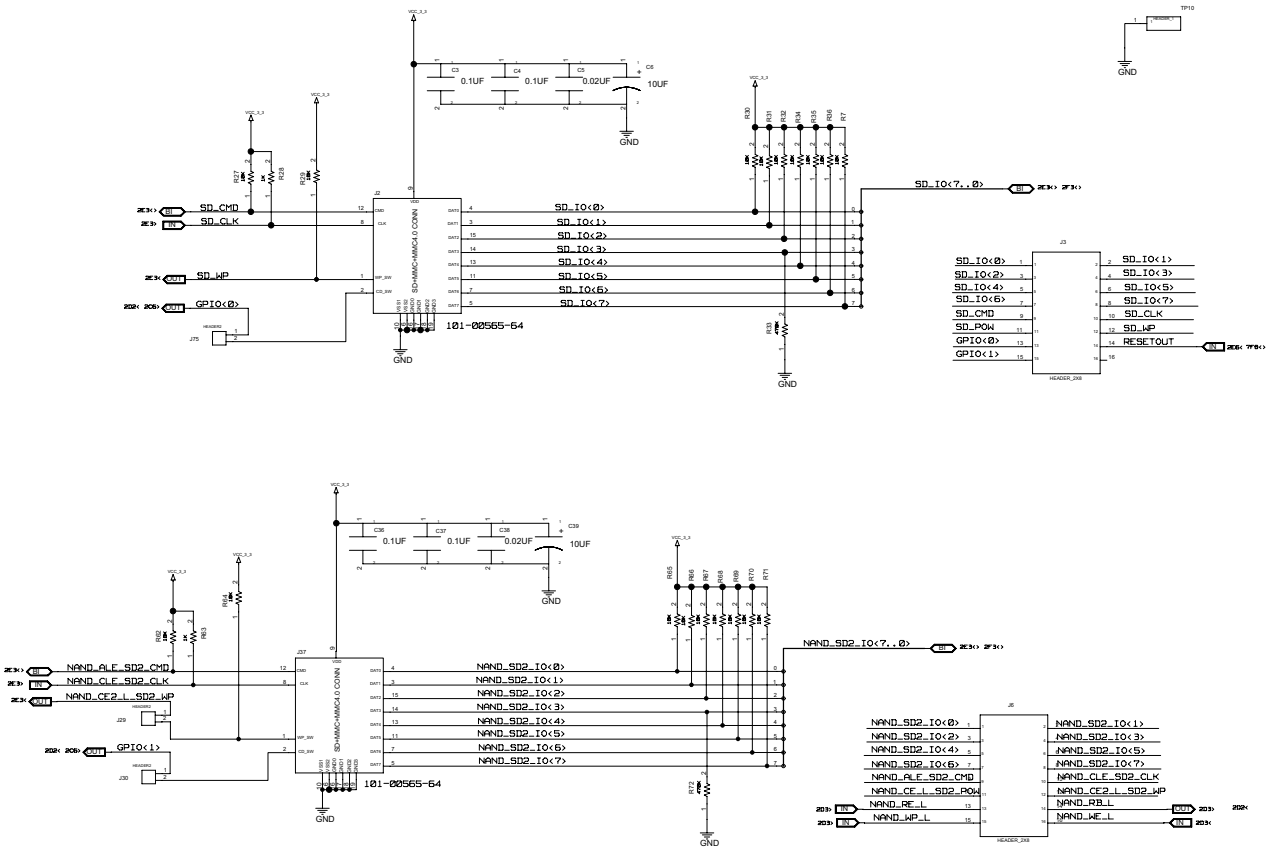
SOD-523
USB1_N
USB1_P
USB2_N
USB2_P
GND
0.02UF
0.1UF
2.2UF


J14
J15
J16
WAKEUP
CLK
GND
QSH06001LDA
HEADER_2X10

TP8
TP9
I2C_SDA
I2C_SCL
P_ADDR_5<5>
P_ADDR<5>
P_ADDR<6>
SW5
GND


SD_CMD
SD_CLK
SD_WP
GPIO<0>
SD_IO<0>
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SD_IO<2>
SD_IO<3>
SD_IO<4>
SD_IO<5>
SD_IO<6>
SD_IO<7>
SD_IO<7..0>
101-00565-64
GND
NAND_ALE_SD2_CMD
NAND_CLE_SD2_CLK
NAND_CE2_L_SD2_WP
GPIO<1>
NAND_SD2_IO<0>
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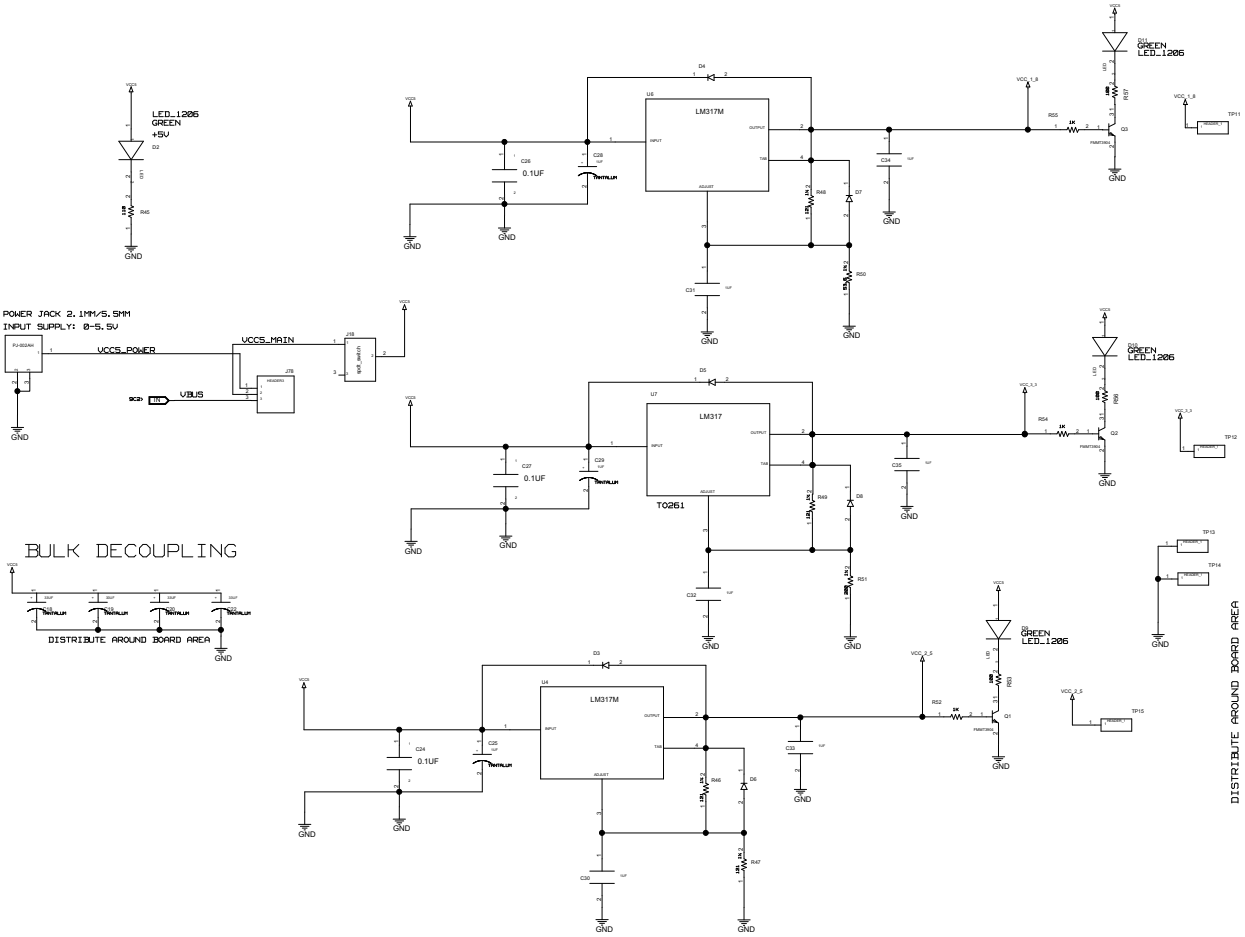
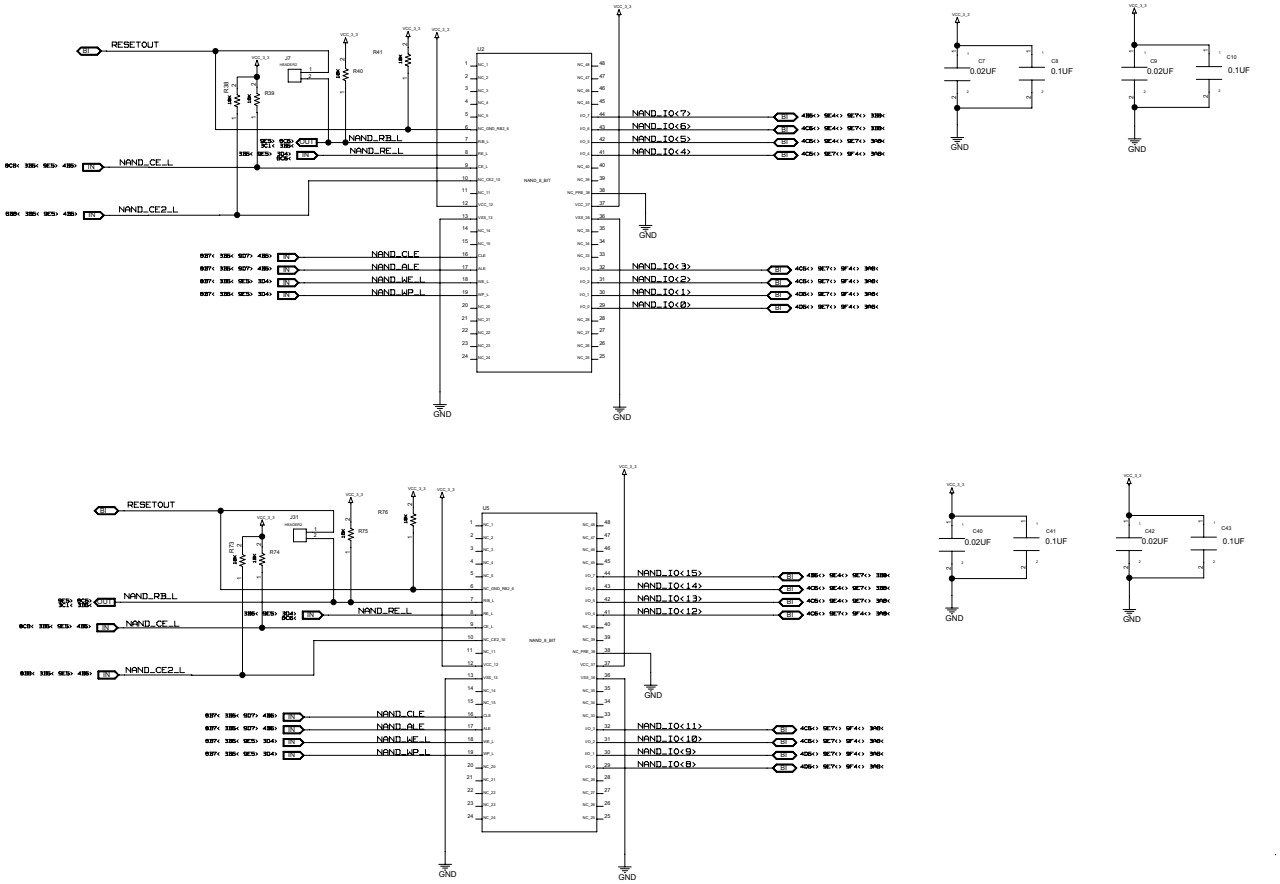
GND


LED_1206
GREEN
+5V
D2
R45
GND
POWER JACK 2.1MM/5.5MM
INPUT SUPPLY: 8-5.5V
J17
VCC5_POWER
VCC5_MAIN
J18
J19
VBUS
C26
0.1UF
C28
D4
U6
LM317M
INPUT
OUTPUT
ADJUST
R48
D7
C31
R50
C34
R55
Q3
VCC_1.8
TP11
LED_1206
GREEN
D11
R57
C27
0.1UF
C29
D5
U7
LM317
TO261
R49
D8
C32
R51
C35
R54
Q2
VCC_1.2
TP12
BULK DECOUPLING
DISTRIBUTE AROUND BOARD AREA
TP13
TP14
C24
0.1UF
C25
D3
U4
R46
D6
C30
R47
C33
R52
Q1
VCC_2.5
TP15
DISTRIBUTE AROUND BOARD AREA


RESETOUT
NAND_RB_L
NAND_CE_L
NAND_CE2_L
NAND_RE_L
NAND_CLE
NAND_ALE
NAND_WE_L
NAND_WP_L
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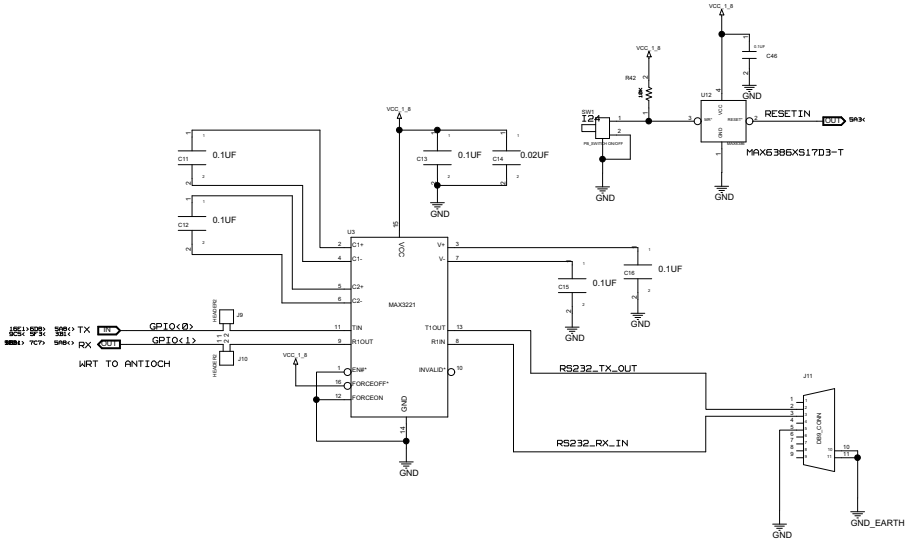
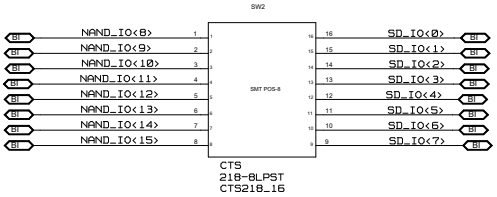
0.02UF
0.1UF
GND


VCC_1_8
C11
0.1UF
C12
0.1UF
C13
0.1UF
C14
0.02UF
C15
0.1UF
C16
0.1UF
C46
0.1UF
R42
U3
MAX3221
C1+
C1-
C2+
C2-
V+
V-
VCC
TIN
R1OUT
T1OUT
R1IN
ENB*
FORCEOFF*
FORCEON
INVALID*
GND
SW1
U12
RESETIN
MAX6386XS17D3-T
GPIO<0>
GPIO<1>
TX
RX
WRT TO ANTIOCH
J9
J10
HEADER2
HEADER6
RS232_TX_OUT
RS232_RX_IN
J11
DB9_CONN
GND_EARTH


SW2
NAND_IO<8>
NAND_IO<9>
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SD_IO<2>
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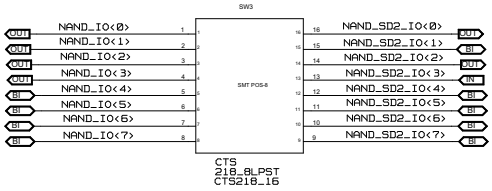
SD_IO<4>
SD_IO<5>
SD_IO<6>
SD_IO<7>
SMT POS-8
CTS
218-8LPST
CTS218_16


SW3
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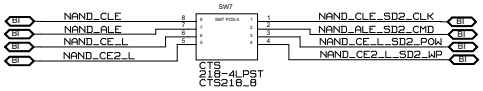
NAND_IO<1>
NAND_IO<2>
NAND_IO<3>
NAND_IO<4>
NAND_IO<5>
NAND_IO<6>
NAND_IO<7>
NAND_SD2_IO<0>
NAND_SD2_IO<1>
NAND_SD2_IO<2>
NAND_SD2_IO<3>
NAND_SD2_IO<4>
NAND_SD2_IO<5>
NAND_SD2_IO<6>
NAND_SD2_IO<7>
SMT POS-8
CTS
218-8LPST
CTS218_16


SW7
NAND_CLE
NAND_ALE
NAND_CE_L
NAND_CE2_L
NAND_CLE_SD2_CLK
NAND_ALE_SD2_CMD
NAND_CE_L_SD2_POW
NAND_CE2_L_SD2_WP
SMT POS-4
CTS
218-4LPST
CTS218_8

A.2 Board Layouts

Figure A-1. Top View

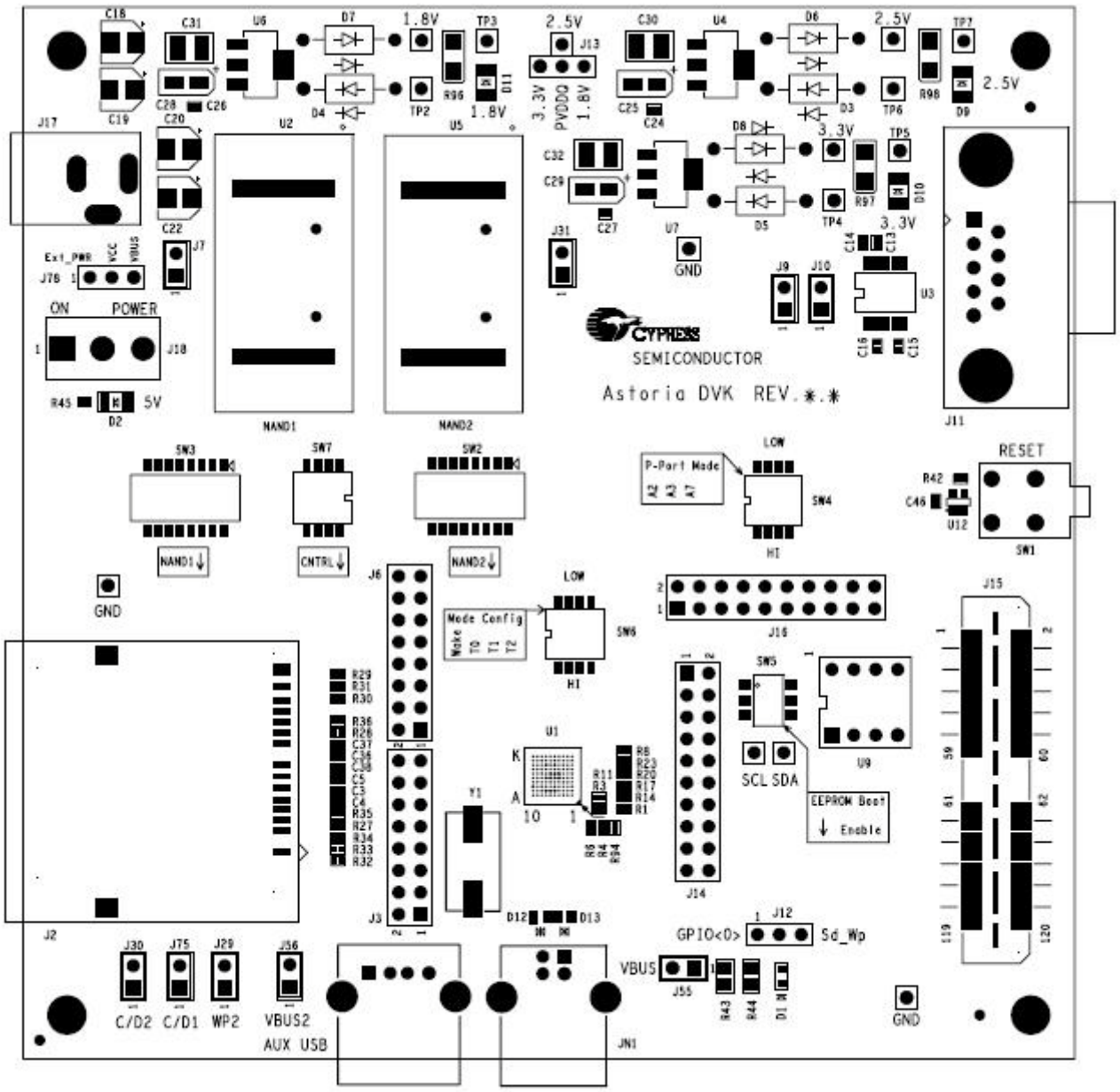
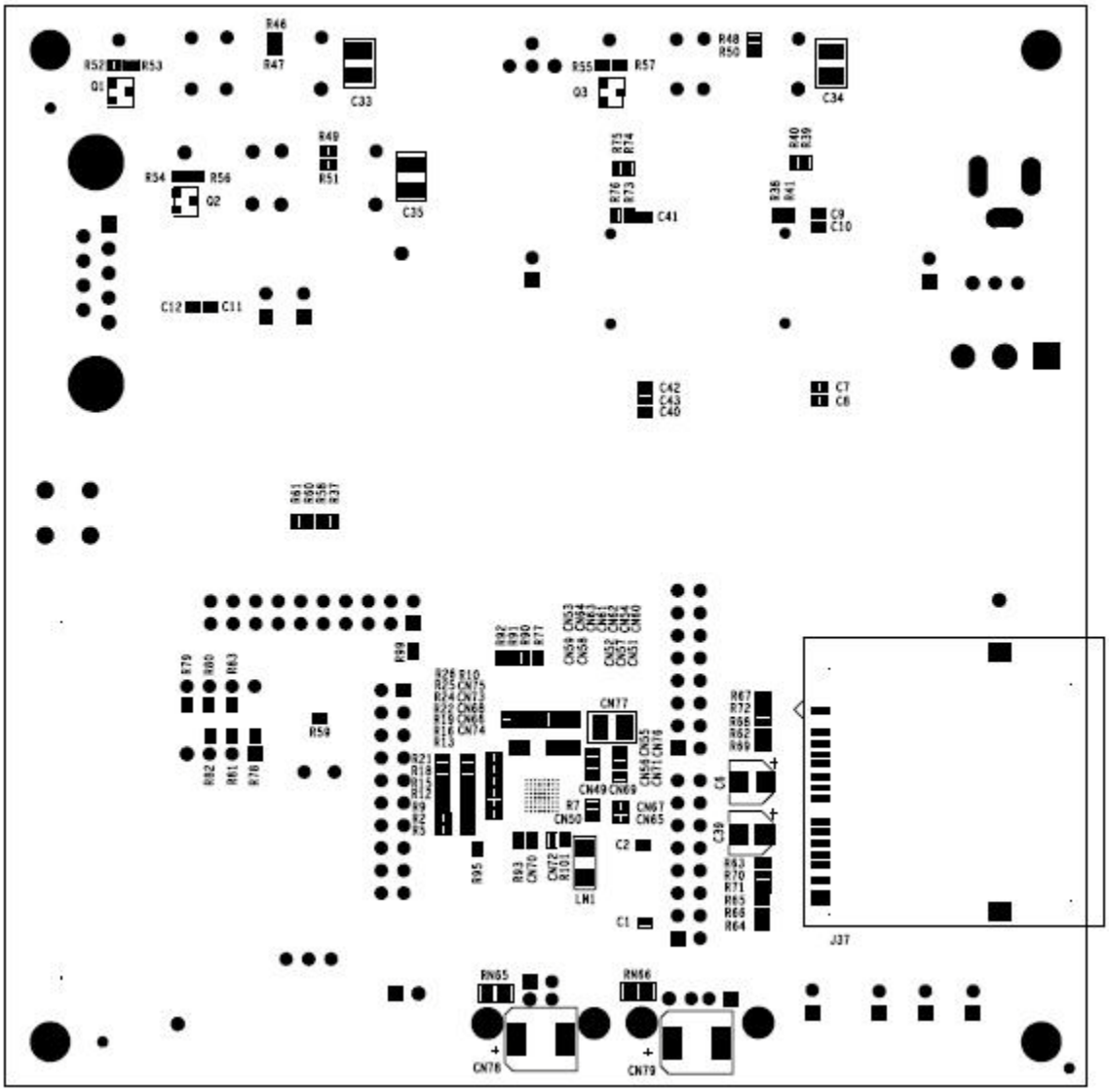


Figure A-2. Bottom View



A.3 Bill of Materials (BOM)

Sl.No.	Qty.	Reference	Description	Manufacturer	Manufacturer Part No.
1	21	C5,C7,C9,C14,C38,C40, C42,CN49, CN54, CN61, CN63,CN65,CN66, CN69, CN70,CN73, CN74	Capacitor, 10nF, 10%, 16V, ceramic, X7R, SMD 0402	AVX	0402YC103KAT
2	31	C3,C4,C8,C10, C13, C15, C16,C24,C26,C27,C36,C 37,C41,C43,C46,CN55, CN60, CN62,CN64,CN67, CN68,CN71,CN72,CN75, CN76	Capacitor, 0.1uF, 10%, 10V, ceramic, X5R, SMD 0402	AVX	0402ZD104KAT
3	2	C6,C39	Capacitor, 10uF, 16V, 20%,electro-lytic, SMD	Panasonic	EEV-FK1C100R
4	6	D3-D8	Diode General Purpose 100V 1A DO41	Fairchild	1N4002
5	6	C30-C35	Capacitor, 1uF, 10%, 50V, ceramic, X7R, SMD 1210	AVX	12105C105KAT
6	3	C25,C28,C29	Capacitor, 1uF, Tantalum, 20V 10% 1206 SMD	Kemet	T491A105K020AS
7	1	U9	Socket, 8Pin, MS TIN/TIN .300	Mill-Max	110-99-308-41-001000
8	1	CN77	Capacitor, 2.2uF, 10%, 25V, ceramic, X7R, SMD 1210	AVX	12103C225KAT
9	4	C18, C20,C22	Capacitor, 33uF, 20%, 10V, Tantalum, 1311 SMD, low ESR	Kemet	T520B336M010ASE070
10	1	JN1	Connector, USB Receptacle, Type B PCB	Amp/Tyco	787780-1
11	2	C1,C2	Capacitor, 12pf, 50V COG 5% 0402 SMD	TDK Corpora-tion	C1005C0G1H120J
12	1	SW5	SLIDE SWITCH DPDT GULLWING, SMT	Copal Electron-ics	CAS-220TB
13	1	Y1	CRYSTAL 12.5PF 24.00MHZ 50/ 50PPM -40-85C, SMD	Gentech Crys-tals	GCE-SMD-HC/49US-A-1-12.5-24.00MHZ-EXT-50/ 50PPM
14	1	U1	CYWB01AB_Socket, VFBGA_100	-	-
15	1	J11	Connector, DB9, Female .318" RA Met Shell	Norcomp Inc.	182-009-212-181
16	1	D1	DIODE SCHOTTKY 40V 150MW SOD-523	Diodes Incorpo-rated	SDM03U40
17	2	D12,D13	SUPPRESSOR ESD 24VDC 0603 SMD	LITTLE FUSE	PGB0010603MR
18	2	SW2,SW3	Switch, DIP, 8 position, half size, SMD	CTS Corpora-tion	218-8LPST

Sl.No.	Qty.	Reference	Description	Manufacturer	Manufacturer Part No.
20	2	CN78,CN79	Capacitor, 4.7NF 250VAC Ceramic SMD	Panasonic	ECK-TBC472MF
21	1	LN1	Ferrite bead, 100 ohm, 3A, SMD 1206	Laird-Signal	HI1206N101R-00
22	3	Q1-Q3	TRANS GP NPN 40V 200MA SOT23-3	Zetex	FMMT3904TA
23	9	J7,J9,J10,J29, J31, J55, J56,J75	Header, 2-pos, 0.100"	Sullins	PTC36SAAN
24	3	J12,J13,J78	Header, 3-pos, 0.100"	Sullins	PTC36SAAN
25	2	J14,J16	-	-	-
26	2	J3,J6	-	-	-
27	4	D2,D9-D11	LED 565NM GREEN DIFF 1206 SMD	Lumex	SML-LX1206GW-TR
28	1	U7	3-Terminal Adjustable Regulator, DCY Package, SOT-223-4	Texas Instru-ments	LM317MDCY
29	2	U4,U6	3-Terminal Adjustable Regulator, DCY Package , SOT-223-4	Texas Instru-ments	LM317MDCY
30	1	U3	IC, RS232 Transceiver, 16-SSOP, SMD,120KBPS	Maxim	MAX3221CAE
31	1	U12	IC, single supply supervisor, O/D reset_n, 1.67V, 140mS, SMD	Maxim	MAX6386XS17D3-T
32	2	U2,U5	Socket, TSOP 48 Position, w/Align-ment Pins, SMD	Emulation Tech-nology	S-TSO-SM-048-A
33	1	SW1	Switch, Pushbutton, RA PCB mount, SPST-NO 0.4VA 20V	C&K	TP11SH8ABE
34	1	J17	Connector, Power Jack 2.1 mm x 5.5 mm High Current	CUI Inc	PJ-002AH
35	1	J15	QSH Series, 120 positions connector, SMD	Samtec	QSH-060-01-L-D-A-K-TR
36	8	R1-R6,R10,R95	-	-	-
37	2	R83,R101	Resistor, 0.0 (ZERO) ohm, 1/10W, 0402 SMD	Panasonic	ERJ-2GE0R00X
38	16	R9,R11-R25	Resistor, 22 OHM, 1/10W, 5%, 0402 SMD	Panasonic	ERJ-2GEJ220X
39	44	R7,R8,R26,R27,R29, R32,R34-R42,R58, R62, R64-R71,R73, R78,R81, R82,R90-R94,R99	Resistor, 10K ohm, 1/10W, 5%, 0402 SMD	Panasonic	ERJ-2GEJ103X
40	5	R28,R52,R54,R55,R63	Resistor, 1.0K ohm, 1/10W, 5%, 0402 SMD	Panasonic	ERJ-2GEJ102X
41	2	R33,R72	Resistor, 470K ohm, 1/16W, 5%, 0402 SMD	Yageo America	9C04021A4703JLHF3

Sl.No.	Qty.	Reference	Description	Manufacturer	Manufacturer Part No.
42	1	R45	Resistor, 110 ohm, 1/10W, 5%, 0402 SMD	Panasonic	ERJ-2GEJ111X
43	3	R53,R56,R57	Resistor, 100 ohm, 1/10W, 5%, 0402 SMD	Panasonic	ERJ-2GEJ101X
44	2	R79,R80	Resistor, 2.0K OHM, 1/10W, 5%, 0402 SMD	Panasonic	ERJ-2GEJ202X
45	1	R43	Resistor, 4.99KOhm, 1/8W, 1%, 0805 SMD	Rohm	MCR10EZHF4991
46	1	R44	Resistor, 10KOhm, 1/8W, 5%, 0805 SMD	Vishay/Dale	CRCW080510K0JNEA
47	2	RN65,RN66	Resistor, 1 Meg, 1/8W 5% 0805 SMD	Panasonic	ERJ-6GEYJ105V
48	3	R96-R98	Resistor, 1ohm, 1/4W, 1%, 1206 SMD	Yageo America	RC1206FR-071RL
49	4	R46-R49	Resistor, 121 OHM, 1/10W, 1%, 0402 SMD	Panasonic	ERJ-2RKF1210X
50	1	R50	Resistor, 53.6 ohm, 1/10W, 1%, 0402 SMD	Panasonic	ERJ-2RKF53R6X
51	1	R51	Resistor, 200 ohm, 1/10W, 1%, 0402 SMD	Panasonic	ERJ-2RKF2000X
52	2	J2,J37	CONN SD/MMC/MMC 15POS PCB GOLD	Amphenol	101-00565-64
53	1	J18	Switch, Slide Miniature SPDT, On-None-On	C&K	1101M2S3CQE2
54	3	SW4,SW6,SW7	Switch, DIP, 4 position, half size, SMD	CTS Corpora-tion	218-4LPST
55	11	TP1-TP7,TP10,TP13-TP15	-	-	-
56	2	TP11,TP12	-	-	-
57	2	TP8,TP9	-	-	-
58	1	JN2	1010BLF USB S/D RECEPT LF	FCI	87520-1010BLF
59	1	Astoria DVK Board	-	Pactron	305-PD-11-0748