Application Note

AN-ICE2QS01

Design Tips for Flyback Converters Using the Quasi-Resonant PWM Controller ICE2QS01 (ANPS0005)

Power Management & Supply

Never stop thinking.

Edition 2011-12-14

Published by Infineon Technologies Asia Pacific,
168 Kallang Way,
349253 Singapore, Singapore

Attention please!

The information herein is given to describe certain components and shall not be considered as a guarantee of characteristics.

Terms of delivery and rights to technical change reserved.

We hereby disclaim any and all warranties, including but not limited to warranties of non-infringement, regarding circuits, descriptions and charts stated herein.

Information

For further information on technology, delivery terms and conditions and prices please contact your nearest Infineon Technologies Office (www.infineon.com).

Warnings

Due to technical requirements components may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies Office.

Infineon Technologies Components may only be used in life-support devices or systems with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support device or system, or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body, or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.

ICE2QS01

Revision History:	2011-12-14	V1.1
Previous Version:	1.0	

Page	Subjects (major changes since last revision)
9	Revise typo in equation

Design Tips for Flyback Converters Using the Quasi-Resonant PWM Controller ICE2QS01
Licensed to Infineon Technologies Asia Pacific Pte Ltd <ANPS0005>

Hu Jing
Jing.hu@infineon.com
He Yi
Yi.he@infineon.com
Luo Junyang
Junyang.luo@infineon.com
Jeoh Meng Kiat
Mengkiat.jeoh@infineon.com

We Listen to Your Comments

Any information within this document that you feel is wrong, unclear or missing at all?
Your feedback will help us to continuously improve the quality of this document.
Please send your proposal (including a reference to this document) to:

ap-lab.admin@infineon.com

Table of Contents Page

1 Introduction 5
2 Design Tips 6
2.1 ZC Time Delay Circuit 6
2.2 Changing Power at Entering and Leaving Burst Mode Operation 7
2.3 Influence of the Foldback Point Correction on System Design 10
2.4 Selection of Switching Frequency 11
2.5 VCC Power Supply Circuit Arrangement 11
2.6 PCB Layout 11
3 Literature 12

1 Introduction

Quasi-resonant flyback converter is a cost-effective topology and commonly used for off-line power supply systems in low and medium power range. Typical application circuit and key waveforms of such a converter are shown in Figure 1 and Figure 2, respectively.

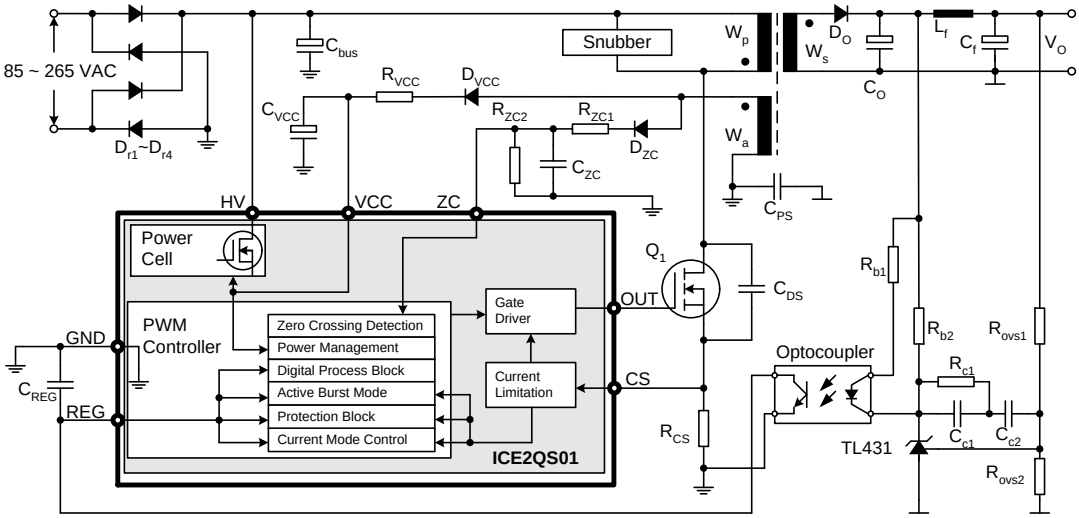

Figure 1 A Typical Application of ICE2QS01

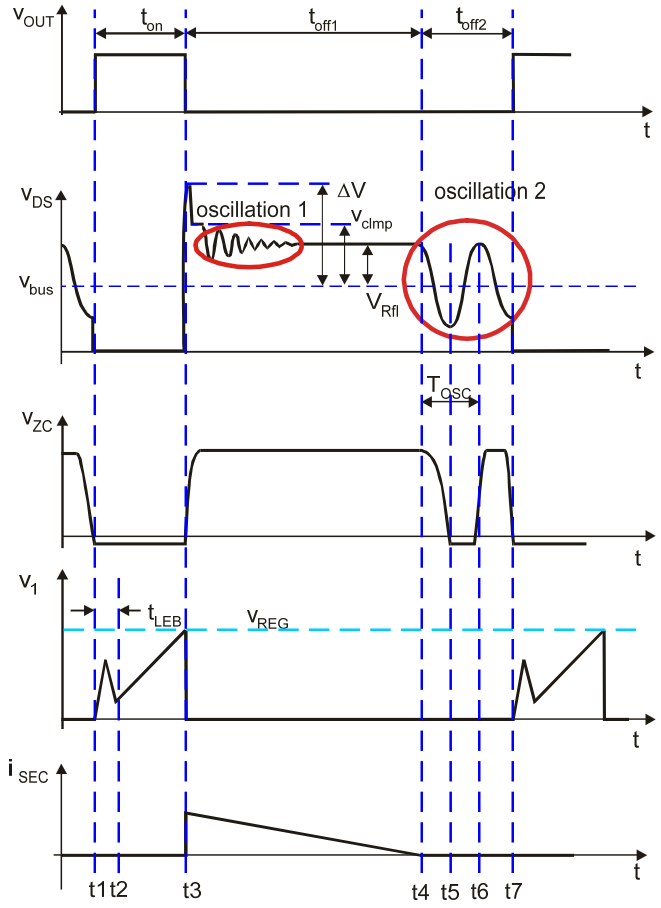

Figure 2 Key waveforms of a quasi-resonant flyback converter

2 Design Tips

By using the controller ICE2QS01, it is possible for designers to achieve an excellent system performance by fine tune of the converter system. On the other hand, this may mean a challenge for designers since the controller IC offers a lot of flexibility. Therefore, some design tips are given as below for users' reference.

2.1 ZC Time Delay Circuit

As shown in Figure 2, the time delay circuit for the zero-crossing detection consists of D_{zc}, R_{zc1}, R_{zc2} and C_{zc}. Proper design of this circuit is key to realise switching-on at valley of the drain-source voltage. Following points should be taken into consideration for a proper design of this circuit.

First, output overvoltage protection (OVP) is realized by comparing the voltage at this pin V_{zc} with an internal threshold. Therefore, the voltage divider formed by the resistors R_{zc1} and R_{zc2} should be chosen so that the voltage at this pin exceeds the threshold for the output overvoltage protection V_{OVP} only when the output voltage exceeds the specified value V_{oOVP}. This means that the following equation should be fulfilled:

$$\frac{R_{ZC2}}{R_{ZC1}+R_{ZC2}}\cdot\frac{N_{AUX}}{N_S}\cdot(V_{oOVP}+V_{Do})=4.5V \qquad [1]$$

where V_{Do} is the forward voltage drop of the output diode.

Second, threshold for the zero-crossing detection is set to 50mV. Third, the circuit has certain propagation delay from detected zero-crossing to the main power switch is fully turned on. Both of these have their influence on the time delay setting of the circuit. Theoretically, a time-delay of 1/4 of the main oscillation period should be achieved by this circuit for purpose of switching-on at at valley of the drain-source voltage. But taking the set threshold for zero-crossing detection and the propagation delay into consideration, the needed time delay should be:

$$C_{ZC}=\tan\left[2\pi\cdot\left(\frac{1}{4}-(t_{delayInt}+t_r)\cdot f_{osc}\right)\right]\cdot\frac{R_{ZC1}+R_{ZC2}}{R_{ZC1}\cdot R_{ZC2}}\cdot\frac{1}{2\pi\cdot f_{osc}} \qquad [2]$$

where $t_{delayInt}$ is the time delay from the voltage v_{zc} reached 50mV at its falling edge and the output gate drive signal rising from 0 to 90% of the voltage at high level. Typical value of this time delay is around 40ns; and

t_r the main power switch turn-on time.

Theoretically, it is flexible to select the capacitance and the resistance to fulfill the requirement as mentioned above. However, in practice, one should pay attention to the voltage at the auxiliary winding, especially the impact of different load on this voltage. At different loading conditions, the voltage at the auxiliary winding has different waveform, which is shown in Figure 3.

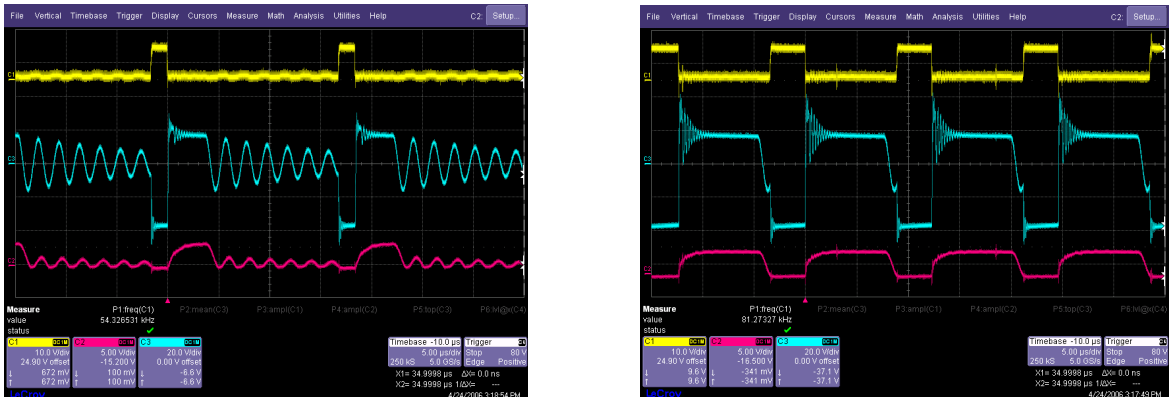

Figure 3 Voltage at the gate (CH1, upper curve), auxiliary winding (CH3, middle curve) and ZC pin (CH2, lower curve) at light load (left) and heavy load (right)

It is seen that after switching-off of the main switch the voltage at the auxiliary winding has certain peak and then followed by a ringing, generally. After this ringing is damped, the voltage at the auxiliary winding

is then proportional to the output voltage. However, the amplitude and duration of the ringing is quite different at light load and heavy load. At light load, the amplitude of the ringing at the auxiliary winding is much smaller and the duration is shorter than at heavy load condition. This is due to the different amplitude of the primary current at switch-off of the main switch. This difference has its impact on both the VCC power supply circuit (will be discussed later) and the ZC time delay circuit. To avoid mistriggering of the output overvoltage protection from this peak and oscillation, it is advisable that a proper capacitance is selected so that the high-frequent oscillation will be filtered by the time delay circuit and does not appear at the ZC pin, and therefore a smooth waveform is shown at the ZC pin, as the waveform taken from a real application shown in Figure 3.

2.2 Changing Power at Entering and Leaving Burst Mode Operation

In the controller IC ICE2QS01, active burst mode is integrated to achieve low input power during standby state. For a stable system operation, certain conditions must be fulfilled for a proper entering of burst mode operation. These include:

the regulation voltage is lower than the threshold of V_{EB}. Accordingly, the peak voltage across the shunt resistor is lower than 0.15V;

the up/down counter has its maximal value of 7; and

a certain blanking time.

The controller enters burst mode operation only when all of these conditions are fulfilled. Attention should be paid to that the regulation voltage should be lower than the threshold during the whole blanking time. Here, the blanking time is set so that a temporary voltage sinking of v_{reg} caused by a load jump down is allowed and this will not trigger the controller to enter active burst mode operation.

From these conditions for entering active burst mode operation, the input power at entering active burst mode operation is calculated as:

$$P_{EB} = \frac{1}{2} \cdot L_P \cdot (\frac{0.15}{R_{CS}})^2 \cdot f_{EB} \quad [3]$$

where f_{EB} is the switching frequency at entering burst mode operation, which is calculated by

$$f_{EB} = \frac{1}{\frac{0.15}{R_{CS}} \cdot L_P \cdot (\frac{1}{V_{BUS}} + \frac{1}{V_{Rfl}}) + 6.5 \cdot 2 \cdot \pi \cdot \sqrt{L_P \cdot C_{DS}}} \quad [4]$$

with L_p the primary main inductance of the transformer;

R_{cs} the current sensing resistance;

V_{bus} the bus voltage;

V_{Rfl} the value of the reflected output voltage at the primary side; and

C_{DS} the capacitance across the drain-source terminal.

During active burst mode operation, the IC monitors the regulation voltage V_{reg} and decides the burst on and off period. Once the regulation voltage exceeds the threshold V_{BH} of 3.6V, a burst-on period starts. During the burst-on, the switch frequency $f_{S\text{-}BURST}$ is fixed at 80 kHz. The voltage across the sensing resistor for current limit is set to 0.25 V, namely 25% of the maximum value during normal operation. When regulation voltage falls beneath the threshold V_{BL} of 3V, the IC stops the switch and monitoring the regulation voltage until it rises and exceeds 3.6 V to entering burst-on again. This period is the burst-off period. During the burst-off period the IC is still active and the regulation voltage V_{reg} is monitored.

When regulation voltage increases and crosses the threshold V_{LB} of 4.5 V, the IC leaves active burst mode operation. The power at leaving burst mode operation is the maximum power that the converter can supply during active burst mode operation where the burst ratio equals to 1. It can be calculated as

$$P_{LB} = \frac{1}{2} \cdot L_P \cdot (\frac{0.25}{R_{CS}})^2 \cdot f_{S\text{-}BURST} \quad [5]$$

It shows that P_{LB} is only influenced by the primary inductance L_p and the value of the current sensing resistor R_{CS} since the switching frequency is fixed.

For a certain design, the power levels at entering and leaving active burst mode operation are influenced by the bus voltage v_{bus}, the primary inductance L_p and the value of the sensing resistor R_{cs}. More exactly, a higher bus voltage results in a higher power at entering active burst mode operation, and a higher primary inductance or a smaller value of the sensing resistor results in a higher power at leaving active burst mode operation. In real application, one may wish to adjust the power levels at entering and/or leaving active burst mode operation. In the following paragraphs, possible solutions to change the power are discussed.

During a system design, one should take the influence of the switching frequency f_{EB} on the power at entering burst mode operation into consideration, as shown in equation [3]. The frequency or the period of the main oscillation has a big impact on the switchng frequency at entering active burst mode operation f_{eB}. The higher the capacitance, the longer the oscillation period, the lower the frequency f_{eB} and therefore the lower the power at entering active burst mode operation. This is one way to modify the power at entering burst mode operation by a proper choice of the capacitance C_{DS} with a certain value of the main inductance L_p. Principally, by changing this capacitance, the power at entering burst mode operation can be adjusted to be higher or lower according to the requirement of the application.

A second way to change the power at entering and leaving burst mode operation is to use an external circuit which can reduce both the power at entering and leaving burst mode operation. This circuit is shown in Figure 4.

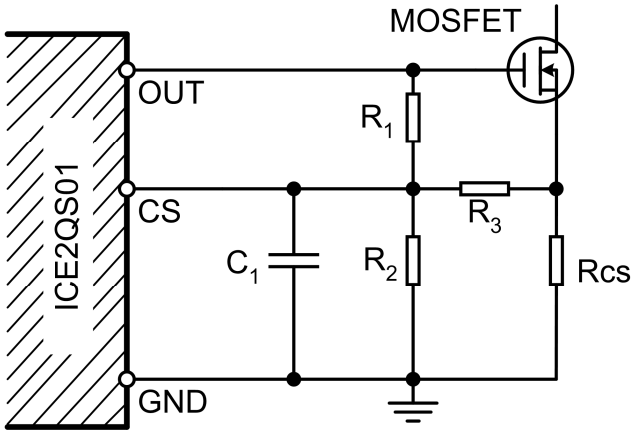

Figure 4 Additional external circuit for adjusting the power at entering burst mode operation

In this circuit, the resistors R_1 and R_2 are added to the original circuit where R_{CS} is the sensing resistor, R_3 and C_1 build up a low-pass filter whose typical value are 100Ω and 100pF, respectively. R_1 is connected to the OUT pin in the ICE2QS01. Influence of these additional components on voltages and then the power at entering and leaving active burst mode operation is discussed as in the following, with the aid of the Figure 5.

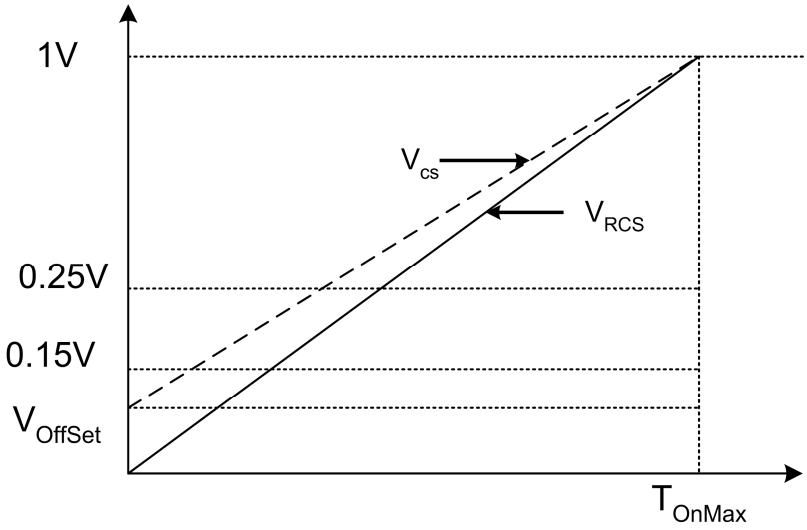

Figure 5 Voltage waveform with external modification circuit

When the MOSFET is turned on, an offset voltage V_{OffSet} is created on the CS pin. This offset voltage can be calculated as following since the resistance R_{cs} is much lower than R_3

$$V_{OFFSET} = V_{OUT} \frac{\frac{R_2 \cdot R_3}{R_2 + R_3}}{R_1 + \frac{R_2 \cdot R_3}{R_2 + R_3}} \quad [6]$$

As MOSFET is on, the current through MOSFET and R_{CS} increases with time. The voltage $V_{CS}(t)$ is then

$$V_{CS}(t) = V_{OFFSET} + V_{Rcs}(t) \frac{\frac{R_1 \cdot R_2}{R_1 + R_2}}{R_3 + \frac{R_1 \cdot R_2}{R_1 + R_2}} \quad [7]$$

While the first part is constant, the second part represents the sensed current and is proportional to the voltage across the current sensing resistor.

With a proper design of this circuit, the MOSFET on-time and the current level of the converter at entering and leaving active burst mode operation are decreased.

To avoid the influence of this circuit on the maximal deliverable power, it should be satisfied that the maximum current limit during normal operation is not changed by this offset voltage, namely 1V across the sensing resistor. This condition can be satisfied by setting below.

$$V_{cs-max} = V_{OUT} \cdot \frac{\frac{R_2 \cdot R_3}{R_2 + R_3}}{R_1 + \frac{R_2 \cdot R_3}{R_2 + R_3}} + V_{RCS-max} \cdot \frac{\frac{R_2 \cdot R_1}{R_2 + R_1}}{R_3 + \frac{R_2 \cdot R_1}{R_2 + R_1}} \quad [8]$$

with

$$V_{Rcs\text{-}max} = V_{cs\text{-}max} = 1V \quad [9]$$

To calculate the power at entering active burst mode, based on [7], the current in primary inductance is obtained as below where V_{CS} = 0.15V and $V_{RCS} = I_{P\_EB} * R_{CS}$.

$$I_{P\text{-}EB} = \frac{0.15V - V_{OFFSET}}{R_{CS}} \cdot \frac{R_3 + \frac{R_2 \cdot R_1}{R_2 + R_1}}{\frac{R_2 \cdot R_1}{R_2 + R_1}} \quad [10]$$

The power at entering active burst mode operation is then obtained as

$$P_{EB} = \frac{1}{2} \cdot L_P \cdot I_{P-EB}^2 \cdot f_{EB} \quad [11]$$

At leaving active burst mode operation, the actual current in primary inductance is then as below where V_{CS} = 0.25V and $V_{RCS} = I_{P\text{-}LB} * R_{CS}$.

$$I_{P\text{-}LB} = \frac{0.25V - V_{OFFSET}}{R_{CS}} \cdot \frac{R_3 + \frac{R_2 \cdot R_1}{R_2 + R_1}}{\frac{R_2 \cdot R_1}{R_2 + R_1}} \quad [12]$$

And the power at leaving active burst mode operation is

$$P_{LB} = \frac{1}{2} \cdot L_P \cdot I_{P-LB}^2 \cdot f_{S\text{-}BURST} \quad [13]$$

A design example for using this additional circuit to change the power at entering and the power at leaving burst mode operation is given below. The system condition is summarised as following.

Input bus voltage: V_{Bus}=375V;

Reflection voltage: V_{Rfl}=100V;

Primary inductance: L_P=132μH;

MOSFET drain-source capacitance: C_{ds}=750pF

Current sensing resistance: R_{CS}=0.11Ω;

OUT pin voltage during on-state: V_{OUT}=10V;

Low-pass filter: R_3=100Ω; and C_1=100pF.

The main oscillation period: T_{OSC}=1.98μs

Without any external modification circuit, the power at entering active burst mode operation is 8.1W and the power at leaving active burst mode operation is 27W.

To reduce the power at entering and leaving burst mode operation, an offset voltage (V_{OFFSET}) of 0.08V is chosen. Substituting the figures V_{OFFSET}=0.08V and V_{OUT}=10V to equation [6], it obtains equation [14].

$$\frac{R_2 \cdot R_3}{R_1 \cdot R_2 + R_2 \cdot R_3 + R_1 \cdot R_3} = 0.008 \quad [14]$$

Substituting the figures $V_{CS\text{-}max}$= $V_{RCS\text{-}max}$=1V and V_{OFFSET}=0.08V to equation [8], it obtains equation [15].

$$\frac{R_1 \cdot R_2}{R_1 \cdot R_2 + R_2 \cdot R_3 + R_1 \cdot R_3} = 0.92 \quad [15]$$

Solving the equation [14] and [15], it can obtain R_1 = 11.5kΩ (11kΩ is chosen) and R_2 = 1271Ω (1.2kΩ is chosen). As a result of selected resistors, the re-calculated offset voltage is 0.077V and the current to enter active burst mode operation is changed to 0.72A. Respectively the entering active burst mode power is changed to 2.4W (from 8.1W) and the leaving active burst mode power is changed to 15.2W (from 27W).

2.3 Influence of the Foldback Point Correction on System Design

In the controller ICE2QS01, the function of foldback point correction is integrated for purpose of a roughly constant maximum output power at different values of the bus voltage. To achieve this, the maximum current limit is designed to be dependent on the MOSFET on time. When the input voltage is higher, then the on time is shorter and therefore the maximum current limit is lower. To design converters with ICE2QS01, the designer can find the current limit ($V_{CS\text{-}max}$) from Figure 6 with the designed maximum on time. Then the current sense resistor need to calculated based on $V_{CS\text{-}MAX}$ and primary peak current. To ensure the power supply can start up at full load condition, it is suggested the current sense resistor to be chosen about 10% less than the calculated value. This is to provide some additional power overshoot at start up.

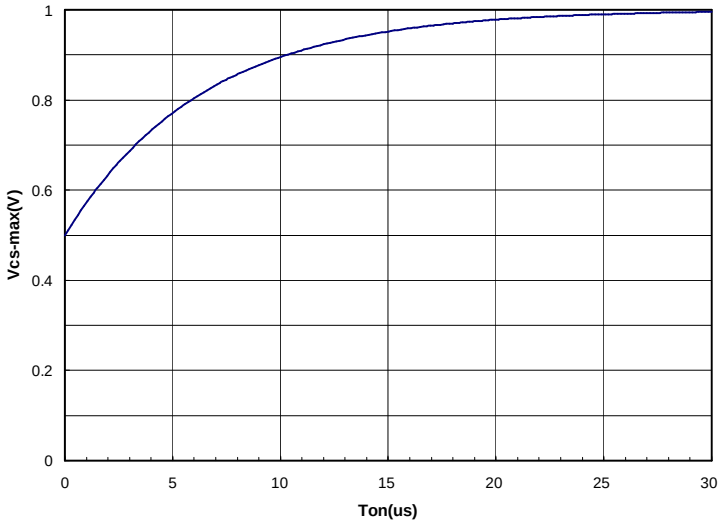

Figure 6 Maximum current limit on CS pin versus MOSFET on time

2.4 Selection of Switching Frequency

Switching frequency is a key parameter for the converter system and it is highly dependent on the application. Generally, for high power, the switching frequency is selected to be high to have a small transformer and to be low for low power application. Attention should be paid that the selected switching frequency has also impact on the power entering burst mode operation, and leaving burst mode operation with the current version of the controller which has a fixed switching frequency during burst mode operation. But with above mentioned solutions, the power can also be changed by deliberately used high or low capacitance of C_{DS} or using the additional external circuit. To minimize the effect of the foldback correction on the system performance, the possible lowest switching frequency is advisable.

2.5 VCC Power Supply Circuit Arrangement

Typical circuit for the VCC power supply is shown in Figure 1. In this case, the voltage at the auxiliary winding is rectified by the diode D_{VCC}, smoothed by the capacitors C_{vcc1} and C_{vcc2} and then supplies the VCC capacitor. The resistor R_{VCC} is used which limits the current through the Diode, to ensure that the VCC voltage will not exceed the upper limit for the VCC voltage at the highest load, where the peak voltage across the auxiliary winding is much higher than at low load as mentioned above. With this circuit arrangement, the VCC voltage may be kept in certain range to make the IC working properly. However, this VCC supply circuit has a big influence on the standby power consumption. To achieve ultra-low input power consumption (e.g., less than 100mW at no load), circuit shown in Figure 7 is proposed.

In case of no load, the burst ratio is very low, especially at the highest bus voltage. The transferred energy during the burst-on period is limited and not enough to support the IC. Though it is no problem for the IC to maintain its full function under this circumstance since the integrated power cell can supply the IC, but the power cell consumes certain energy which may reach 200mW and makes it difficult to fulfill the requirement on the input power limit of 100mW during burst mode operation at no load.

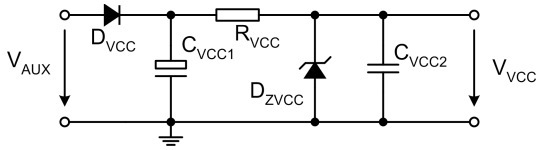

Figure 7 VCC circuit for low standby power

Compared to the VCC circuit in Figure 7, capacitor C_{vcc3} and Zener diode D_{zvcc} are added in this approach. The capacitor C_{vcc3} stores energy before the energy goes to the capacitor C_{vcc1} and C_{vcc2} through the resistor R_{vcc} when the main power switch is turned off. With this circuit arrange, more energy is available for supplying the IC and the VCC voltage may be kept above the value V_{VCCBL} below which the power cell delivers energy to keep VCC voltage constant at this level. As a result, ultra-low input power consumption can be achieved. For the parameter selection, the voltage of the zener diode should be higher than the VCC on threshold which is 22V, typically. In case the voltage of the Zener diode is low than the IC on threshold, a resistor is needed to be connected in series with the Zener diode. Additionally, the turns-ratio of the auxiliary winding to the secondary winding and the resistor R_{vcc} should be fine defined so that the voltage at the auxiliary winding is high enough to offer the energy needed for the IC at no-load burst mode operation. When all these parameters are fine tuned, an input power at no load condition can be far below 100mW. Measured at one 60W adapter application, it is only 50mW at high line and no load condition.

2.6 PCB Layout

In power supply system, PCB layout is a key point for a successful design. Following are some suggestions for this.

- Minimize the loop with pulse shape current or voltage; Examples are the loop formed by the bus voltage source, primary winding, main switch and current sensing resistor or the loop consisting of secondary winding, output diode and output capacitor, or the loop of VCC power supply.

- Good grounding of the controller IC; As the controller IC sees every signal to the reference point of the IC ground which is also the ground of the VCC power supply, it is advisable that the ground of the IC is connected to the bus voltage ground through short and thick PCB track in a star structure.

- Good grounding of other parts / functions. This includes the regulation loop ground and the VCC loop. It is advisable that for the controller all grounds connected to the VCC ground and then connected to the bus voltage ground using a star-structure

- The HV pins are connected to bus voltage in typical applications. During lighting test, the noise on bus voltage is high. It is suggested that the track to HV pin shall be as thin as possible and this track shall be kept away from other small signal tracks. The distance is better to be more than 3mm.

3 Literature

[1] ICE2QS01 datasheet, Infineon Technologies AG, 2006

[2] ANPS0003 Converter design using the quasi-resonant PWM controller ICE2QS01, Infineon Technologies AG, 2006

[3] AN-ICE1QS01 A new Quasiresonant Controller for Switch Mode Power Supplies Supporting Low Power Standby and Power Factor Correction (PFC), Infineon Technologies AG, 2004

[4] ICE3Axxx / ICE3Bxxx CoolSET F3 design guide, Infineon Technologies AG, 2004