Hybrid-flyback converter design with XDP™ digital power XDPS2201

About this document

Scope and purpose

Introduction of the hybrid-flyback (HFB) converter and its novel digital control IC XDP™ digital power XDPS2201, converter main stage design, parametrization via .dp vision tool and PCB layout hints.

Intended audience

Design engineers of power supply with high performance and ultrahigh power density.

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1 Introduction

Hybrid-flyback (HFB) is the most promising topology for ultrahigh power density and cost effective switching mode power supplies (SMPS). In this topology, both the transformer and the resonant capacitor store energy intermediately during the energy transferring from the primary to the secondary side. This reduces the necessary transformer size in comparison to the flyback converter and its variants. Additionally, due to the resonant characteristics, this topology operates very well with a wide input range while the switching frequency is limited within a relatively small range, which is beneficial for the EMI filter design.

XDPS2201 is a novel controller IC for this HFB converter. The key features and advantages of the IC are:

- 600 V depletion MOSFET integrated to support the VCC charge-up
- Integrated high-side (HS) and low-side (LS) MOSFET driver enabling a compact design
- Zero-voltage (ZV) switching without additional components for high efficiency, low system cost and ultrahigh power density design
- Multiple operation modes for optimized efficiency over the line, load current and output voltage ranges
- Complete configurable parameter set, and easy configuration via MFIO pin for easy design and platform approach
- High system robustness through comprehensive protection features
- Failure code communicated at the MFIO pin for ease of use

This document provides information about the control IC XDPS2201, and the HFB design describes the following topics:

- HFB topology and operating principle (***Chapter 2***)
- HFB control IC XDPS2201 (***Chapter 3***)
- HFB power stage design (***Chapter 4***)
- Parametrization (***Chapter 5***)
- PCB design tips (***Chapter 6***)
- Other information (***Chapter 7***)
- Summary (***Chapter 8***)
- References (***Chapter 9***)

2 HFB topology and operating principle

2.1 Hybrid-flyback topology

Figure 1 shows the HFB converter main stage.

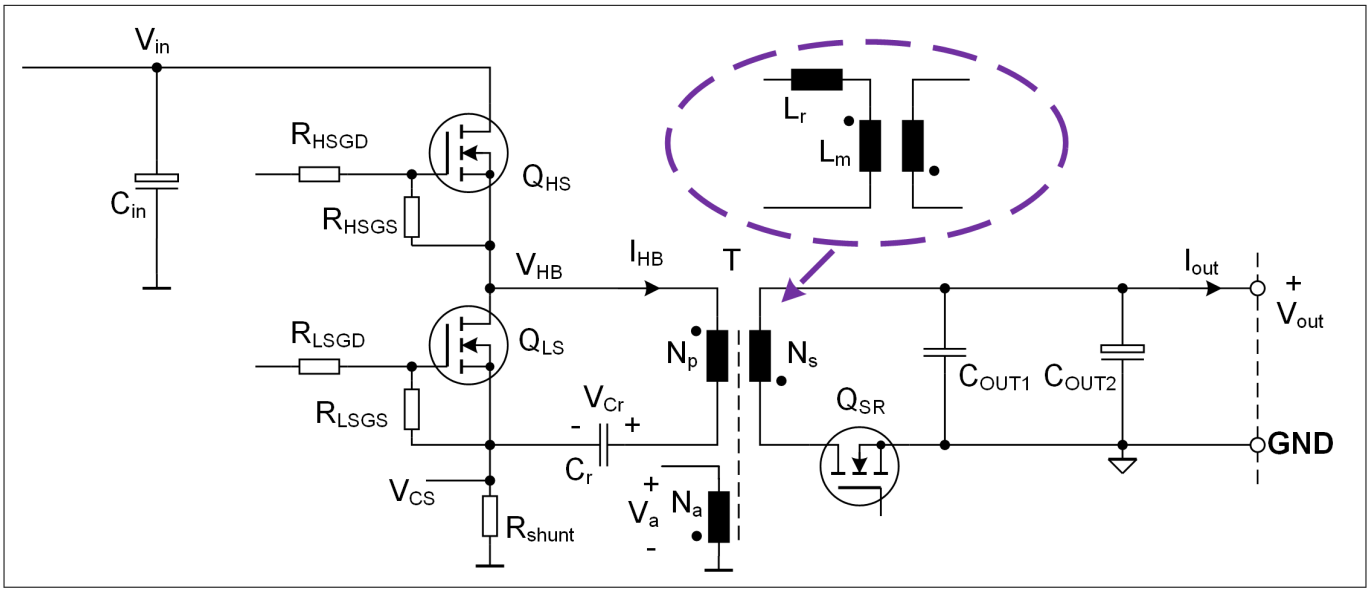


Figure 1 HFB main stage

The HFB converter consists of a HS switch (Q_{HS}) and a LS switch (Q_{LS}), the energy transfer elements out of a transformer *T* and a resonant capacitor C_r, and the output stage out of a synchronous rectifier (SR) MOSFET and output capacitors. In ***Figure 2***, the typical operating waveforms are shown in the continuous resonant mode (CRM) at the nominal output power P_{outnom}, defined as:

$$P_{outnom} = V_{outnom} \cdot I_{outnom}$$

Equation 1

with

- V_{outnom} as the maximum nominal output voltage, and
- I_{outnom} the maximum nominal output current

In the CRM operation, the primary inductance is magnetized during the on-time of the switch Q_{HS} (t_{HSon}) and demagnetized during the on-time of the switch Q_{LS} (t_{LSon}). Per a proper time control, HFB is running under the ZV turn-on for both MOSFETs. The ZV turn-on of the LS MOSFET is always achieved, since the current i_{HB} at that moment is adequate to force the body diode of the LS MOSFET to conduct before the LS MOSFET is turned on. The controller IC controls the LS gate pulse width to generate sufficient negative current to bring the voltage V_{HB} back to the voltage V_{in} before the HS MOSFET is turned on. In this way, the ZV turn-on is ensured for both MOSFETs, which ensures high system efficiency without additional components. Therefore, this HFB topology is very promising for cost effective and ultrahigh power density converters, such as USB-PD fast charger. A typical application circuit for this application is illustrated in ***Figure 3***.

2 HFB topology and operating principle

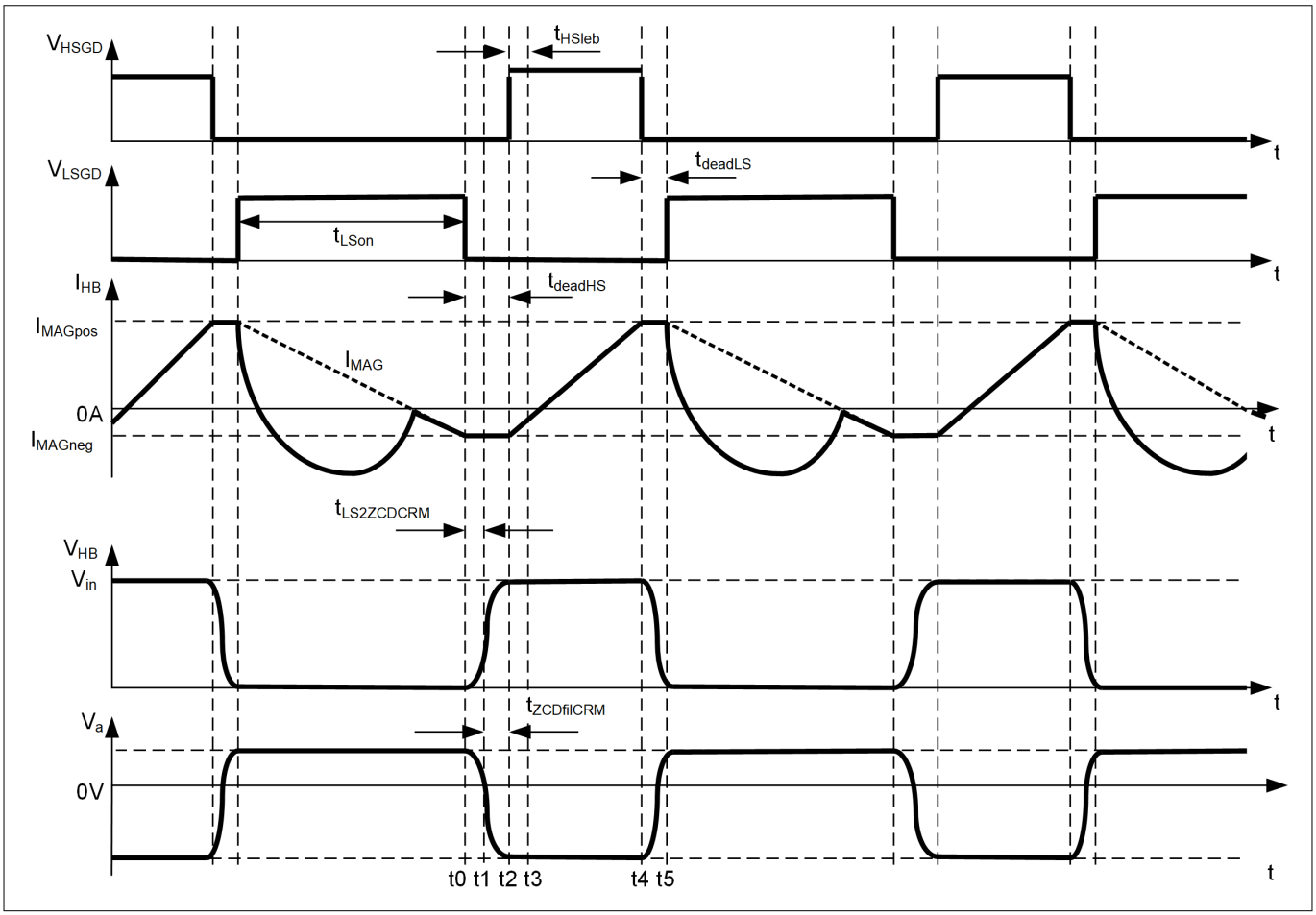


Figure 2 Typical waveforms in the CRM operation

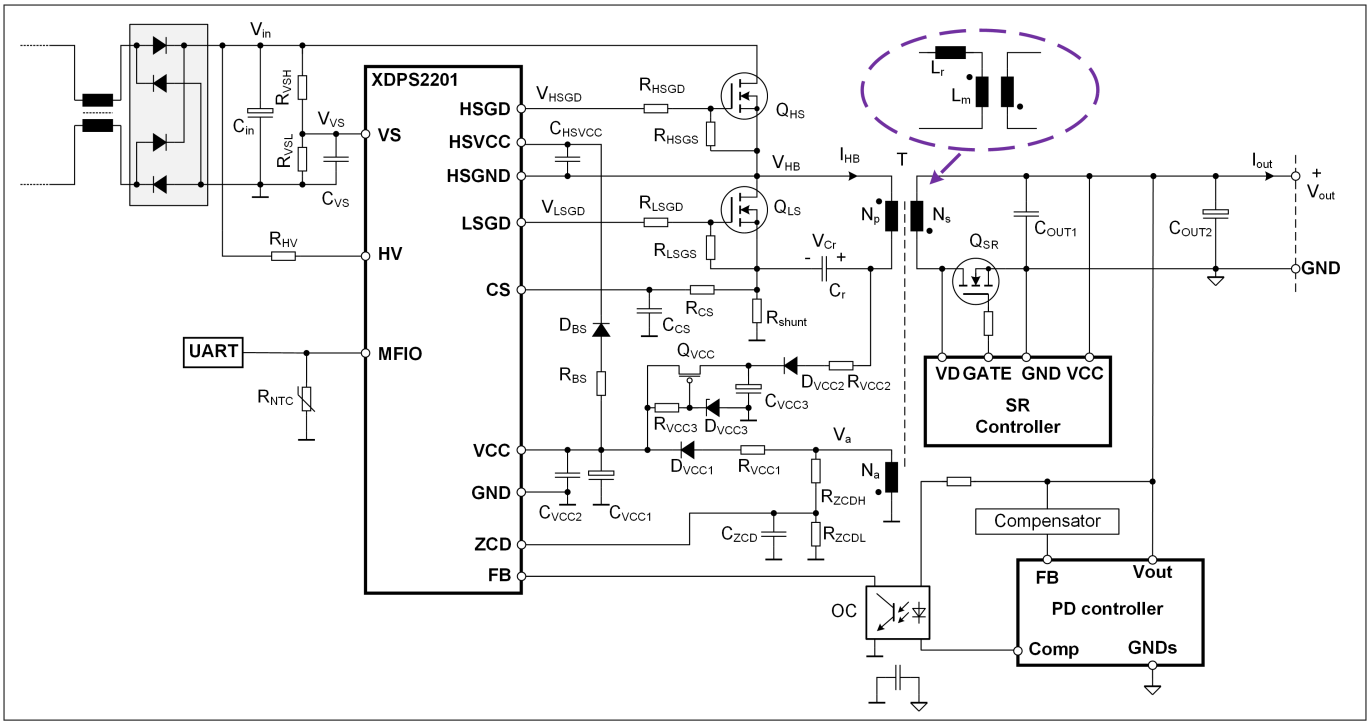


Figure 3 HFB in the USB-PD application

In this application, the PD controller senses the output voltage and sends the feedback signal at the Comp pin. Through the opto-coupler, the signal V_{FB} is generated at the FB pin of the controller XDPS2201, which is utilized to regulate the output voltage. Since the output is of wide range for the USB-PD application, the controller XDPS2201 cannot be powered only via the auxiliary winding N_a as in a convention flyback with only one output voltage level. A linear regulator is also required to generate the VCC supply voltage from the resonant capacitor at low output voltage.

Naturally, HFB is not only suitable for this USB-PD application, but also promising for conventional SMPS due to its outstanding performance. A typical application circuit for SMPS is shown in ***Figure 4***. Depending on the rated output power, a PFC stage may apply which is not depicted here.

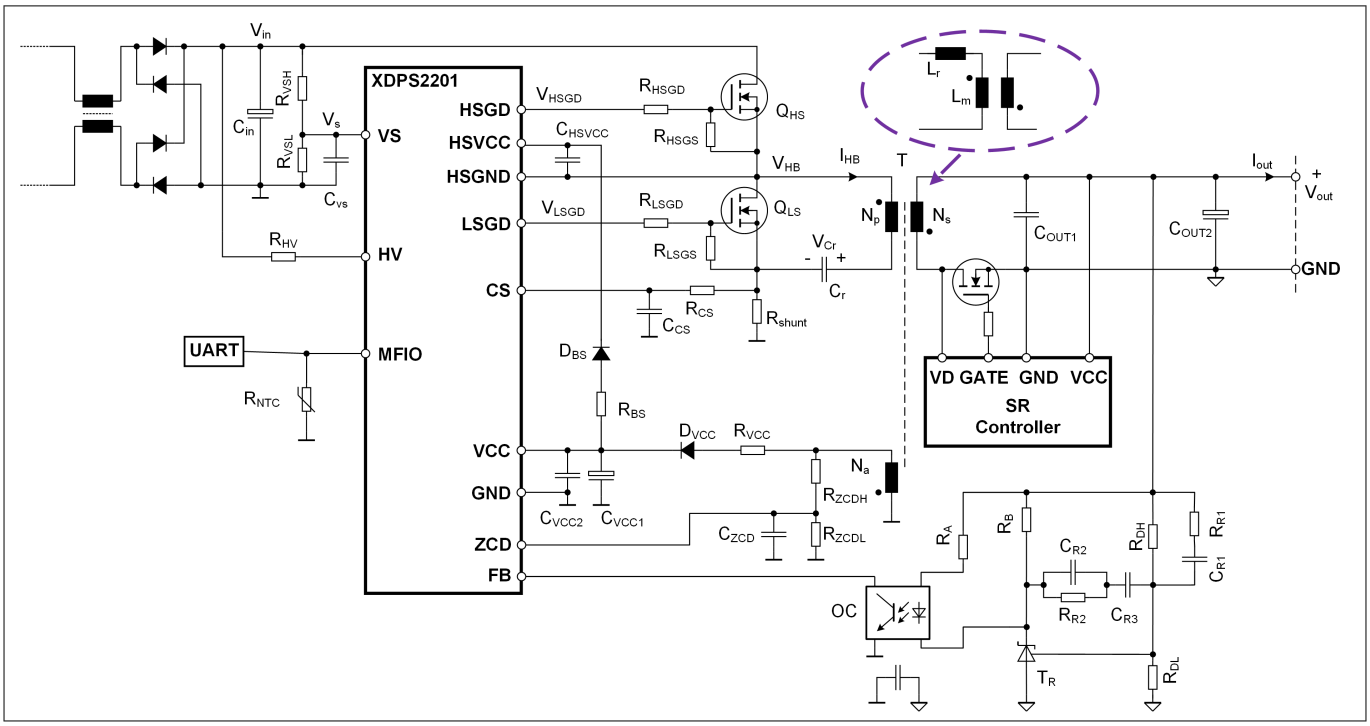


Figure 4 HFB in the conventional SMPS application

2.2 Operating principle

The following assumptions are made to simplify the analysis:

- CRM operation at the nominal load
- Dead-time before the HS and LS switches turn-on $t_{deadHSCRM}$ and t_{deadLS} (***Figure 2***) ignored
- Much lower ripple than the average value of the voltage across the resonant capacitor
- Transformer magnetizing inductance L_m much higher than the leakage inductance L_r
- On-time of the HS switch t_{HSon} much shorter than the resonant period T_{r2} based on the primary magnetizing inductance L_p and the resonant capacitance C_r (***Figure 5***)
- Conduction voltage drop of the SR MOSFET ignored
- All losses ignored

The operating principle of HFB, along with these assumptions, is discussed as follows:

- Voltage transfer function (***Chapter 2.2.1***)
- Current transfer function (***Chapter 2.2.2***)
- Two resonant periods (***Chapter 2.2.3***)

2.2.1 Voltage transfer function

As shown in the typical application waveforms (***Figure 2***), the magnetizing inductance is regulated by the voltage-second balance law during the steady-state operation, which gives:

$$(V_{\text{in}} - V_{\text{cr}}) \cdot D = N \cdot V_{\text{out}} \cdot (1 - D)$$

Equation 2

with

- V_{in} as the HB input voltage across the input capacitor C_{in}
- V_{cr} the average voltage across the resonant capacitor C_{r}
- D the HS MOSFET Q_{HS} on-time duty ratio $\frac{t_{\text{HSon}}}{T}$
- N the transformer turns ratio $\frac{N_p}{N_s}$, and
- V_{out} the output voltage

In the steady-state operation, the average voltage across the resonant capacitor in HFB is described as:

$$V_{\text{cr}} = N \cdot V_{\text{out}}$$

Equation 3

From these equations, the voltage transfer function k_{v} is given by:

$$k_{\text{v}} = \frac{V_{\text{out}}}{V_{\text{in}}} = \frac{D}{N}$$

Equation 4

This indicates the output voltage is controlled by the on-time duty ratio of the HS switch D.

2.2.2 Current transfer function

During the steady-state operation in CRM, the following equations are valid:

$$T = t_{\text{HSon}} + t_{\text{LSon}}$$

Equation 5

$$t_{\text{LSon}} = \frac{\left(I_{\text{MAGpos}} - I_{\text{MAGneg}}\right) \cdot L_{\text{p}}}{N \cdot V_{\text{out}}}$$

Equation 6

$$P_{\text{in}} = V_{\text{in}} \cdot \frac{1}{2} \cdot \left(I_{\text{MAGpos}} + I_{\text{MAGneg}}\right) \cdot D$$

Equation 7

$$P_{\text{out}} = V_{\text{out}} \cdot I_{\text{out}}$$

Equation 8

From these equations, the output current can be expressed as:

$$I_{\text{out}} = \frac{N}{2} \cdot \left(I_{\text{MAGpos}} + I_{\text{MAGneg}}\right)$$

Equation 9

This equation shows the output current I_{out} is purely dependent on the positive and negative peak currents in the primary magnetizing inductor.

Based on the voltage and current transfer functions, the output voltage can be regulated by peak current control, where the feedback signal V_{FB} sets the peak of the positive current I_{MAGpos}. A proper LS gate pulse controls the amplitude of the negative current for the ZV switching of the HS switch.

2.2.3 Two resonant periods

The detailed operation intervals of HFB in CRM is illustrated in the datasheet [2], while the equivalent circuit at different switching time phases and the related resonant periods are illustrated in ***Figure 5***.

Once the LS switch is turned on, a resonant circuit is built out of the transformer leakage inductance L_{r} and the resonant capacitor C_{r}, while the entire secondary side circuitry is acting as a voltage source in parallel to the magnetizing inductance since the SR MOSFET diode is forwarded biased. The energy stored in the magnetizing inductance L_{m} and the capacitor C_{r} charges the secondary side capacitors. This energy transfer lasts until the time reaches half of the period T_{r1}, which is mainly defined by the resonant inductance L_{r} and the capacitance C_{r}:

$$T_{\text{r1}} = 2\pi\sqrt{L_{\text{r}} \cdot C_{\text{r}}}$$

Equation 10

Up the time $\frac{T_{\text{r1}}}{2}$, the secondary side rectifier is reverse biased and blocks, and the primary side circuit begins to resonant including the main magnetizing inductance L_{m}. The resonant period T_{r2} is defined by:

$$T_{\text{r2}} = 2\pi\sqrt{(L_{\text{r}} + L_{\text{m}}) \cdot C_{\text{r}}} = 2\pi\sqrt{L_{\text{p}} \cdot C_{\text{r}}}$$

Equation 11

This equation is valid until the switch Q_{HS} is turned off. For the system design, these two different resonant periods have to be taken into account, which is explained in ***Chapter 4***.

2 HFB topology and operating principle

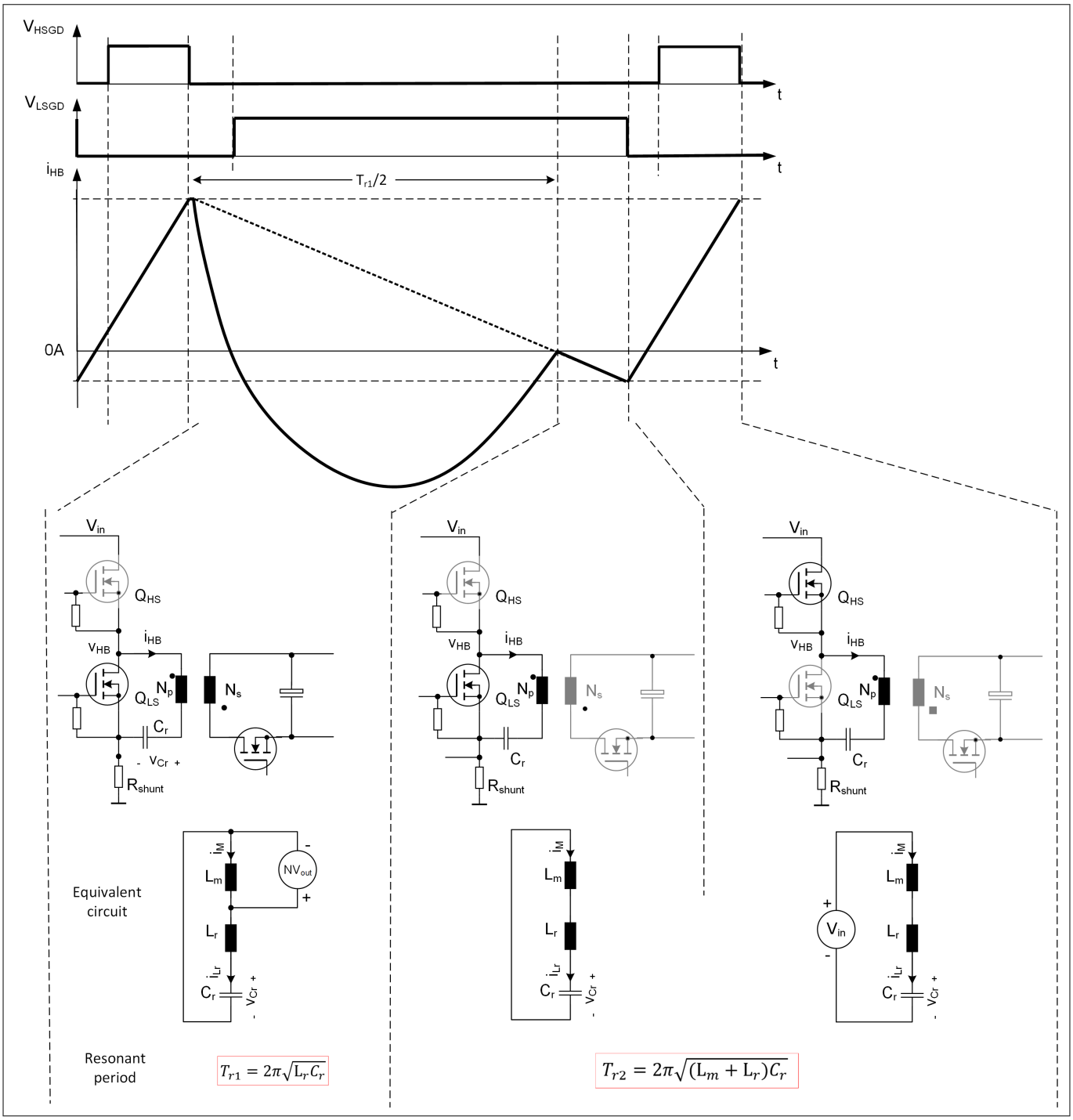


Figure 5 Equivalent circuit and resonant period at different intervals

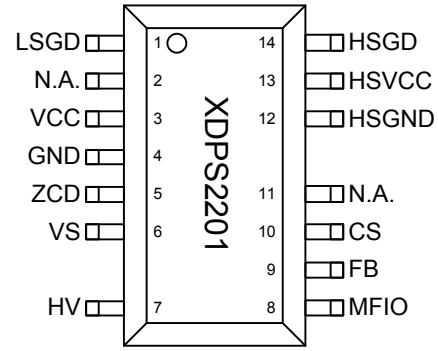
3 HFB control IC XDPS2201

The control IC XDPS2201 is a digital control IC for HFB. The basic operating principle is explained in the following sub-chapters:

- Pin configuration (***Chapter 3.1***)
- Peak current control and zero-voltage turn-on (***Chapter 3.2***)
- Output regulation and operation modes (***Chapter 3.3***)
- Frequency jitter (***Chapter 3.4***)
- Protection (***Chapter 3.5***)

3.1 Pin configuration

The pin configuration is shown in ***Figure 6*** and ***Table 1***. The pin functions are described in the sequel.



PG-DSO-14 (150mil)

Figure 6 Pin configuration

Table 1 Pin definitions and functions

Symbol	Pin	Type	Function
LSGD	1	O	**Low-side gate driver** Low-side gate driver of half-bridge driver stage
N.A.	2	—	**Not available** This pin is internally connected but not used, and should be connected to GND
VCC	3	I	**Positive voltage supply** IC power supply
GND	4	O	**Ground** Combined power and signal ground
ZCD	5	I	**Zero-crossing detection** *ZCD* pin provides zero-crossing detection after the low-side gate driver is turned off, during pause phase in skip cycle and burst mode. Furthermore, the reflected output voltage at auxiliary winding can be measured during the low-side gate driver turn-on phase
VS	6	I	**Voltage sensing** Low leakage input voltage sensing pin for controlling the negative magnetization and protections. *VS* pin is connected to a resistor divider for measuring the bulk voltage

Table 1 Pin definitions and functions (continued)

Symbol	Pin	Type	Function
HV	7	I	**High-voltage input** *HV* pin is connected to the AC line via external resistors and 2 diodes. An internally connected 600 V HV start-up cell is used for the initial VCC charge
MFIO	8	IO	**Multi-functional input-output** UART communication for parameter configuration and failure mode reporting is provided by this pin. In addition, a connected NTC can be measured
FB	9	I	**Feedback** Input pin receiving the feedback control signal from the optocoupler
CS	10	I	**Current sensing** Input pin for current sensing during the high-side gate driver turn-on phase
N.A.	11	—	**Not available** This pin is internally connected but not used, and should be connected to GND
HSGND	12	O	**High-side ground** Ground reference node for floating driver domain
HSVCC	13	I	**High-side power supply** Power supply input for floating driver domain
HSGD	14	O	**High-side gate driver** Floating high-side gate driver of half-bridge driver stage

3.2 Peak current control and zero-voltage turn-on

In the controller XDPS2201, the peak current control is implemented for the primary inductor current, both positive and negative peaks. ***Figure 7*** shows the positive peak control scheme.

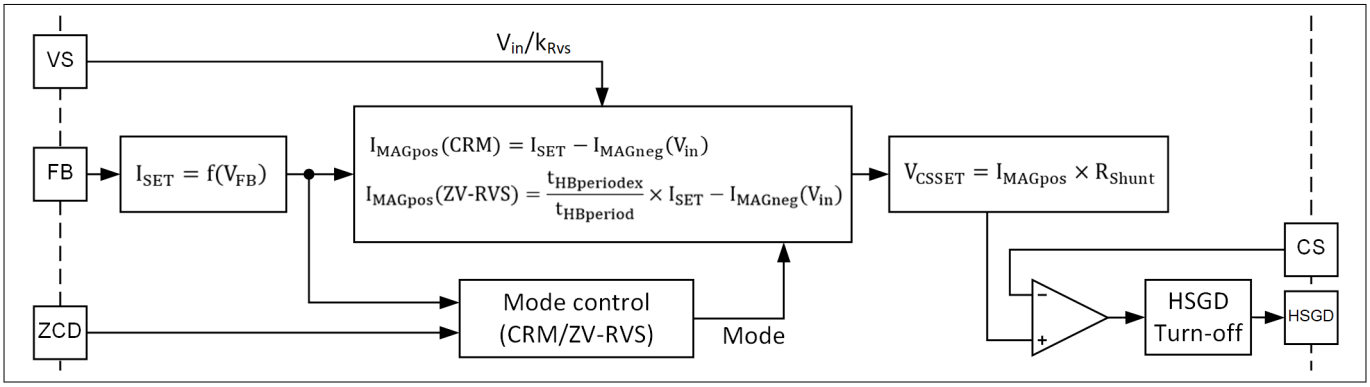


Figure 7 Positive peak current setting

The controller sets the target peak current I_{MAGpos} based on the feedback signal V_{FB}, bus voltage and output voltage level. The target voltage V_{CSSET} is then calculated and compared with the voltage V_{CS} at the CS pin. Once the voltage V_{CS} exceeds the target V_{CSSET}, the HS switch Q_{HS} is turned off. This defines the on-time of the HS switch Q_{HS} based on the feedback signal, input voltage and output voltage level for the output voltage regulation.

To ensure ZV turn-on of the HS switch, the negative current requires a certain amplitude. As from the main stage of HFB (***Figure 1***), the negative peak current during on-time of the LS switch cannot be sensed via the shunt

resistor. For the inductor negative peak current control, an adaptive control is implemented in the controller XDPS2201.

The on-time of the LS switch is calculated based on the parameter t_{TRANS}, voltage V_{in}, and time setting of $t_{LS2ZCDnom}$ and $t_{LS2ZCDmin}$. After the LS switch is turned off, the LS gate on-time for the next switching cycle is adjusted based on the measured time $t_{LS2ZCDCRM}$, to ensure the necessary negative current amplitude for ZV turn-on of the HS switch. The measured time $t_{LS2ZCDCRM}$ has information about the amplitude of the negative current: the higher the amplitude of the negative current, the shorter the measured time $t_{LS2ZCDCRM}$. If the measured time $t_{LS2ZCDCRM}$ is longer than the internal target time, the magnitude of the negative peak current is smaller than its target. In this case, the controller will increase the on-time of the LS switch in the next cycle or vice versa. In this way, the amplitude of the negative current is controlled in a certain level to achieve ZV turn-on of the HS switch and for high efficiency of the power transferring as low as possible.

3.3 Output regulation and operation modes

The control IC XDPS2201 employs several operation modes to ensure high system efficiency over the whole input and output ranges.

Figure 2 shows the waveform in CRM at the nominal output condition. In a certain power range around the nominal output power, the controller just modifies the amplitude of the positive peak current for the output voltage regulation. The lower the load level, the smaller the amplitude of the positive current and the shorter the on-time of the HS switch, while the negative peak current is adjusted according to the HFB input voltage. At the same level of the voltage V_{in} and therefore the same level of the negative peak current, the switching frequency at lighter load increases and the system efficiency decreases. To avoid this, the controller XDPS2201 implements the first discontinuous operation – zero-voltage resonant valley switching (ZV-RVS) – for the load in a certain range with the typical switching waveforms, as shown in ***Figure 8***.

In this operation mode, a waiting time $t_{waitgap}$ is added after the LS switch is turned off at t_{TRANS}, once the amplitude of the positive current reduces to below the value from $I_{SETCRM2RVS}$ ($I_{setnom} \cdot I_{SETCRM2RVS\_perc}$) (***Figure 9***). In this way, the effective switching period $t_{HBperex}$ is increased and the system efficiency is improved. In the controller XDPS2201, the added time break $t_{waitgap}$ depends on the load current. The lower the load current, the higher the number of ringing cycles N_{RVSval} and, therefore, the longer the waiting time $t_{waitgap}$.

To generate the required amplitude of the negative current for the ZV turn-on of the HS switch in the next switching cycle, the LS switch is turned on at a time of $t_{ZCDrefilRVS}$ after the rising edge of the ZCD signal, where the valleys N_{RVSval} is counted after the LS gate turn-off. This LS gate pulse is called ZVS pulse, and has a pulse width of t_{ZVS}. The SR MOSFET is forward biased during the time of t_{zvs} and conducts. This will cause the energy flows from the secondary side to the primary side of the converter. The backward energy transferring does not have much impact on the system efficiency since the energy is not consumed as power losses, but it helps to build up the required negative current in the magnetizing inductance while the resonant capacitor is charged up.

Note: In the real application, the minimum time of t_{zvs} should at least be equal to or higher than the minimum on-time of the SR controller to avoid a conduction overlap of the HS switch and the SR MOSFET.

If the load current increases while the system is running in the ZV-RVS mode, the operation may revert back into CRM, depending on the load voltage and current level. This transition is controlled by the programmable parameters: $I_{SETCRM2RVS\_perc}$, $I_{SETRVS2CRM\_perc}$, $V_{out\_CRM2RVS}$ and $V_{out\_RVS2CRM}$. ***Figure 9*** shows an overview of the different operating modes. While the boundary between the CRM and ZV-RVS mode can be set by these parameters, the time $t_{waitgap}$ is controlled with a right number of ZC N_{RVSval}, as shown in ***Figure 10***.

3 HFB control IC XDPS2201

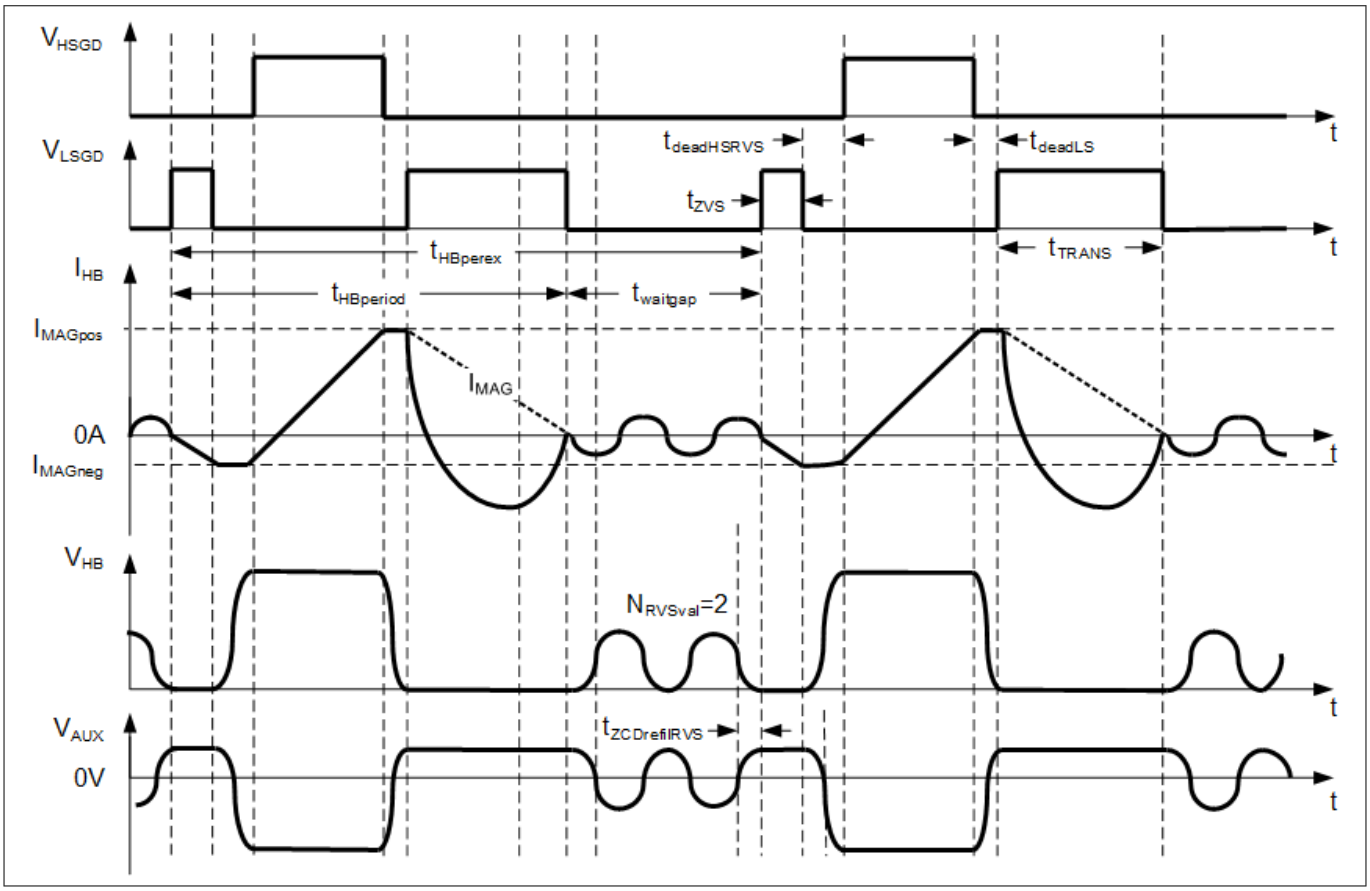


Figure 8 Discontinuous operation case 1 – ZV-RVS

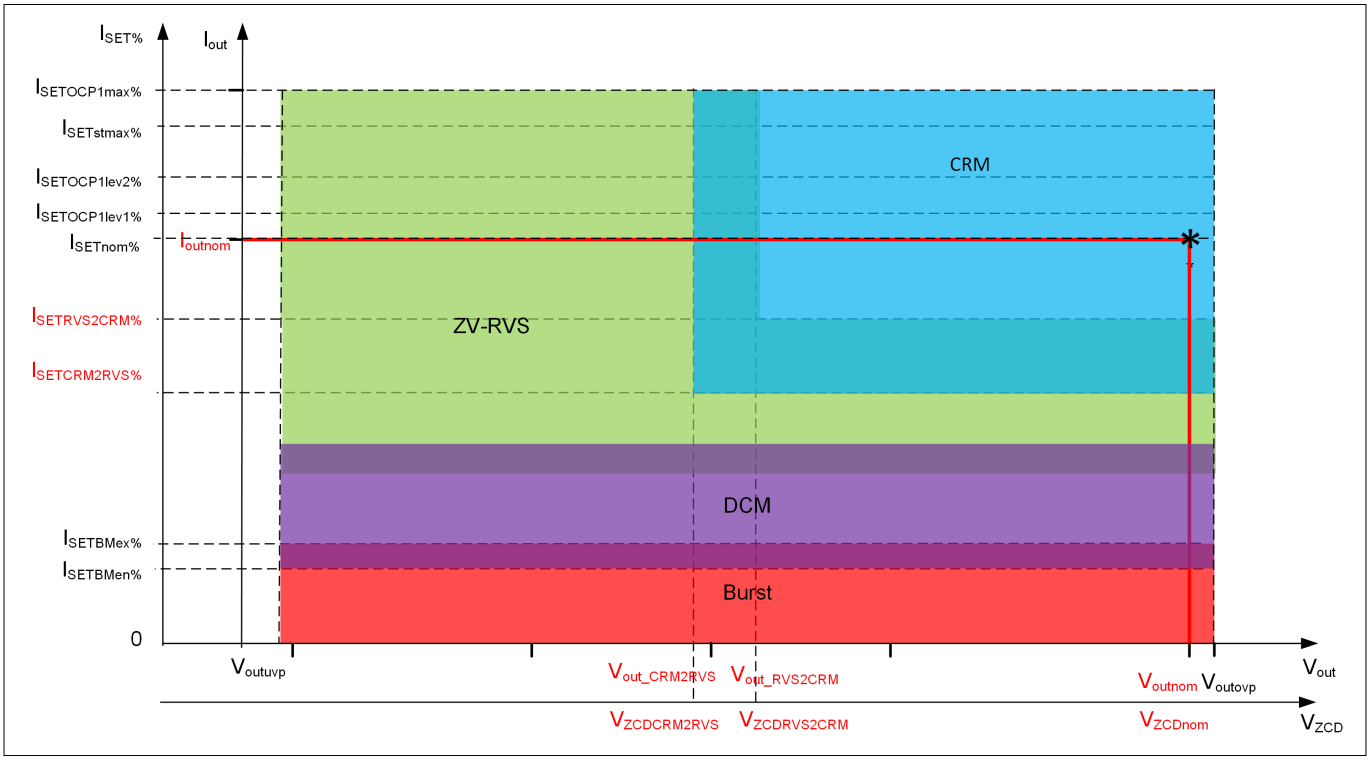


Figure 9 Operating modes

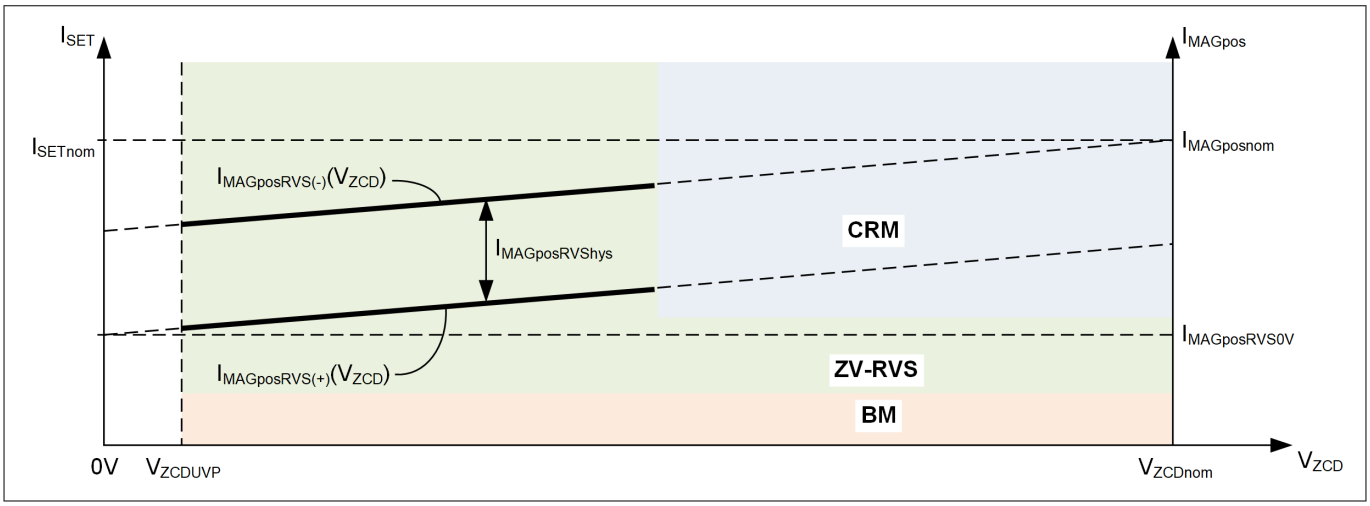


Figure 10 ZV-RVS waiting time control

In the ZV-RVS mode, the break time $t_{waitgap}$ is realized by counting the number of the ZC valley N_{RVSval} (***Figure 8***). If the set peak current is higher than the threshold $I_{MAGposRVS(-)}$ at the set output voltage level, then the target number for the ZC valley N_{RVSval} will be reduced by 1. On the other hand, if the set peak current is lower than the threshold $I_{MAGposRVS(+)}$ at the set output voltage level, then the target number for the ZC valley N_{RVSval} will be increased by 1. The hysteresis is determined by:

$$I_{MAGposRVShys} = \frac{1}{3} \cdot I_{MAGposnom}$$

Equation 12

The straight line $I_{MAGposRVS(+)}$ is determined by two end points (0, $I_{MAGposRVS0V}$) and (V_{ZCDnom}, $I_{MAGposnom}$). The value $I_{MAGposRVS0V}$ can be configured via the parameter $I_{MAGposRVS0V\_perc}$ by $I_{MAGposnom} \cdot I_{MAGposRVS0V\_perc}$, while the value of $I_{MAGposnom}$ is constant. Together with the hysteresis $I_{MAGposRVShys}$, the line $I_{MAGposRVS(-)}$ is determined.

In the real system, the ringing during the time $t_{waitgap}$ is damped and the amplitude is decreasing with time. Therefore, the number of this ringing N_{RVSval} is limited to the configurable $N_{RVSvalmax}$ for a reliable ZC detection. When the counted ZC number reaches the value of $N_{RVSvalmax}$, the system may operate in the discontinuous conduction mode (DCM), which is enabled or disabled by the parameter EN_{DCM}.

Directly after the system enters the DCM mode, the system operates with a slightly increased peak current of $125\,\% \cdot I_{MAGposRVS(+)}$ to have a hysteresis for the stable mode transition from ZV-RVS to the DCM operation. With a decreasing load current, the switching frequency sinks, but is limited by the set DCM minimum switching frequency F_{DCMmin}. With a further decreasing load current, the peak current is reduced for the output voltage regulation.

In case the output current sinks further and reaches the burst entry level $I_{outBMen}$ configured per the parameter $I_{SETBMen\_perc}$ by $I_{outnom} \cdot I_{SETBMen\_perc}$, the system enters another discontinuous operation – burst mode (BM) – for a further decreasing of the equivalent switching frequency and improvement of the system efficiency. The operation of the burst mode is illustrated in ***Figure 11***.

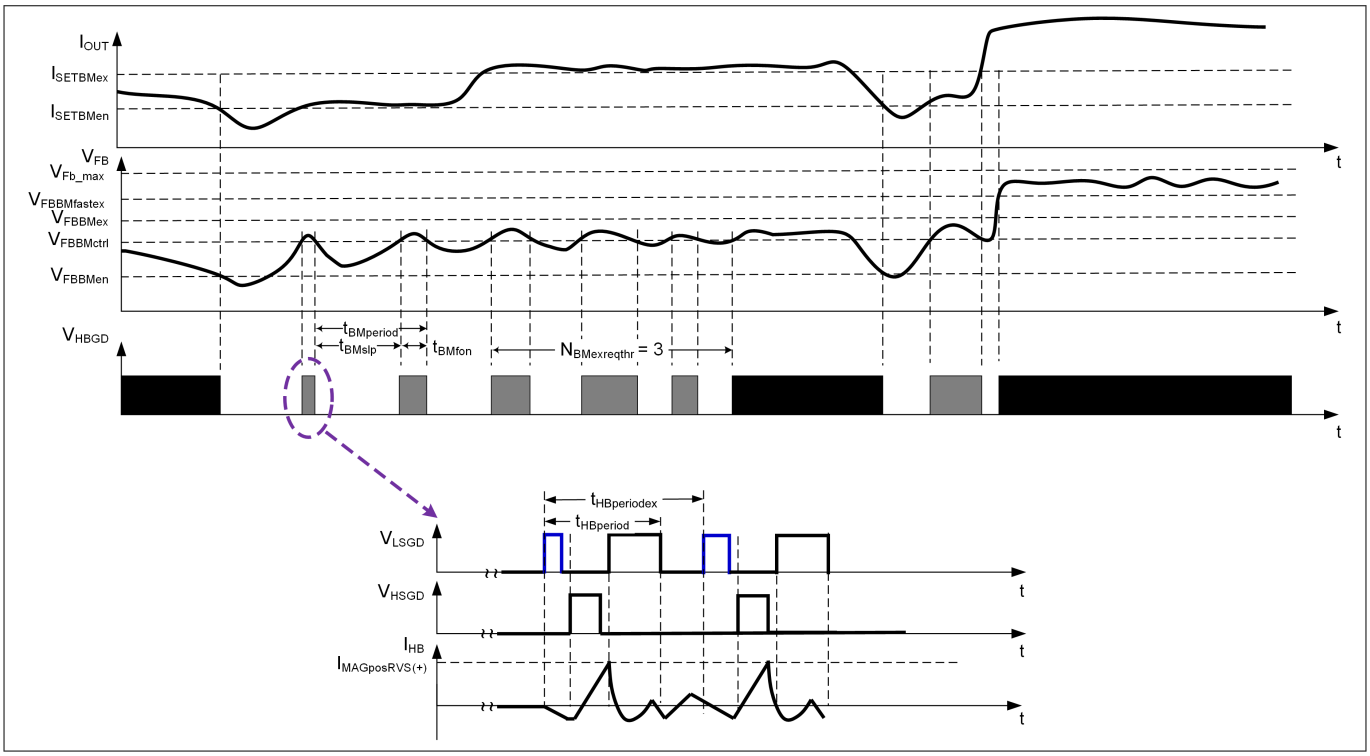


Figure 11 Discontinuous operation case 2 – burst mode operation

Based on the parameter $I_{SETBMen\_perc}$, the respected voltage at the FB pin V_{FBBMen} for burst entry is derived. Once the voltage V_{FB} is lower than the value of V_{FBBMen}, the system enters burst mode operation, beginning with a burst break – burst frame off-time. Later, when the feedback voltage rises above the threshold $V_{FBBMctrl}$, the break time ends and the next burst – burst frame on-time – begins. During the burst frame on-time, the feedback voltage sinks. When the feedback voltage under-crosses the threshold $V_{FBBMctrl}$, the next burst break begins. During the burst operation, the peak current is set by the line $I_{MAGposRVS(+)}$ according to the output voltage level (***Figure 10***).

Once the load power increases, the system may exit the BM operation. There are two types of burst exits: a fast and a slow burst exit. In case of a large load power jump-up, the feedback voltage rises above the set threshold $V_{FBBMfastex}$, the system exits the burst mode operation, and begins to operate in CRM or in the ZV-RVS mode, controlled by $EN_{BMfastexCRM}$. This is the fast burst exit scheme. In the other case, the output power increases slowly. During the BM operation, the output current is estimated based on the peak current set point $I_{MAGposRVS(+)}$, the burst frame on-time t_{BMfon} and the burst frame period $t_{BMperiod}$. Once the estimated output current is above the threshold $I_{SETBMex}$ (configurable per the parameter $I_{SETBMenx\_perc}$ by $I_{outnom} \cdot I_{SETBMex\_perc}$) for consecutive burst cycles defined by $N_{BMexreqthr}$, the system exits the burst mode operation. This is the slow burst exit scheme. With this fast and slow burst mode exit controls, the controller ensures a well-regulated output voltage and reliable burst exit transition.

3.4 Frequency jitter

Switching frequency jitter spreads the switching frequency spectrum around its center point to achieve a lower noise level, which is beneficial for the EMI filter design.

Two conditions must be fulfilled for activating the jitter function: system in the CRM operation and up the configured instantaneous input voltage V_{in_jitter}. The time duration of each frequency jitter step $t_{Jitterstpdel}$ must be much longer than the settling time of the regulation loop.

3.5 Protection

The IC pin MFIO is the interface for the communication between IC and computer for the parametrization. Additionally, the error code is sent out from this pin once a protection is triggered. The following table shows the protection features implemented in the control IC, failure code , reaction, evaluation criterion and the possible root cause.

Table 2 Failure code versus protection features

Failure code	Failure	Reaction	Evaluation criteria	Possible root cause
1	Slow BROWN_OUT 1	Immediate restart	V_{in} average value over 25.6 ms below $V_{brownout\_avg}$ [1)]	V_{in} average voltage too low
2	Slow BROWN_OUT 2	Immediate restart	V_{in} peak did not reach V_{in_SBOP} for longer than 44 ms	V_{in} value too low for more than 44 ms; too high capacitance at the VS pin
3	START-UP_TONMAX	Auto restart	$t_{HSon} > t_{HSonmax}$ with $t_{HSonmax} = 2 \cdot t_{TRANSnom}$ for the first $\frac{V_{outnom} \cdot N}{V_{VS} \cdot k_{Rvs}}$. HS gate pulse	Shunt resistor shorted; HS gate shorted to HS GND; HS VCC too low; improper connection of the CS pin or any of the HS driver pins
4	START-UP_TIMEOUT	Auto restart	Start-up failure due to timeout of no drop of the signal V_{FB} before the timeout threshold defined by $t_{startto}$	Output overload; output shorted; feedback circuit or pin open
5	START-UP_NO_ZCD	Auto restart	No ZCD detected during start-up time phase	Output shorted; wrong dimensioning of the ZCD voltage or ZCD voltage divider; wrong polarity of the auxiliary winding
6	VOUT_OVP	Latch/auto restart	$V_{ZCD} > V_{ZCDOVP}$, output overvoltage	Output overvoltage; open loop; wrong ZCD divider ratio; disturbance on the ZCD signal
7	VOUT_UVP	Auto restart	$V_{out} < V_{out\_UVP}$ during normal operation	Output overloaded; wrong ZCD divider ratio; disturbance on the ZCD signal
8	OCP1max	Auto restart	$I_{OUT} > I_{outnom} \cdot I_{SETOCP1max\_perc}$ for longer than the blanking time $t_{OCP1maxbl}$	Output shorted; heavy overload; disturbance on signal at the FB pin
9	OCP1lev1	Auto restart	$I_{OUT} > I_{outnom} \cdot I_{SETOCP1lev1\_perc}$ for longer than the blanking time $t_{OCP1lev1bl}$	Overpower; wrong shunt resistor value
10	OCP1lev2	Auto restart	$I_{OUT} > I_{outnom} \cdot I_{SETOCP1lev2\_perc}$ for longer than the blanking time $t_{OCP1lev2bl}$	Overpower; wrong shunt resistor value

1 The threshold is set to zero in FW = this protection disabled.

Table 2 Failure code versus protection features (continued)

11	Fast brown-out (VIN_UVP)	Immediate restart	$V_{in} < V_{in\_FBOP}$ during normal operation	V_{in} too low; bus capacitor too small
12	VIN_OVP	Auto restart	$V_{in} > V_{in\_OVP}$ during normal operation	V_{in} too high; wrong divider ratio for V_{VS}
13	OCP2	Latch	$V_{CS} > V_{CSOCP2}$	Damaged HS MOSFET; shorted transformer primary winding; charge current of the bootstrap circuit too high
14	START-UP_VFB_LOW	Auto restart	$V_{FB} < V_{FBBMctrl}$ before start-up	Output capacitor charged; wrong feedback signal
15	ZCD_ERROR at overload	Auto restart	Missing ZCD during normal operation	Output shorted; overload; erroneous ZCD signal
16	OTP	Auto restart and latch, or auto restart only	$R_{NTC} < V_{MFIOOTPtrig}$	V_{MFIO} pulled down; over temperature
17	OTP_START-UP	Auto restart	$R_{NTC} < V_{MFIOOTPrel}$ during start-up	V_{MFIO} pulled down at start up; over temperature
18	VIN_OO_RANGE	Immediate restart	$V_{in} < V_{in\_FBOP}$ or $V_{in} < V_{in\_SBOP}$ or $V_{in} > V_{in\_OVP}$	V_{in} either too high or too low; wrong V_{VS} divider or settings
19	Watchdog bite	Auto restart or latch	Reset timeout	CPU overload or run timing

For example, ***Figure 12*** shows the signal at the MFIO when the output overcurrent protection OCP1max (***Figure 46***) is triggered. The failure code begins with an initial indicator pulse which is of 2 µs. The total number of all the falling and rising edges after the initial pulse gives the failure code number as shown in ***Table 2***. For easy capture of the failure code, the oscilloscope trigger can be set to be *single trigger* with a pulse width above 1.5 µs at the level of 3 V.

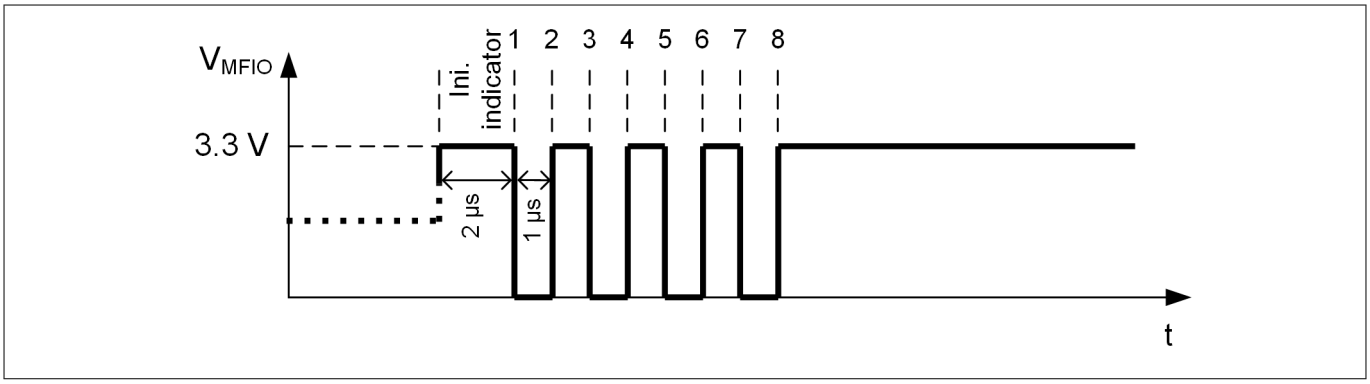


Figure 12 Failure code at the OCP1max triggered

4 HFB power stage design

This chapter focuses on the general design flow and design consideration of a HFB power converter including:

- Key initial design parameters (***Chapter 4.1***)
- Transformer key parameters and resonant capacitance (***Chapter 4.2***)
- Components connected to IC pins (***Chapter 4.3***)
- Output regulator (***Chapter 4.4***)

4.1 Key initial design parameters

Besides the previously mentioned parameters (V_{outnom}, I_{outnom} and V_{in_OVP}), the following parameters are defined:

- The minimum operating input voltage V_{in_min}
- The blocking voltage of the secondary side rectifier diode or synchronous rectifier (SR) MOSFET, here the SR MOSFET V_{DS_SR}
- Voltage derating factor of the SR MOSFET k_{VDS_SR}

4.2 Transformer key parameters and resonant capacitance

The following topics are discussed here:

- Transformer key parameters (***Chapter 4.2.1***)
- Resonant capacitor (***Chapter 4.2.2***)
- Design constraints (***Chapter 4.2.3***)

4.2.1 Transformer key parameters

Determination of the transformer turns ratio N

The transformer turns ratio is related to the SR MOSFET blocking voltage and the switch Q_{HS} maximum on-time duty ratio selection. The explanation is provided as follows.

In general, the SR MOSFET drain-source voltage during on-time of the HS switch is:

$$V_{DS\_SR\_op} = \frac{V_{in} - V_{Cr}}{N} + V_{out}$$

Equation 13

In this equation, the value of the voltages V_{Cr} and V_{out} depends on the operating condition, such as:

- The initial LS pulse at cold start-up
- During the normal operation

The HFB system operation begins with turn-on of the LS switch, to enable the charge-up of the capacitor C_{HSVCC} of the HS MOSFET Q_{HS} driver. At this first LS gate pulse, the resonant capacitor is discharged, which has been pre-charged by the HFB input voltage through the capacitive voltage divider built up by the drain-source capacitance of the switches Q_{HS} and Q_{LS}, and the resonant capacitor C_r. This is illustrated in ***Figure 13***.

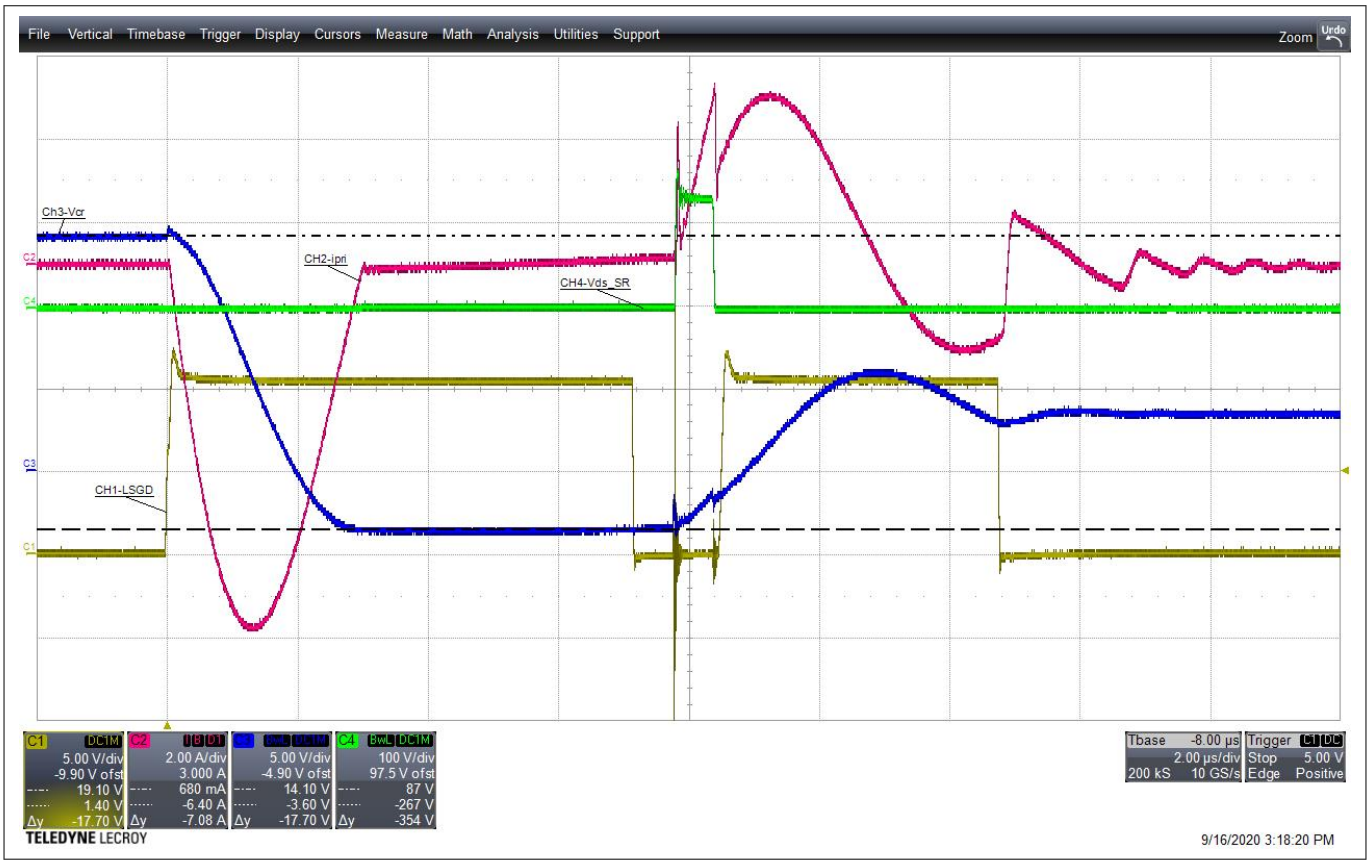


Figure 13 Voltage V_{Cr} at cold start-up

Here, the blue curve shows the voltage across the resonant capacitor, the pink curve represents the resonant tank current, and the green curve shows the voltage across the drain-source of the SR MOSFET. It is seen that the voltage across the resonant capacitor is around -3.6 V at turn-on of the switch Q_{HS}.

In the case of a normal operation, the voltage $V_{ds\_SR\_op}$ can be simplified, taking ***Equation 3*** into consideration as:

$$V_{DS\_SR\_op} = \frac{V_{IN}}{N}$$

Equation 14

Considering both the cases, the overvoltage protection level V_{in_OVP} defines the required minimum turns ratio of the transformer N_{min} by:

$$N_{min} = \frac{V_{in\_OVP}}{V_{DS\_SR} \cdot k_{VDS\_SR}}$$

Equation 15

For a conventional flyback converter, the value of k_{VDS_SR} is typically around 80%. To determine the maximum of the turns ratio N_{max}, the value of the minimum operating bus voltage V_{in_min} and the maximum duty ratio of the HS switch D_{max} must be considered. From the voltage-second balance, it is valid that:

$$N_{max} = D_{max} \cdot \frac{V_{in\_min}}{V_{outnom}}$$

Equation 16

4 HFB power stage design

Here, the N_{max} depends on the values of D_{max} and V_{in_min}. While the dependence of the maximum value D_{max} on the transformer inductance ratio $\frac{L_r}{L_p}$ is discussed in ***Chapter 4.2.3***, the determinative factors for the minimum operating voltage V_{in_min} are discussed in the following text.

For a AC-DC converter without PFC stage, the input current conducts only during a portion of the AC half-cycle t_{cond}, as shown in ***Figure 14***, and can be described by:

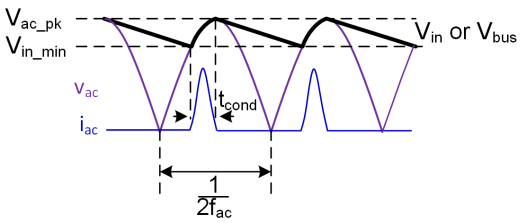


Figure 14 AC input current conduction period t_{cond}

$$t_{cond} = \frac{1}{2 \cdot f_{ac}} \cdot \left(\frac{1}{2} - \frac{\sin^{-1}\left(\frac{V_{in\_min}}{\sqrt{2} \cdot V_{ac\_minRMS}} \right)}{\pi} \right)$$

Equation 17

The minimum voltage V_{in_min} is related to many factors: the system maximum output power P_{out_max}, the system efficiency η, the selected bus capacitance C_{in}, the minimum input voltage V_{ac_minRMS} and the line frequency f_{ac}, which is described by the following equations.

The energy change in the capacitor C_{in} within half-cycle of the AC voltage is:

$$\Delta E_{Cin} = \frac{1}{2} \cdot C_{in} \cdot \left(2 \cdot {V_{ac\_minRMS}}^2 - {V_{in\_min}}^2 \right)$$

Equation 18

The energy drown by the output:

$$\Delta E_{Cin} = \frac{P_{out\_max}}{\eta} \cdot \left(\frac{1}{2 \cdot f_{ac}} - t_{cond} \right)$$

Equation 19

Based on these equations, the capacitance C_{in} and the related V_{in_min} can be expressed as:

$$C_{in} = \left(\frac{1}{2} + \frac{\sin^{-1}\left(\frac{V_{in\_min}}{\sqrt{2} \cdot V_{ac\_minRMS}} \right)}{\pi} \right) \cdot \frac{P_{out\_cont}}{\eta} \cdot \frac{1}{f_{ac}} \cdot \frac{1}{\left(2 \cdot {V_{ac\_minRMS}}^2 - {V_{in\_min}}^2 \right)}$$

Equation 20

Here, P_{out_cont} is the maximum continuous output power.

A further factor for the turns ratio determination is the transformer construction, such as the used core, bobbin and wires. Based on this information, the desired turns ratio of the transformer can be decided as N.

Determination of the transformer inductance

The HS switch on-time duty ratio D is 50% for operation at the nominal output condition and the input voltage V_{in_OpC1} (OpC1 = operating condition case 1, to distinguish this condition from others) is:

$$V_{\text{in\_OpC1}} = 2 \cdot N \cdot V_{\text{outnom}}$$

Equation 21

Based on the current transfer function of HFB, the positive peak current will be:

$$I_{\text{MAGposnom}} = 2 \cdot \left(1 + I_{\text{MAGnegnom\_perc}}\right) \cdot \frac{I_{\text{outnom}}}{N}$$

Equation 22

Here, the parameter $I_{\text{MAGnegnom\_perc}}$ is the factor of the negative peak current I_{MAGneg} (***Figure 2***) over the current $2 \cdot \frac{I_{\text{outnom}}}{N}$ for the ZV switching of the switch Q_{HS} and set to 15% as the starting point.

The peak-peak current in the magnetizing inductance will be:

$$I_{\text{MAGpkpknom}} = 2 \cdot \left(1 + 2 \cdot I_{\text{MAGnegnom\_perc}}\right) \cdot \frac{I_{\text{outnom}}}{N}$$

Equation 23

By giving a desired switching frequency f_{des} at the condition OpC1, the on-time of the LS switch $t_{\text{LSon\_OpC1}}$ is calculated by:

$$t_{\text{LSon\_OpC1}} = \frac{1}{f_{\text{des}}} \cdot \frac{V_{\text{in\_OpC1}} - N \cdot V_{\text{outnom}}}{V_{\text{in\_OpC1}}}$$

Equation 24

Now, the required magnetizing inductance L_{p} can be calculated from:

$$L_p = \frac{t_{\text{LSon\_OpC1}} \cdot N \cdot V_{\text{outnom}}}{I_{\text{MAGpkpknom}}}$$

Equation 25

Based on the given turns ratio and core shape, the magnetizing inductance L_{p} is decided. The factor of the leakage inductance k_{Lr} can be estimated based on the core shape and the winding construction. From this, the leakage inductance L_{r} can be calculated from:

$$L_r = k_{\text{Lr}} \cdot L_p$$

Equation 26

Naturally, this leakage inductance can be measured if the transformer is available.

4.2.2 Resonant capacitor

Determination of the value of the resonant capacitor

The resonant capacitance C_{r} can be calculated by:

$$C_r = \left(\frac{t_{\text{LSon\_OpC1}}}{\pi}\right)^2 \cdot \frac{1}{L_r}$$

Equation 27

So far, the design process of the main circuit is described and the value of the main stage parameters are calculated.

4.2.3 Design constraints

For a cost effective design, the resonant capacitance should be as low as possible, and with as few capacitors as possible in case many capacitors are connected in parallel to achieve a certain value. But there are some design constraints for choosing the value of both C_r and L_r for a certain value of t_{TRANS}.

Maximum duty ratio D_{max} for the switch Q_{HS}

Figure 5 shows the two resonant periods in the HFB converter. These resonant periods and the peak current control method set the limitation for the maximum on-time duty ratio for the HS switch D_{max}.

The HFB employs a peak current control. Usually, the on-time of the switch Q_{HS} is a small portion of the resonant period T_{r2} (t_{HSon} in ***Figure 15***), and the primary current arises almost linearly during this on-time t_{HSon}. Considering the extreme case, the possible maximum on-time of the switch Q_{HS} t_{HSon_max} is ¼ of the resonant period T_{r2} for the peak current control.

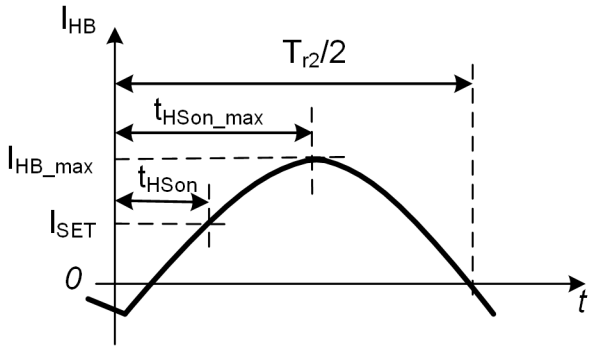


Figure 15 Possible resonant current during HS on-time and the maximal possible HS on-time

$$t_{HSon\_max} = \frac{T_{r2}}{4}$$

Equation 28

Ignoring the dead-time for both switches and the time for the negative current, the complete switching period is:

$$T_1 = t_{HSon\_max} + \frac{T_{r1}}{2} = \frac{T_{r2}}{4} + \frac{T_{r1}}{2}$$

Equation 29

Based on this equation, the relationship between the maximum duty ratio D_{max} and the transformer inductance ratio is:

$$D_{max} = \frac{\frac{T_{r2}}{4}}{\frac{T_{r2}}{4} + \frac{T_{r1}}{2}}$$

Equation 30

Applying ***Equation 10*** and ***Equation 11***, it is given that:

$$\frac{L_r}{L_p} = \frac{1}{4} \cdot \left(\frac{1}{D_{max}} - 1\right)^2$$

Equation 31

From this equation, the maximum duty ratio D_{max} of the switch Q_{HS} is limited by the transformer inductance ratio $\frac{L_r}{L_p}$, which is defined by the transformer structure and technique. With 55%, 70% and 75% for the D_{max}, the ratio $\frac{L_r}{L_p}$ are 16.7%, 4.59% and 2.78%, respectively.

Note: A high D_{max} means high RMS current at the secondary side, which has negative impact on the system efficiency curve.

Selection of resonant capacitance C_r

The USB-PD application has a wide range of output voltage. For this application, the resonant capacitor will be less dependent on the operating voltage, for example, film capacitor. For the cost effective and ultrahigh power density design, the value of the resonant capacitor must be as low as possible. However, there are some physical limitations for using a small resonant capacitance. This is discussed based on the simulated waveform for the CRM operation, as shown in ***Figure 16***.

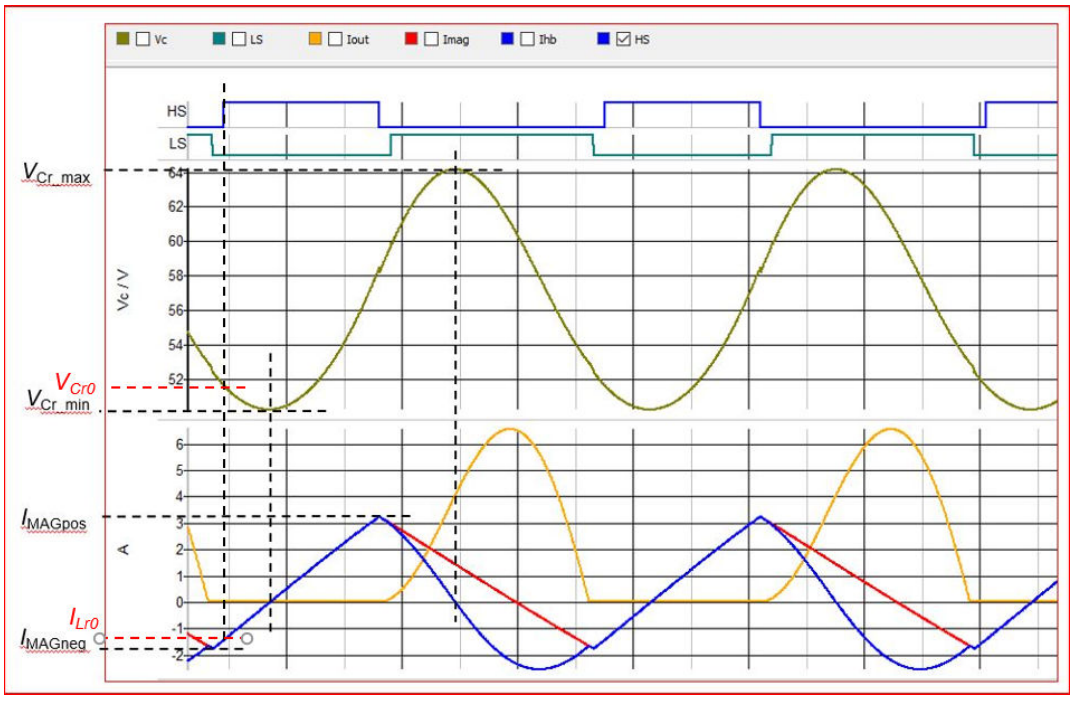


Figure 16 Key waveforms per simulation

During the on-time of the switch Q_{HS}, the current through the primary winding of the transformer (blue curve at the bottom) can be described as:

$$i_{Lp}(t) = i_{Lr0} \cdot \cos(w_{r2}t) + \frac{V_{in} - V_{Cr0}}{Z_{r2}} \cdot \sin(w_{r2}t)$$

Equation 32

The voltage across the resonant capacitor (yellow curve) is:

$$v_{Cr}(t) = V_{in} - (V_{in} - V_{Cr0}) \cdot \cos(w_{r2}t) + Z_{r2} \cdot i_{Lro} \cdot \sin(w_{r2}t)$$

Equation 33

with

$$w_{r2} = \frac{2\pi}{T_{r2}}$$

Equation 34

$$Z_{r2} = \sqrt{\frac{L_p}{C_r}}$$

Equation 35

From these equations, the maximum achievable primary side current is limited by the parameter Z_{r2}. Keeping L_p and V_{in} constant, the lower the capacitance C_r, the smaller the maximum peak current and the smaller the deliverable power. Therefore, for a certain maximal deliverable power, the capacitance C_r is limited. Furthermore, by using a small capacitance C_r, the voltage V_{in_min} has to be increased for a certain peak current, which needs a higher value for the capacitor C_{in}. This may be critical due to the size limitation. Additionally, the voltage ripple across the resonant capacitor C_r is higher with a lower capacitance C_r. Accordingly, a higher voltage rating for the resonant capacitor C_r is required. This leads to a higher cost, and it is contrary to the original intention for lowering down the system cost with a smaller capacitance C_r.

For the system optimization, it is recommended to follow the provided design flow, and optimize the system based on that design and the measurement results.

4.3 Components connected to IC pins

The design of the components connected to the IC pins are described, considering the schematic shown in ***Figure 3*** as an example.

4.3.1 CS pin: shunt resistor

The maximum value for the peak current control through the CS pin ($V_{CSOCP1max}$) is typically 0.437 V. The shunt value is given by:

$$R_{shunt} = \frac{V_{CSOCP1max} \cdot I_{setnom\_perc}}{\frac{2 \cdot I_{outnom}}{N}}$$

Equation 36

With I_{setnom_perc} is set to 50% for good overpower capability.

For the shunt resistor on the board, the value must be close to this calculated value. Once the shunt resistor's value is determined, the worst case peak current can be calculated by:

$$I_{HB\_pk\_wc} = \frac{V_{CSOCP2}}{R_{shunt}} + \frac{V_{in\_OVP} - N \cdot V_{outnom}}{L_p} \cdot t_{CSOCP2pd}$$

Equation 37

where, the second part of the equation derives from the propagation delay at the HS switch turn-off.

4.3.2 VS pin: voltage divider

The VS pin is utilized for the HFB input voltage V_{in} sensing, via the voltage divider from the resistor R_{VSH} and R_{VSL}. The following are the three main factors for the value selection of these resistors:

- The measurement range of the pin VS
- The pin leakage current
- The power losses in these resistors

Accordingly, the voltage divider resistors need to fulfill the following conditions:

$$k_{R\_VS} = \frac{R_{VSL}}{R_{VSL} + R_{VSH}} \leq \frac{V_{VSmax}}{V_{in\_max}}$$

Equation 38

$$\frac{V_{in\_min}}{R_{VSL} + R_{VSH}} \geq k_{I\_vs} \cdot I_{VSlkmax}$$

Equation 39

with

- V_{VSmax} as the maximal measurable voltage at the VS pin
- V_{in_max} the maximum bus voltage
- $I_{VSlkmax}$ the VS pin maximum leakage current, and
- K_{I_vs} the ratio of the current through the voltage divider resistor and the pin leakage current, normally 10

Once these requirements are fulfilled, the resistor value must be as high as possible to minimize the power losses in these resistors.

For this pin, a capacitor with a small capacitance may be needed to filter the switching noise. It is normally up to several hundred pF, while a large capacitance results in a greater time delay, and therefore, a lower value of the signal V_{VS} at the AC valley where the fast brown-out protection may be triggered.

4.3.3 Auxiliary winding turns ratio and voltage divider

Conventionally, the auxiliary winding voltage V_a is used for supplying the control IC and for ZCD. In the controller XDPS2201, this voltage is additionally utilized for the output voltage level measurement. For a proper output voltage measurement, the values of both the turns ratio of the auxiliary winding N_a over the secondary side winding N_S ($\frac{N_a}{N_s}$) and the resistive voltage divider ratio $\frac{R_{ZCDL}}{R_{ZCDH} + R_{ZCDL}}$ have to be properly designed.

For the turns ratio $\frac{N_a}{N_s}$, the main factors are the maximum output voltage level V_{out_OVP} and the IC maximum operating voltage V_{VCCmax}. This turns ratio $\frac{N_a}{N_s}$ must fulfill the following requirement, while the value should be as high as possible:

$$\frac{N_a}{N_s} \leq \frac{V_{VCCmax}}{V_{out\_OVP}}$$

Equation 40

Once this turns ratio is decided, the voltage divider ratio can be calculated based on:

- The output overvoltage level setting V_{out_OVP}
- The pin leakage current

This IC provides the output overvoltage protection by comparing the voltage at the ZCD pin during the on-time of the switch Q_{LS} with the fixed overvoltage protection threshold V_{ZCDOVP}. Based on this factor, the divider ratio of the ZCD pin resistors is defined by:

$$k_{Rzcd} = \frac{R_{ZCDL}}{R_{ZCDL} + R_{ZCDH}} = \frac{V_{ZCDOVP}}{V_{out\_OVP}} \cdot \frac{N_s}{N_a}$$

Equation 41

If this resistance ratio is met, the resistor value can be further calculated by taking the pin leakage current into account. A minimum current through the voltage divider resistors is necessary for minimizing the error of the measured output voltage, as the voltage divider resistors of the VS pin.

Note: The ZCD pin leakage current given in the datasheet is the clamping current, which is much higher than the leakage current when the voltage at the ZCD pin is lower for ZC detection and output voltage measurement. Considering this leakage current as a reference for design, the factor of the current through the resistive divider over the leakage current does not need to be as high as usual, such as 10 for the VS pin voltage divider, but a factor of 2 or 3 is sufficient.

A capacitor C_{ZCD} may be needed for a ZCD signal with minimized switching noise. But its capacitance must be as low as possible to minimize the time delay of the ZCD signal in comparison with the voltage V_{HB}. The value of the resistive voltage divider should not be too high for the same reason as the low time delay of the ZCD signal, since the power losses in these resistors are usually not of a concern.

For the application with a wide output voltage range and ceramic capacitors used in the resonant tank, the resonant capacitance changes often according to the output voltage. If this dependence is not well compensated by the parameter $t_{TRANSRVS0V\_perc}$ and the switch Q_{LS} on-time is shorter than $\frac{T_{r1}}{2}$ at a lower output voltage, the ZCD signal has a glitch and the ZC detection is disturbed. This kind of disturbance can only be resolved by a proper value for the parameter $t_{TransRVS0V\_perc}$, but not with a larger C_{ZCD}.

4.3.4 HV pin: HV resistor

The HV pin has external resistors to limit power losses inside the IC during the VCC charge-up. The values of the resistor is limited mainly by the charge-up time of the capacitor C_{VCC} as:

$$R_{HV} \leq \frac{V_{in\_min} \cdot t_{VCC\_chargeup}}{C_{VCC} \cdot V_{VCCon}}$$

Equation 42

where, the $t_{VCC\_chargeup}$ is the target time to charge up the VCC capacitor to the IC VCC turn-on threshold V_{VCCon}.

The following are the two options to connect the HV pin resistors for the VCC charge-up:

- Connected to the input capacitor C_{in}, as shown in ***Figure 3***
- Connected to the AC line and neutral of the supply terminals via the two high-voltage diodes, as shown in the datasheet

Both of these options have their own advantages and drawbacks. The first option does not need high-voltage diodes and, therefore, is more cost effective. But de-latch of the system takes longer time than that with the second option, since it is only possible after the capacitor C_{in} is discharged to be below the $V_{VCC\text{-}UVLO}$ level. The real de-latch time depends on the value of C_{in} and the instantaneous input voltage V_{in}. The higher the value of C_{in} and V_{in}, the longer the de-latch time.

4.3.5 FB pin: filter capacitor

The FB pin has an internal pull-up resistor R_{FBpu}. In the application, this pin is connected to the feedback opto-coupler, while a small capacitor C_{FB} helps to filter the high-frequent switching noise for a stable operation. Typically, this capacitor has a value of around 100 pF.

4.3.6 FMIO pin: external thermal resistor

The following are the three functions that are integrated via the MFIO pin:

- UART communication for parametrization
- External temperature sensing with an external NTC resistor
- Failure code output for debugging purpose

For the UART communication, the necessary hardware and software are described in ***Chapter 5.1*** and ***Chapter 5.2***.

The MFIO pin has an internal resistor R_{MFIOpu}. Along with an external NTC resistor, the control IC checks the NTC temperature by measuring the voltage level at the MFIO pin and indirectly the NTC resistance, and compares that with the over-temperature protection (OTP) trigger and release threshold $R_{MFIOOTPtrig}$ and $R_{MFIOOTPrel}$ for the OTP protection.

Note: In the case of open MFIO pin, the pin is pulled up by the internal resistor to the reference voltage V_{REF}, which is well above the default equivalent OTP triggering voltage threshold, and the OTP is disabled.

Additionally, this pin is utilized for the failure code output if a protection is triggered. The details about the failure code is discussed in ***Chapter 3.5***.

4.3.7 LSGD and HSGD: gate resistor and bootstrap circuit

The driver for a half-bridge configuration is integrated inside the IC. For a typical USB-PD application (***Figure 3***) and the other SMPS (***Figure 4***) below several hundred watts, the driver output can be connected to each MOSFET with just a resistor around 10 Ω for thermal consideration (R_{HSGD} and R_{LSGD}), while the resistors around 10 kΩ between the MOSFET gate and source (R_{HSGS} and R_{LSGS}) are needed as usual.

A bootstrap circuit is required for the HS driver. The resistor in the bootstrap circuit (R_{BS}) should not be too small. Otherwise, it may mis-trigger the protection OCP2 due to the resulted high charging current which flows through the shunt resistor. On the contrary, a very high resistor causes a non-effective charge-up of the HS driver capacitor. Normally, a 2 to 5.1 Ω resistance is used, and a capacitor around 100 nF for the HS gate driver (C_{HSVCC}) will satisfy the application.

4.3.8 VCC supply: VCC capacitor

The following are the three possible sources for the VCC supply:

- The start-up cell, mainly for VCC charge-up at the cold start-up and during protection
- The auxiliary winding during operation with a relatively high output voltage
- The resonant capacitor at a low output voltage

The VCC supply during the normal operation, including burst mode operation, should be generated from the auxiliary winding and the resonant capacitor. The start-up cell may be turned on during the burst mode operation to maintain the VCC voltage, in case that the VCC capacitor voltage drops below the level $V_{VCCslpHVon}$ during a very long burst break. However, this turn-on of the start-up cell during the burst mode operation should be avoided to keep the system efficiency high at a light-load condition. For this purpose, a relatively high value of the VCC capacitor helps either the capacitor C_{VCC1} connected to the VCC pin or the buffer capacitor C_{VCC3}, as shown in ***Figure 3***.

For the VCC capacitors, the total value is mainly dependent on the VCC charge-up time, the system start-up time requirement and the burst break time. For a long burst break time, the value of this capacitor must be high. Typically, a value between 47 and 100 µF should satisfy most of the application cases.

4.4 Output regulator

HFB supports fast line and load response via feedback signal with a wide bandwidth. This requires a type III (***Figure 17***) or a similar compensator. The characteristic and parameter design of such a compensator is well explained in the literature [3]. For the USB-PD application, the HFB controller reacts on the feedback signal for the voltage regulation in terms of speed or output ripple, while the output voltage offset or accuracy is controlled by the secondary side PD device.

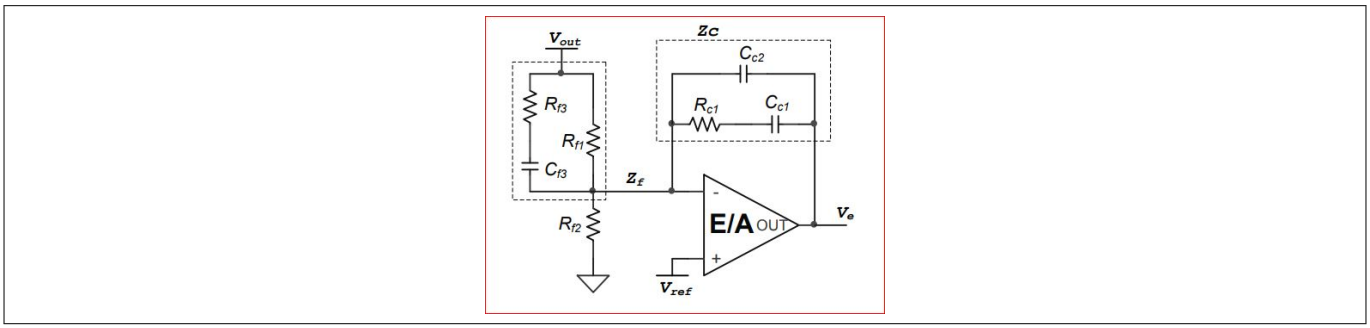


Figure 17 Type III compensator

5 Parameterization

The controller IC offers a flexible parameter configuration for ease of use. For the parameter configuration, a certain assistant hardware and software are needed. These are illustrated as follows:

- Required hardware (***Chapter 5.1***)
- .dp vision tool (***Chapter 5.2***)
- Configurable parameters (***Chapter 5.3***)

5.1 Required hardware

To communicate with the control IC, the dp interface board Gen 2 is required, as shown in ***Figure 18***.

Figure 18 dp interface board

The dp interface board is connected to a computer via the mini-B USB port at the left-side end of the board. Upon a successful communication with the computer, the LED USB is ON. At the right-side end of the interface board, an 8-pin connector is available for the communication with the control IC XDPS2201 (***Figure 19***), where the pin VCC, Comm and GND must be connected to the IC VCC, MFIO and ground pin, respectively.

Figure 19 8-Pin connector to the target control IC

Note: Both the connecting cables to the computer and the application IC must be as short as possible. For example, the USB cable to the computer must not be longer than 1 m to avoid the voltage drop along that cable, which is critical for burning the parameter into the control IC XDPS2201.

The interface board requires the FW version 2.5 (dpIfGen2_V2.5.0_2017_6_27) or later for the communication with the control IC XDPS2201. This can be verified in the .dp vision tool under **Tools\DpifGen2 firmware update**.

5.2 .dp vision tool

This chapter provides information about the .dp vision tool, the procedure for test and burn configuration set, and the .csv file.

5.2.1 .dp vision GUI

Besides the dp interface board, the .dp vision tool is required. To support the control IC XDPS2201, the .dp vision version 2.1.0.0 or later is required. The graphical user interface (GUI) of this tool is shown in ***Figure 20***.

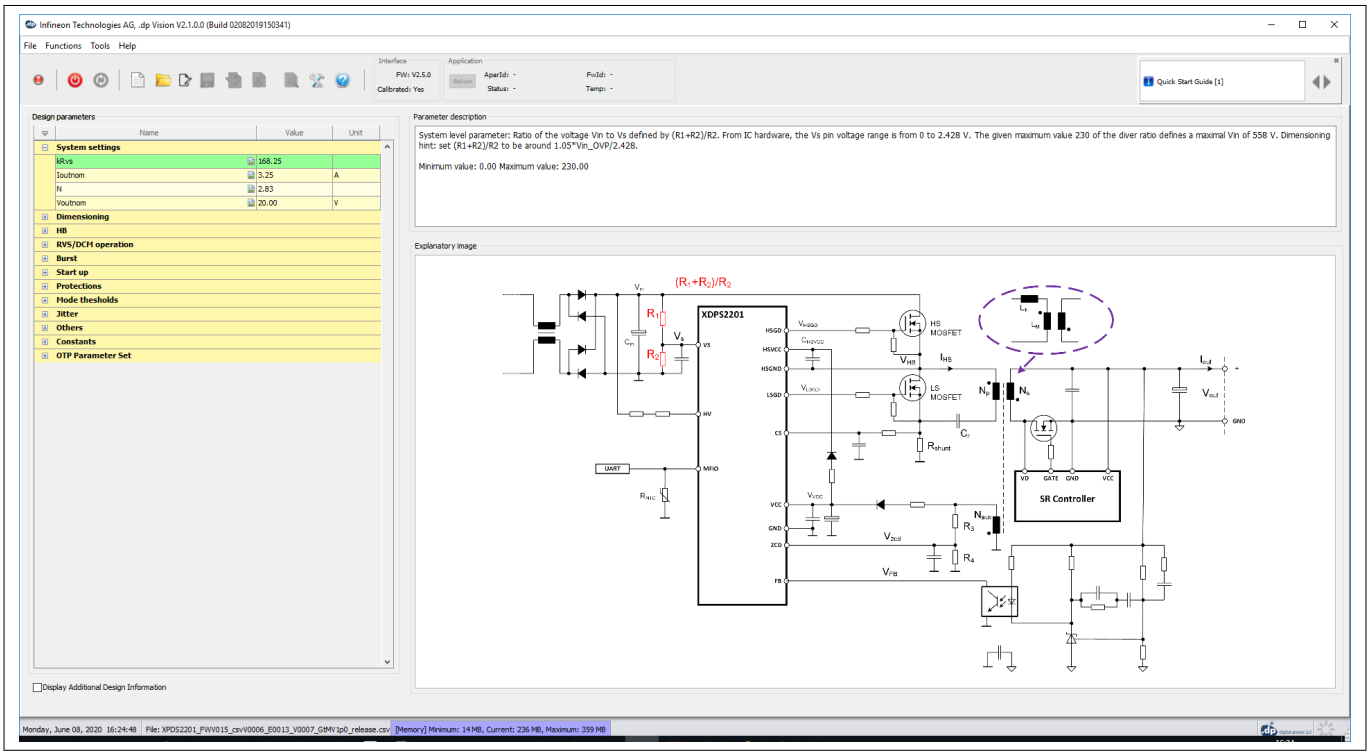


Figure 20 .dp vision GUI

The version number of the .dp vision is shown at the upper-left corner of the GUI. The command icons enable fast access to the functions, which can also be accessed via the command on the top of the main window. For the parameters, three sub-windows are available: design parameter, parameter description and explanatory image. The use of these windows is self-explained, while the user manual about the .dp vision is available under the **Help** menu. Once a .csv file is successfully loaded, the loaded .csv file name is shown at the bottom-left corner of the GUI.

*Note: If the explanatory images are not included in the installation package, the zip file containing all of the images must be unzipped and saved to the **images** folder under the .dp vision, as shown in **Figure 21**. The **Infineon Technologies AG** folder can be found under the **user folder** window.*

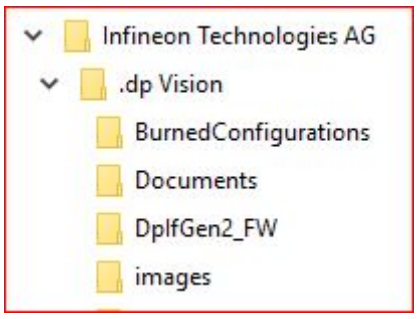


Figure 21 Images folder

There is a check-box "**Display Additional Design Information**" at the bottom-left corner of the .dp vision GUI. Once checked, some of the derived parameters are shown that have important information for the system setup, such as the shunt resistor R_{shunt} in the "System settings" group.

5.2.2 Parameter value change

In the .dp vision GUI, the value of all input parameters can be changed. While changing the value, it is highly recommended to read the description of that parameter and its limit(s). Once the value change of a parameter is confirmed by pressing the return key, the .dp vision will check the plausibility of the parameter value. If the input value violates any of the limits, the .dp vision turns that value into red, gives a warning sound and then shows the error in the sub-window at the upper-right corner (***Figure 22***). If one parameter value is correlated to the other parameter(s), the change of that parameter may cause the other parameter value(s) to be invalid. It is mandatory to correct the invalid value before saving the configuration, test or burning the configuration set.

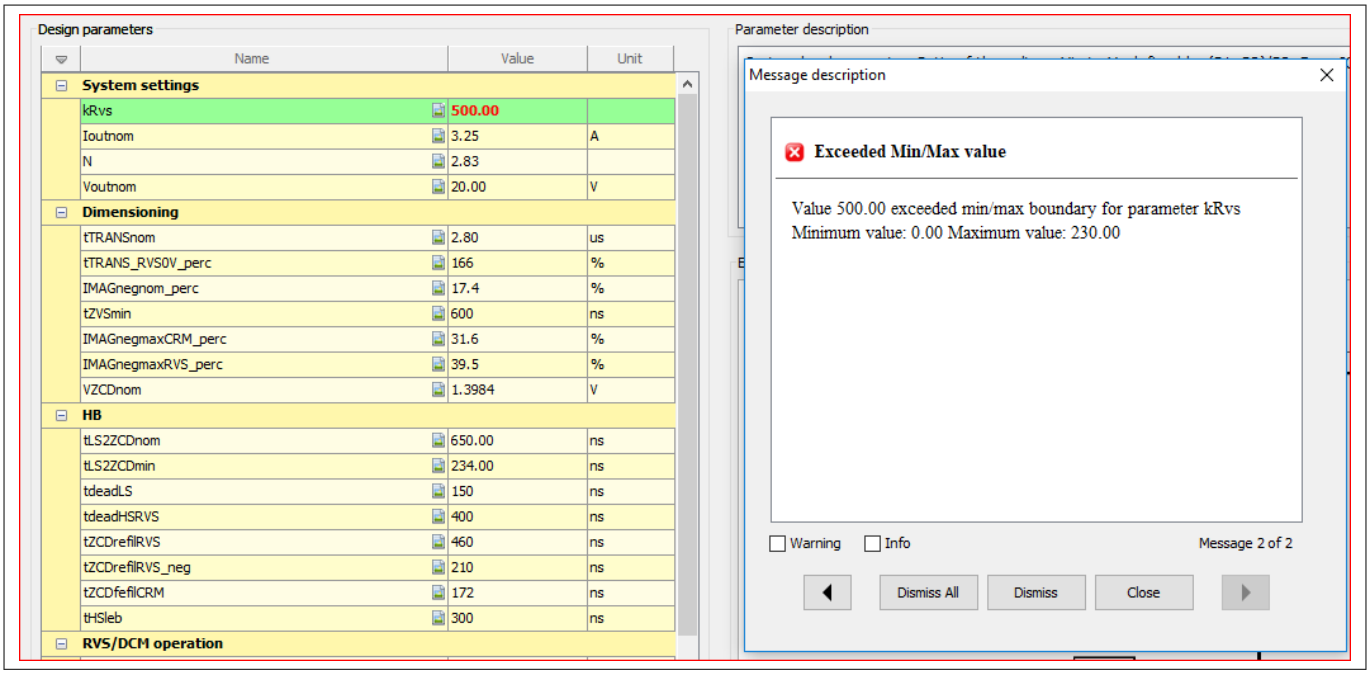


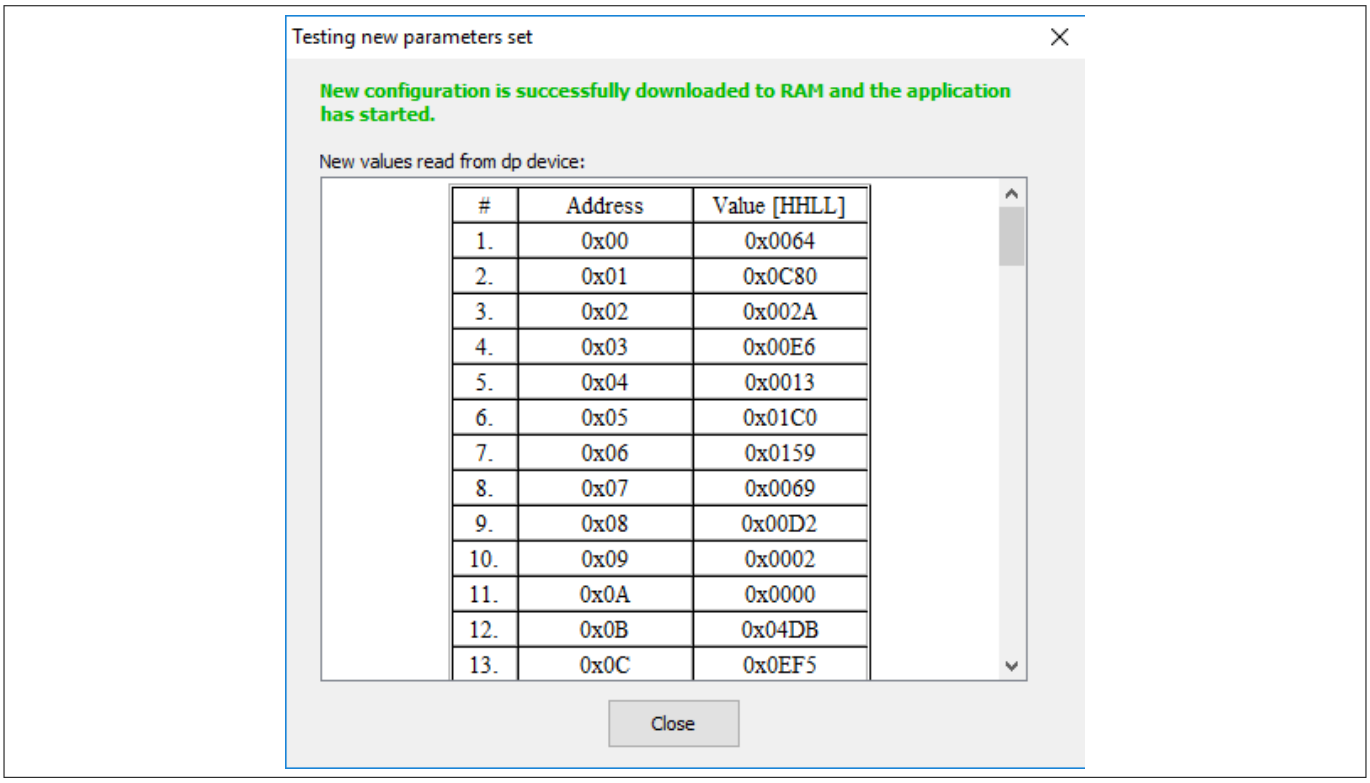
Figure 22 Error message from .dp vision

5.2.3 Procedure for test configuration set

Depending on the application, the default parameter value set may need some fine adjustment for a better performance. For a trial with the new parameter set, the .dp vision enables test for the parameter set without burning it to the memory cells of the control IC. This is the **Test Configuration Set** function, and the following sequential steps need to be performed:

1. Load the .csv file
2. Set the value properly
3. Save the .csv file
4. Power on device
5. Turn on the AC source
6. **Test Configuration Set**

After these steps, the following message window (***Figure 23***) displays, while the application is started automatically with the newly configured parameter set.



#	Address	Value [HHLL]
1.	0x00	0x0064
2.	0x01	0x0C80
3.	0x02	0x002A
4.	0x03	0x00E6
5.	0x04	0x0013
6.	0x05	0x01C0
7.	0x06	0x0159
8.	0x07	0x0069
9.	0x08	0x00D2
10.	0x09	0x0002
11.	0x0A	0x0000
12.	0x0B	0x04DB
13.	0x0C	0x0EF5

Figure 23 Message at Test Configuration Set

*Note: If Step 6 **"Test Configuration Set"** is executed before Step 5 "Turn on the AC source", then the latest stored parameter set is used instead of the newly configured parameter set.*

The message in ***Figure 23*** shows only the affected FW application parameter (APARAM): address and the corresponding values, but not the original input parameters. In fact, the input parameter values have to be calculated, converted into the defined format and arranged in the correct order by the .dp vision tool based on the loaded .csv file, respectively. Only in this way, the control IC can receive the APARAM values and run accordingly.

5.2.4 Procedure for burn configuration set

After the parameter set is tested and fixed, the parameter can be burnt into the memory cells to avoid repeating the above-mentioned steps with **Test Configuration Set**. Click the **Burn Configuration Set** icon, the following message window displays:

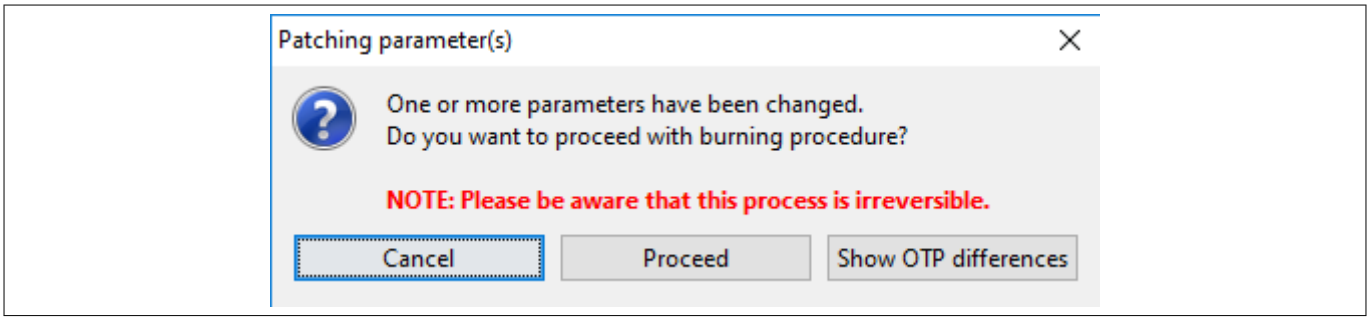
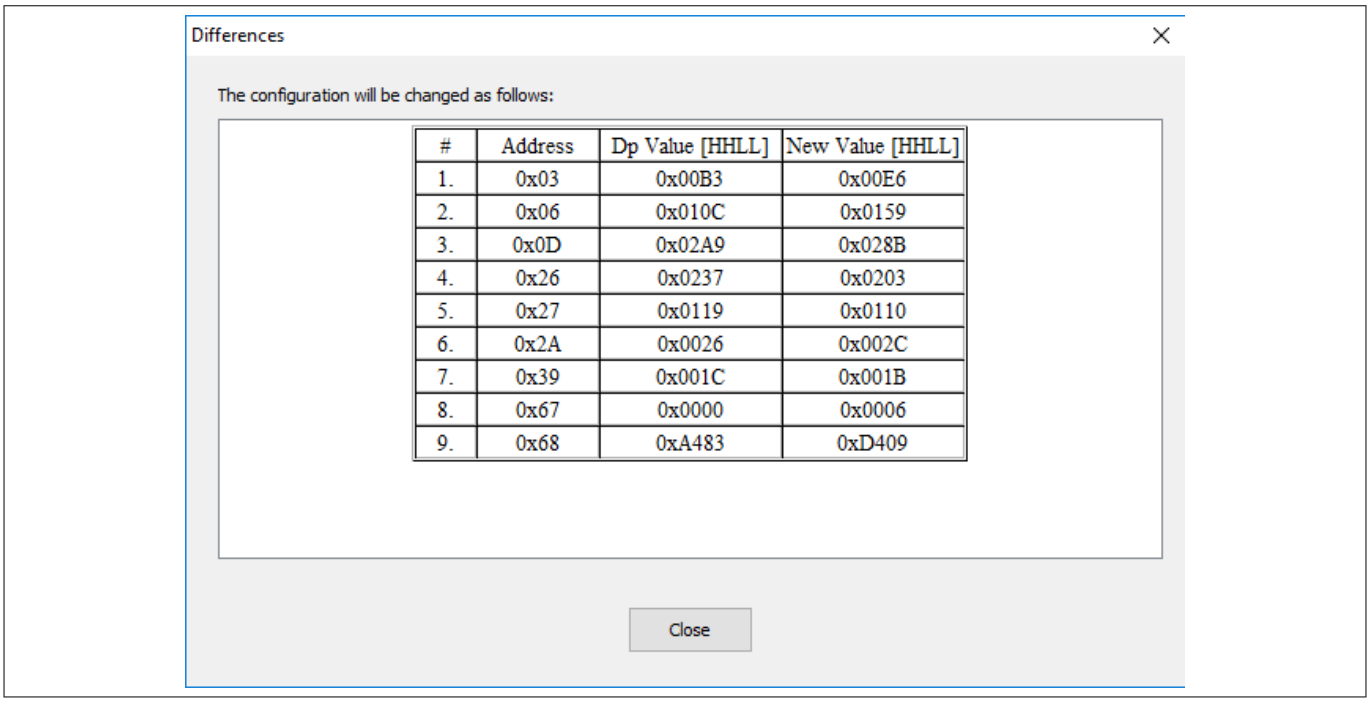


Figure 24 Message at Burn Configuration Set

As the title of the message window "Patching parameter(s)" indicates, the **Burn Configuration Set** changes only those APARAM values which are different from the ones stored in the control IC XDPS2201, and not the entire APARAM set. With the **Show OTP differences** button, the parameters with different values will be shown, as seen in ***Figure 25***, where only the input parameter I_{outnom} was changed.



#	Address	Dp Value [HHLL]	New Value [HHLL]
1.	0x03	0x00B3	0x00E6
2.	0x06	0x010C	0x0159
3.	0x0D	0x02A9	0x028B
4.	0x26	0x0237	0x0203
5.	0x27	0x0119	0x0110
6.	0x2A	0x0026	0x002C
7.	0x39	0x001C	0x001B
8.	0x67	0x0000	0x0006
9.	0x68	0xA483	0xD409

Figure 25 Message at Show OTP differences

As shown in the figure, the value of several parameters are different even though only the input parameter I_{outnom} is changed. In this example, the first seven changes are dependent on that input parameter. The item no. 8 at address 0x67 is related to the .csv file version number. The IC from factory is burnt with a certain firmware .ahex file containing a default .csv file version number, here 0x0000, but the currently loaded .csv file has another version number, here 0x0006. This .csv file version number is only for the tracking purpose, and has no impact on the system performance. The item no. 9 at the address 0x68 is the CRC checksum of the parameter values and varies according to the value setting. In case the default parameter set satisfies the application, the **Burn Configuration Set** is not necessary. But if it is already performed, then this window will display only the change of the item at addresses 0x67 and 0x68, due to different .csv file version numbers and the CRC checksum result.

For burning a configuration set, the procedure is as follows:

1. Load the .csv file
2. Set the appropriate parameter value
3. Save the .csv file
4. ***Burn Configuration Set***

After Step 4, the IC is ready for application with the newly burnt parameter set.

5.2.5 .csv file

For parameter value adjustment, a .csv file is required. The .csv file is just an intermediate means to get the correct APARAM for the IC operation, which takes customer **Design parameters**, calculates some important derived parameters for customer information and the APARAMs for IC. Therefore, the .csv file is necessary if the application parameter value is different from the default setting.

Additionally, the .csv file includes the information about the FW version number. The FW version number stored in the IC and the loaded .csv file must match. If not, then it is impossible to change the IC APARAM with that .csv file.

Normally, the APARAM burning can be performed several times with the same IC, since only the parameter with a new value will be burnt to the IC each time. Depending on the number of parameters with a changed value, the times of parameter re-burning varies. In general, the memory size is big enough for the design phase. In case the left free memory cells are not big enough, then a new IC is required for a new parametrization.

Note: Any change of parameter value must only be done within the .dp vision tool based on a signed .csv file. A .csv file modified using any editor, without singed by Infineon, will not be supported by the .dp vision tool. In case that one tries to load an unsigned .csv file, the .dp vision displays the following error message.

Figure 26 Message at Show OTP difference

In addition, for all of the projects under development, the latest FW and .csv file should be used, which contains the latest improvement for the best performance.

5.3 Configurable parameters

For production release of the configurable parameter set, the following rules apply:

- Parameter set must be fully evaluated and only released for production by the end user of the control IC – our customer
- Make sure that the parameter set fulfills the application's needs and requirements, including the system technical performance and safety norms
- Ensure the whole hardware setup – including programming/OTP burning hardware – is fully tested and working properly
- Each parameter set is only valid for that dedicated and evaluated SMPS hardware, including the PCB layout and all the used electronic components, such as MOSFETs, transformer etc.

This chapter describes the parameter set in the firmware version 1.2.0, which are grouped as follows in the .dp vision GUI:

- System setting (***Chapter 5.3.1***)
- Dimensioning (***Chapter 5.3.2***)
- HB (***Chapter 5.3.3***)
- RVS/DCM operation (***Chapter 5.3.4***)
- Burst (***Chapter 5.3.5***)
- Start-up (***Chapter 5.3.6***)
- Protections (***Chapter 5.3.7***)

- Mode threshold (***Chapter 5.3.8***)
- Jitter (***Chapter 5.3.9***)
- Others (***Chapter 5.3.10***)

5.3.1 System setting

The input parameters in this group are: k_{Rvs}, I_{outnom}, N and V_{outnom}. The two important derived parameters R_{shunt} and V_{crnom} can be found in this group, once the **Display Additional Design Information** option is checked in the .dp vision GUI.

Input parameter k_{Rvs} (***Figure 27***)

It is the ratio of the voltage V_{in} to V_s defined by $\frac{R_{VSH}+R_{VSL}}{R_{VSL}}$. From the IC hardware, the VS pin operating voltage range is from 0 to V_{VREF}. Typically, the given maximum value of 230 of the diver ratio defines a maximum V_{in} of 558 V. In general, the ratio of $\frac{R_{VSH}+R_{VSL}}{R_{VSL}}$ is set to be around $\frac{1.05 \cdot V_{in\_OVP}}{V_{REF}}$, with V_{in_OVP} as the HFB input overvoltage protection level.

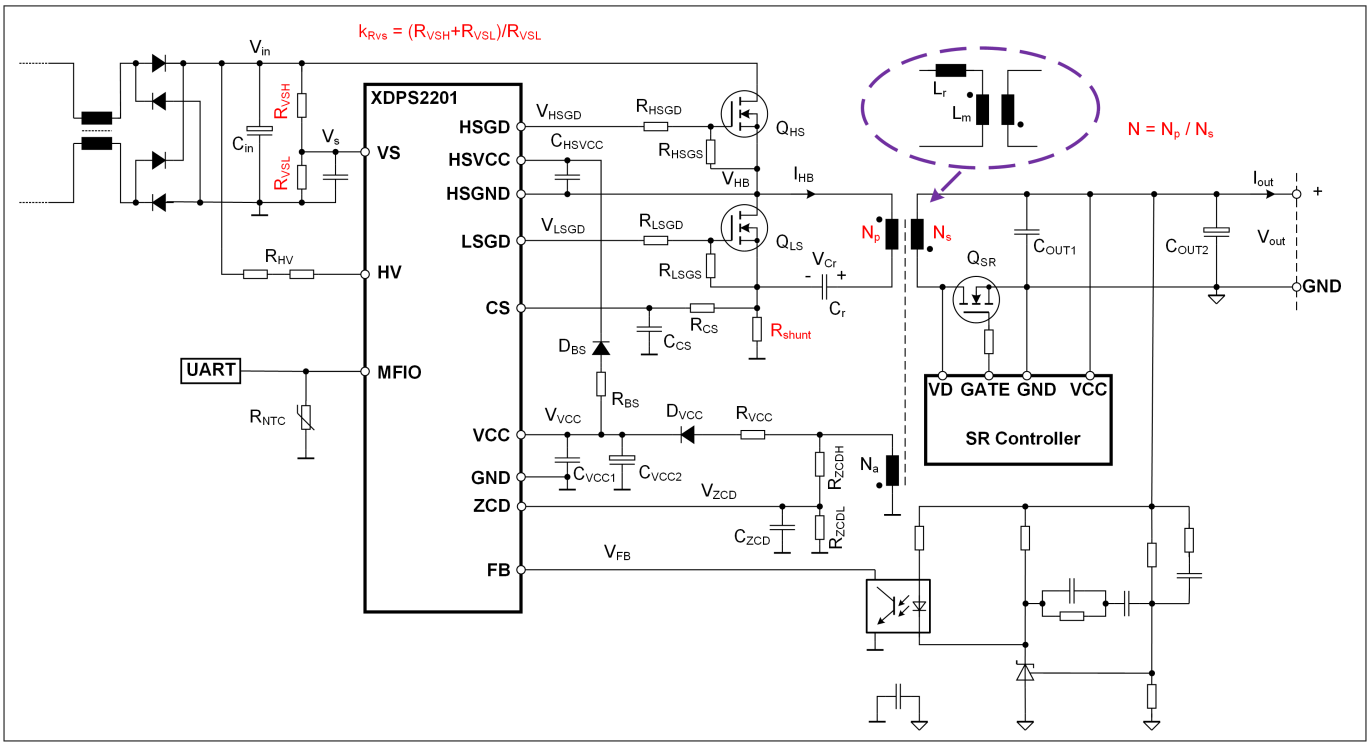


Figure 27 Parameters for the system hardware

Input parameter N (***Figure 27***)

It is the transformer turns ratio of the primary winding N_p over the secondary winding N_s, defined by $\frac{N_p}{N_s}$.

Important derived parameter R_{shunt} (***Figure 27***)

It is the required shunt resistor value for the given nominal output current, calculated based on $\frac{V_{CSOPmax} \cdot I_{SETnom\_perc}}{2 \cdot \frac{I_{outnom}}{N}}$ [2], with $V_{CSOPmax}$ of typically 0.437 V. If the nominal output current or the transformer turns ratio is changed on the board, the shunt resistor value must be changed accordingly to keep the FW and HW matched for a proper system operation.

2 The **%** symbol is reserved in the .dp vision tool, and the parameter name of this **%** symbol is replaced with **_perc** in the Design Guide and the .csv file.

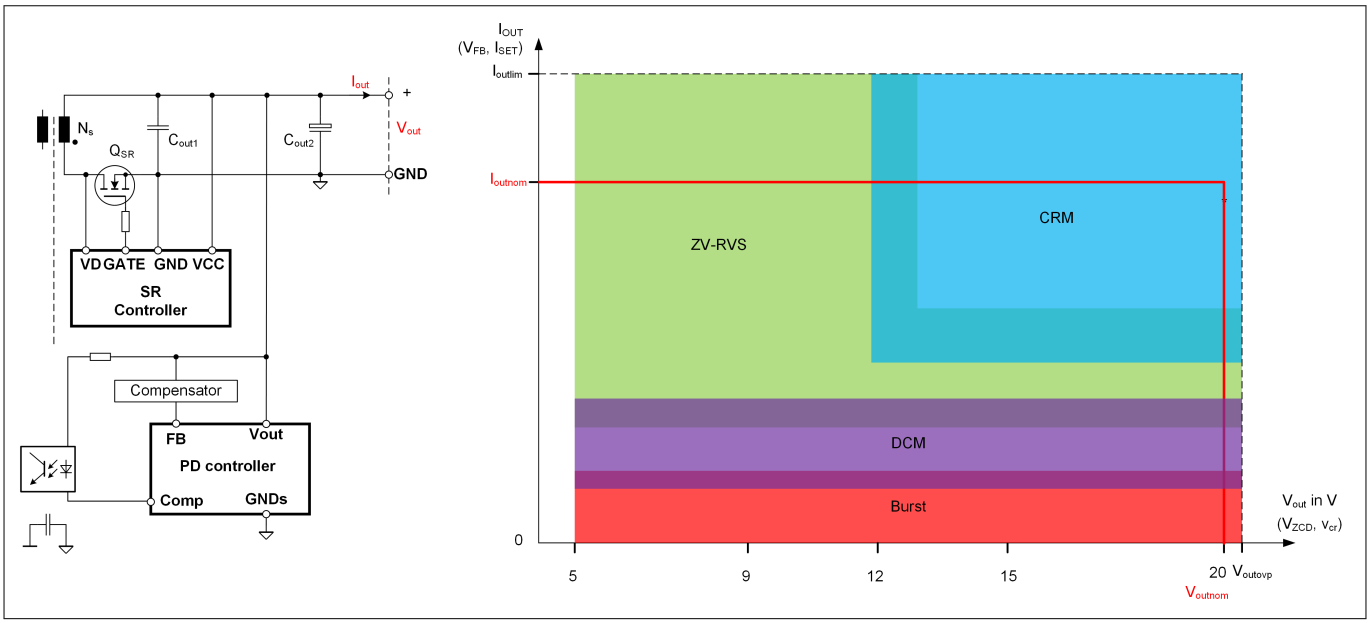


Figure 28 Nominal output current and voltage of USB-PD

Input parameter I_{outnom} (***Figure 28***)

It is the nominal maximum continuous output current at the nominal output power, and the maximum nominal output voltage for the USB-PD application or the rated output voltage for a conventional SMPS. This current is defined as the nominal output current for this controller.

Input parameter V_{outnom} (***Figure 28***)

It is the nominal maximum regulated output voltage, such as 20 V, for the USB-PD application with the output voltage levels of 5 V, 9 V, 12 V, 15 V and 20 V. For a conventional SMPS, it is the rated output voltage. This voltage is defined as the nominal output voltage in this controller.

5.3.2 Dimensioning

The input parameters in this group are: $t_{TRANSnom}$, $t_{TRANSRVS0V\_perc}$, $I_{MAGnegnom\_perc}$, t_{ZVSmin}, $I_{MAGnegmaxCRM\_perc}$, $I_{MAGnegmaxRVS\_perc}$ and V_{ZCDnom}.

Input parameter $t_{TRANSnom}$ (***Figure 29***)

It is the energy transferring time and should be equal to $\frac{T_{r1}}{2}$ (***Figure 5***). The time must be checked on the real board at the nominal output voltage and current, and at the input voltage around $N \cdot V_{out}$.

Input parameter V_{ZCDnom} (***Figure 29***)

It is the measured ZCD pin voltage during the LS switch turn-on at the nominal output voltage V_{outnom}.

Note: The output OVP level sensed at the ZCD pin (V_{zcdovp}) is typically 1.62 V, which is fixed in this controller.

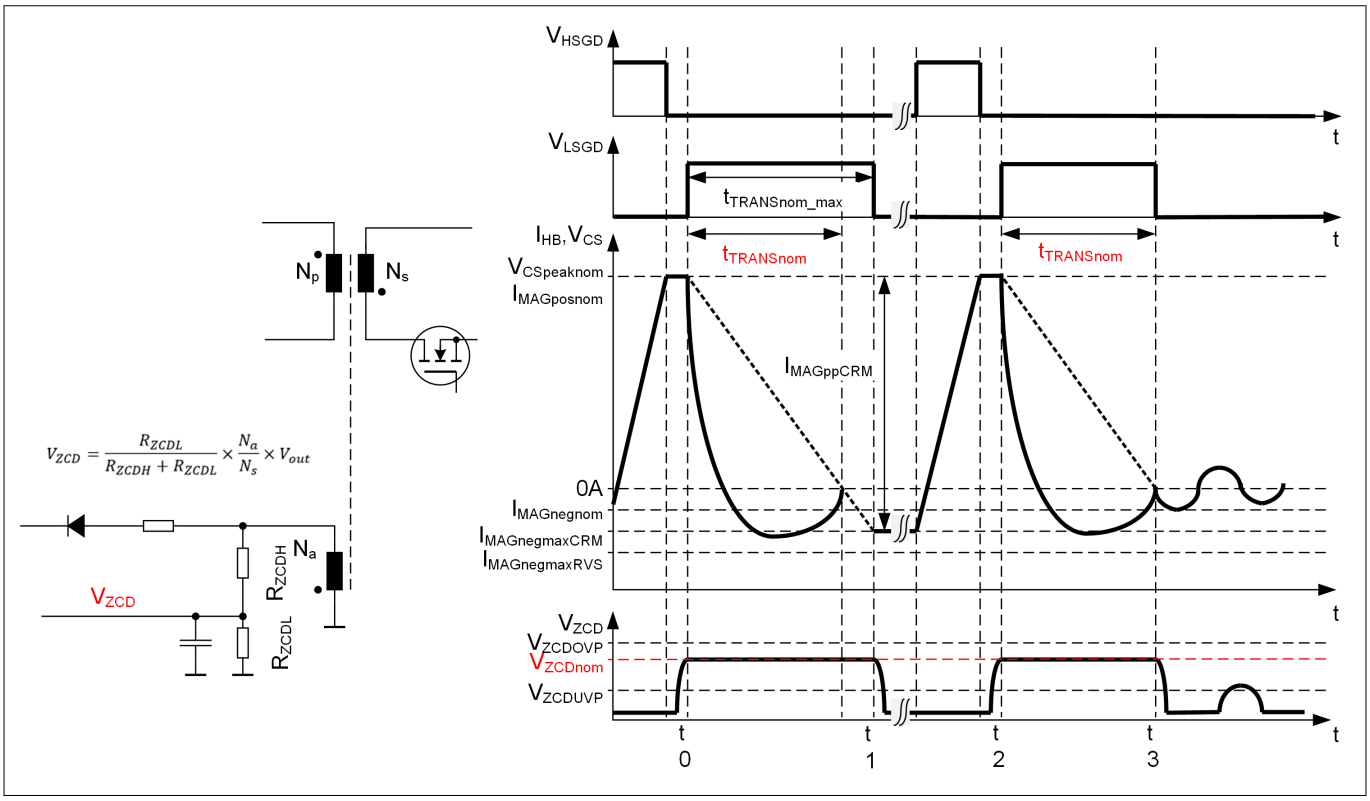


Figure 29 Energy transfer time $t_{TRANSnom}$

Input parameter $t_{TRANSRVS0V\_perc}$ (*Figure 30*)

The real time duration t_{TRANS} changes with the output voltage level V_{out}. This input parameter $t_{TRANSRVS0V\_perc}$ represents the ratio of $\frac{t_{TRANS0V}}{t_{TRANSnom}}$, with $t_{TRANS0V}$ as the energy transferring time at the lowest operating output voltage.

This value is dependent on the type of the capacitor used in the resonant tank. While a film capacitor's value has less or even negligible dependence on the bias voltage, the capacitance of a ceramic capacitor is strongly dependent on the bias voltage, the package and the material. *Figure 30* is only for illustration purpose. The end user has to check the dependence of the used resonant capacitor, and configure the parameter $t_{TRANSRVS0V\_perc}$ accordingly on the board to ensure that the time t_{LSon} at the lowest output voltage is long enough and no glitches are seen at the ZCD pin.

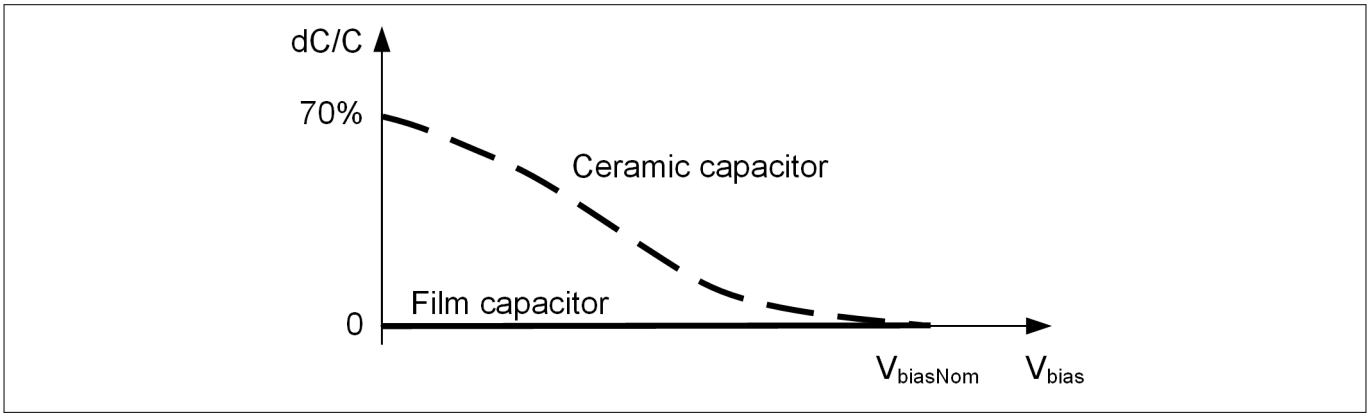


Figure 30 Dependence of capacitance on bias voltage

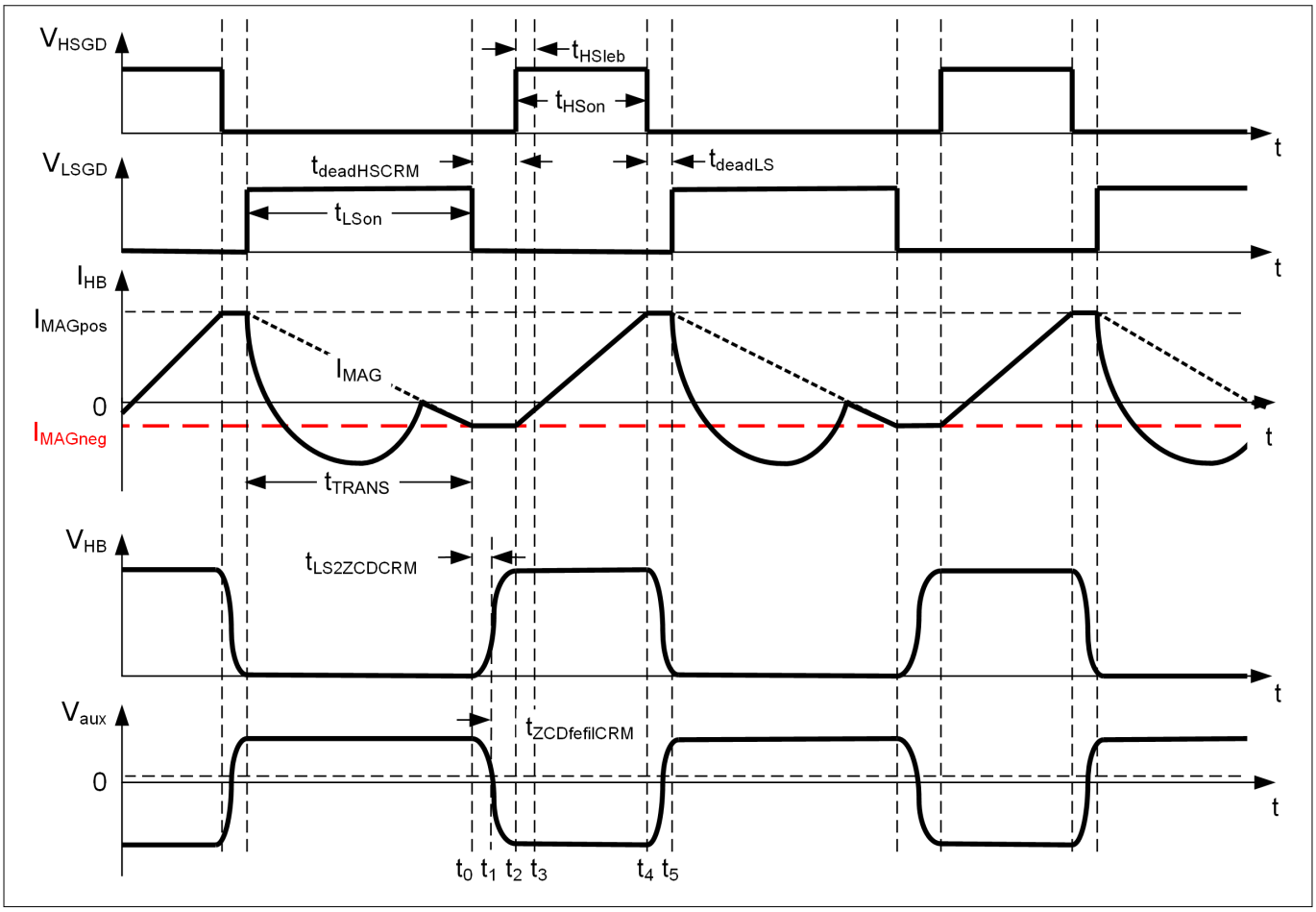


Figure 31 Magnitude of the negative current in the CRM operation

Input parameter $I_{MAGnegnom\_perc}$ (***Figure 31***)

It is the ratio of $\frac{I_{MAGneg}}{2 \cdot \frac{I_{outnom}}{N}}$, where the I_{MAGneg} is the magnitude of the negative magnetizing current for achieving the HS switch ZV turn-on if $V_{in} \leq 2 \cdot V_{Cr}$ and in the CRM operation. This negative current I_{MAGneg} will be compensated with the positive peak current set-point I_{MAGpos} for the output voltage regulation. The amplitude of the negative current I_{MAGneg} used for this parameter calculation should be equal to the negative current amplitude during the free HB oscillation.

Input parameter $I_{MAGnegmaxCRM\_perc}$ (***Figure 31***)

It is the ratio of $\frac{I_{MAGneg}}{2 \cdot \frac{I_{outnom}}{N}}$, where the I_{MAGneg} is the magnitude of the negative magnetizing current for achieving the HS switch ZV turn-on if $V_{in} = V_{in\_OVP}$ and in the CRM operation. This negative current I_{MAGneg} will be compensated with the positive peak current set-point I_{MAGpos} for the output voltage regulation.

Input parameter $I_{MAGnegmaxRVS\_perc}$ (***Figure 32***)

It is the ratio of $\frac{I_{MAGneg}}{2 \cdot \frac{I_{outnom}}{N}}$, where the I_{MAGneg} is the magnitude of the negative magnetizing current for achieving the HS switch ZV turn-on if $V_{in} = V_{in\_OVP}$ and in the ZV-RVS operation. This negative current I_{MAGneg} will be compensated with the positive peak current set-point I_{MAGpos} for the output voltage regulation.

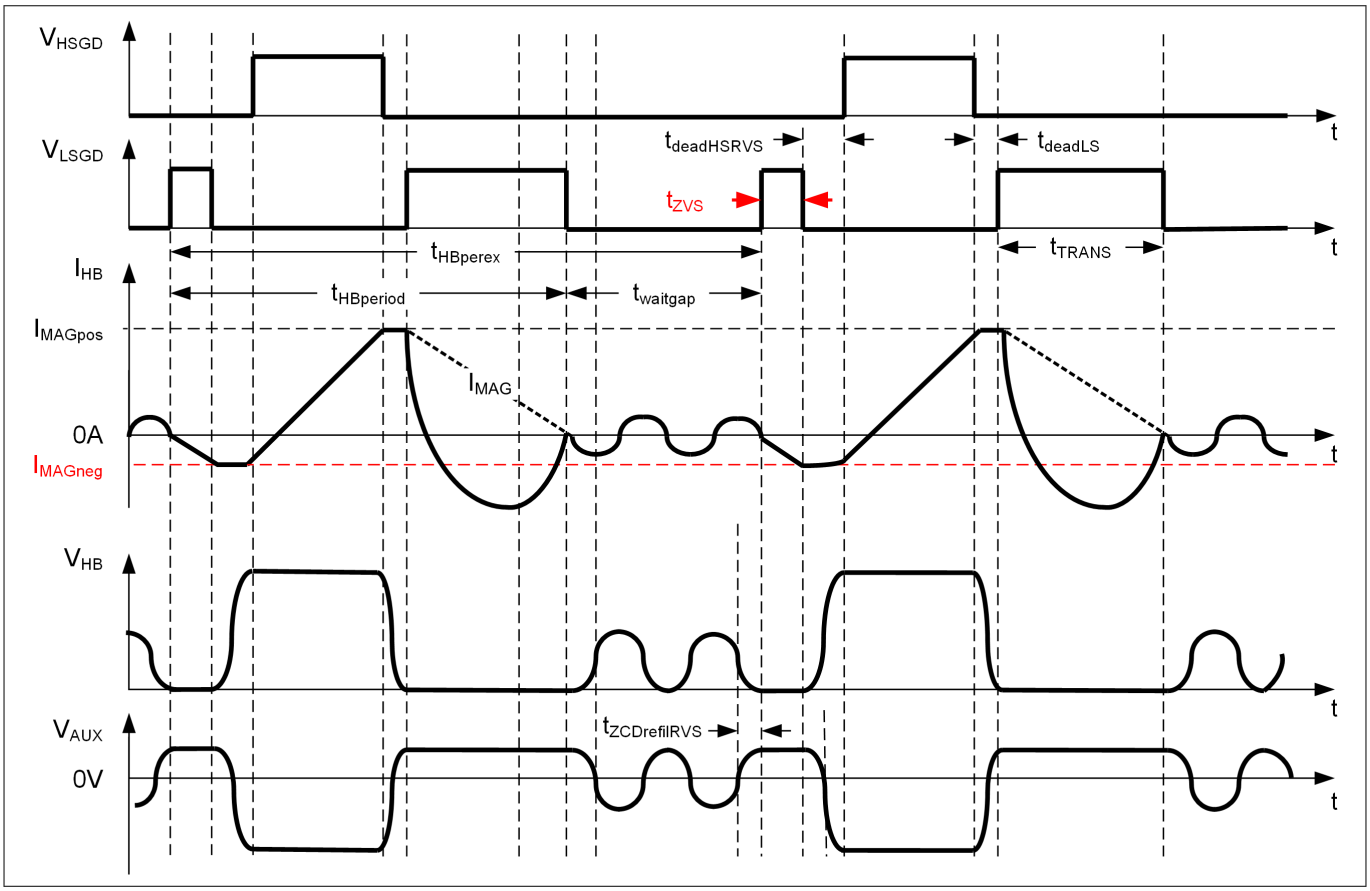


Figure 32 Parameters for the ZV-RVS operation

Input parameter t_{ZVSmin} (*Figure 32*)

It is the minimum ZVS pulse width during the ZV-RVS mode operation.

Note: It is defined by the required negative current for ZV turn-on of the HS switch. Additionally, the time t_{ZVSmin} must be equal to or longer than the minimum on-time of the SR controller for a proper operation, to avoid a simultaneous conduction of the HS MOSFET and the SR MOSFET.

5.3.3 HB

The input parameters in this group are: $t_{LS2ZCDnom}$, $t_{LS2ZCDmin}$, t_{deadLS}, $t_{deadHSRVS}$, $t_{ZCDrefilRVS}$, $t_{ZCDfefilRVS}$, $t_{ZCDfefilCRM}$ and t_{HSleb}.

Input parameter $t_{LS2ZCDnom}$ (*Figure 33*)

It is the target time delay from the LSGD falling edge to the following ZCD falling edge if $V_{in} \leq 2 \cdot N \cdot V_{outnom}$ and in the CRM operation, shown as $t_{LS2ZCDCRM}$ in the figure. This time has an impact on the amplitude of the negative magnetizing current, which has further impact on the ZV turn-on of the HS switch. The shorter the time, the bigger the amplitude of the negative magnetizing current required.

Input parameter $t_{LS2ZCDmin}$ (*Figure 33*)

It is the target time delay from the LSGD falling edge to the following ZCD falling edge if $V_{in} = V_{in\_OVP}$ and in the CRM operation, shown as $t_{LS2ZCDCRM}$ in the figure. This time has an impact on the amplitude of the negative magnetizing current, which has further impact on the ZVS turn-on of the HS switch. The shorter the time, the bigger the amplitude of the negative magnetizing current required.

5 Parameterization

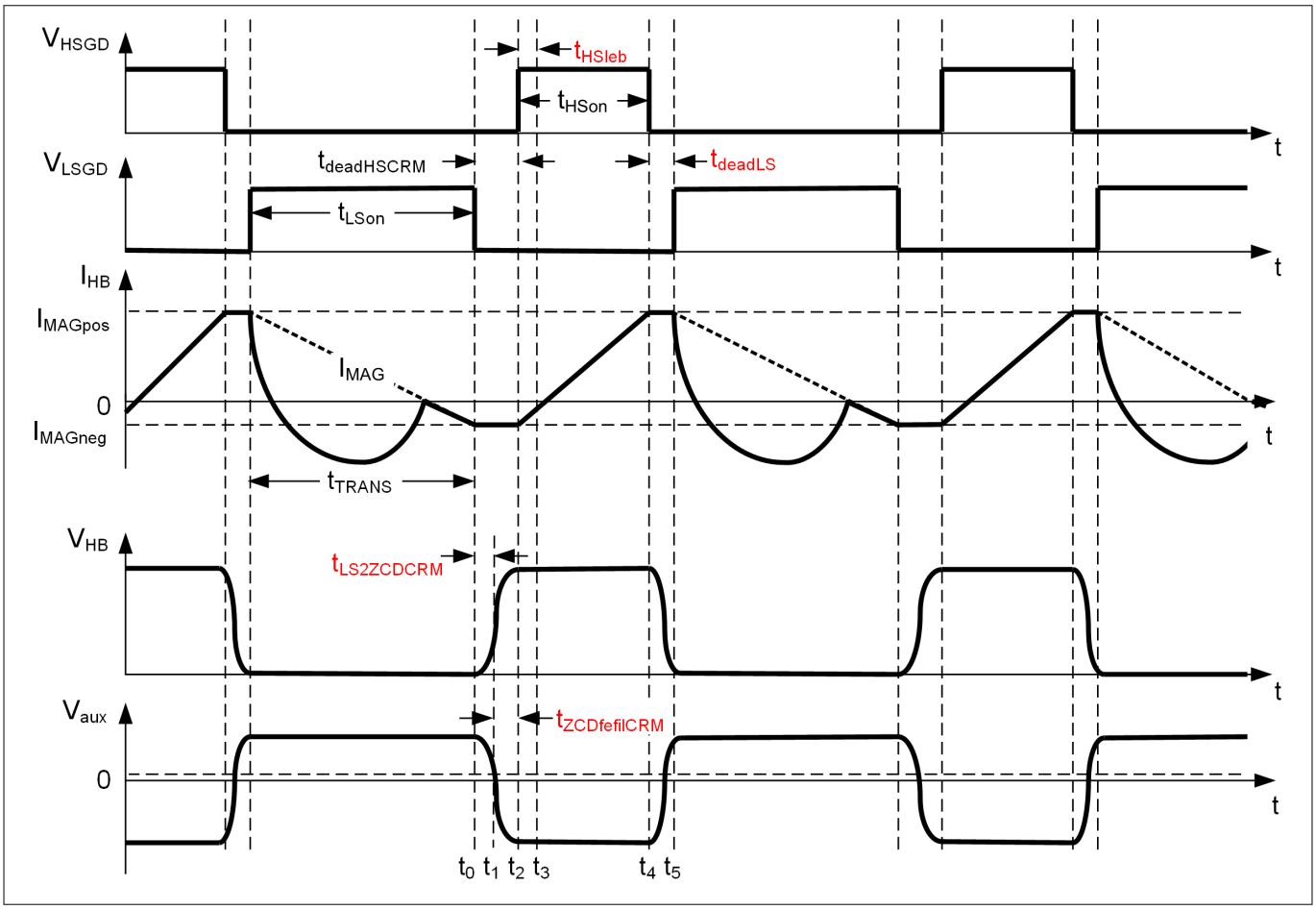


Figure 33 Parameters for the CRM operation

Input parameter t_{deadLS} (*Figure 33*)

It is the dead-time between the HS gate falling edge and the following LS gate rising edge in both the CRM and ZV-RVS mode operation.

Input parameter $t_{ZCDfefilCRM}$ (*Figure 33*)

It is the filter and delay time in the CRM mode for the ZCD signal falling edge. It determines the delay between the ZCD signal falling edge and the following HS gate pulse (rising edge) to ensure V_{HB} reaches V_{in} before the HS switch is turned on. Together with the parameter $t_{LS2ZCDCRM}$, it defines the value for the HS dead-time $t_{HSdeadCRM}$ by $t_{HSdeadCRM} = t_{LS2ZCDCRM} + t_{ZCDfefilCRM}$.

Input parameter t_{HSleb} (*Figure 33*)

It is the HS switch leading edge blanking (LEB) time, which is the minimum on-time of the HS switch during the normal operation. This blanking time is used to avoid early turn-off of the HS switch due to the switching noise at the CS pin. In case that OCP2 is triggered within the time t_{HSleb}, the HS gate is turned off by the OCP2 event.

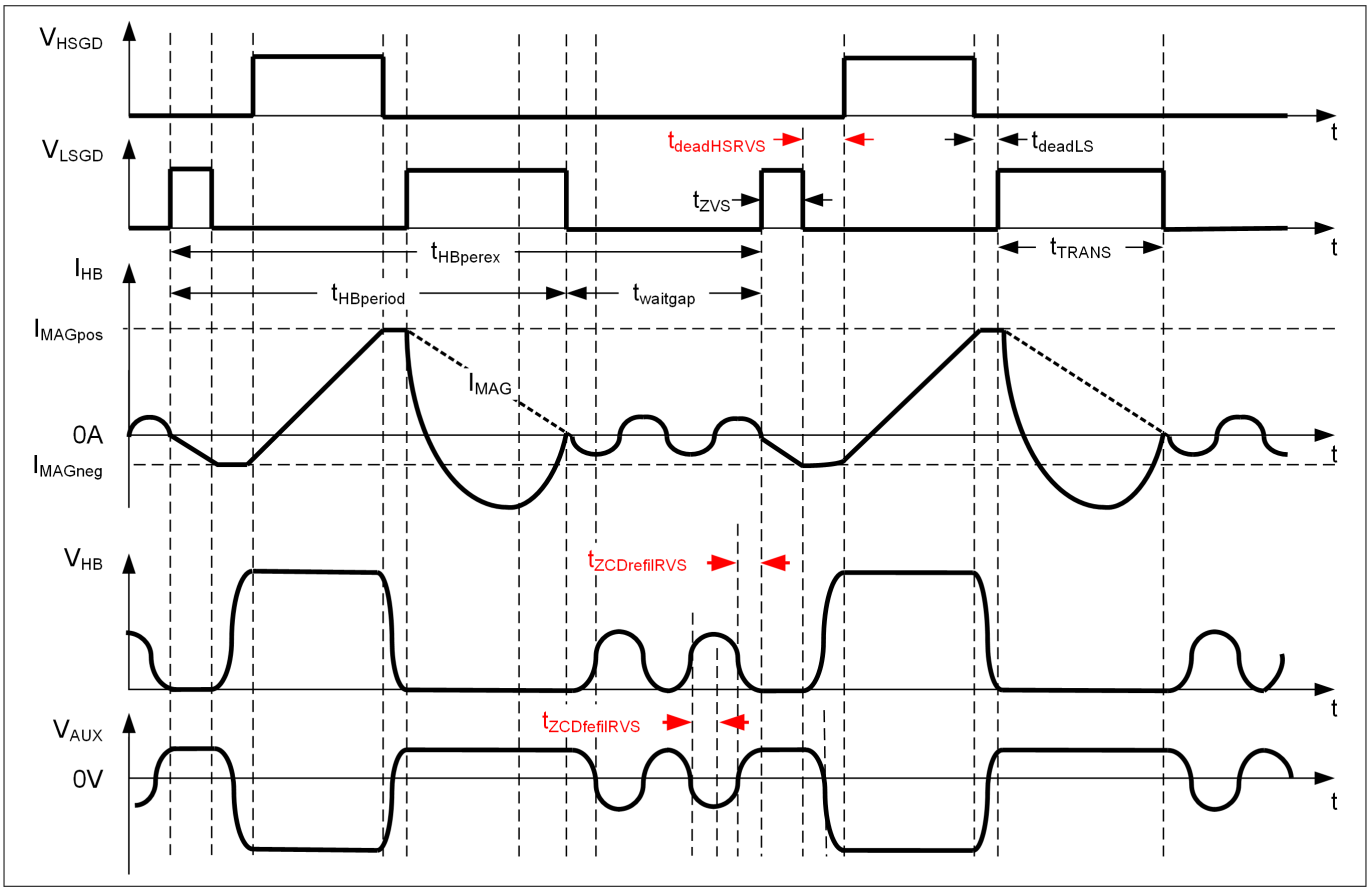


Figure 34 Parameters for the ZV-RVS operation case 1

Input parameter $t_{deadHSRVS}$ (***Figure 34***)

It is the dead-time between the LS ZVS pulse and the next HS gate pulse in the ZV-RVS operation.

Input parameter $t_{ZCDrefilRVS}$ (***Figure 34***)

It is the filter and delay time in the ZV-RVS mode for the ZCD signal rising edge. It determines the delay between the ZCD signal rising edge and the ZVS pulse rising edge to ensure the voltage at the switching node V_{hb} reaches valley to minimize the LS switch turn-on losses.

Input parameter $t_{ZCDfefilRVS}$ (***Figure 34***)

It is the filter and delay time in the ZV-RVS mode for the ZCD signal falling edge. It is lower than $t_{ZCDrefilRVS}$ and ¼ of the measured time duration of the negative voltage across the auxiliary winding V_{aux}, which is a good starting point for the parametrization.

Figure 34 shows the case of switches Q_{HS} and Q_{LS} that have less non-linearity of the capacitance C_{oss} with respect to the drain-source voltage. For modern fast MOSFETs, the C_{oss} has stronger non-linearity of the drain-source voltage. In this case, the voltage at the switching node of HB and the voltage V_{aux} are shown in ***Figure 35***.

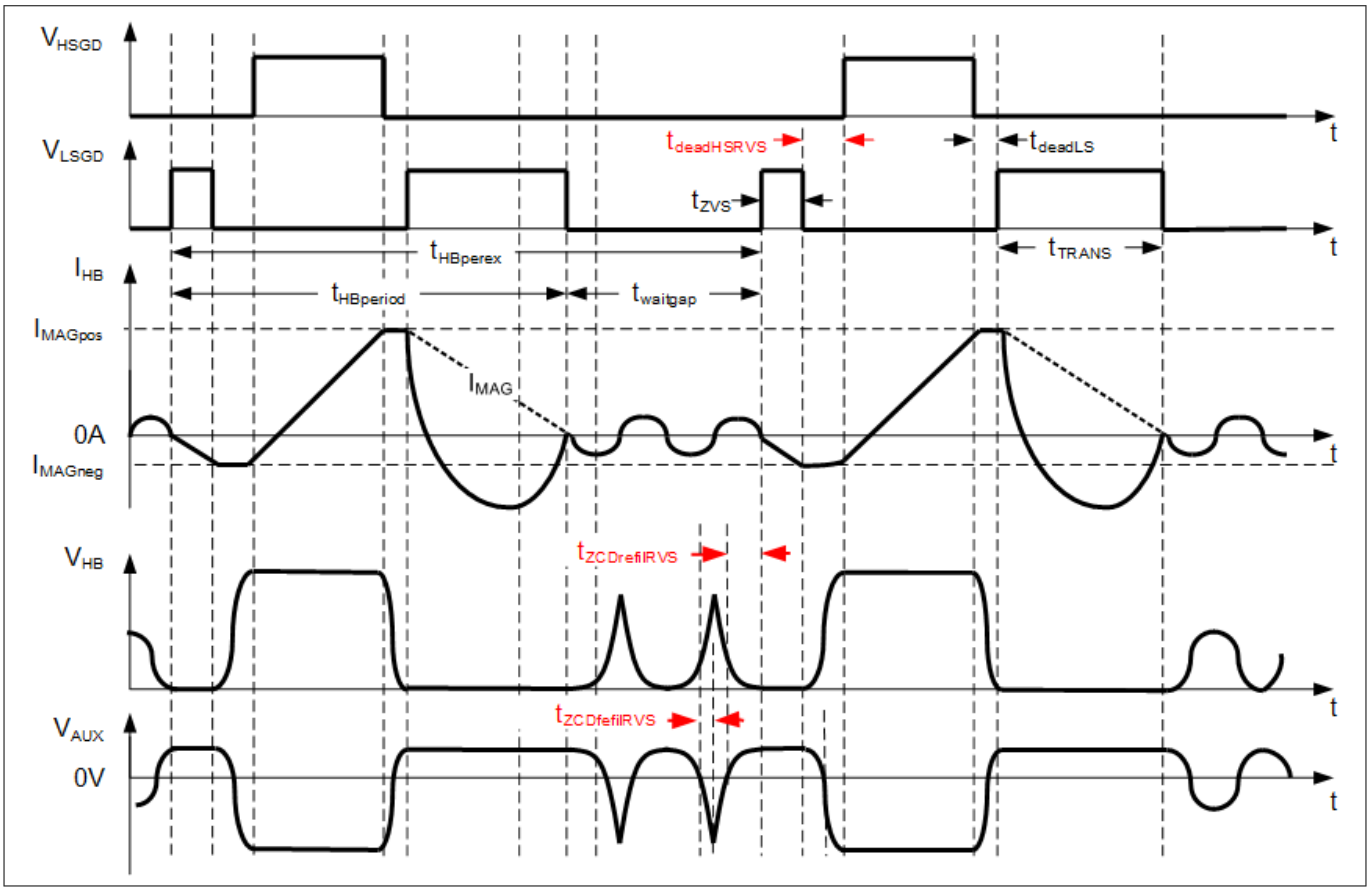


Figure 35 Parameters for the ZV-RVS operation case 2

5.3.4 RVS/DCM operation

The input parameters in this group are: EN_{DCM}, F_{DCMmin} and $N_{RVSvalmax}$.

Input parameter EN_{DCM} (*Figure 36*)

This parameter enables or disables the DCM operation at a low load level before the BM entry. Once DCM is enabled, the system enters the DCM operation when the maximum valley in the ZV-RVS operation $N_{RVSvalmax}$ is reached. In the DCM operation, the rising edge of the ZVS pulse is independent of the resonant valley of the voltage V_{HB}.

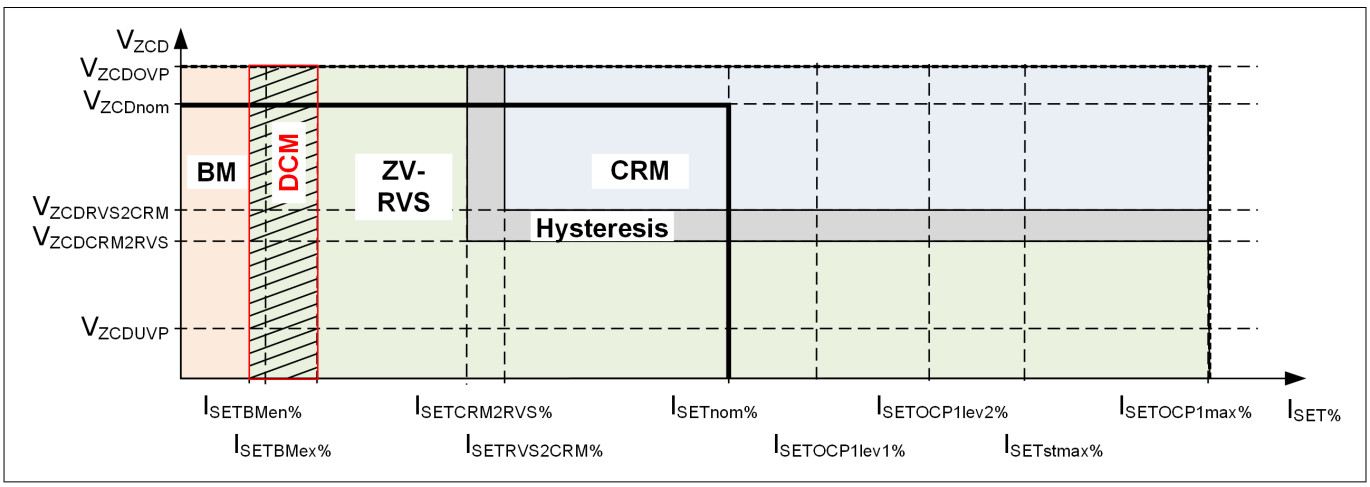


Figure 36 Enable or disable the DCM operation

Input parameter F_{DCMmin}

It determines the minimum switching frequency limit for the DCM operation.

Input parameter $N_{RVSvalmax}$ (*Figure 37*)

It defines the maximum number of valleys for the ZV-RVS operation. In the following figure, the input parameter value is set to 4, as an example.

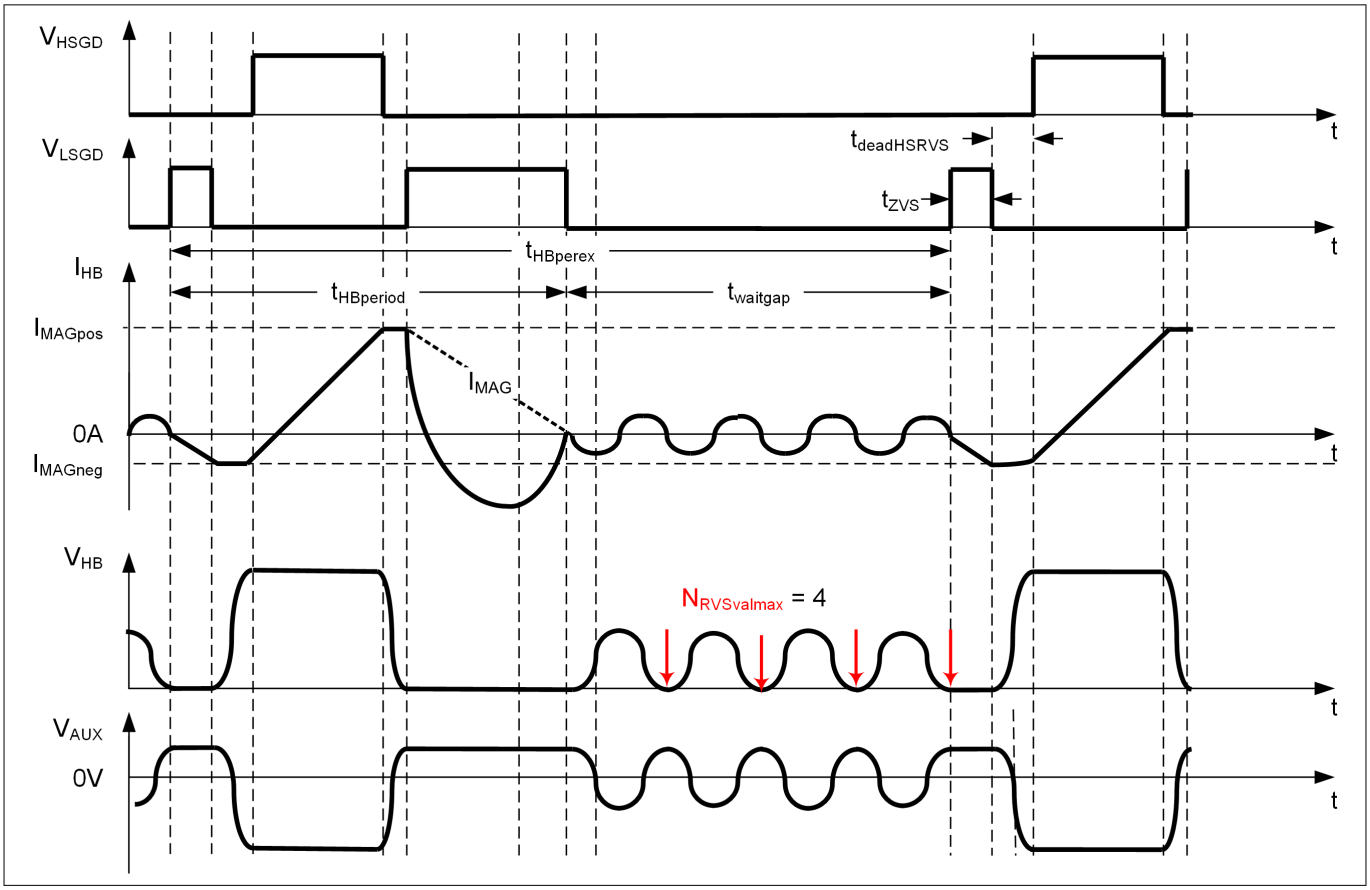


Figure 37 Maximum valley in the ZV-RVS mode

5.3.5 Burst

The input parameters in this group are: $I_{SETBMen\_perc}$, $I_{SETBMex\_perc}$, $t_{BMprepulse}$, $t_{BMslpthrpp}$, $N_{BMexreqthr}$, $N_{BMexreqthr}$, $EN_{BMfastexCRM}$ and $V_{FBBMfastex}$.

Input parameter $I_{SETBMen\_perc}$ (*Figure 38*)

It is the ratio of $\frac{I_{outBMen}}{I_{outnom}}$, where the current $I_{outBMen}$ is the output current for the burst mode entry.

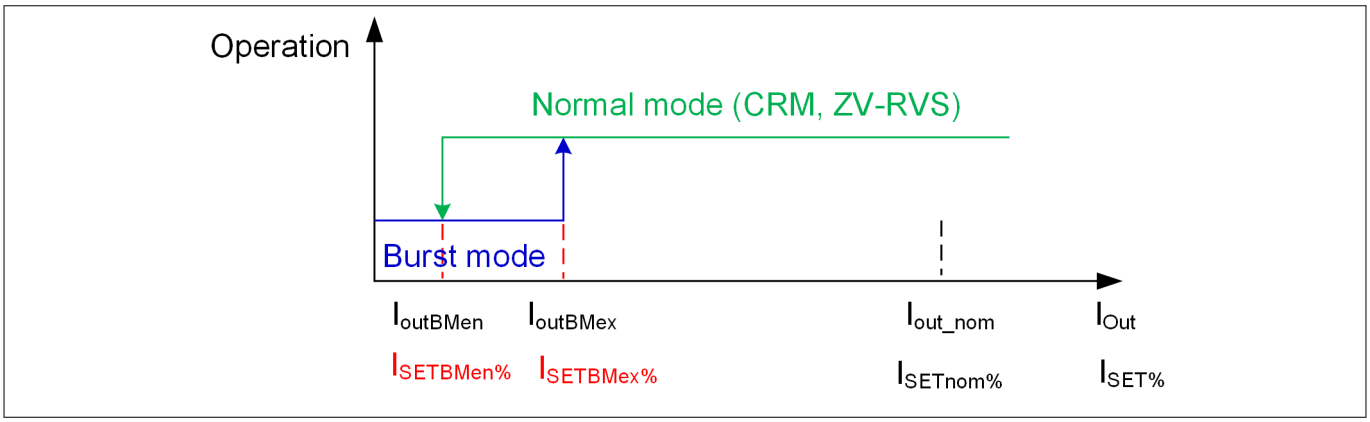


Figure 38 Parameters for the burst entry and exit

Input parameter $I_{SETBMex\_perc}$ (*Figure 38*)

It is the ratio of $\frac{I_{outBMex}}{I_{outnom}}$, where the current $I_{outBMex}$ is the output current for the slow burst mode exit.

Input parameter $t_{BMprepulse}$ (*Figure 39*)

This parameter provides the LS gate pulse width to pre-charge the bootstrap capacitor after a burst pause longer than the value defined by the parameter $t_{BMslpthrpp}$.

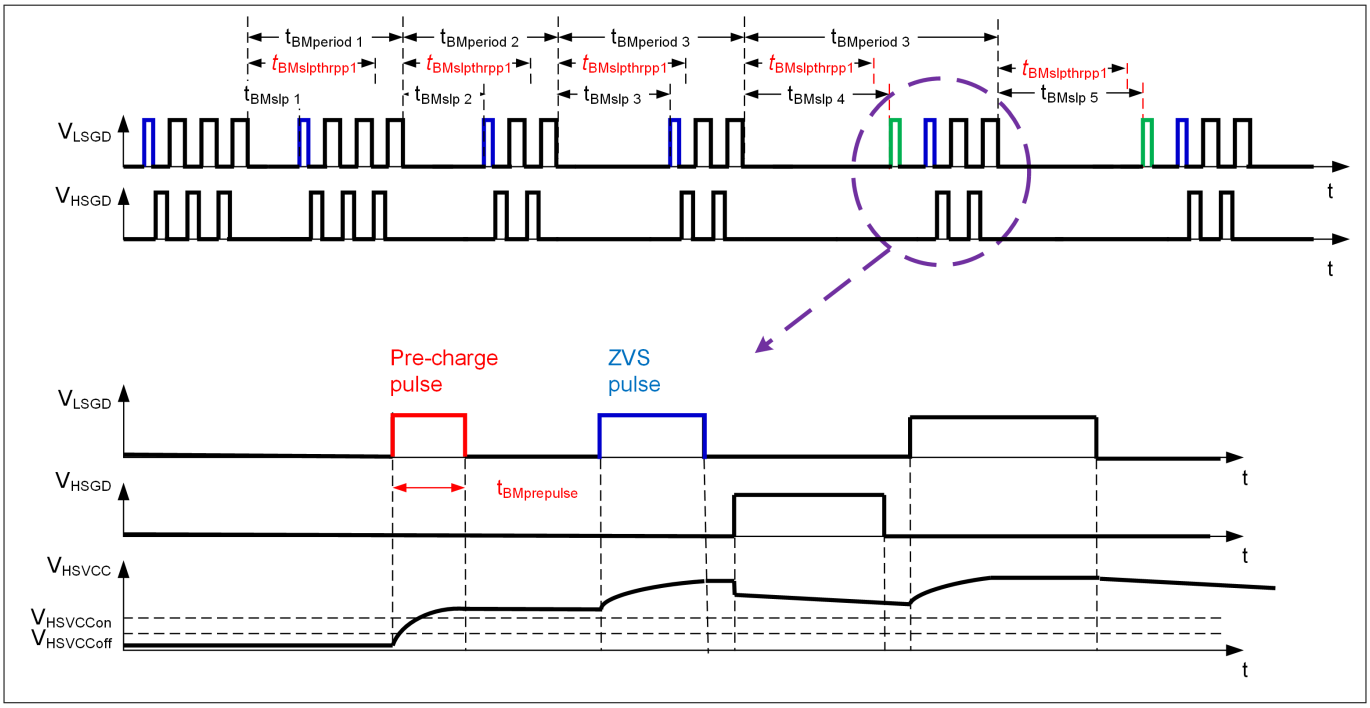


Figure 39 Parameters for the burst operation

Input parameter $t_{BMslpthrpp}$ (*Figure 39*)

It is the time threshold for enabling the bootstrap pre-charge pulse defined by $t_{BMprepulse}$. If the burst pause is longer than this threshold $t_{BMslpthrpp}$, the pre-charge pulse will be applied at the burst starting before the ZVS pulse.

Input parameter $N_{BMexreqthr}$ (*Figure 40*)

It is the number threshold of burst frame for the slow burst mode exit, defined as the number of burst frames with an average output current level higher than the value defined by the parameter $I_{SETBMex\_perc}$.

5 Parameterization

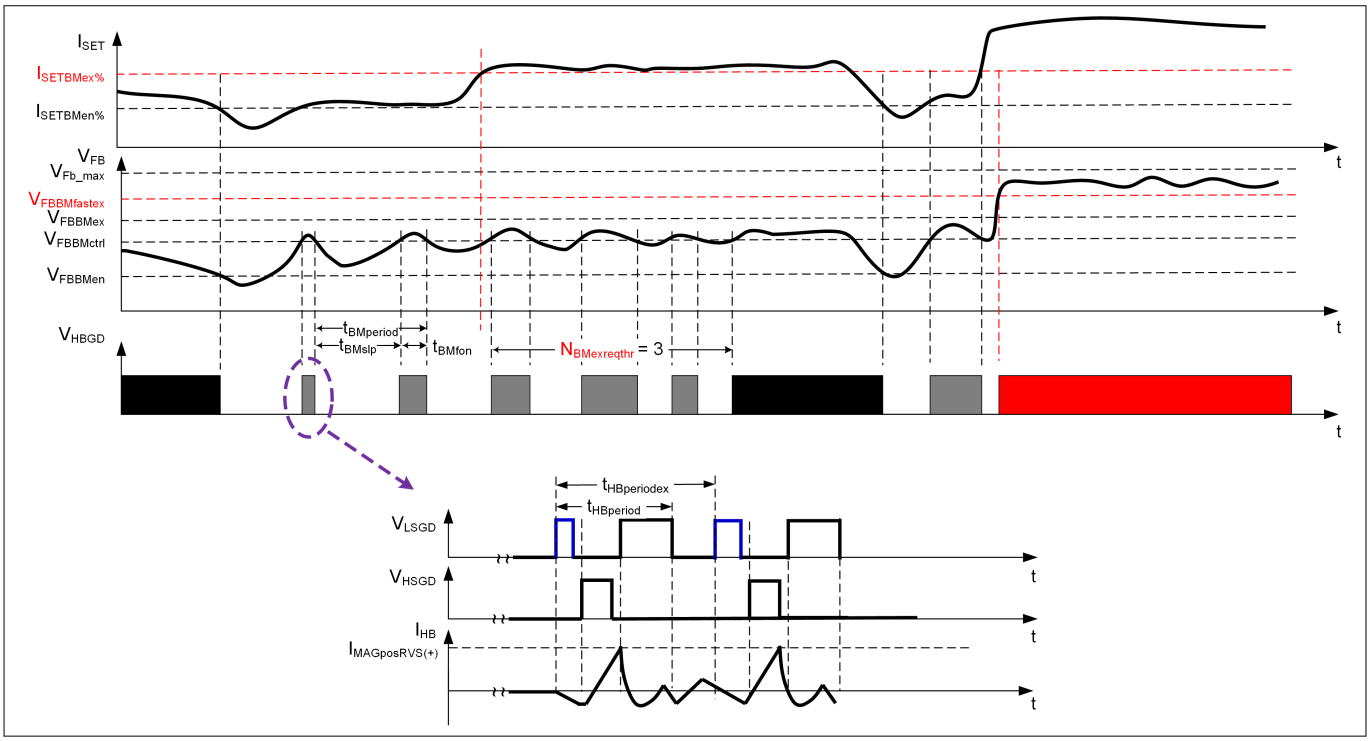


Figure 40 Parameters for the burst exit

Input parameter $EN_{BMfastexCRM}$ (*Figure 40*)

This switch enables or disables the CRM operation directly after the fast burst mode exit. If it is enabled and the CRM operation is allowed by the measured output voltage level through the signal V_{zcd} (*Figure 9*), the system runs in the CRM operation upon burst mode exit. If disabled, the ZV-RVS mode control applies first.

Input parameter $V_{FBBMfastex}$ (*Figure 40*)

It is the voltage threshold for the fast burst mode exit, based on the feedback voltage V_{fb}.

5.3.6 Start-up

The input parameters in this group are: V_{in_BIP}, $t_{ZVSst1st}$, $I_{SETstmax\_perc}$, $t_{startramp}$, $N_{HBcyclemax}$ and $t_{startzcdto}$.

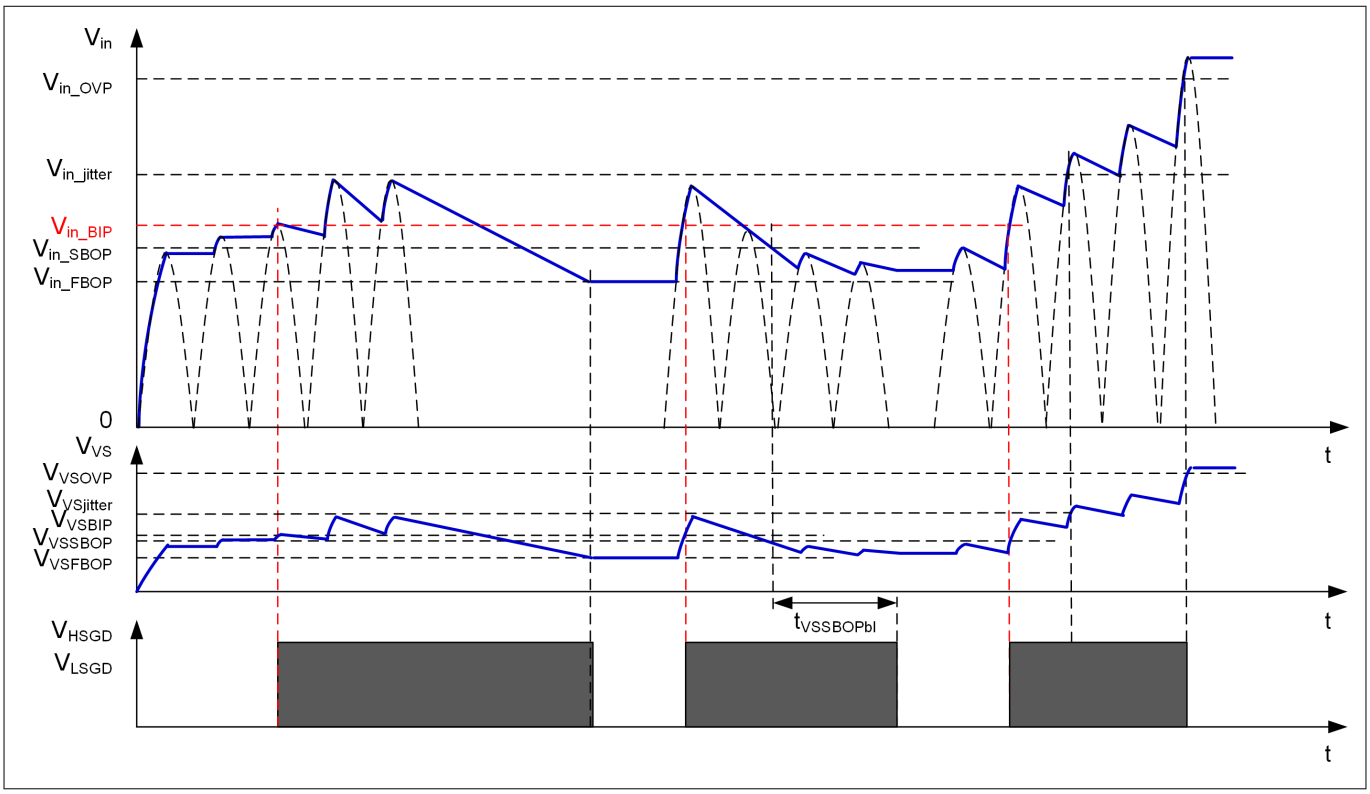


Figure 41 Brown-in

Input parameter V_{in_BIP} (*Figure 41*)

It is the voltage threshold for the brown-in detection based on the measured instantaneous (peak) input voltage V_{in}.

Once the voltage V_{VCC} reaches the IC turn-on threshold V_{VCCon}, the following conditions are verified for the system start-up:

- V_{in} is between V_{in_BIP} and V_{in_OVP}
- Feedback pin is above a fixed level of $V_{FBBMctrl}$
- Resistance of the external NTC over release threshold $R_{MFIOOTPrel}$

Only when all of these conditions are fulfilled, the system starts up.

5 Parameterization

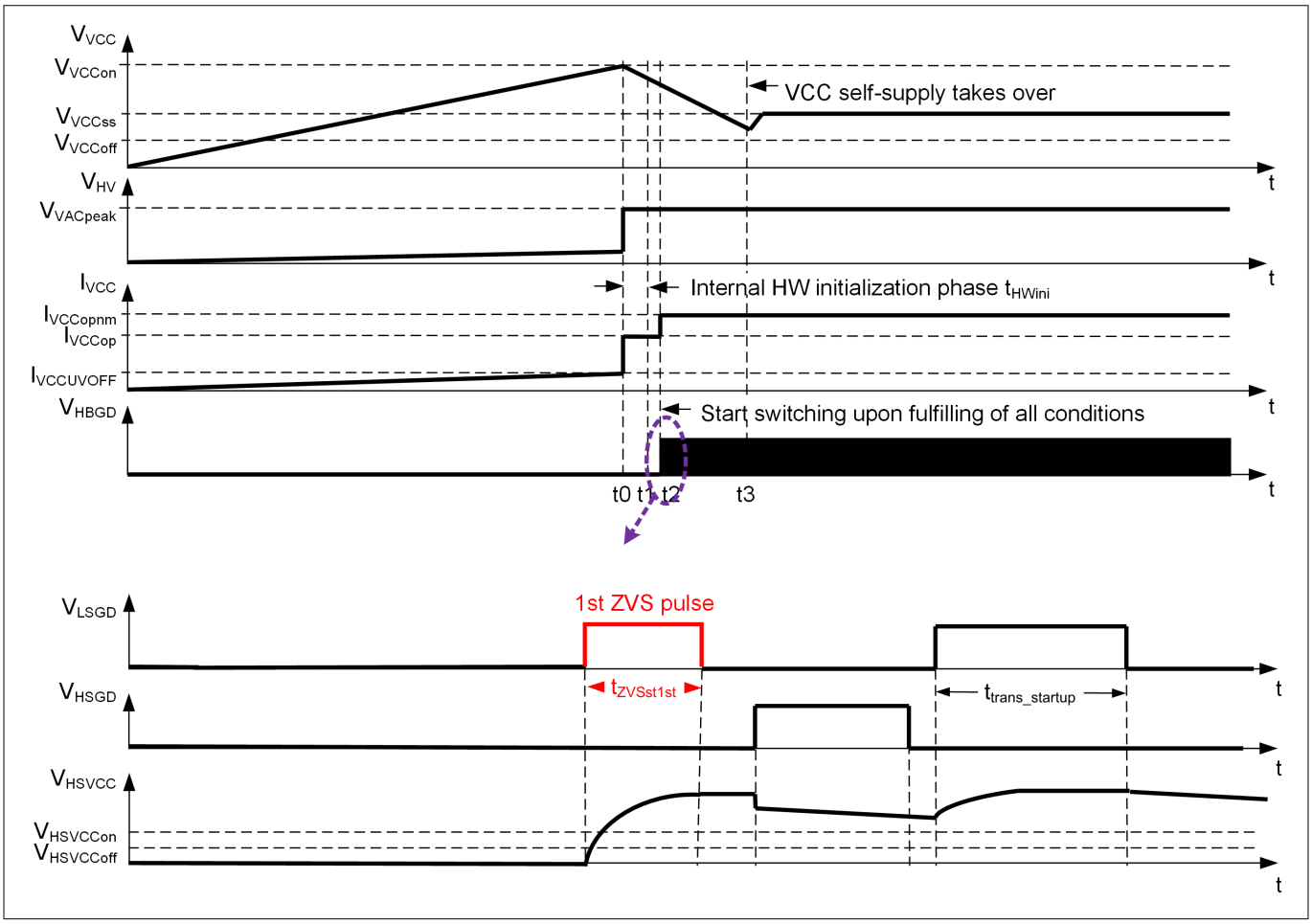


Figure 42 Width of the initial LS gate pulse for HS VCC pre-charge

Input parameter $t_{ZVSst1st}$ (*Figure 42*)

It defines the width of the initial LS gate pulse for pre-charging the HS bootstrap capacitor at the system cold start-up and after the auto restart break.

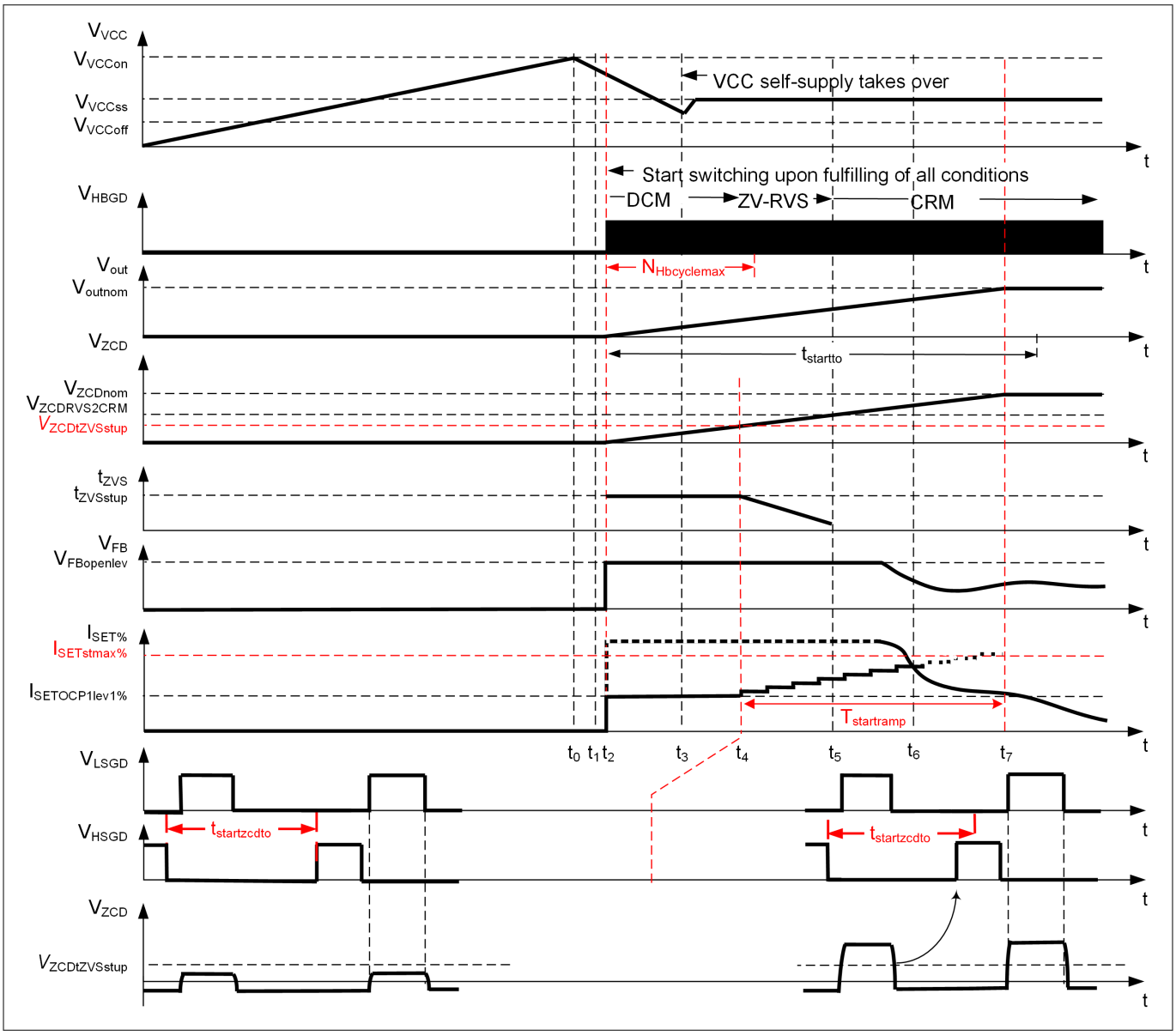


Figure 43 Parameters for start-up

Input parameter $I_{SETstmax\_perc}$ (*Figure 43*)

It is the ratio of $\frac{I_{SETstmax}}{I_{outnom}}$, where the current $I_{SETstmax}$ is the maximum current during the start-up phase. During the system start-up, the output capacitors need to be charged up while the nominal output current may apply. For this reason, the value of this parameter must be higher than 100 percent. The start-up phase ends when the feedback pin voltage begins to control the positive peak current.

Input parameter $t_{startramp}$ (*Figure 43*)

It is the time threshold for output voltage ramping-up to its target value during the start-up phase. The positive voltage at ZCD pin (V_{zcd}) is used for the peak current control during start-up before the feedback signal takes over the peak current setting. It is targeted to have a linear rising signal V_{ZCD} over the start-up time $t_{startramp}$. If the measured V_{ZCD} is lower than the target, the primary current is increased, otherwise, decreased.

Input parameter $N_{HBcyclemax}$ (*Figure 43*)

It is the threshold of the maximum number of the switching cycles allowed without the subsequent ZC detected during ZCD search phase at the system start-up. If the counted switching cycles without ZC detected from

the first switching cycle reaches this threshold during the system start-up, the system stops switching, reports FAIL_start-up_TIMEOUT error, and enters auto restart.

Input parameter $t_{startzcdto}$ (*Figure 43*)

It is the maximum time period for ZCD signal monitoring (ZCD timeout) during the ZCD search phase. At the beginning of the system start-up, there is no ZCD signal available. A new HB cycle is triggered once this time is elapsed after the LS gate signal. Later, a valid ZCD signal is available within this time, and the new HB cycle is triggered by the ZCD signal.

5.3.7 Protections

The input parameters in this group are: V_{in_SBOP}, V_{in_FBOP}, V_{in_OVP}, EV_{ZCDOVP}, $EN_{BMVoutUVP}$, V_{out_UVP}, $t_{startto}$, $I_{SETOCP1lev1\_perc}$, $t_{OCP1lev1bl}$, $I_{SETOCP1lev2\_perc}$, $t_{OCP1lev2bl}$, $I_{SETOCP1max\_perc}$, $t_{OCP1maxbl}$, EV_{CSOCP2}, t_{ARMslp}, $R_{MFIOOTPtrig}$, $R_{MFIOOTPrel}$, $N_{OTPevmax}$ and EV_{WDOG}.

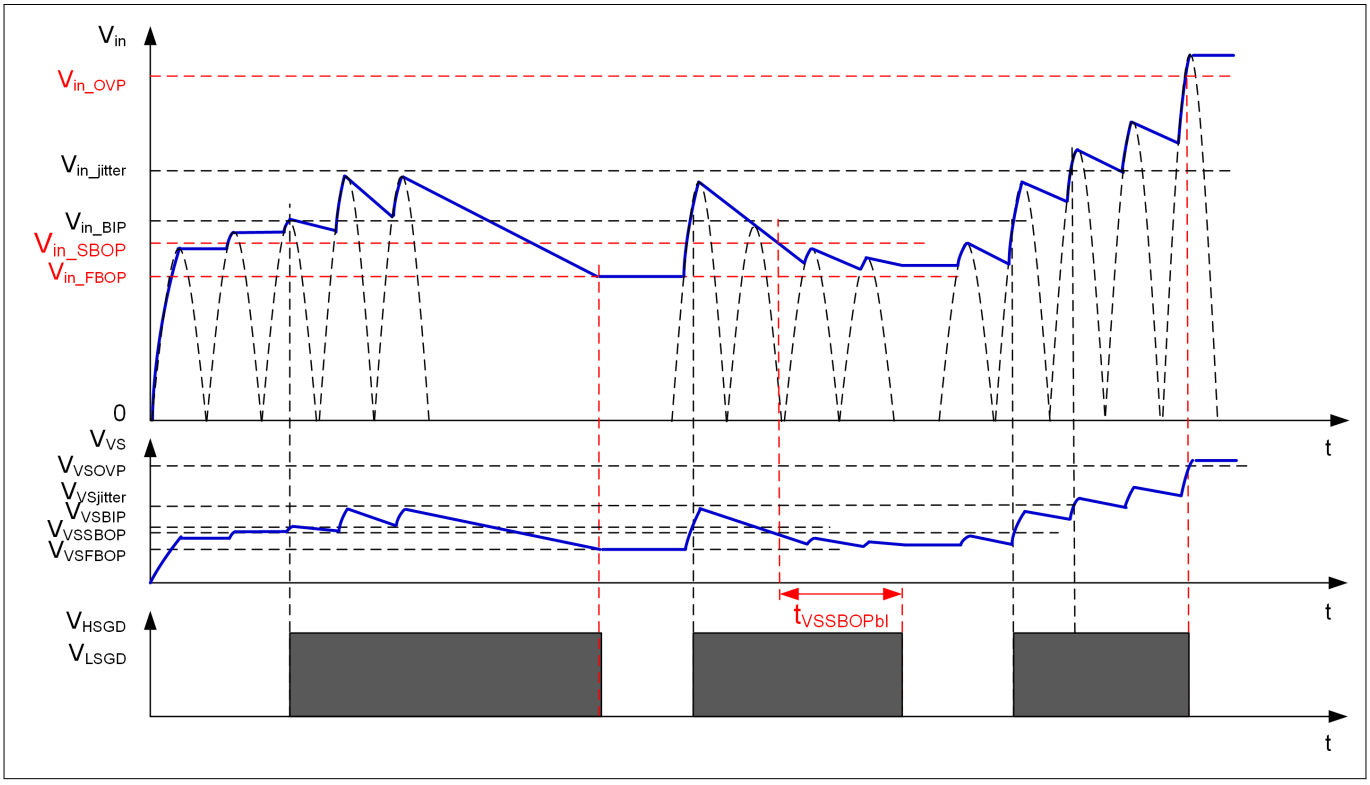


Figure 44 Parameters for brown-out and OVP

Input parameter V_{in_SBOP} (*Figure 44*)

It is the threshold for slow brown-out protection. If the average value of the input voltage V_{in} drops below this value for more than 44 ms, the input slow brown-out protection is triggered, the system stops switching, reports BROWN_OUT_AVG 2 error, and enters intermediate restart.

Input parameter V_{in_FBOP} (*Figure 44*)

It is the threshold for fast brown-out protection defined as the minimum operating input voltage. This voltage is sampled every 100 µs and the sampled value is compared with the threshold. If the sampled voltage V_{in} drops below this value, the fast input brown-out protection is triggered, the system stops switching, reports Fast brown-out error, and enters intermediate restart.

Input parameter V_{in_OVP} (*Figure 44*)

It is the threshold for V_{in} overvoltage protection defined as the maximum operating input voltage. This voltage is sampled every 100 µs. If the input voltage V_{in} is above this threshold, the input overvoltage protection is triggered, the system stops switching, reports FAIL_VIN_OVP error, and enters auto restart.

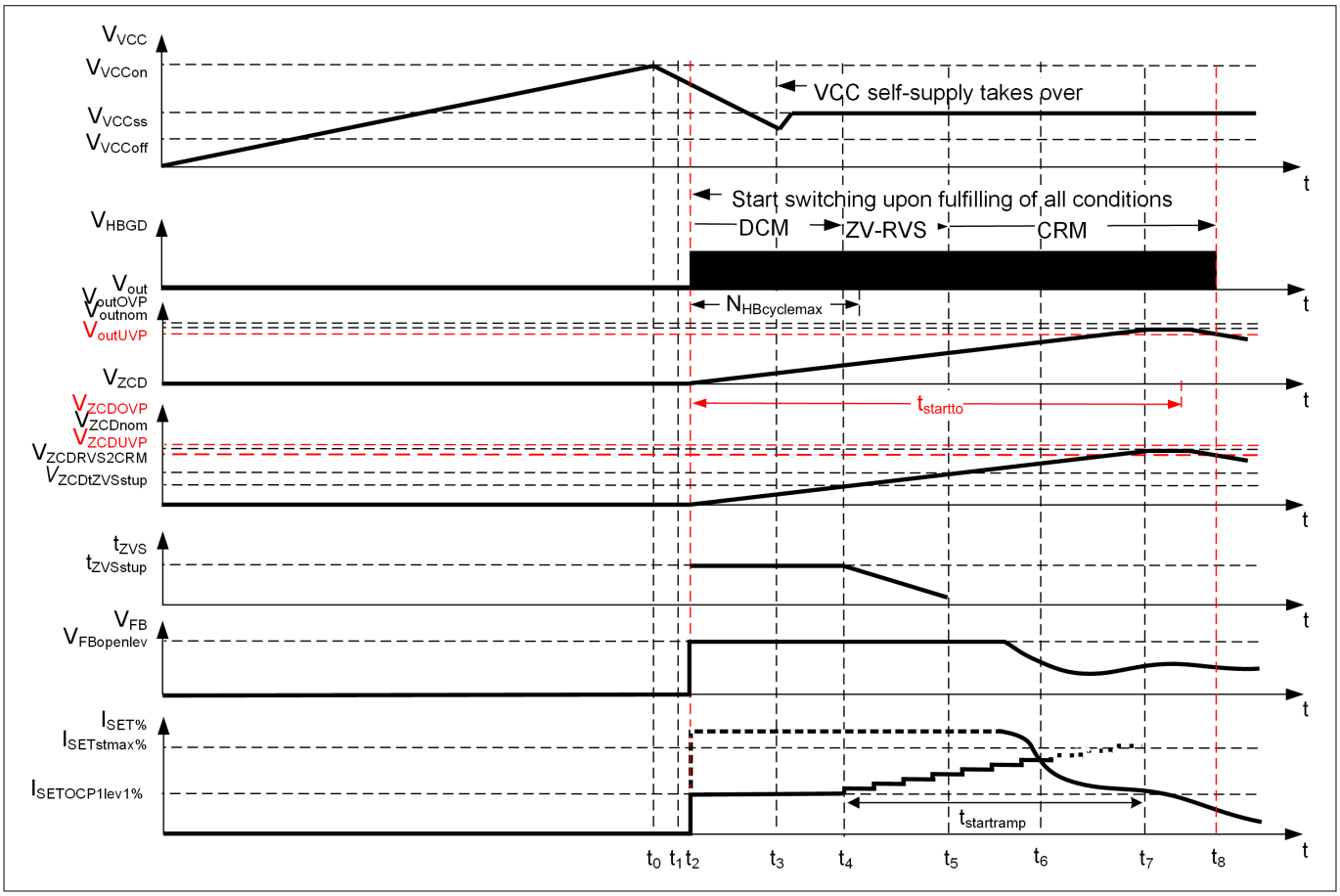


Figure 45 Parameters for the output voltage-related protections

Input parameter EV_{ZCDOVP} (***Figure 45***)

It is the switch for reaction on a detected output overvoltage event based on the ZCD pin voltage evaluation, either auto restart or latch.

Input parameter $EN_{BMVoutUVP}$ (***Figure 45***)

It is the enabling or disabling the output undervoltage protection during the burst mode operation. It is useful to capture the failure of low V_{VCC} level in a deep BM operation.

Input parameter V_{out_UVP} (***Figure 45***)

It is the voltage threshold for output undervoltage protection based on the ZCD pin voltage. This protection is only active after the time $t_{startto}$. If the average value of the voltage V_{zcd} drops below this value, the output undervoltage protection is triggered, the system stops switching, reports FAIL_VOUT_UVP error, and enters auto restart.

Input parameter $t_{startto}$ (***Figure 45***)

It is the time threshold for start-up timeout monitoring. It is the maximal allowed start-up time, measured from the first LS gate pulse to drop of the feedback voltage from its open loop level. If there is no drop of the feedback voltage within this time period, the start-up timeout protection is triggered, the system stops switching, reports FAIL_start-up_TIMEOUT error, and enters auto restart.

5 Parameterization

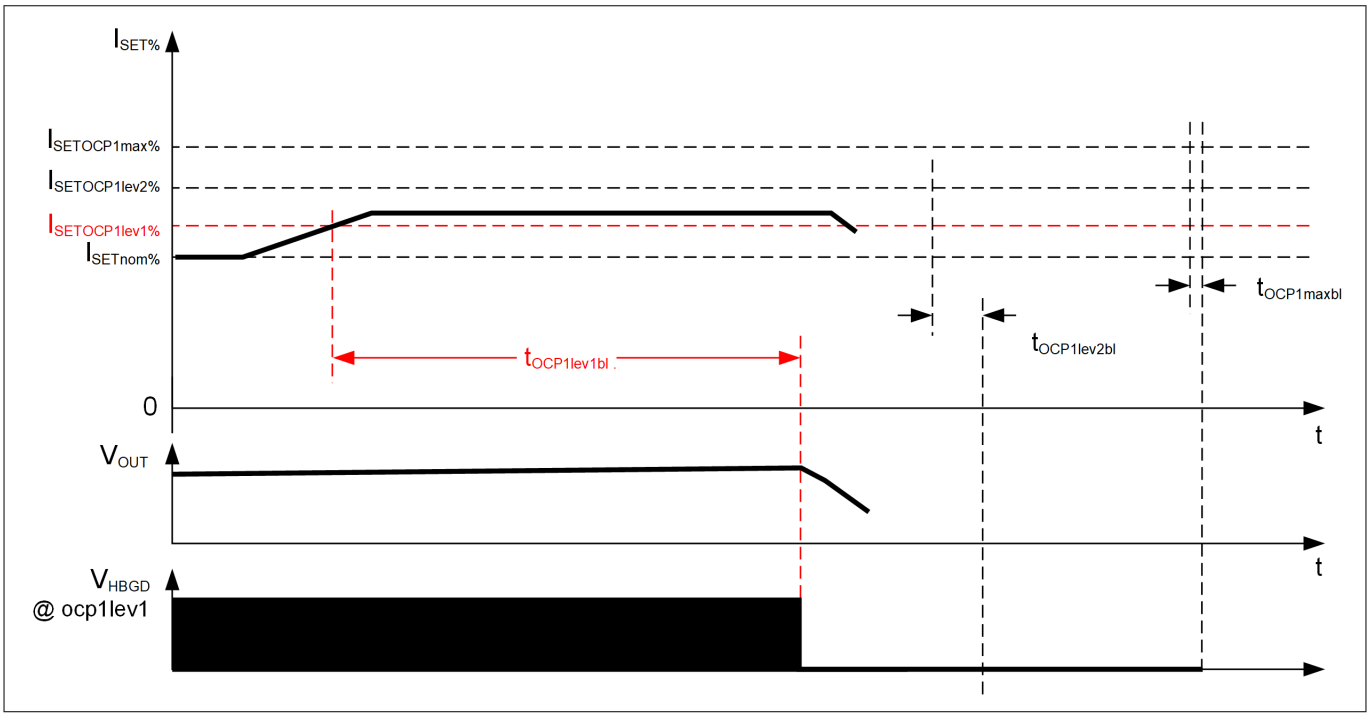


Figure 46 Parameters for the OCP1 level 1 protection

Input parameter $I_{SETOCP1lev1\_perc}$ (*Figure 46*)

It is the ratio of $\frac{I_{outOCP1lev1}}{I_{outnom}}$, where the current $I_{outOCP1lev1}$ is the output current threshold for the first-level output overcurrent protection (OCP1, level 1, also the lowest OCP level). If the output current is above $I_{outOCP1lev1}$ for longer than the monitoring time window $t_{OCP1lev1bl}$, and neither the output overcurrent protection OCP1lev2 nor OCP1max is triggered, the output overcurrent protection OCP1lev1 is triggered, the system stops switching, reports FAIL_OCP_TH1 error, and enters auto restart.

Input parameter $t_{OCP1lev1bl}$ (*Figure 46*)

It is the monitoring/blanking time window for the output overcurrent protection OCP1lev1.

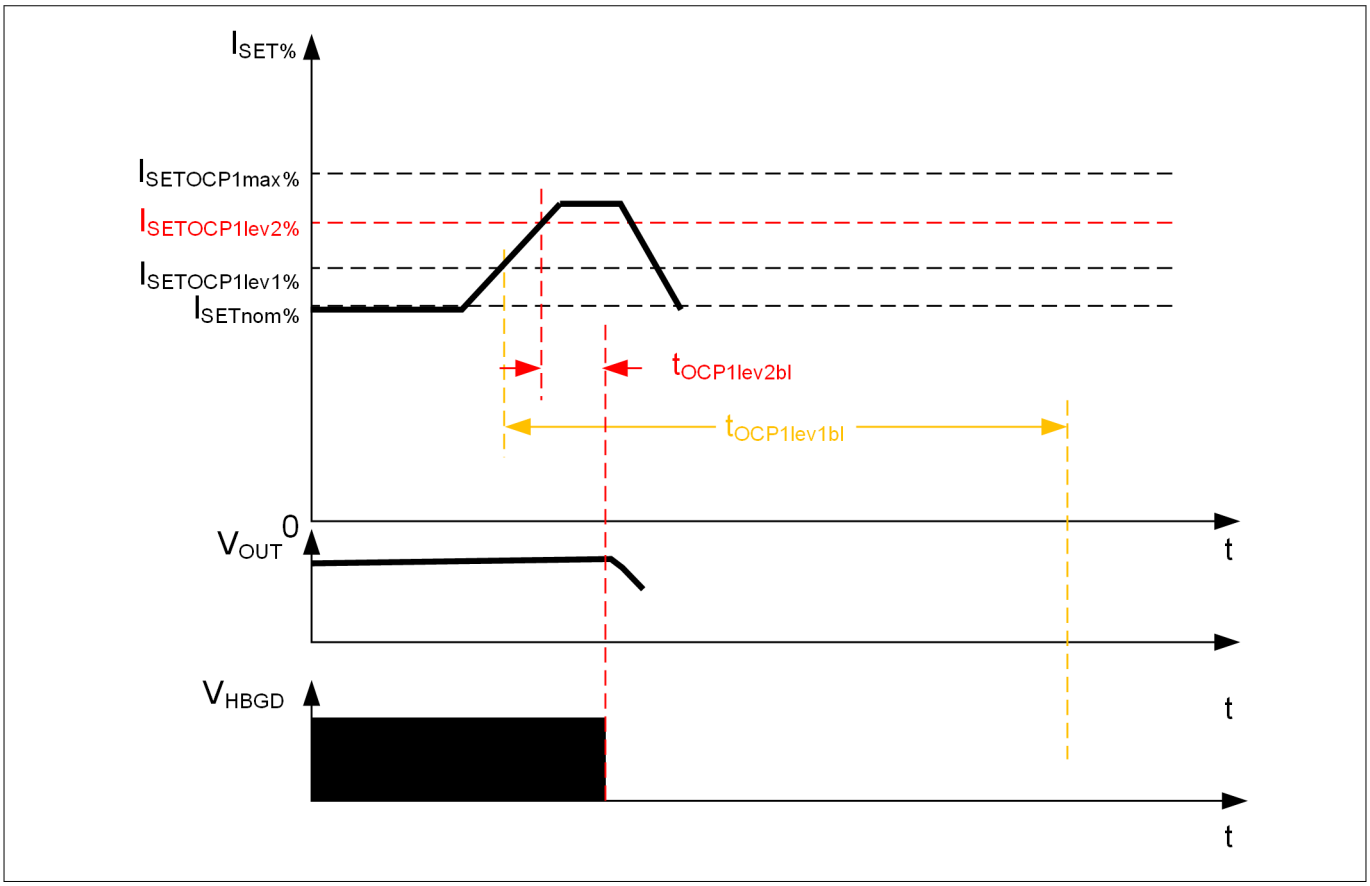


Figure 47 Parameters for the OCP1 level 2 protection

Input parameter $I_{SETOCP1lev2\_perc}$ (*Figure 47*)

It is the ratio of $\frac{I_{outOCP1lev2}}{I_{outnom}}$, where the current $I_{outOCP1lev2}$ is the output current threshold for the second-level output overcurrent protection (OCP1, level 2). If the output current is above $I_{outOCP1lev2}$ for longer than the monitoring time window $t_{OCP1lev2bl}$ and the output overcurrent OCP1max is not yet triggered, the output overcurrent protection OCP1lev2 is triggered, the system stops switching, reports FAIL_OCP_TH2 error, and enters auto restart.

Input parameter $t_{OCP1lev2bl}$ (*Figure 47*)

It is the monitoring/blanking time window for the output overcurrent protection OCP1lev2.

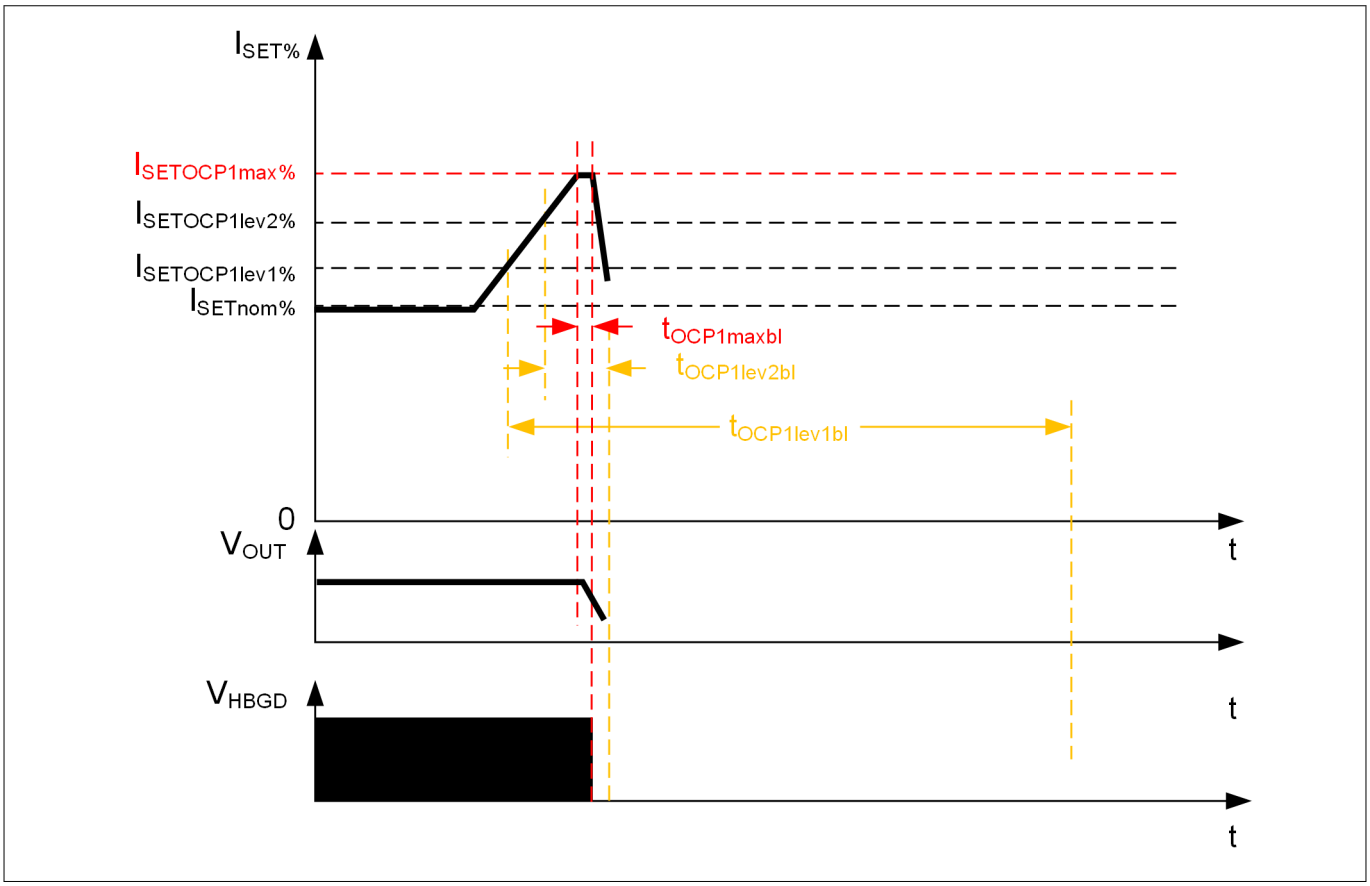


Figure 48 Parameters for the OCP1 max protection

Input parameter $I_{SETOCP1max\_perc}$ (***Figure 48***)

It is the ratio of $\frac{I_{outOCP1max}}{I_{outnom}}$, where the current $I_{outOCP1max}$ is the output current threshold for the highest-level overcurrent protection (OCP1max). If the output current is above $I_{outOCP1max}$ for longer than the monitoring time window $t_{OCP1max}$, the output overcurrent protection OCP1max is triggered, the system stops switching, reports FAIL_OCP1_max error, and enters auto restart.

Input parameter $t_{OCP1maxbl}$ (***Figure 48***)

It is the monitoring/blanking time window for the OCP1max protection.

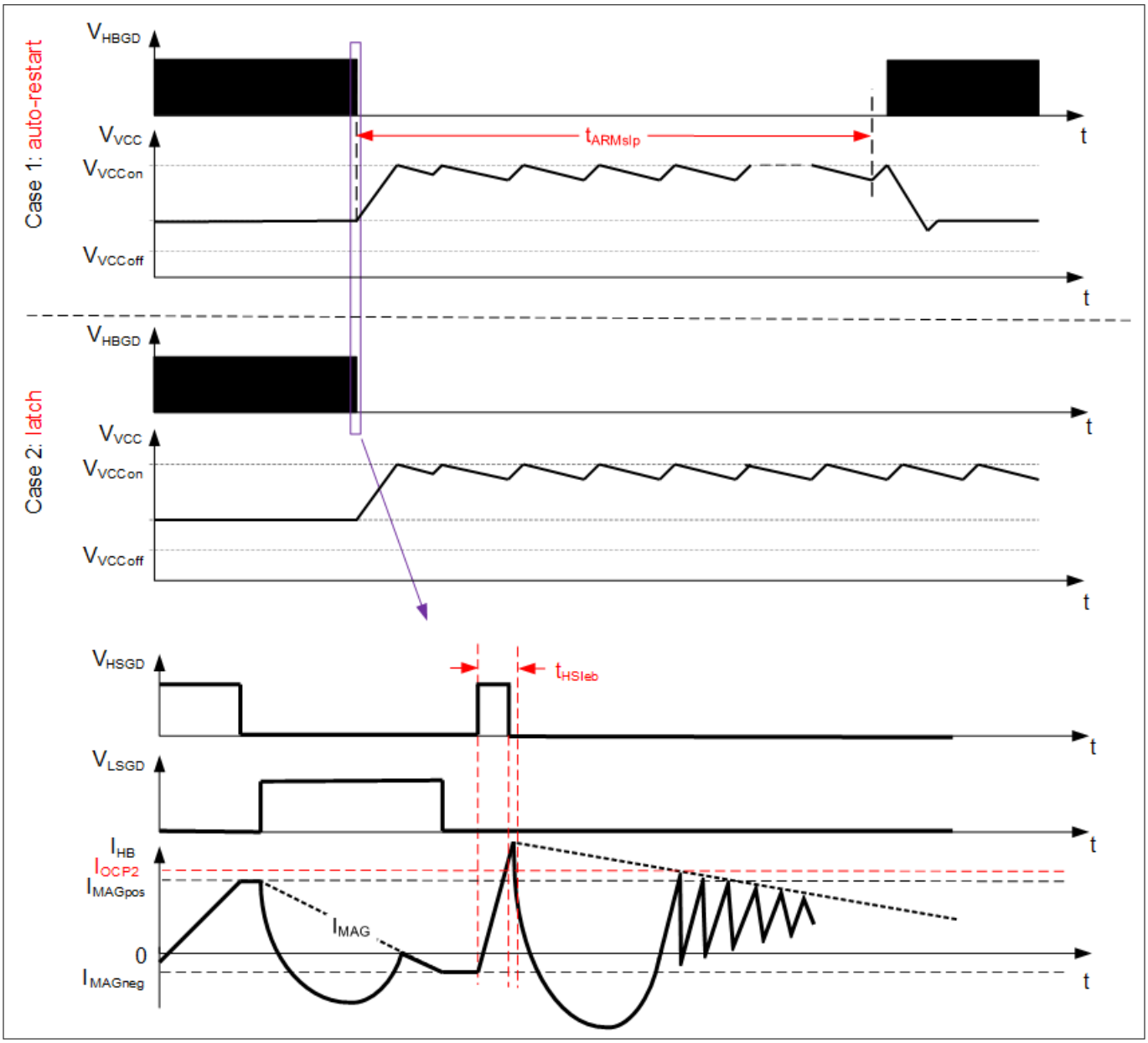


Figure 49 Reaction on the OCP2

Input parameter *EV$_{CSOCP2}$* (*Figure 49*)

It is the switch for reaction on the overcurrent protection 2 (OCP2), either auto restart or latch.

While the output overcurrent protections, OCP1lev1, OCP1lev2 and OCP1max, have configurable threshold and monitoring time that is longer than the switching period, the protection OCP2 has the fixed threshold V_{CSOCP2} and is active in every switching cycle. Once the voltage across the shunt resistor is higher than the threshold V_{CSOCP2}, the protection OCP2 is triggered and the switching is stopped within that switching cycle.

Note: For the OCP2 protection, the leading edge blanking time t_{HSleb} does not apply to the current sensing signal. As shown in Figure 49, the HS gate is turned off once the current sense signal V_{CS} is higher than the threshold V_{CSOCP2} even within the time t_{HSleb}.

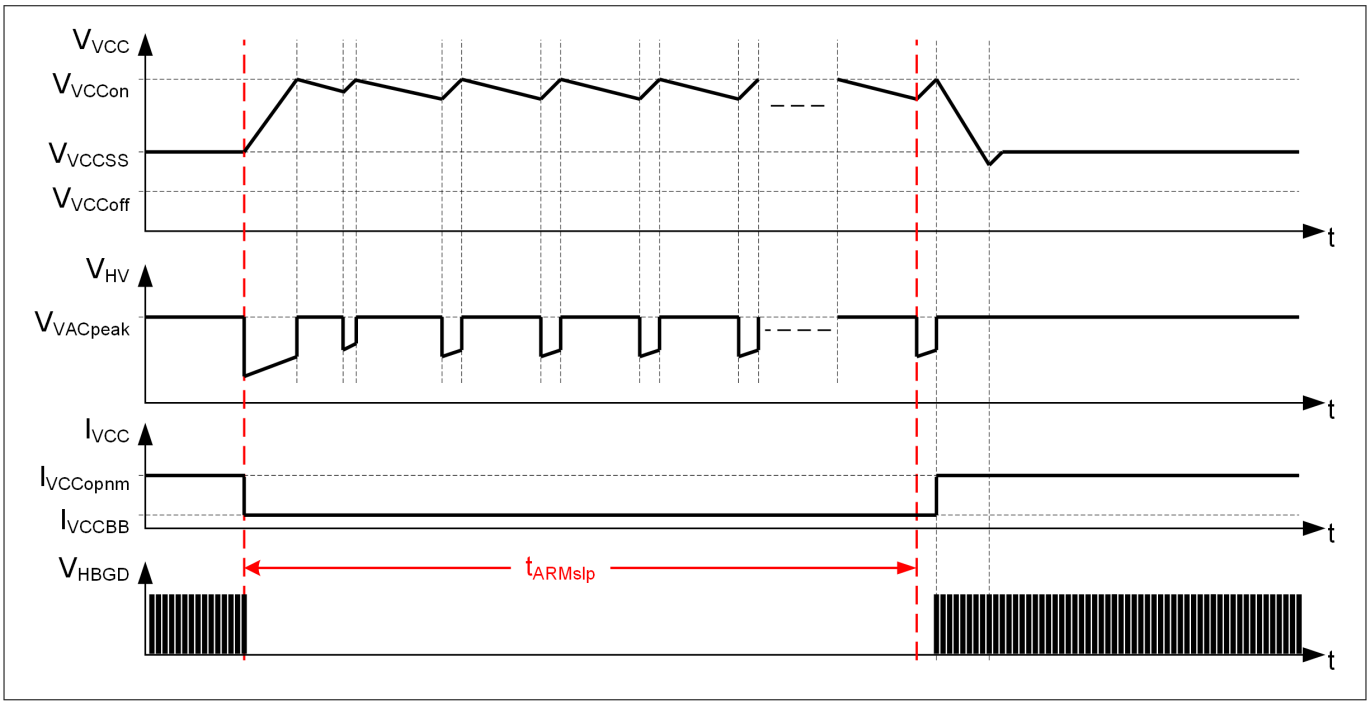


Figure 50 Time break for auto restart

Input parameter t_{ARMslp} (*Figure 50*)

It is the auto restart time break after a failure is detected. The break time is counted in time steps defined by $t_{ARMbase}$.

Input parameter $R_{MFIOOTPtrig}$ (*Figure 51*)

It is the resistance threshold for the external OTP triggering at the MFIO pin, if a NTC resistor is connected between the MFIO pin and IC ground for the external OTP. If the measured resistance reduces below this threshold $R_{MFIOOTPtrig}$, then the external OTP is triggered and the application is stopped. If OTP is triggered during the normal operation, the FAIL_OTP error is reported or if OTP is triggered at start-up, the FAIL_OTP_start-up error is reported..

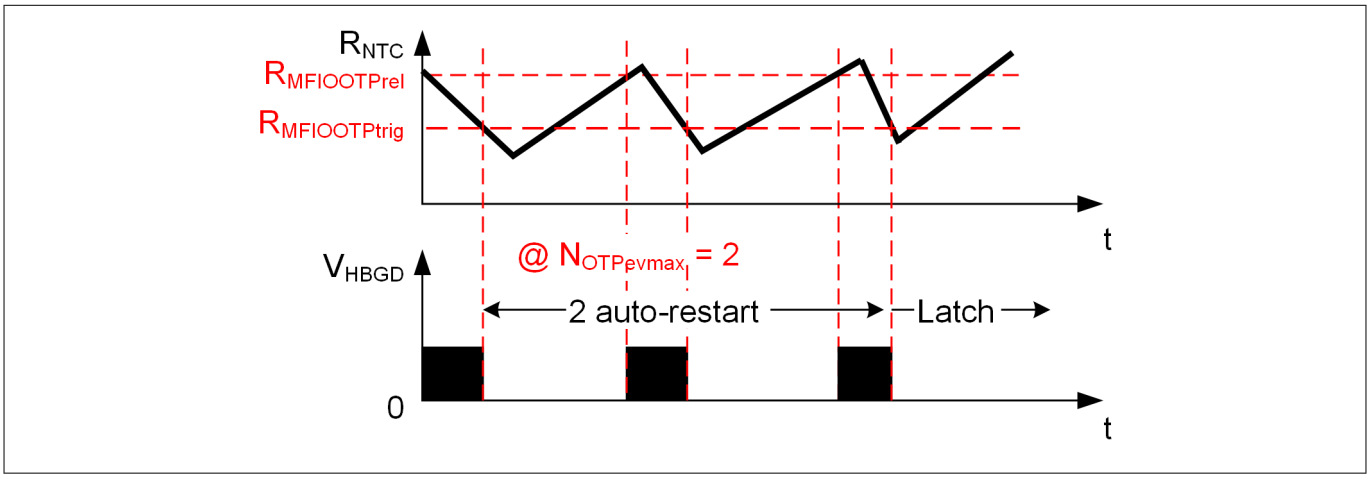


Figure 51 Parameters for OTP

Input parameter $R_{MFIOOTPrel}$ (*Figure 51*)

It is the resistance threshold for the external OTP releasing at the MFIO pin. With the decreasing temperature, the NTC resistance increases again. Once the value rises above the threshold $R_{MFIOOTPrel}$, the system may resume its operation with the start-up process or latch depending on the value set for $N_{OTPevmax}$.

Input parameter $N_{OTPevmax}$ (*Figure 51*)

Two cases are possible with respect to the reaction to OTP. In the first case, the value of $N_{OTPevmax}$ is below the given maximum value. In this case, the system will auto restart until the given number of $N_{OTPevmax}$. After that, the system enters the latch and only a VCC power off can de-latch the system, and the FAIL_OTP error is reported at each OTP event. In the other case, when the value is set to the given maximum value (65535), the system will *always* auto restart after the temperature decreases and the NTC value increases above the threshold $R_{MFIOOTPrel}$, while the FAIL_OTP error is reported at each OTP event.

Input parameter EV_{WDOG}

This parameter defines the reaction if watch dog is not reset in time for any reason, either auto restart or latch.

5.3.8 Mode threshold

The five input parameters in this group are: $I_{SETRVS2CRM\_perc}$, $I_{SETCRM2RVS\_perc}$, $V_{out\_RVS2CRM}$, $V_{out\_CRM2RVS}$ and $I_{MAGposRVS0V\_perc}$.

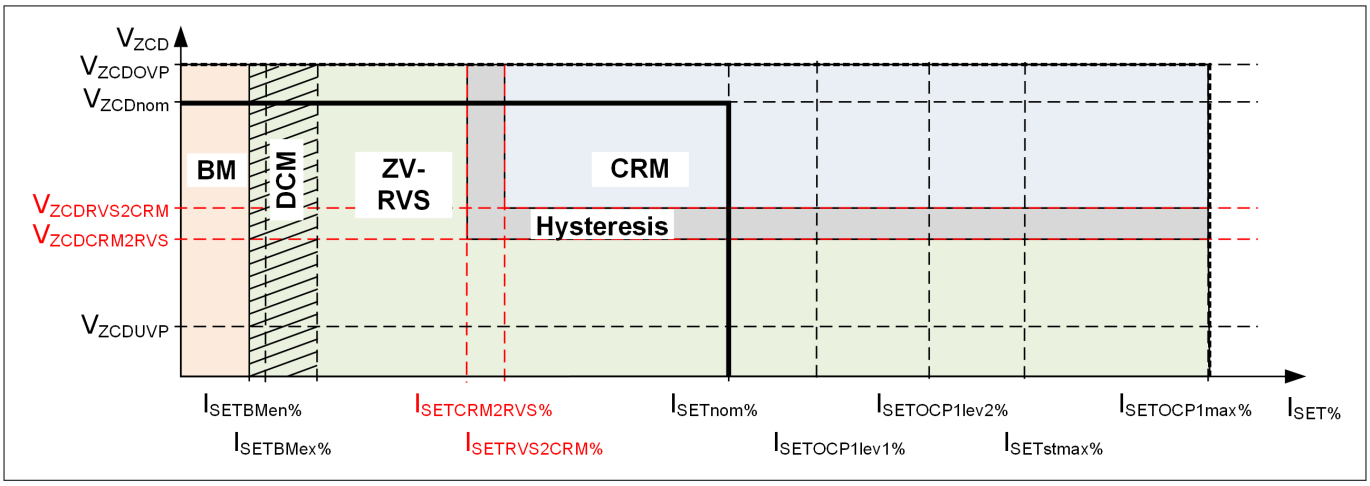


Figure 52 Parameters for the ZV-RVS and CRM transition

Input parameter $I_{SETRVS2CRM\_perc}$ (*Figure 52*)

It is the ratio of $\frac{I_{outRVS2CRM}}{I_{outnom}}$, where the current $I_{outRVS2CRM}$ is the output current threshold for switching over from the ZV-RVS mode to CRM.

Input parameter $I_{SETCRM2RVS\_perc}$ (*Figure 52*)

It is the ratio of $\frac{I_{outCRM2RVS}}{I_{outnom}}$, where the current $I_{outCRM2RVS}$ is the output current threshold for switching over from CRM to the ZV-RVS mode.

Input parameter $V_{out\_RVS2CRM}$ (*Figure 52*)

It is the ratio of $\frac{V_{outRVS2CRM}}{V_{outnom}}$, where the voltage $V_{outRVS2CRM}$ is the output voltage threshold for transition from the ZV-RVS mode to CRM.

Input parameter $V_{out\_CRM2RVS}$ (*Figure 52*)

It is the ratio of $\frac{V_{outCRM2RVS}}{V_{outnom}}$, where the voltage $I_{outCRM2RVS}$ is the output voltage threshold for transition from CRM to the ZV-RVS mode.

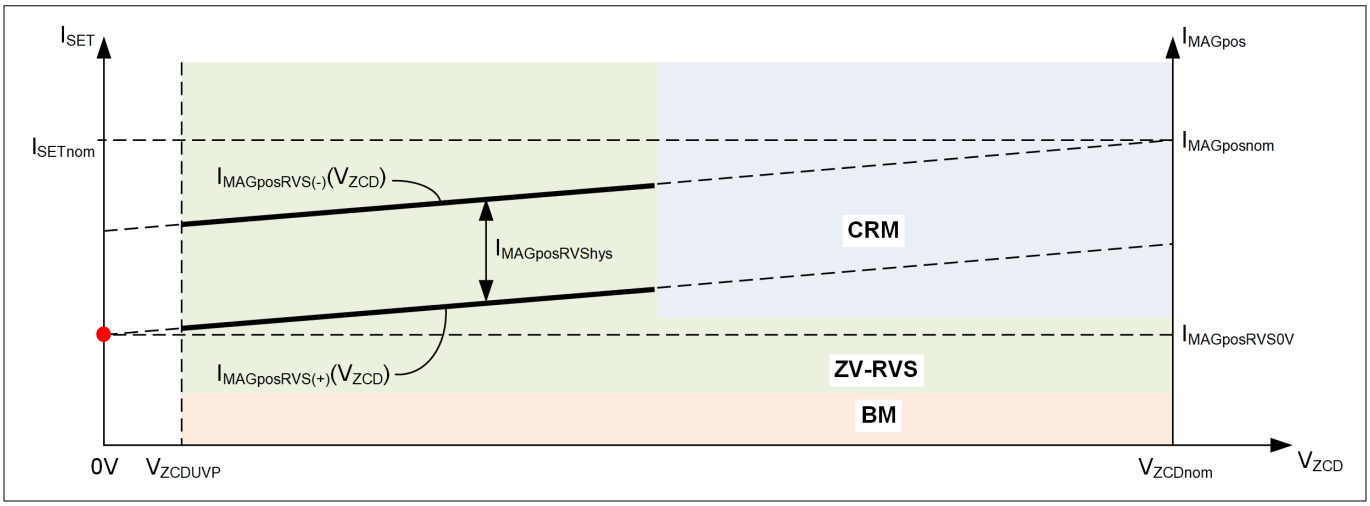


Figure 53 Valley control starting point

Input parameter $I_{MAGposRVS0V\_perc}$ (*Figure 53*)

It is the ratio of $\frac{I_{MAGposRVS0V}}{2 \cdot \frac{I_{outnom}}{N}}$, where the current $I_{MAGposRVS0V}$ is the current positive peak at the output voltage V_{out} of 0 V. The value of this parameter defines the line $I_{MAGposRVS(+)}$, which further determines the threshold for change of the valley number and the time $t_{waitgap}$ in the ZV-RVS mode operation. Additionally, the line $I_{MAGosRVS(+)}$ defines the positive peak current during the burst mode operation according to the output voltage level.

5.3.9 Jitter

The input parameters in this group are: V_{in_jitter}, $d_{Jitterspread\_perc}$ and $t_{Jitterstpdel}$.

Input parameter V_{in_jitter} (*Figure 54*)

It is the voltage threshold for activating and deactivating the switching frequency jitter function. If the measured input voltage is higher than this threshold, the switching frequency jitter is activated, otherwise, deactivated.

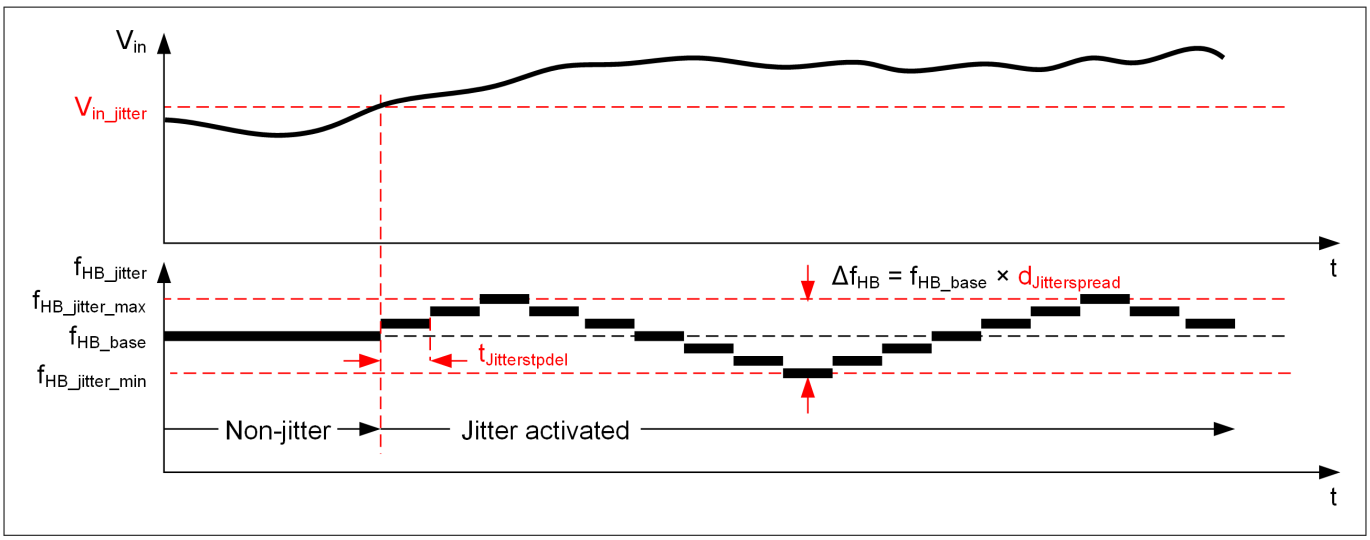


Figure 54 Parameters for switching frequency jitter

Input parameter $d_{Jitterspread\_perc}$ (*Figure 54*)

It is the frequency jitter spread setting in percentage of the base switching frequency. For a base switching frequency of 200 kHz and with this parameter set to 10%, the switching frequency is in the range of 180 kHz to 220 kHz.

Input parameter $t_{Jitterstpdel}$ (*Figure 54*)

It is the time delay between the steps in frequency variations. The value of this parameter must be longer than the system regulation settling time.

5.3.10 Others

Input parameter t_{PDC}

It is the time period for propagation delay compensation of the peak current comparator.

For HFB, an easy way to obtain the correct value is to verify the real and the targeted $I_{OCP1lev1}$ based on the parameter $I_{SETOCP1lev1\_perc}$. If both the values match with each other, then the parameter value of t_{PDC} is correct. Otherwise, if the measured $I_{OCP1lev1}$ is lower than the set target level, then the value of the parameter t_{PDC} has to be decreased and vise versa.

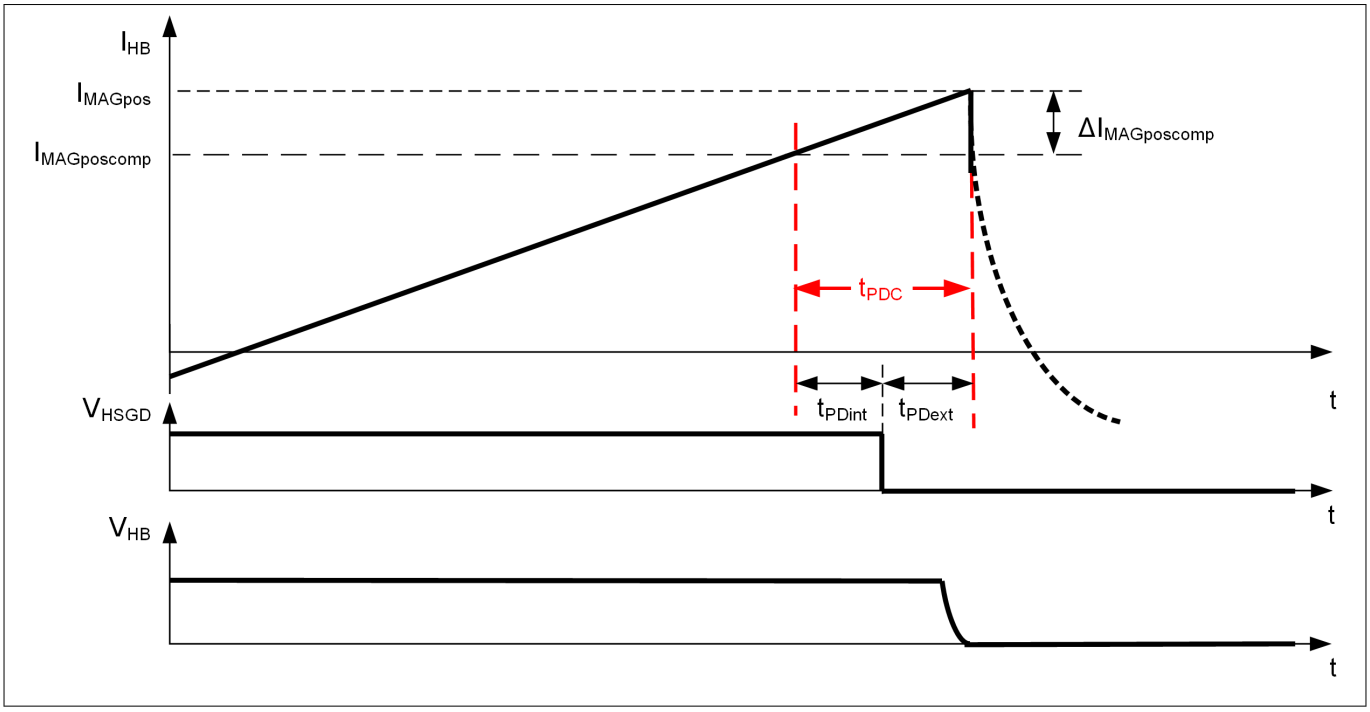


Figure 55 Propagation delay compensation time

6 PCB design tips

There are a few general rules for the PCB layout. In this sub-chapter, some of the practical PCB layout hints are given for a good system performance, including the IC footprint, consideration for the PCB tracks layout and design for a good EMI performance. The following points are included:

- IC package and footprint (***Chapter 6.1***)
- Consideration for PCB layout (***Chapter 6.2***)

6.1 IC package and footprint

The IC has a footprint PG-DSO-14 with 14 pins bonded, but two pins (2 and 11) are not actively used for the HFB controller.

*Note: It is recommended to connect these pins to IC ground to avoid any noise pick-up through the unused pins. This footprint has an outline dimension of the conventional DSO-16 package, as illustrated in **Figure 56**.*

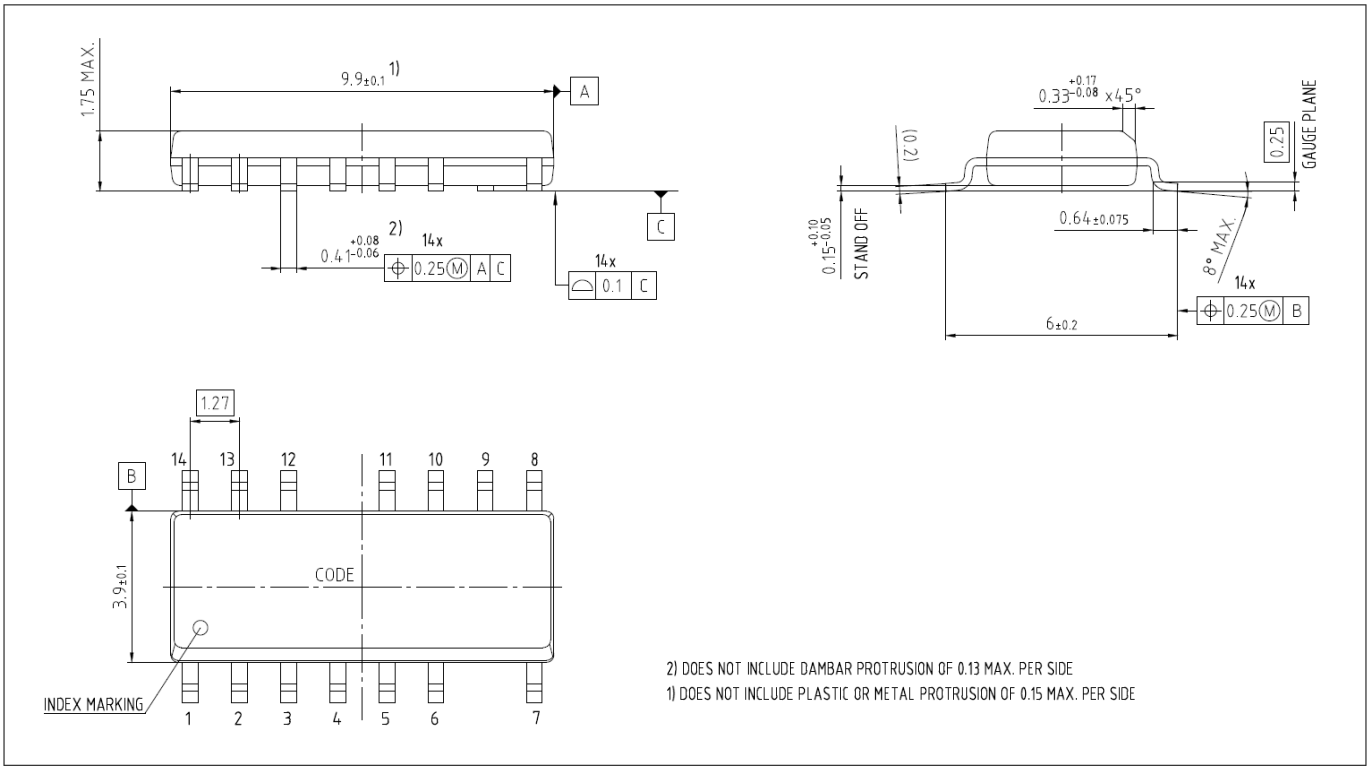


Figure 56 PG-DSO-14 outline

6.2 Consideration for PCB layout

For the PCB layout, attention has to be paid to the path and loop with high $\frac{dv}{dt}$ and high $\frac{di}{dt}$, grounding and PCB track impedance. This will be illustrated graphically as follows.

Sensitive signals

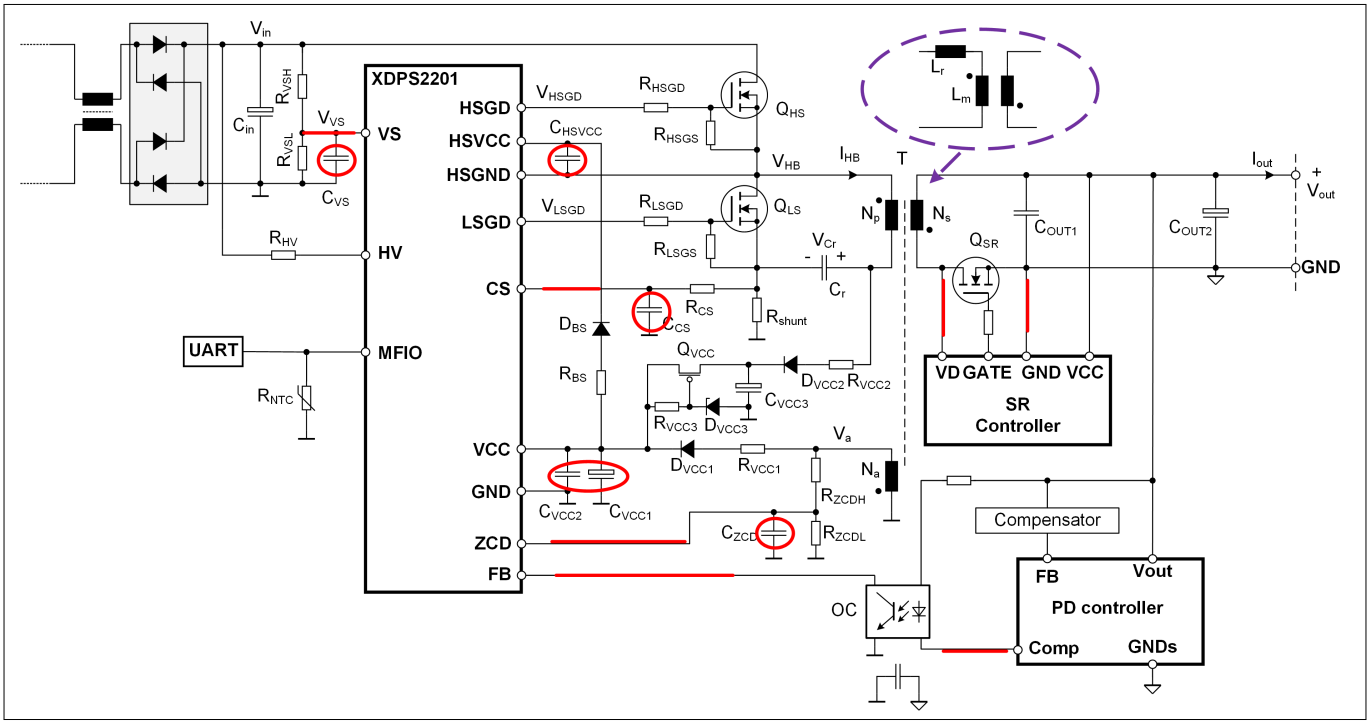


Figure 57 Sensitive signals and filter capacitors

It is essential that the PCB trace should be as short as possible for such sensitive signals, while the filter capacitors must be placed close to the IC. For the VS pin divider, place the resistors also close to the IC. With a long PCB trace between the resistors R_{VSH} and R_{VSL}, the signal V_{VS} can be easily disturbed.

6 PCB design tips

PCB trace with high $\frac{dv}{dt}$

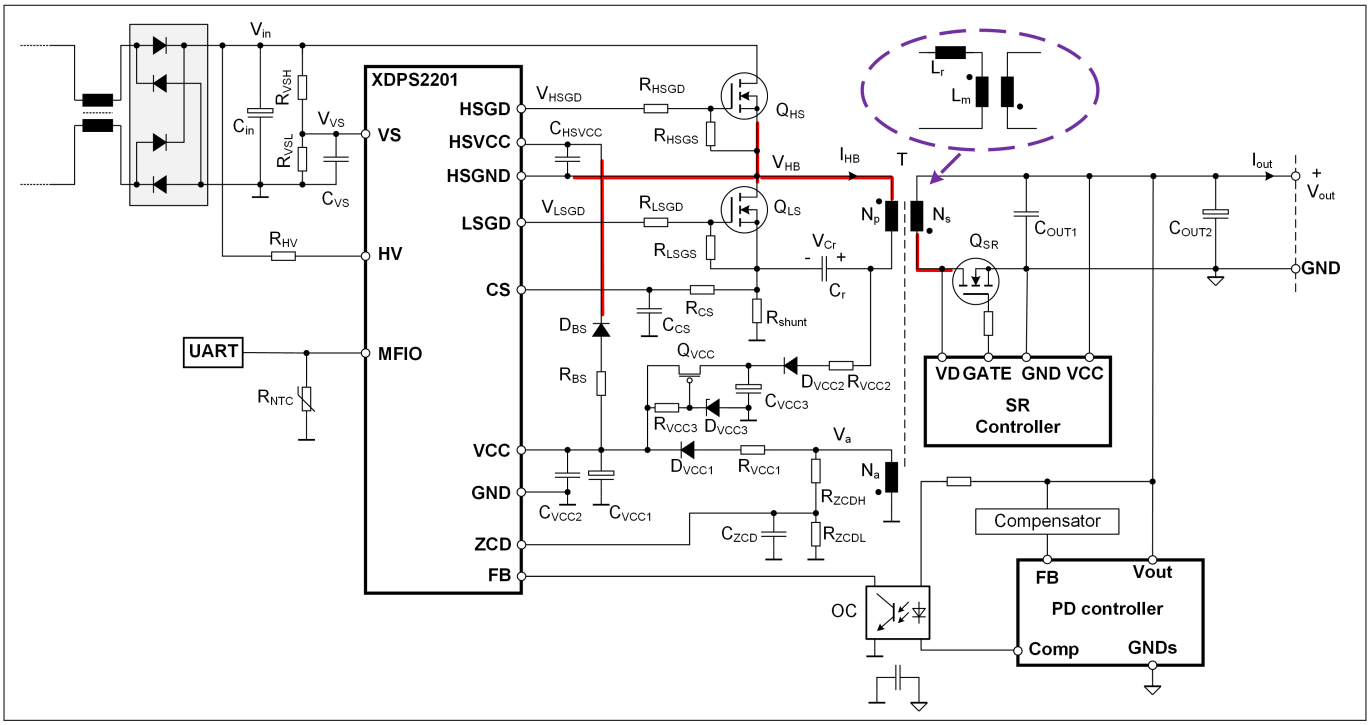


Figure 58 **PCB trace with high $\frac{dv}{dt}$**

For the PCB trace with high $\frac{dv}{dt}$, which is one of the most common noise source, it should be as short as possible and maintain enough distance to the sensitive signals to minimize the coupled noise.

6 PCB design tips

PCB trace with high $\frac{di}{dt}$

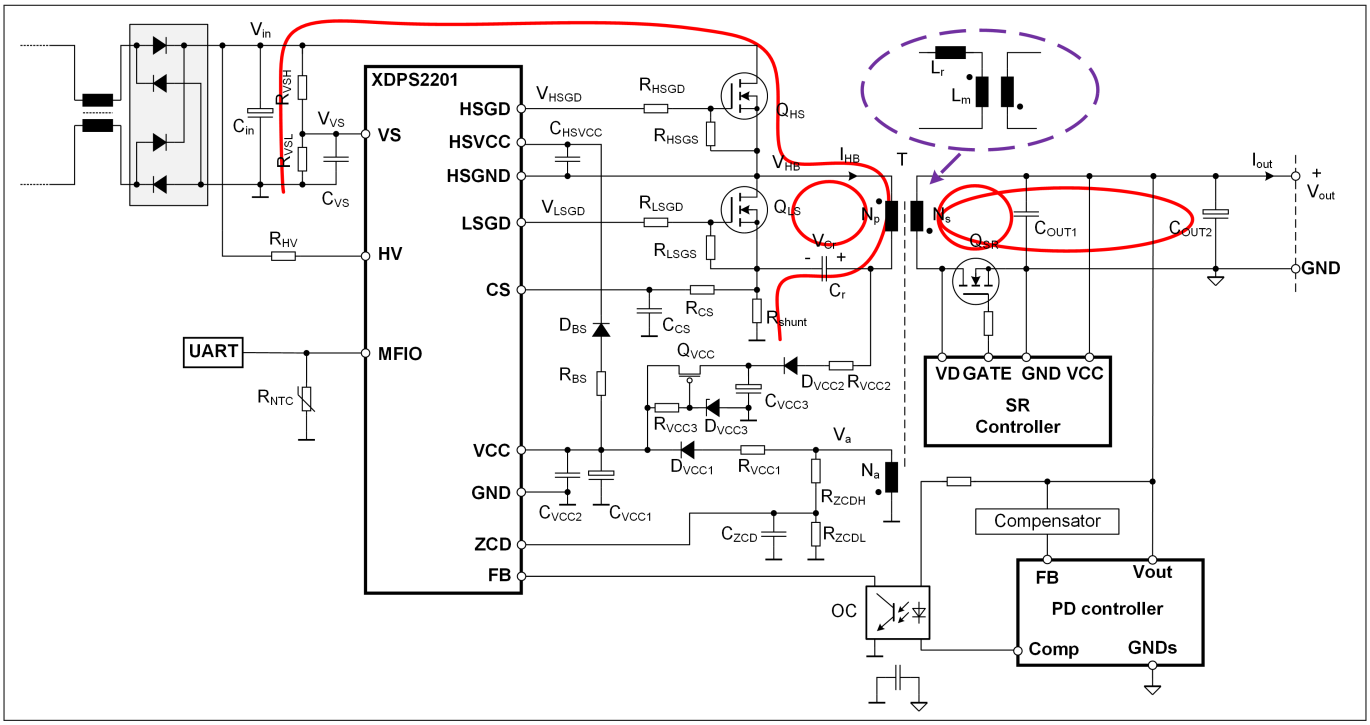


Figure 59 PCB trace with high $\frac{di}{dt}$

The PCB trace for such signals should be of a low impedance, both the trace resistance and inductance, and the loop size must be small. For the multi-layer PCB design, the loop can be minimized by using the overlapped layers.

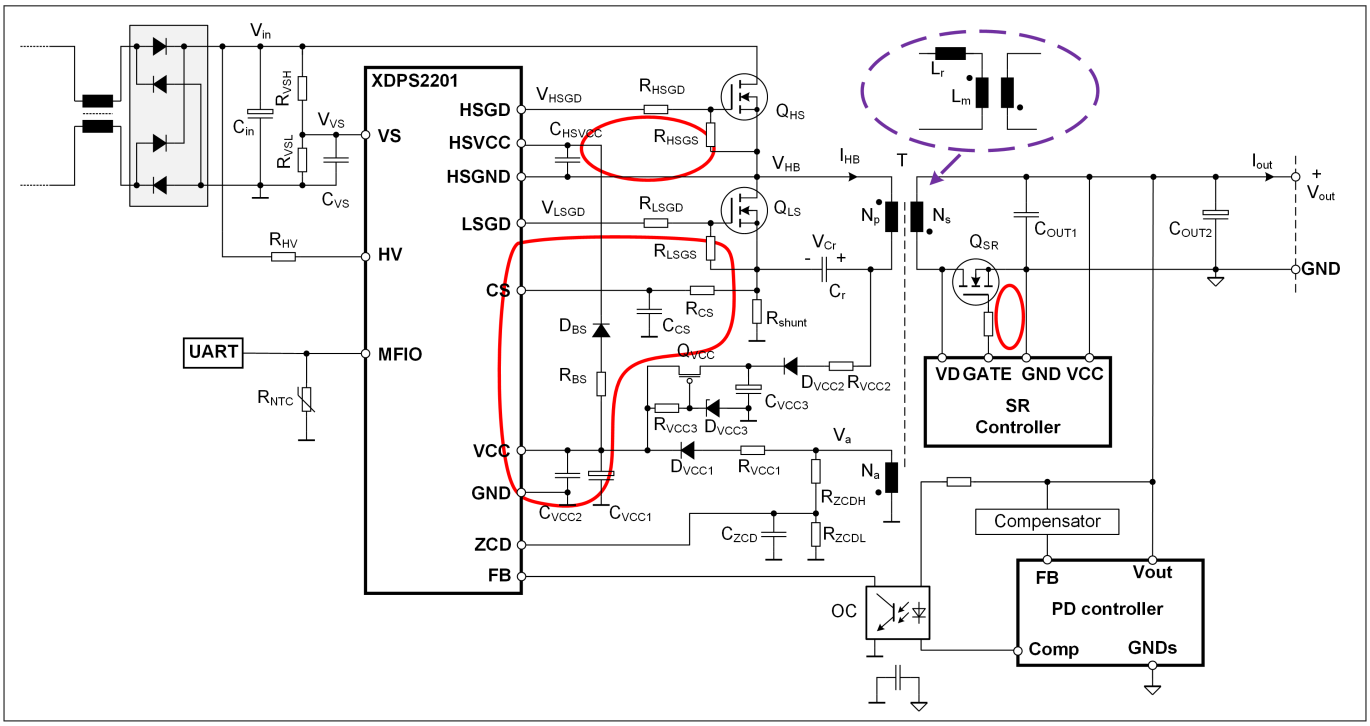


Figure 60 Gate driver loop

The gate driver loop size must be as small as possible.

6 PCB design tips

Grounding

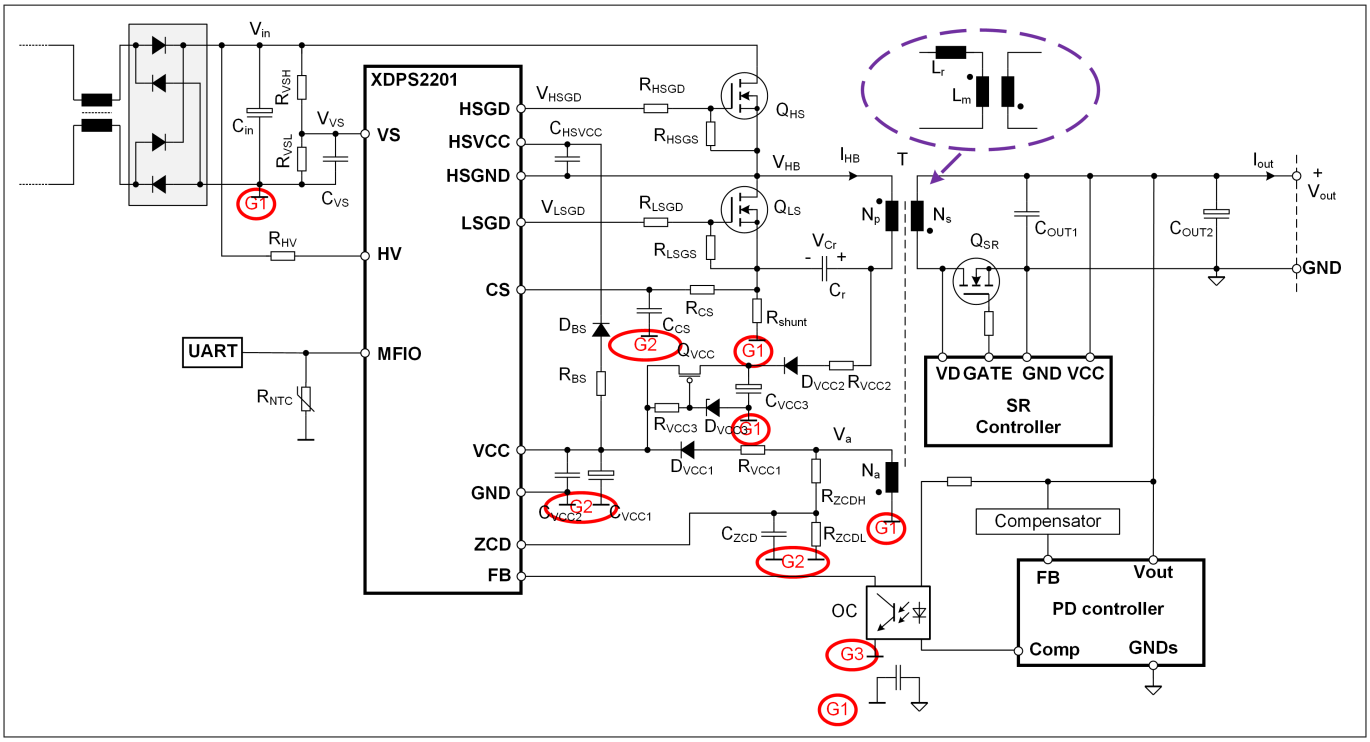


Figure 61 Grounding concept

There are three basic ground types, G1 to G3, where G1 is the power ground, G2 is the IC ground and G3 is the special ground, which belongs to G1 or G2 depending mainly on the coupling capacitance of the opto-coupler. With a small coupling capacitance, it can be taken as G2, otherwise, it is better taken as G1.

The different ground groups should be connected together with short connections. Later, the different ground groups must be connected to the bus capacitor ground forming a star-ground connection.

PCB layout tips for a good EMI

A well-designed PCB helps to improve the EMI performance on the board level, including:

- Small loop of the EMI filter
- Enough space between the EMI filter element and switching elements, and high $\frac{dv}{dt}$ and $\frac{di}{dt}$ PCB traces
- Bus capacitor with a low ESR
- Proper connection of the Y-capacitor at the primary and secondary side. Normally, the Y-capacitor is connected to the noise-free points, such as power ground or stable voltage

7 Other information

There are some other general hints for a good design and ease of design. These are covered here:

- Design for a good EMI performance (***Chapter 7.1***)
- Parameter adjustment for ZVS (***Chapter 7.2***)
- Output capacitance (***Chapter 7.3***)
- Resonant capacitor (***Chapter 7.4***)
- Wide output voltage range design (***Chapter 7.5***)
- Probing signal on the board (***Chapter 7.6***)

7.1 Design for a good EMI performance

The EMI performance of the system depends on the several factors. Besides those mentioned in the PCB design part, the following points may contribute for a good EMI performance.

Switching frequency selection

Generally, the lower the switching frequency below the starting frequency for EMI rule, the easier the EMI filter design. However, this may be limited by the other factors, such as the required transformer size.

On the other hand, the switching frequency should not be higher than 300 kHz due to a certain time limitation related to the gate pulse width, signal sensing and processing.

Common mode choke

For the common mode choke, the winding construction plays an important role. A parallel winding with bifilar wires on a ring core minimizes the switching noise pick-up, which is critical for a compact design.

Transformer construction

With some of the measures, the transformer-coupled noise emission can be minimized, for example, using an inner shielding layer between the primary and secondary side winding. As seen in some of the tests, the multi-strand litz wire is preferred for the shielding layer to have enough attenuation of the noise and less impact on the system efficiency.

7.2 Parameter adjustment for ZVS

The ZVS of both the switches Q_{HS} and Q_{LS} can only be ensured by a proper value setting of $t_{LS2ZCDnom}$, $t_{LS2ZCDmin}$, $I_{MAGnegnom\_perc}$, $I_{MAGnegmaxCRM\_perc}$ and $I_{MAGnegmaxRVS\_perc}$. Among these parameters, $t_{LS2ZCDnom}$ and $I_{MAGnegnom\_perc}$ are valid for the operation at the nominal output voltage and current and the input voltage around V_{in_OpC1}, while the others are applied at the highest operating input voltage V_{in_OVP}. The value of $t_{LS2ZCD*}$ [3] is adjusted depending on the input voltage V_{in} to have a ZV turn-on for the switch Q_{HS}, and the negative current amplitude $I_{MAGneg*}$ is measured. The value for the parameter $I_{MAGnegnom\_perc}$, $I_{MAGnegmaxCRM\_perc}$ and $I_{MAGnegmaxRVS\_perc}$ is then calculated based on:

$$I_{MAGneg*\_perc} = \frac{I_{MAGneg*}}{\frac{2 \cdot I_{outnom}}{N}} \cdot 100$$

Equation 43

For a wide input range design, a doubled value of $I_{MAGnegnom\_perc}$ as the value for $I_{MAGnegmaxCRM\_perc}$ and $I_{MAGnegmaxRVS\_perc}$ is a good starting point.

3 * represents the different cases: nom, maxCRM and maxRVS

7.3 Output capacitance

The output capacitance is determined by the following three main factors:

- Requirement on the ripple at the specified biggest load step
- Requirement on the output voltage ripple during the burst mode operation
- Stable and smooth transitions at the burst entry and exit

The selected output capacitance is defined by the maximum value from these requirements.

7.4 Resonant capacitor

For the resonant capacitor, either a ceramic or a film capacitor can be used. For a cost effective design, the ceramic capacitor is normally used. In comparison to the film capacitor, a ceramic capacitor shows a much higher-voltage coefficient and must be compensated for a wide output voltage range design. In XDPS2201, the parameter for this compensation is $t_{TRANRVS0V\_perc}$ (***Figure 30***). Despite this compensation capability of the control IC, it is recommended not to use too small capacitance for the resonant capacitor due to the voltage ripple across the resonant capacitor and the required rated voltage.

7.5 Wide output voltage range design

For the USB-PD application, the output voltage varies between different levels. At a low output voltage, the signal V_{ZCD} also has a small amplitude during the time t_{LSon}. Per a proper system dimensioning, the voltage V_{ZCD} during t_{LSon} must be well above the threshold V_{ZCDTHR} for a reliable zero-crossing detection.

7.6 Probing signal on the board

It is necessary to directly probe signals on the board. But a normal oscilloscope probe has a long ground connection and extended tip. Such a probe is not suitable to be directly used to do the measurement on a power converter, especially with a highly compact design, which picks up the noise with the big loop from the long tip and ground connection. For the signal probing with a good quality, it is highly recommended to have a small ground loop, direct signal access, and vertical positioning of the probe on the board, as shown in ***Figure 62***.

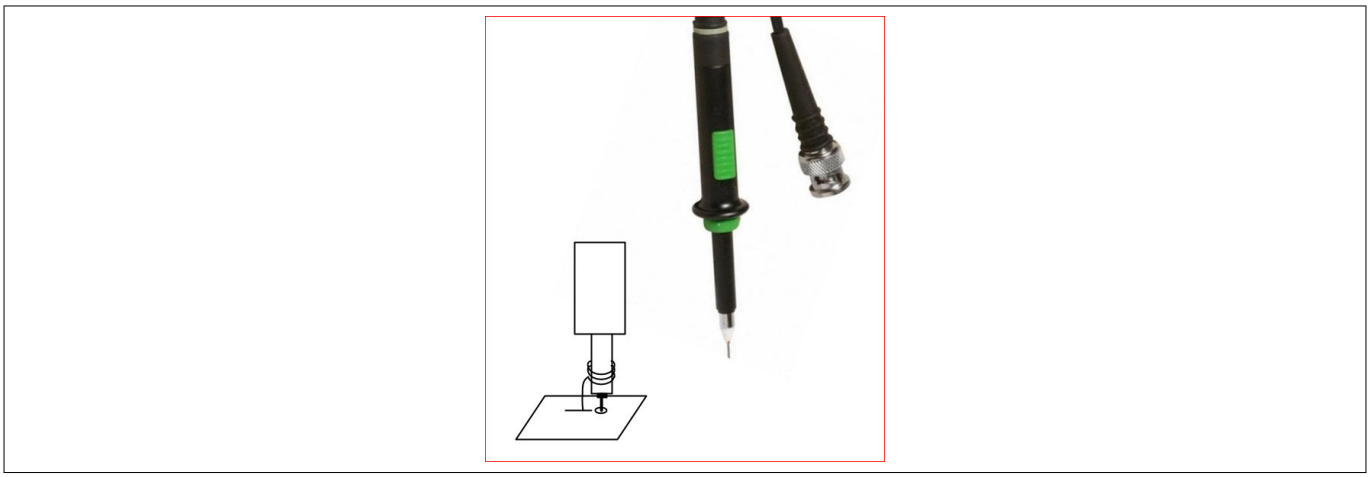


Figure 62 Signal probing on the board

8 Summary

The HFB topology has a simple structure and some of the resonant characteristics. It is the best choice for the ultrahigh power density design with high efficiency for a wide input and output voltage range applications due to the following facts:

- Both the transformer and the resonant capacitor contribute to the intermediate energy storage to minimize the component size
- Zero-voltage switching for both the MOSFETs at the primary side for high efficiency
- Zero-current turn-off of the SR MOSFET for high efficiency
- Supporting the wide input voltage range without any additional components
- Multi-mode operation over a wide output voltage and current range for high efficiency
- Deep sleep mode of the IC supporting low input power consumption at light load
- Complete set of configurable parameters enabling the usage of the controller for a platform approach

The controller IC functionality and design hints, including the configurable parameters, are described in this document.

9 References

1. USB-PD: ***https://www.usb.org/usb-charger-pd***
2. Datasheet "XDP Hybrid-flyback Controller XDPS2201"
3. Type III compensator: ***https://www.infineon.com/dgdl/an-1162.pdf?fileId=5546d462533600a40153559a8e17111a***

10 Related links and support material

A collection of useful internet shortcuts.

- Power Management selection guide
  - ***http://www.infineon.com/powermanagement-selectionguide***
- Search videos
  - ***http://www.infineon.com/mediacenter***
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- Contact and support
  - ***http://www.infineon.com/support***

11 Change history

Table 3 Change history

Date	Revision	Main changes
2020.03.01	V1.0	Initial release

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Edition 2021-03-01

Published by

Infineon Technologies AG

81726 Munich, Germany

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Document reference
IFX-svs1584626679042

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