Design guide for low-noise transistors in SDARS active antenna LNA

RF bipolar transistors

About this document

Scope and purpose

This application note provides application circuit design examples of Infineon's low-noise bipolar silicon (Si) and silicon germanium: carbon (SiGe:C) transistors for satellite digital audio radio service (SDARS) active antenna low noise amplifiers (LNAs). In this document, the transistor-based LNA schematics, printed circuit board (PCB) layouts and measurement results are shown. This document is relevant to the following low-noise transistor:

- BFP450 SDARS LNA for 2320-2345 MHz
- BFP640ESD SDARS LNA for 2320-2345 MHz
- BFP650 SDARS LNA for 2320-2345 MHz
- BFP740F SDARS LNA for 2320-2345 MHz

Intended audience

This document is intended for engineers who need to design active antenna LNA for SDARS applications.

Table of contents

Table of contents

1 Introduction

1.1 SDARS active antenna LNA

SDARS is a digitally encoded satellite radio. The signals are broadcasted from satellites to earth-based receivers directly or via repeater stations operating in the S-band from 2320–2332.5 MHz and 2332.5–2345 MHz. SDARS provides paying subscribers with over 175 channels of "MP3-quality" digital radio wherever they are, in their vehicle or at home.

An SDARS system utilizes dual transmitter broadcasting formats which comprise the simultaneous transmission of signals from both satellites and terrestrial transmitters. The satellite transmissions cover by far most of the geographic broadcast area. The terrestrial transmissions supplement the satellite coverage primarily in urban regions where the satellite signals may be obstructed by tall buildings and structures. An SDARS active antenna is necessary to provide good reception for both terrestrial and satellite signals. The active part of an SDARS active antenna is a cascaded chain of LNAs to achieve both the low noise figure and the high gain while maintaining high linearity. A general topology for the SDARS active antenna is shown in Figure 1. This application note presents Infineon low noise transistors which can be used for active antenna LNA in the SDARS receiver.

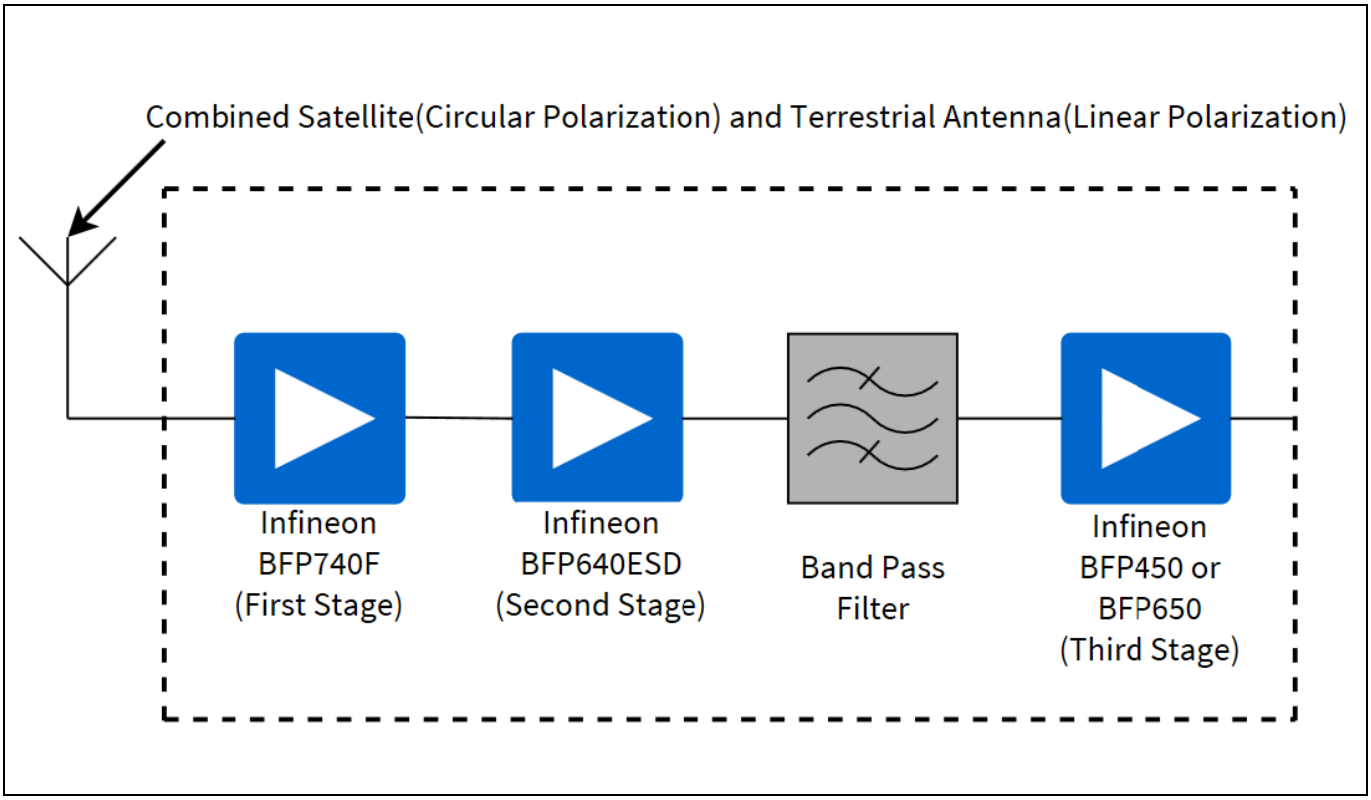

Figure 1 Block diagram example of the SDARS active antenna

1.2 Infineon RF transistor family

Infineon Technologies provides high-performance Radio-Frequency (RF) transistors targeting SDARS applications. Infineon's reliable high-volume RF transistors offer exceptionally low noise figure, high gain, and high linearity at low power consumption levels for RF applications. The fourth-generation transistor is based on bipolar Si technologies, and the sixth- and seventh-generation are based on robust ultra low-noise SiGe: C technologies. Their optimized inner transistor cell structures lead to best-in-class power gain and NF at SDARS operating frequency. The transistors maximize the design flexibility to customer requirements.

2 Application circuits and performance overview

2.1 SDARS active antenna 1st stage LNA

The LNA described in this section can be used for the active antenna 1st stage LNA in the SDARS receiver providing very low NF, higher gain, and high linearity.

2.1.1 Performance overview

The following table shows the performance of the SDARS LNA with RF low noise bipolar transistor BFP740F.

Table 1 Summary of measurement results for SDARS active antenna 1st stage LNA with BFP740F

Parameter	Symbol	Value			Unit	Notes
Device		BFP740F				
Bias voltage	V_{CC}	3.3			V	
Bias current	I_{CC}	12.9			mA	
Frequency	f	2320	2332.5	2345	MHz	
Gain	G	18.3	18.2	18.2	dB	
Noise figure	NF	0.71	0.7	0.68	dB	
Input return loss	RL_{in}	10.2	10.3	10.3	dB	
Output return loss	RL_{out}	11	10.9	10.8	dB	
Reverse isolation	ISO_{rev}	28	27.9	27.9	dB	
Output 1-dB compression point	OP_{1dB}	5.6			dBm	Measured at 2332.5 MHz
Output third-order intercept point	OIP_3	22.95			dBm	P_{IN} = -25 dBm per tone f_1 = 2331 MHz f_2 = 2332 MHz
Stability	K	>1				Measured from 15 MHz to 13 GHz

2.1.2 Schematic

The following figure presents the schematic of the SDARS active antenna 1st stage LNA with BFP740F. Emitter degeneration provides negative feedback to achieve the transistor impedance matching and low-noise matching at the same time. In the LNA circuit, resistors R1 and R2 stand for transistor voltage and current bias, meanwhile, they form a negative DC feedback mechanism to stabilize the transistor bias points in various conditions. Capacitors C2 and C3 serve as the RF bypass. The transistor input matching can be achieved by the capacitor C1 and the inductor L1. The output matching network is formed by L2, C4, C5, R3, and R4. Resistors R3 and R4 also support the improvement of circuit stability.

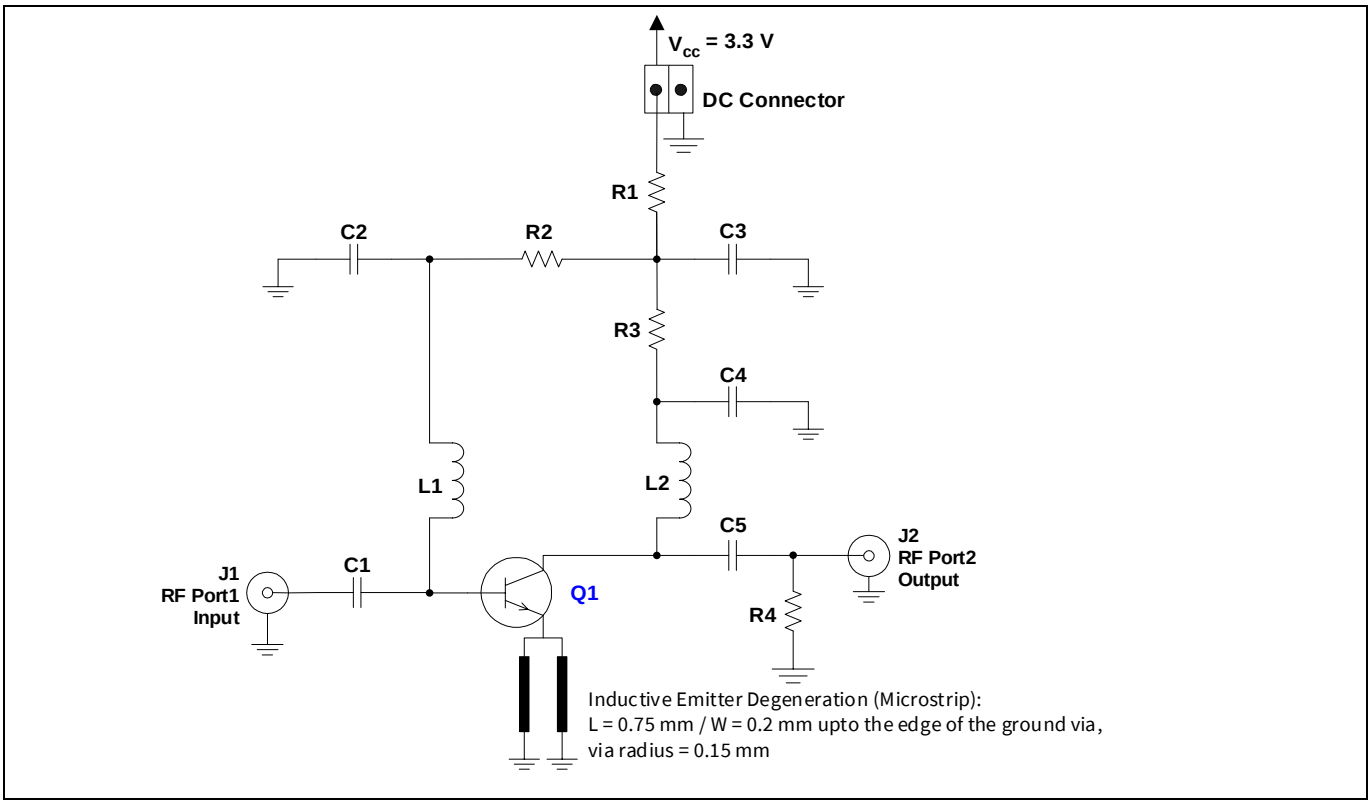

Figure 2 Schematic of the SDARS active antenna 1st stage LNA with BFP740F transistor

2.1.3 Bill of Materials (BOM)

Table 2 BOM of the SDARS active antenna 1st stage LNA with BFP740F transistor

Symbol	Value	Unit	Package	Manufacturer	Notes
Q1	BFP740F		TSFP-4	Infineon	SiGe: C low-noise transistor
C1	22	pF	0402	Various	Input matching and DC blocking
C2	220	nF	0402	Various	RF decoupling
C3	220	nF	0402	Various	RF decoupling
C4	3.3	pF	0402	Various	Output matching and stability improvement
C5	1.5	pF	0402	Various	Output matching and DC blocking
R1	30	Ω	0402	Various	DC biasing
R2	47	kΩ	0402	Various	Base DC biasing
R3	30	Ω	0402	Various	Low-frequency stability improvement
R4	240	Ω	0402	Various	Output matching and stability improvement
L1	10	nH	0402	Murata LQG	Input matching
L2	4.7	nH	0402	Murata LQG	Output matching

2.1.4 Evaluation board and PCB layout information

The evaluation board for the SDARS active antenna 1st stage LNA with BFP740F transistor:

- PCB material: FR4
- PCB marking: M100511

The photo of the evaluation board for the SDARS active antenna 1st stage LNA with BFP740F and the detailed description of the PCB stack are shown in the following figures.

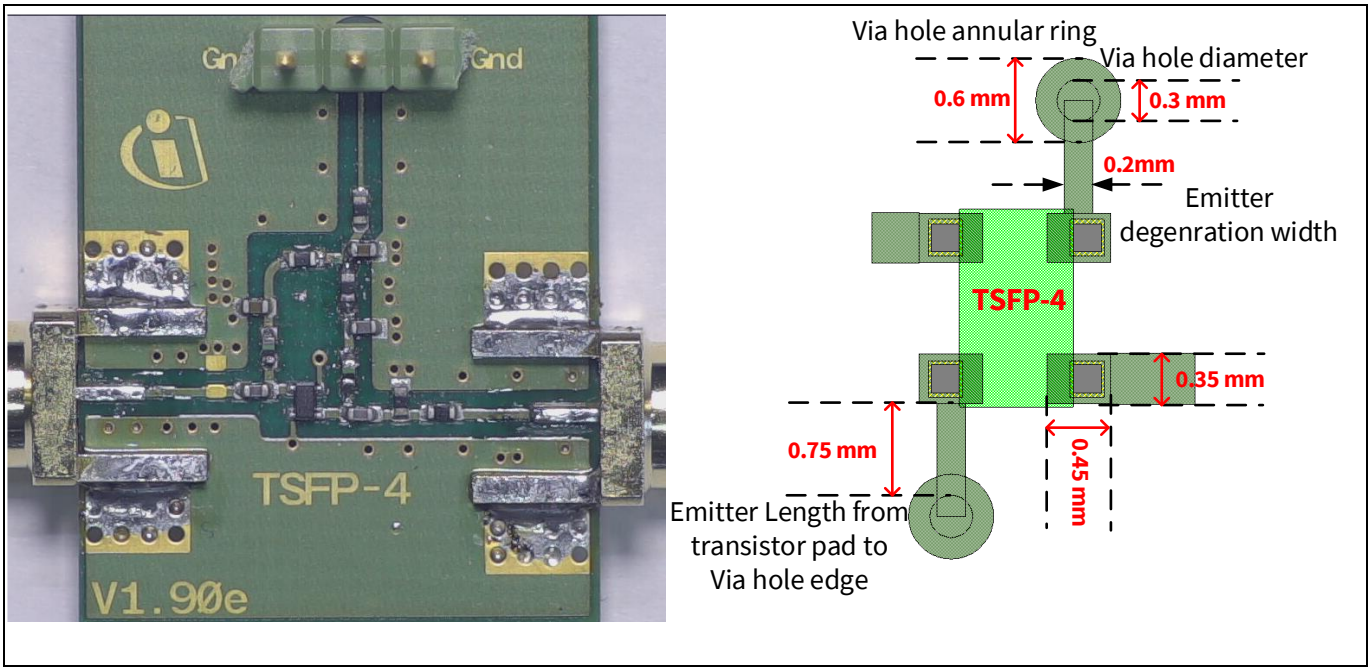

Figure 3 Photo of the evaluation board with PCB marking M100511 (left) and emitter degeneration details (right)

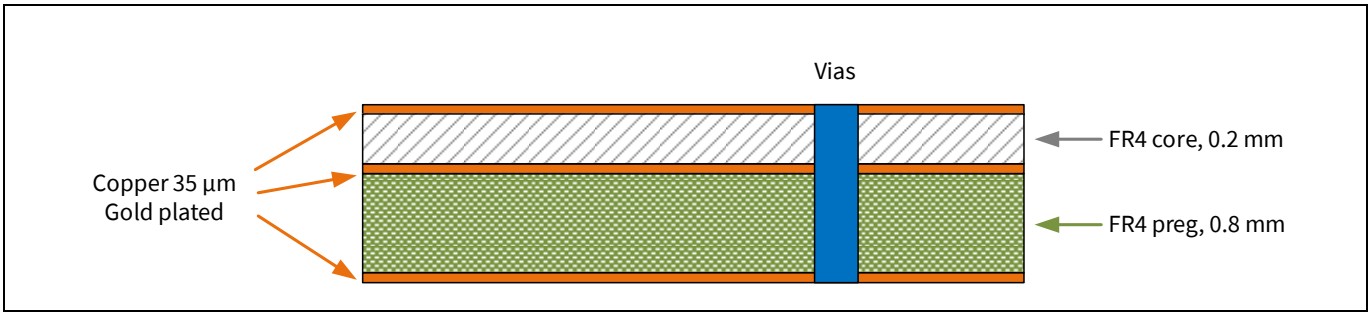

Figure 4 PCB stack information for the evaluation board with PCB marking M100511

2.1.5 Measurement results of the SDARS active antenna 1st stage LNA[1)]

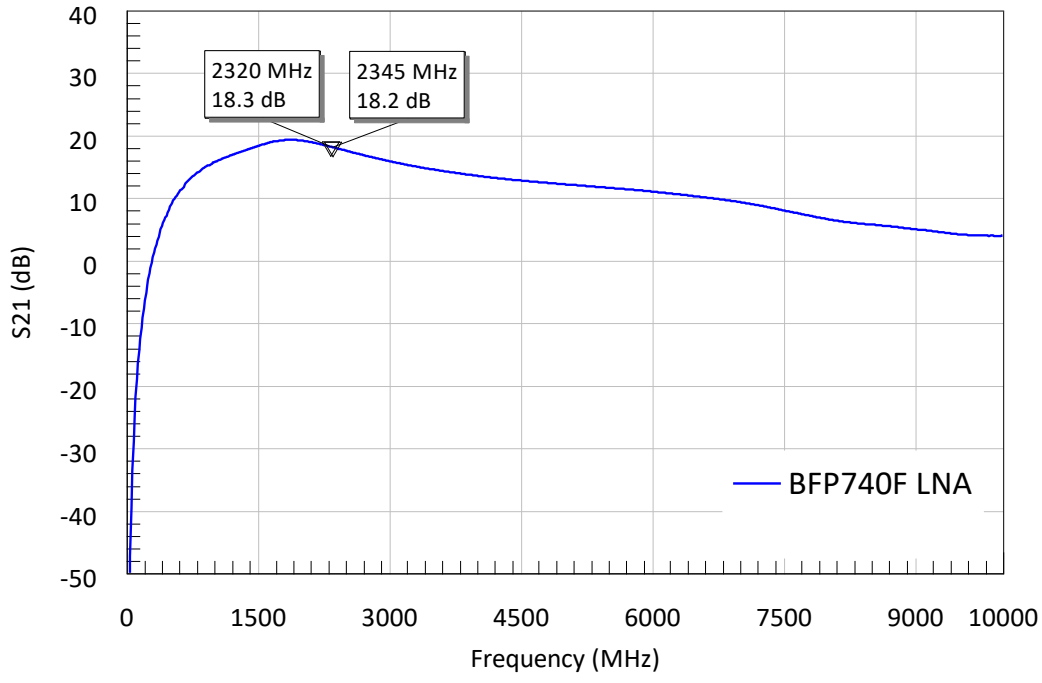

Figure 5 Small signal gain of the SDARS active antenna 1st stage LNA with BFP740F transistor

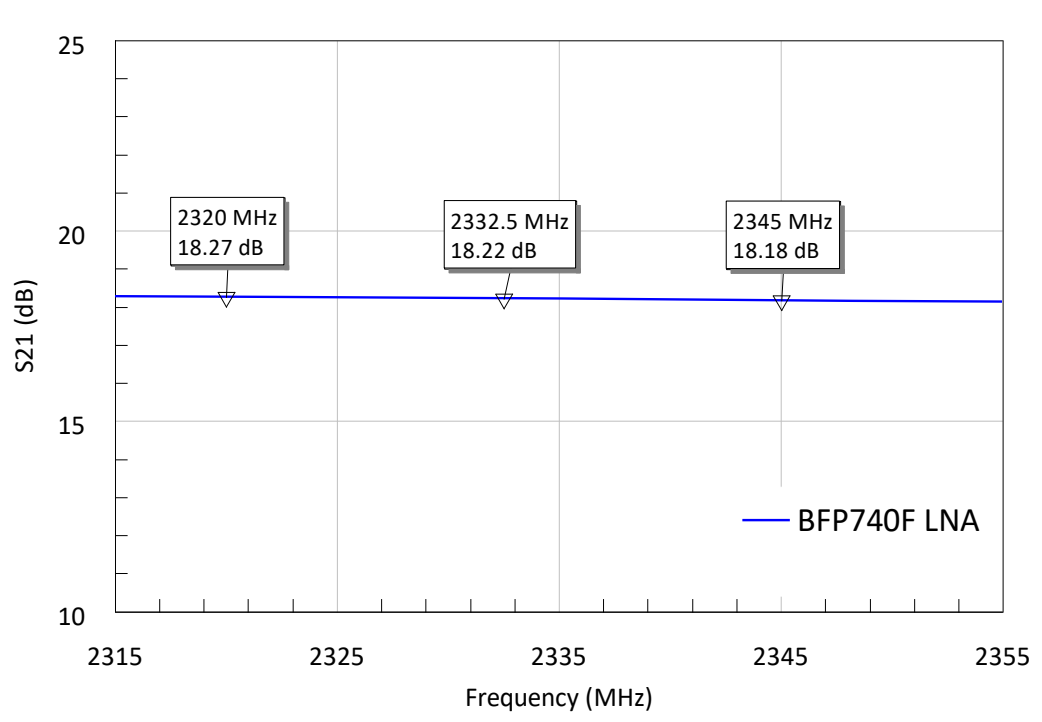

Figure 6 Small signal gain of the SDARS active antenna 1st stage LNA with BFP740F transistor (detail view)

Note: 1) The graphs are generated with the AWR electronic design automation (EDA) software Microwave Office®.

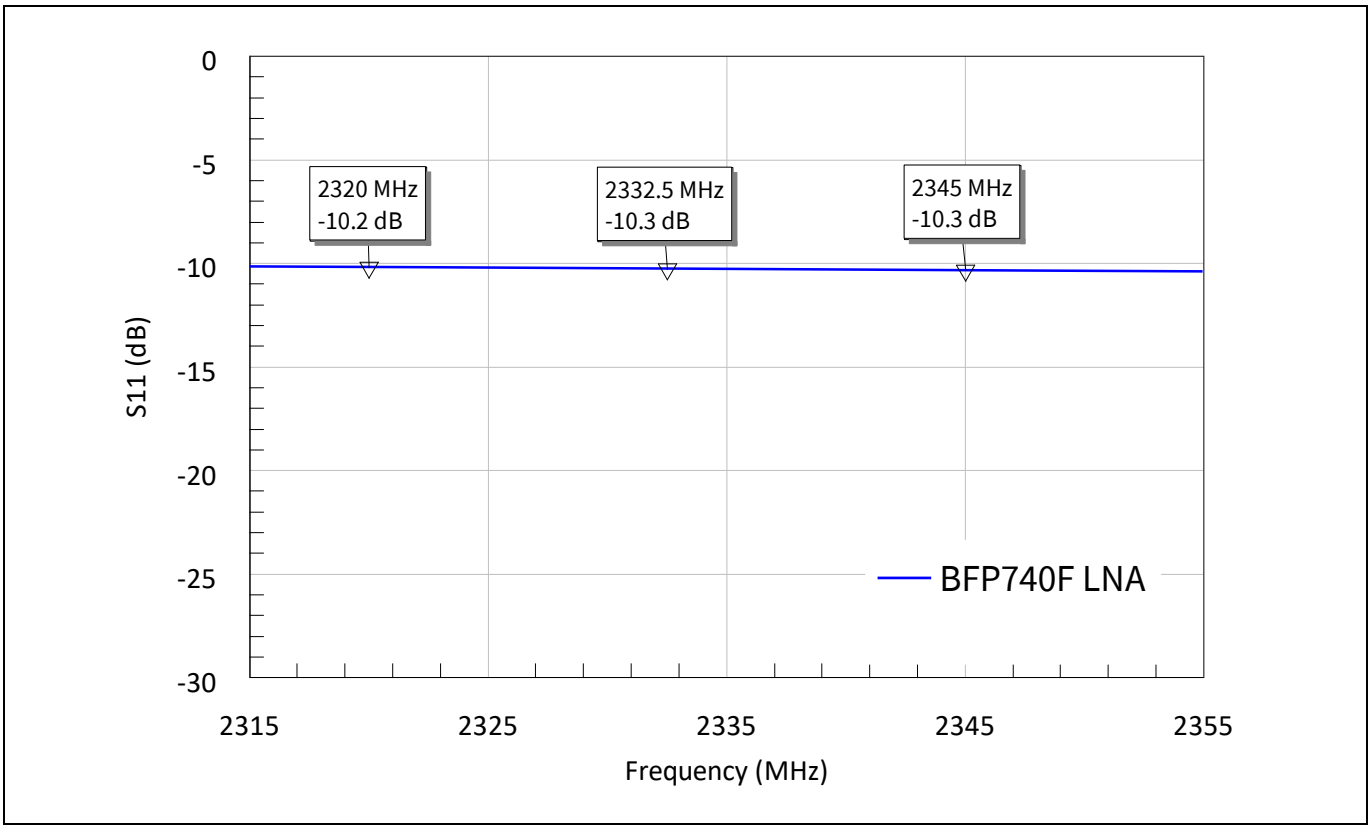

Figure 7 **Input return loss measurement of the SDARS active antenna 1st stage LNA with BFP740F transistor**

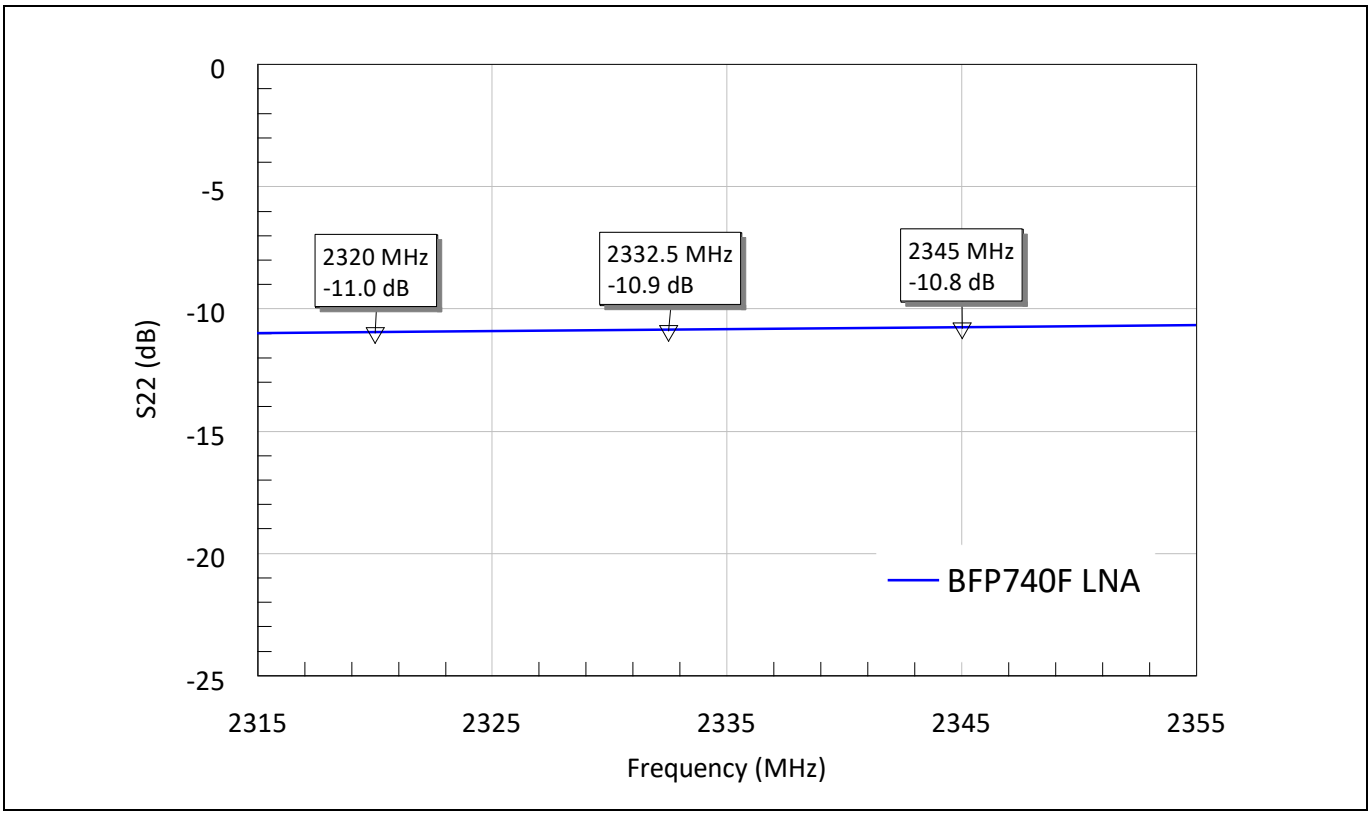

Figure 8 **Output return loss measurement of the SDARS active antenna 1st stage LNA with BFP740F transistor**

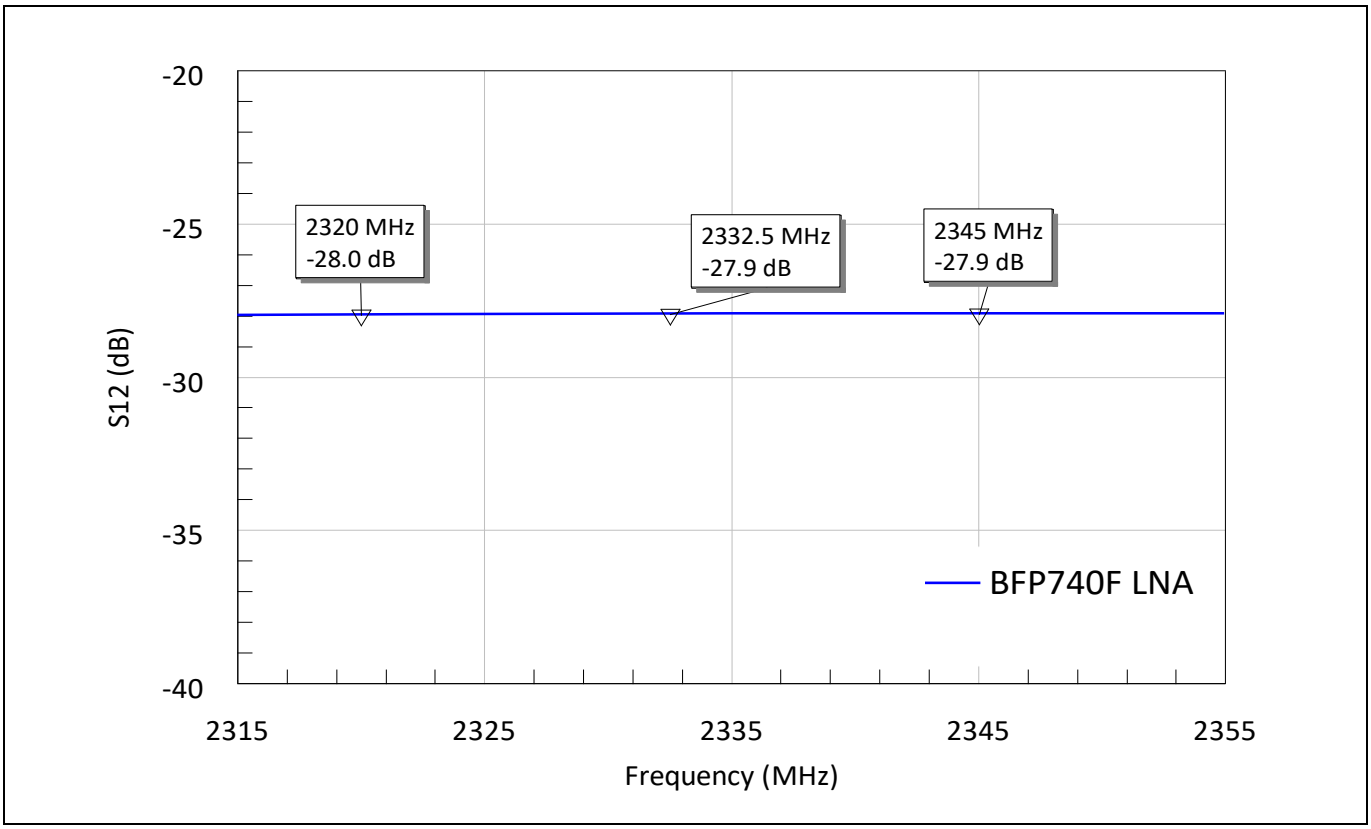

Figure 9 **Reverse isolation measurement of the SDARS active antenna 1st stage LNA with BFP740F transistor**

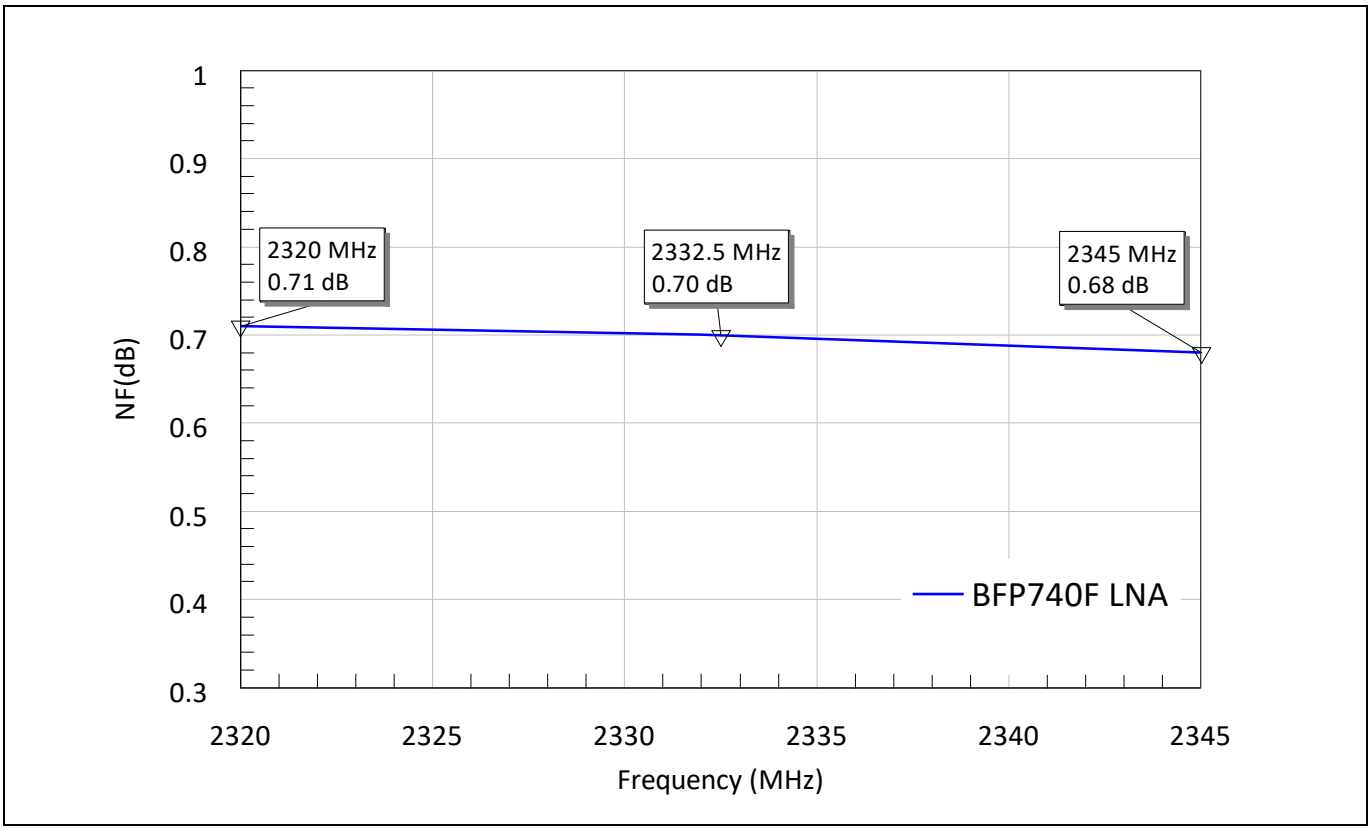

Figure 10 **Noise figure measurement of the SDARS active antenna 1st stage LNA with BFP740F transistor**

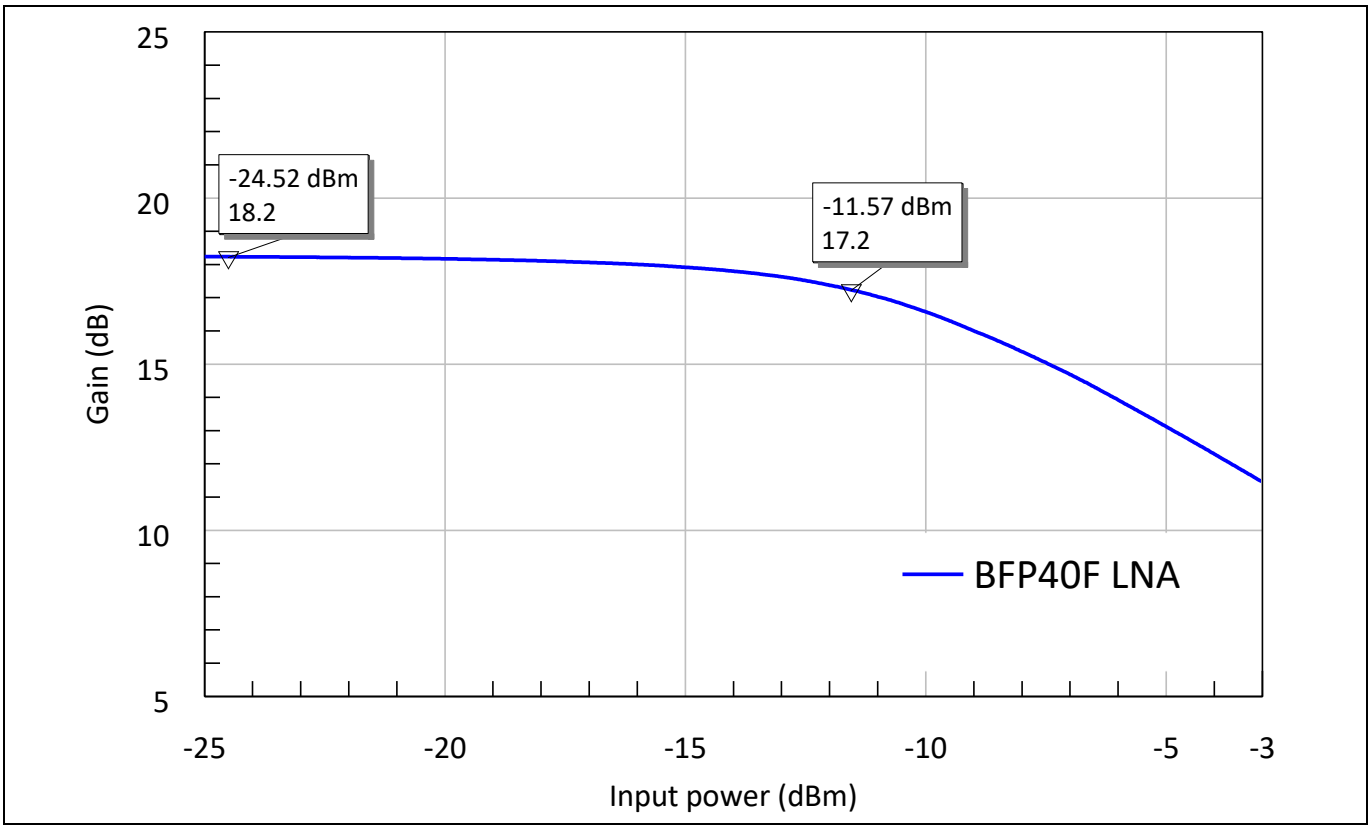

Figure 11 **Input 1-dB compression point measurement of SDARS active antenna 1st stage LNA with BFP740F transistor**

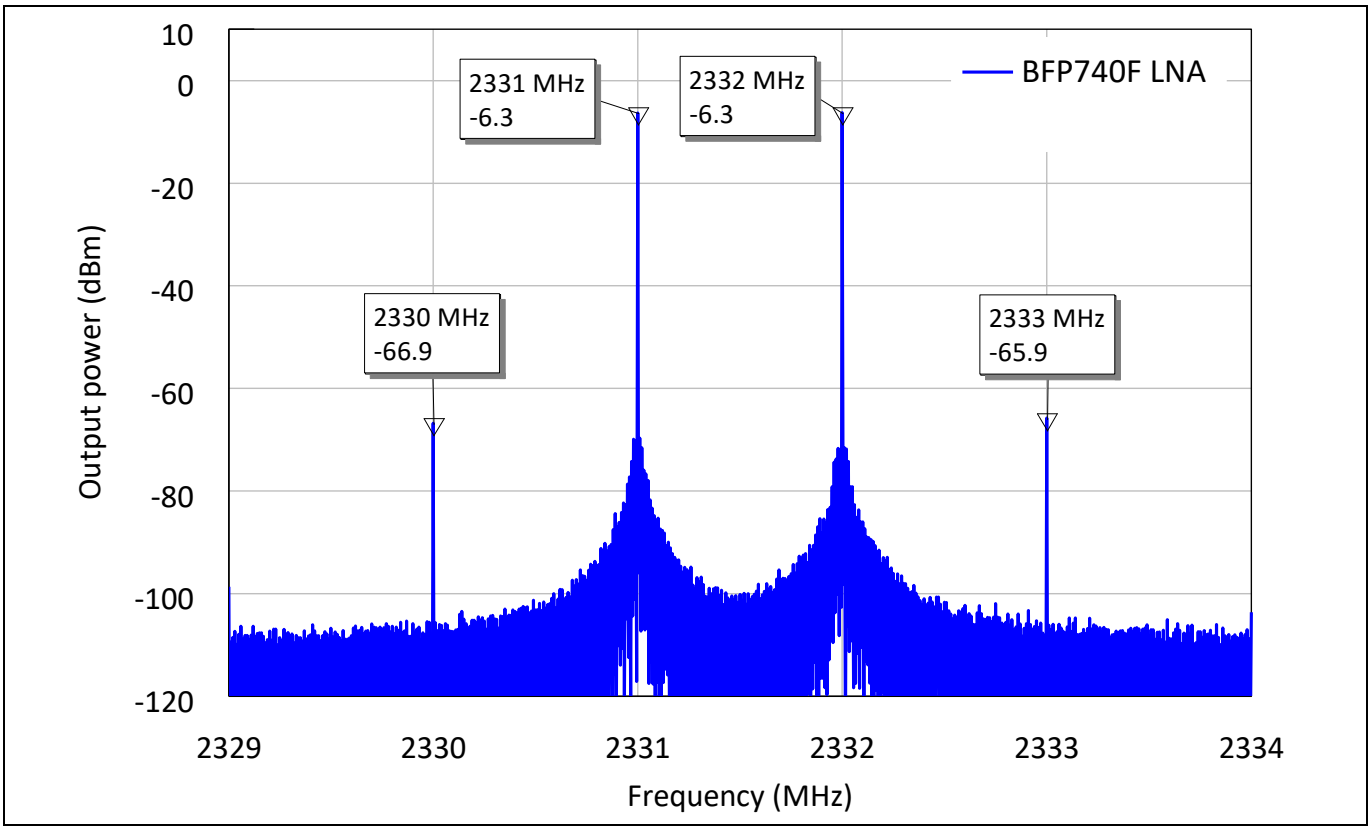

Figure 12 **3rd order Intermodulation distortion measurement of SDARS active antenna 1st stage LNA with BFP740F**

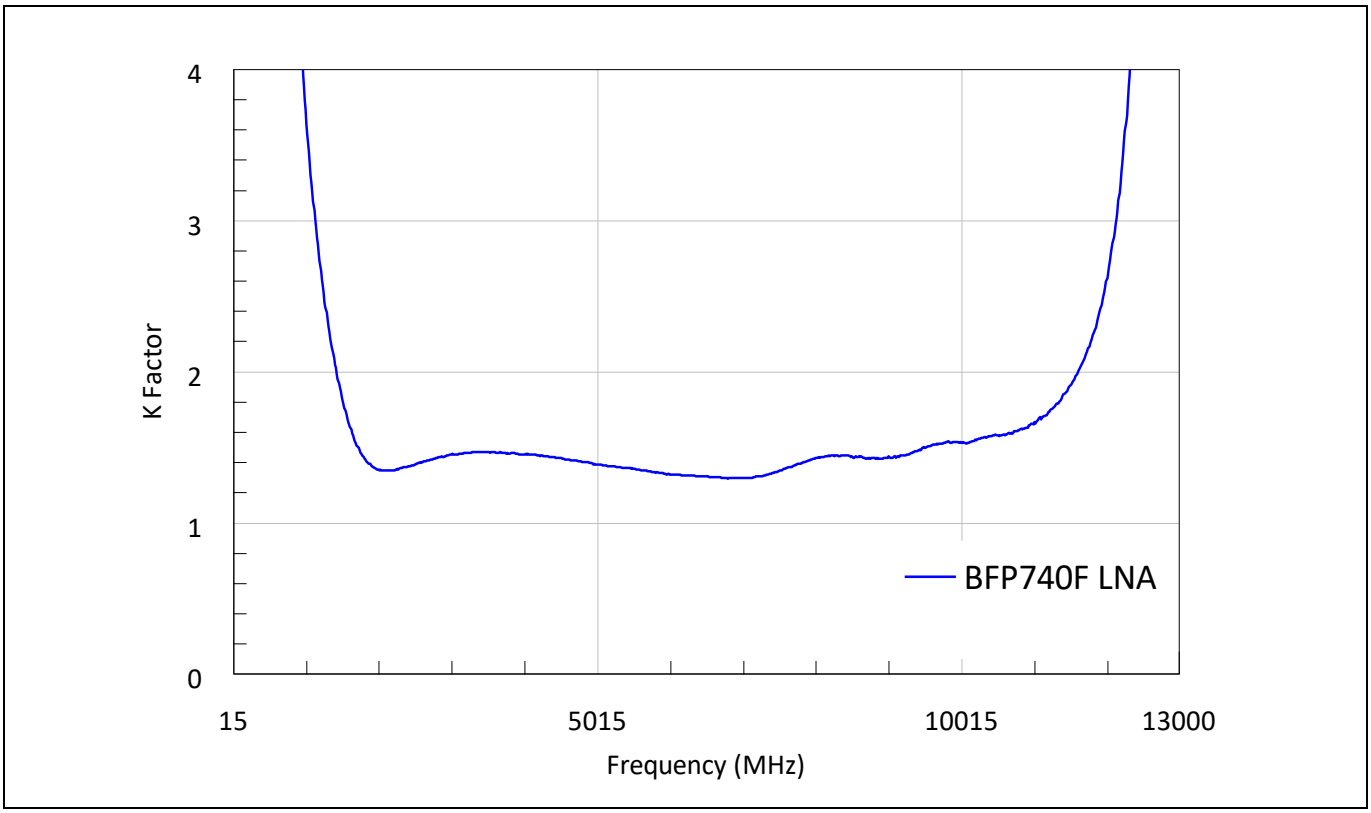

Figure 13 Stability K factor plot of the SDARS active antenna 1st stage LNA with BFP740F transistor

2.2 SDARS active antenna 2nd stage LNA

The LNA described in this section can be used for the active antenna 2nd stage LNA in the SDARS receiver which provides low NF and high linearity.

2.2.1 Performance overview

The following table shows the performance of the SDARS 2nd stage LNA with RF low-noise bipolar transistor BFP640ESD.

Table 3 Summary of measurement results for the SDARS 2nd stage LNA with BFP640ESD

Parameter	Symbol	Value			Unit	Notes
Device		BFP640ESD				
Bias voltage	V_{CC}	3.3			V	
Bias current	I_{CC}	23.6			mA	
Frequency	f	2320	2332.5	2345	MHz	
Gain	G	18.8	18.7	18.7	dB	
Noise figure	NF	1.0	1.0	1.0	dB	
Input return loss	RL_{in}	11.8	11.9	12.1	dB	
Output return loss	RL_{out}	16.8	16.4	16	dB	
Reverse isolation	ISO_{rev}	23.6	23.6	23.5	dB	
Output 1-dB compression point	OP_{1dB}	13.4			dBm	Measured at 2332.5 MHz
Output third-order intercept point	OIP_3	30.1			dBm	P_{IN} = -20 dBm per tone f_1 = 2332 MHz f_2 = 2333 MHz
Stability	K	>11				Measured from 100 MHz to 13 GHz

2.2.2 Schematic

The following figure presents the schematic of the SDARS active antenna 2nd stage LNA with BFP640ESD. Emitter degeneration provides negative feedback to achieve the transistor impedance matching and low-noise matching at the same time. In the LNA circuit, resistors R1 and R3 stand for transistor voltage and current bias, meanwhile, they form a negative DC feedback mechanism to stabilize the transistor bias points in various conditions. Capacitors C2, C3, and C4 serve as RF bypass. The transistor input matching can be achieved by the capacitor C1 and the inductor L1. The output matching network is formed by L2, C5, C6, and R3. Resistor R3 also supports the improvement of circuit stability.

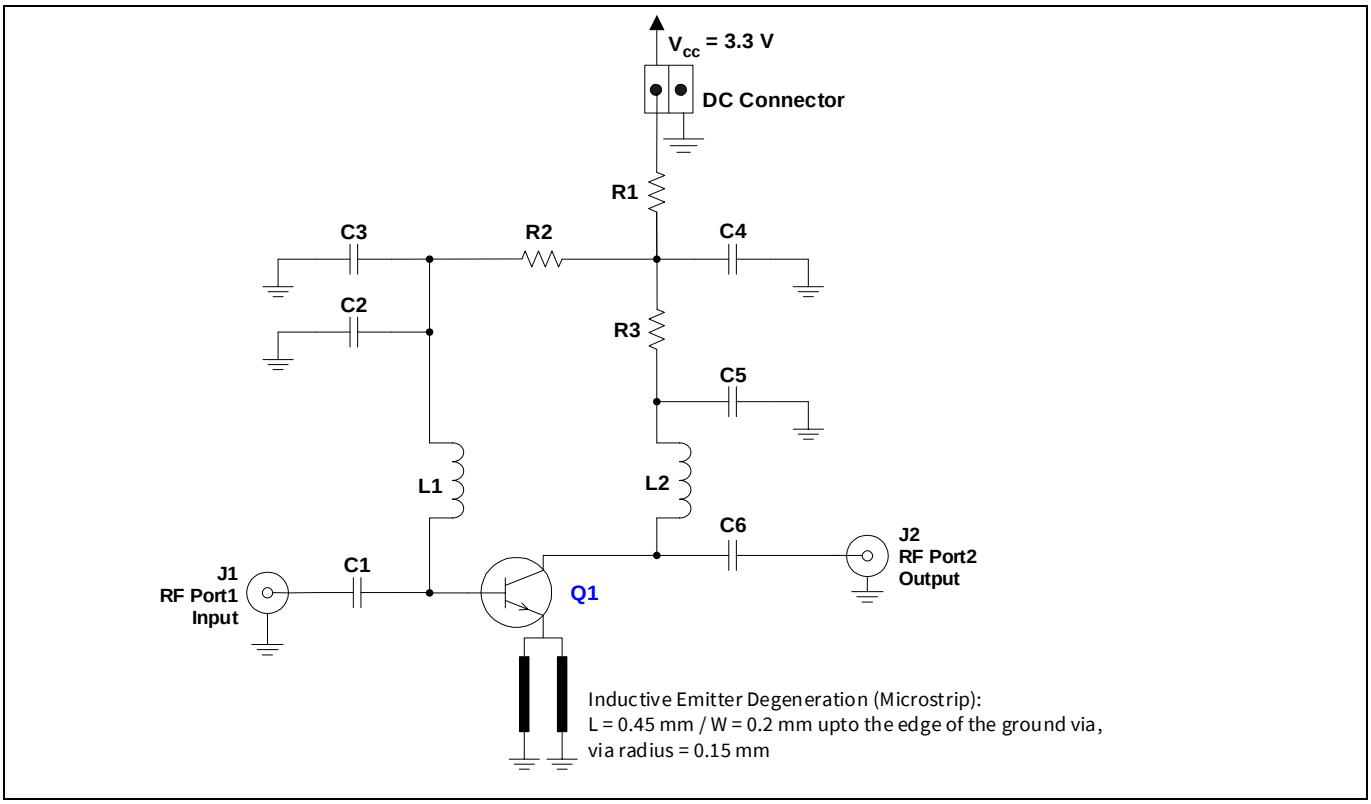

Figure 14 Schematic of the SDARS active antenna 2nd stage LNA with BFP640ESD transistor

2.2.3 Bill of Materials (BOM)

Table 4 BOM of the SDARS active antenna 2nd stage LNA with BFP640ESD transistor

Symbol	Value	Unit	Package	Manufacturer	Notes
Q1	BFP640ESD		SOT343	Infineon	SiGe: C low noise transistor
C1	8.2	pF	0402	Various	Input matching and DC blocking
C2	8.2	pF	0402	Various	RF Decoupling
C3	220	nF	0402	Various	RF decoupling
C4	220	nF	0402	Various	RF decoupling
C5	8.2	pF	0402	Various	Output matching and stability improvement
C6	1.5	pF	0402	Various	Output matching and DC blocking
R1	9.1	Ω	0402	Various	DC biasing
R2	20	kΩ	0402	Various	Base DC biasing
R3	2.2	Ω	0402	Various	Low-frequency stability improvement
L1	15	nH	0402	Murata LQG	Input matching
L2	3.0	nH	0402	Murata LQG	Output matching

2.2.4 Evaluation board and PCB layout information

The evaluation board for the SDARS active antenna 2nd stage LNA with BFP640ESD transistor:

- PCB material: FR4
- PCB marking: M11118

The photo of the evaluation board for the SDARS active antenna 2nd stage LNA with BFP640ESD and the detailed description of the PCB stack are shown in the following figures.

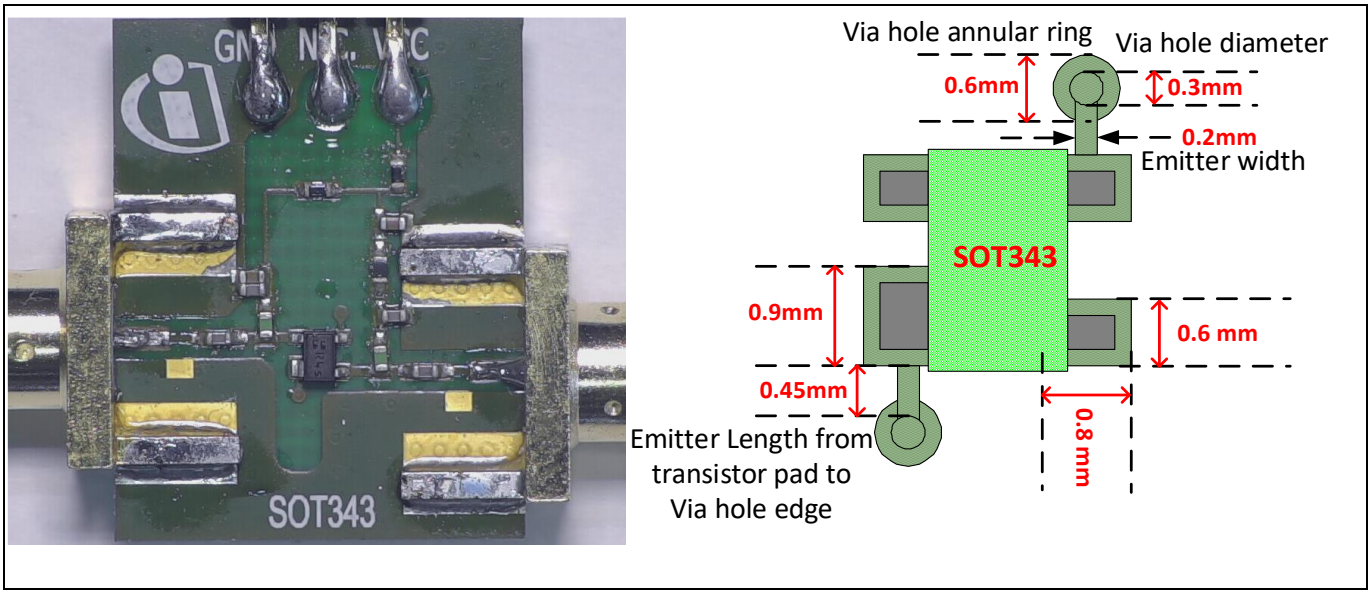

Figure 15 Photo of evaluation board with the PCB marking M11118 (left) and emitter degeneration details (right)

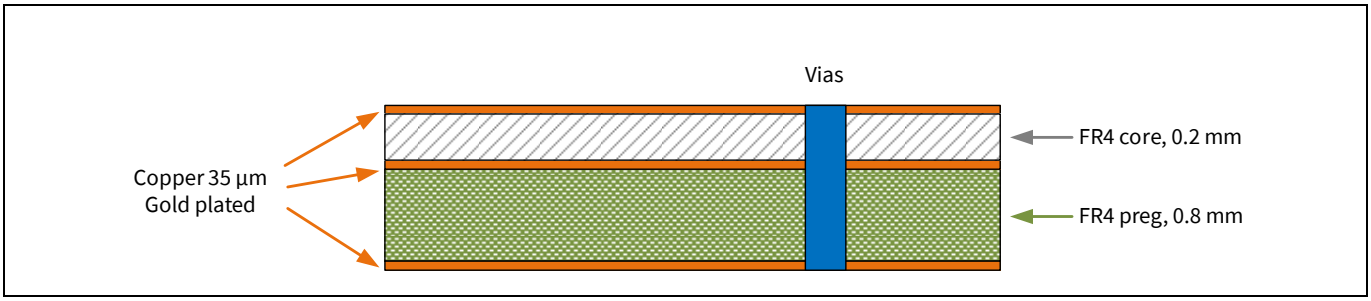

Figure 16 PCB stack information for the evaluation board with the PCB marking M11118

2.2.5 Measurement results of the SDARS active antenna 2nd stage LNA with BFP640ESD transistor[1)]

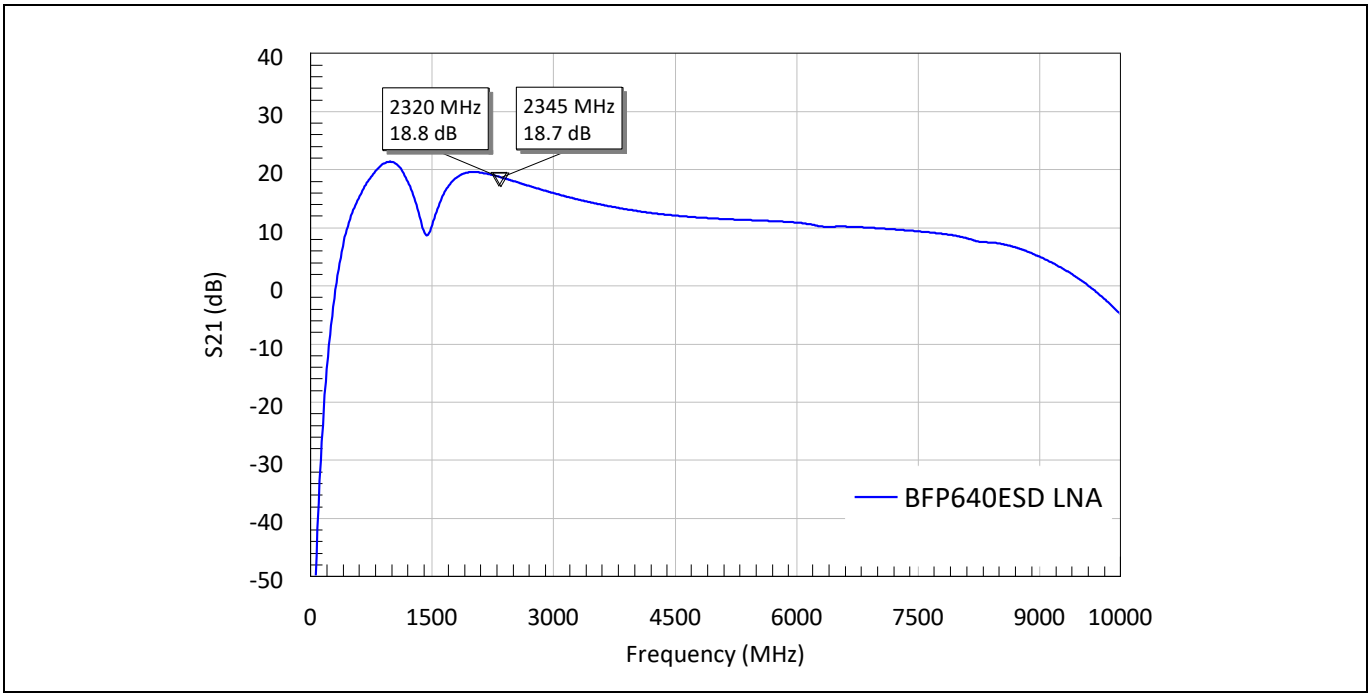

Figure 17 Small signal gain of the SDARS active antenna 2nd stage LNA with BFP640ESD transistor

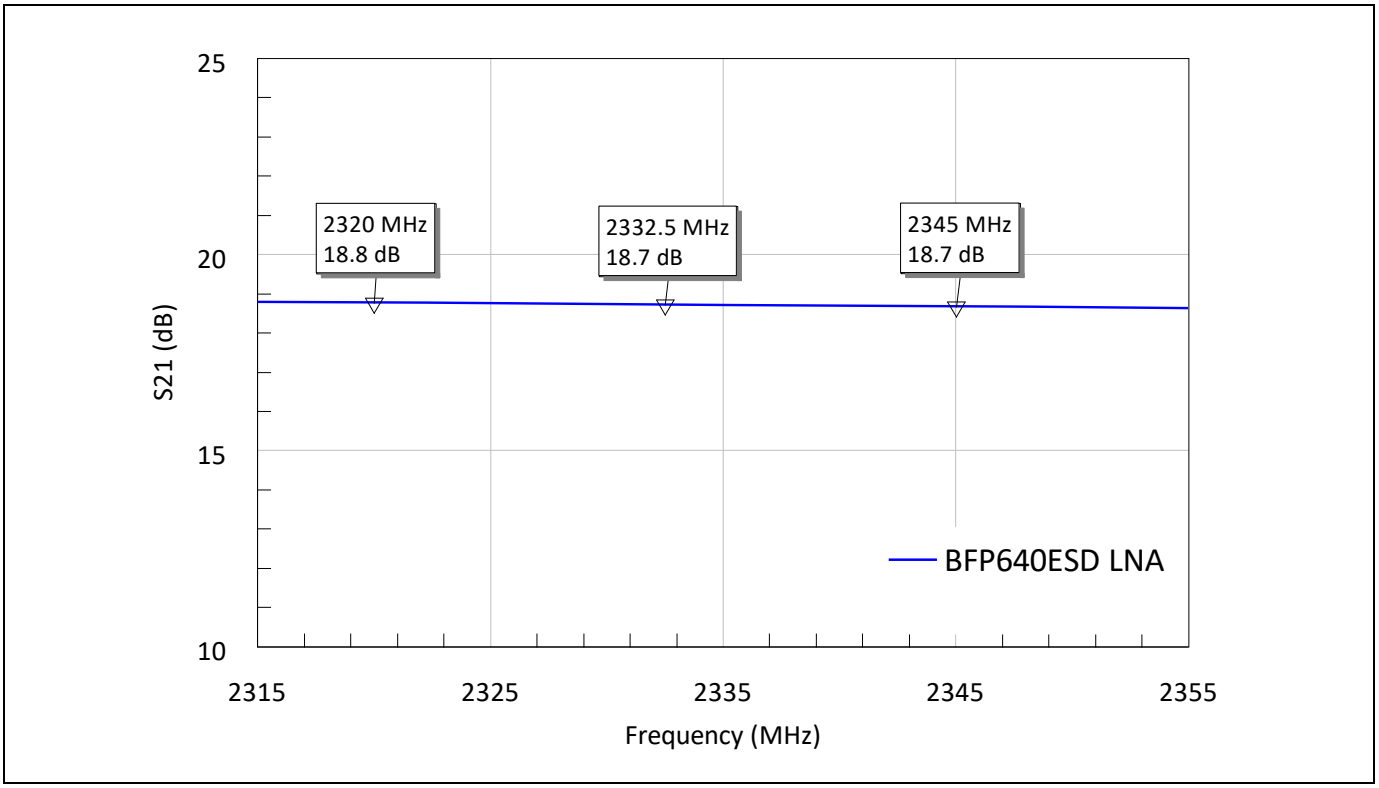

Figure 18 Small signal gain of the SDARS active antenna 2nd stage LNA with BFP640ESD transistor (detail view)

Note: 1) The graphs are generated with the AWR EDA software Microwave Office®.

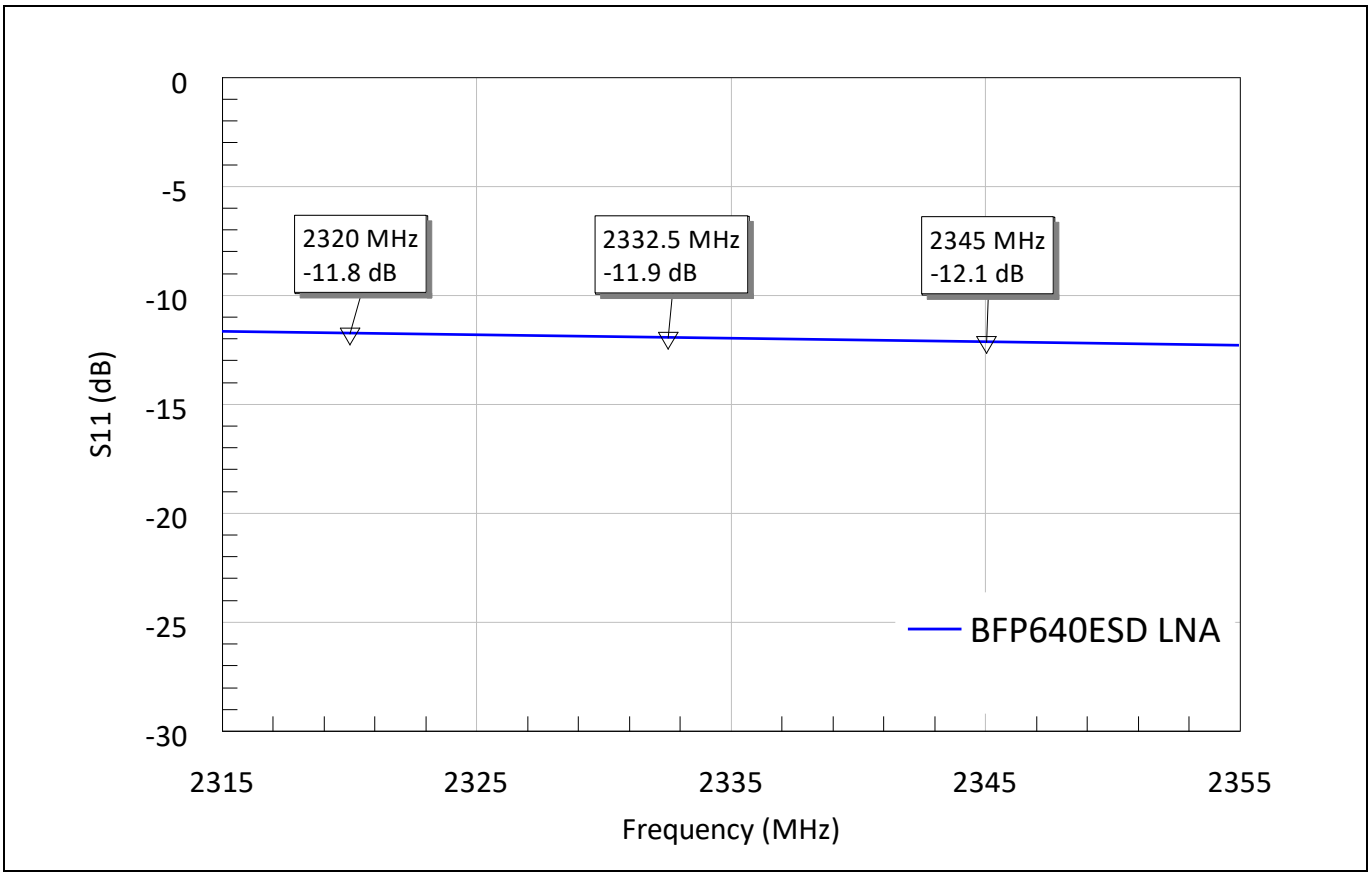

Figure 19 **Input return loss measurement of the SDARS active antenna 2nd stage LNA with BFP640ESD transistor**

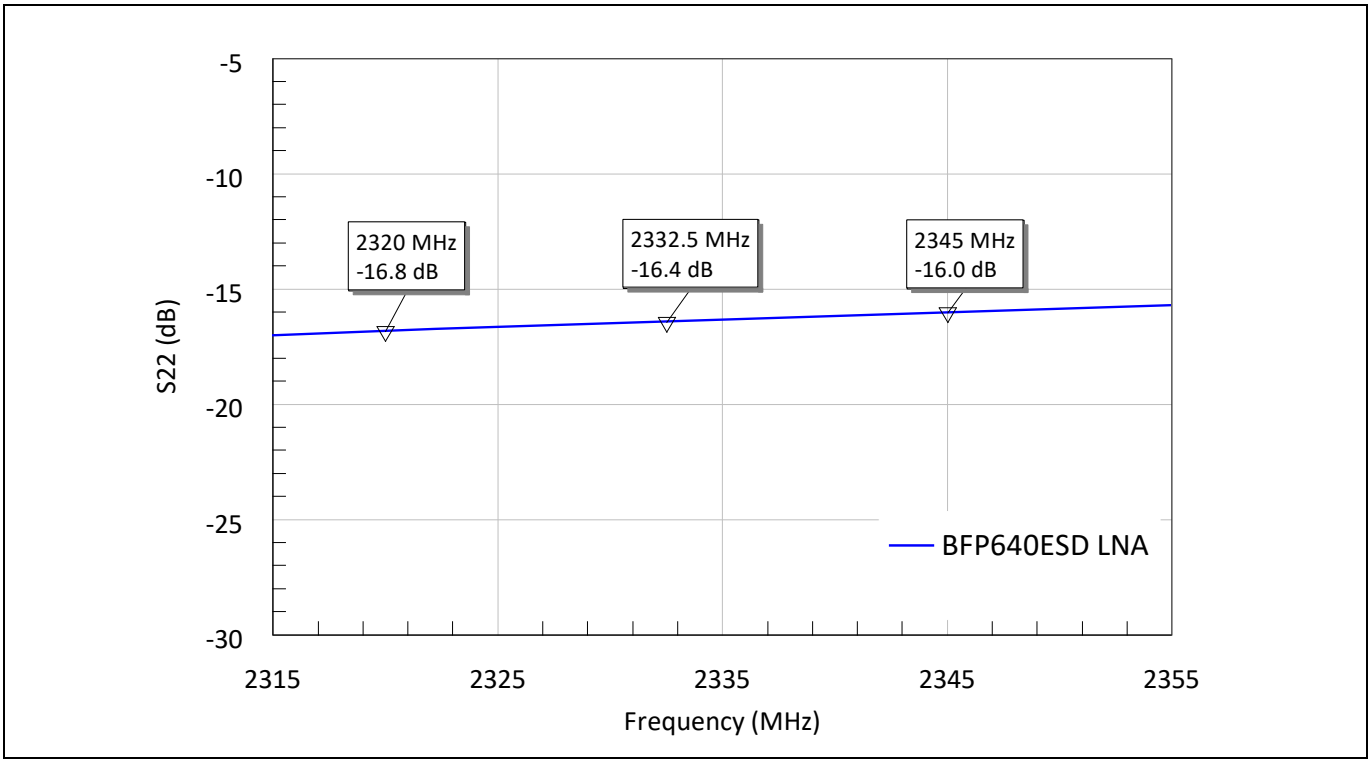

Figure 20 **Output return loss measurement of the SDARS active antenna 2nd stage LNA with BFP640ESD transistor**

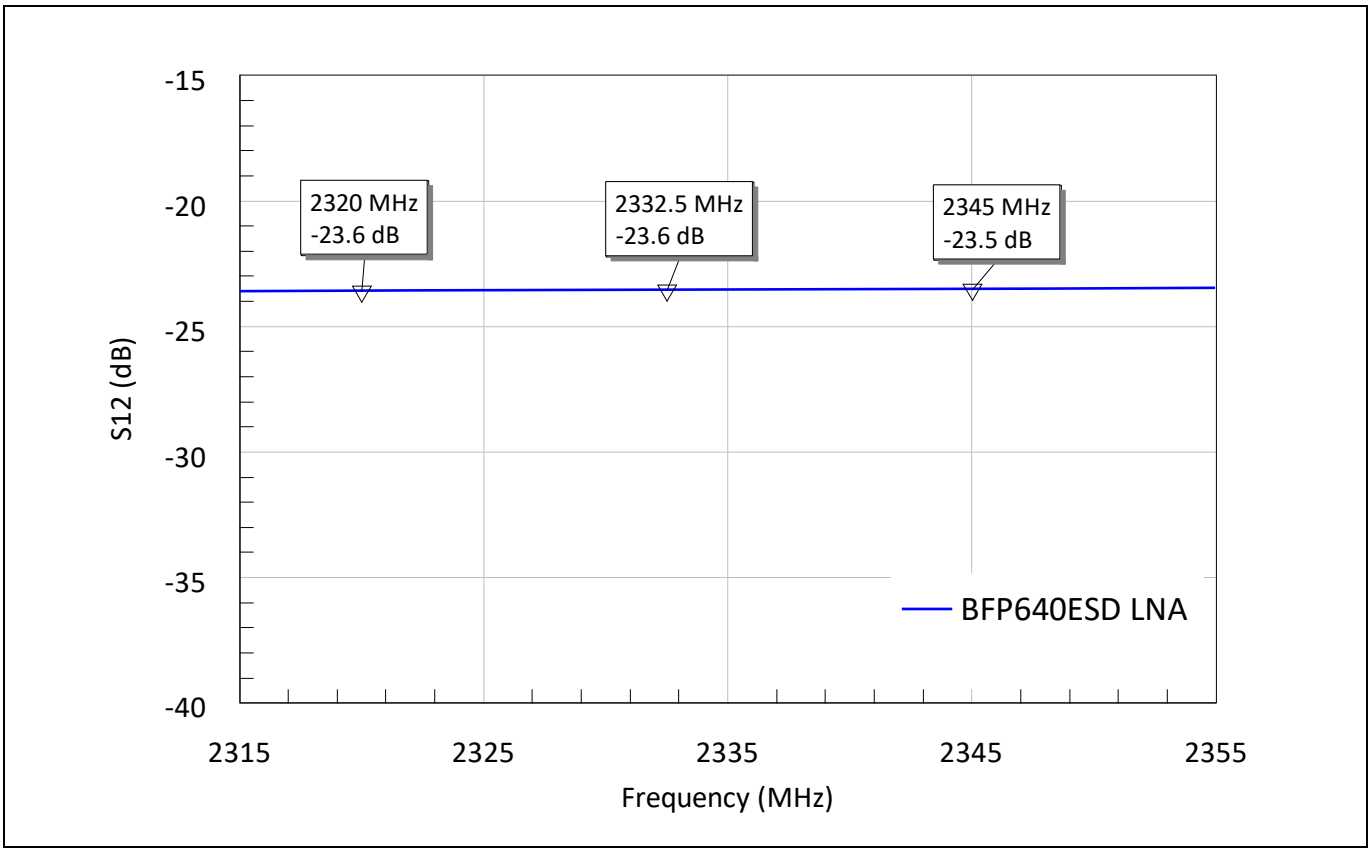

Figure 21 **Reverse isolation measurement of the SDARS active antenna 2nd stage LNA with BFP640ESD transistor**

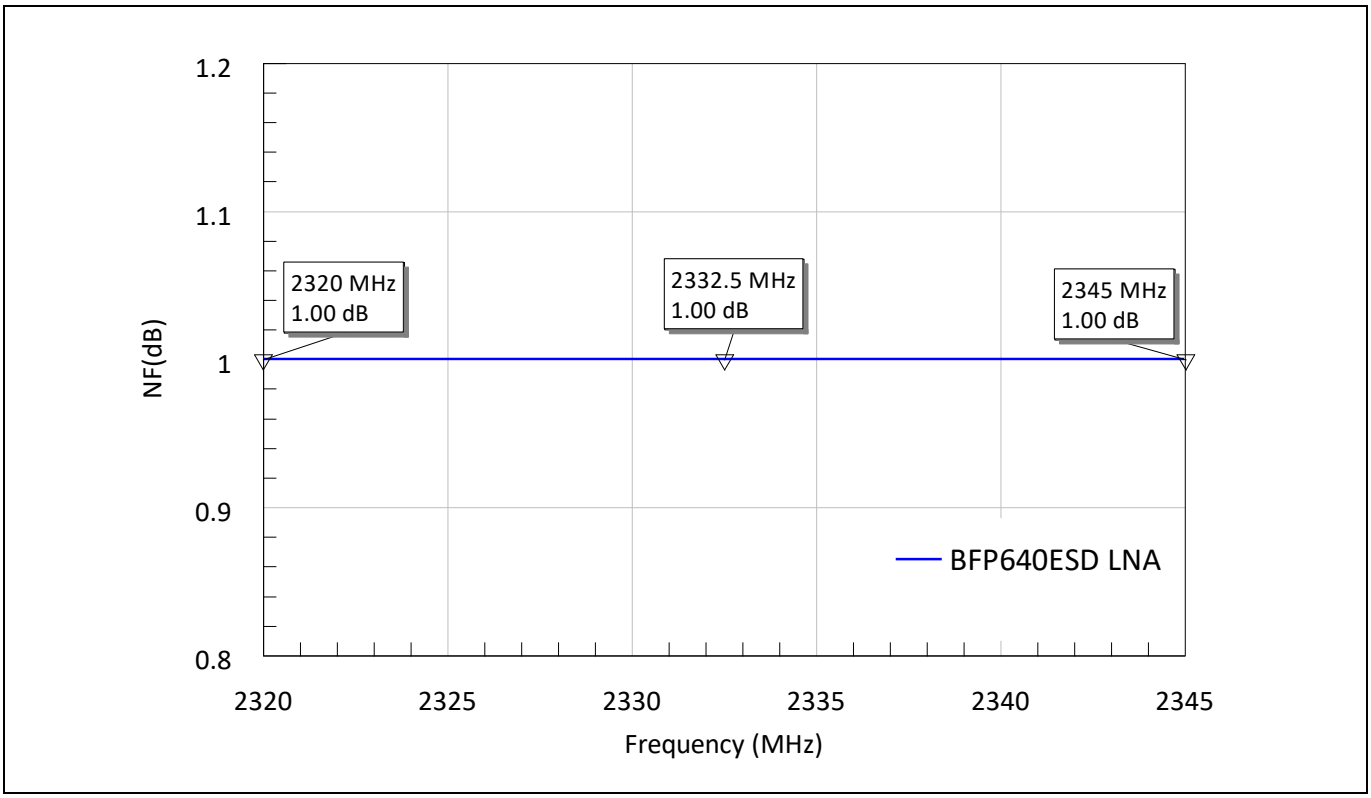

Figure 22 **Noise figure measurement of the SDARS active antenna 2nd stage LNA with BFP640ESD transistor**

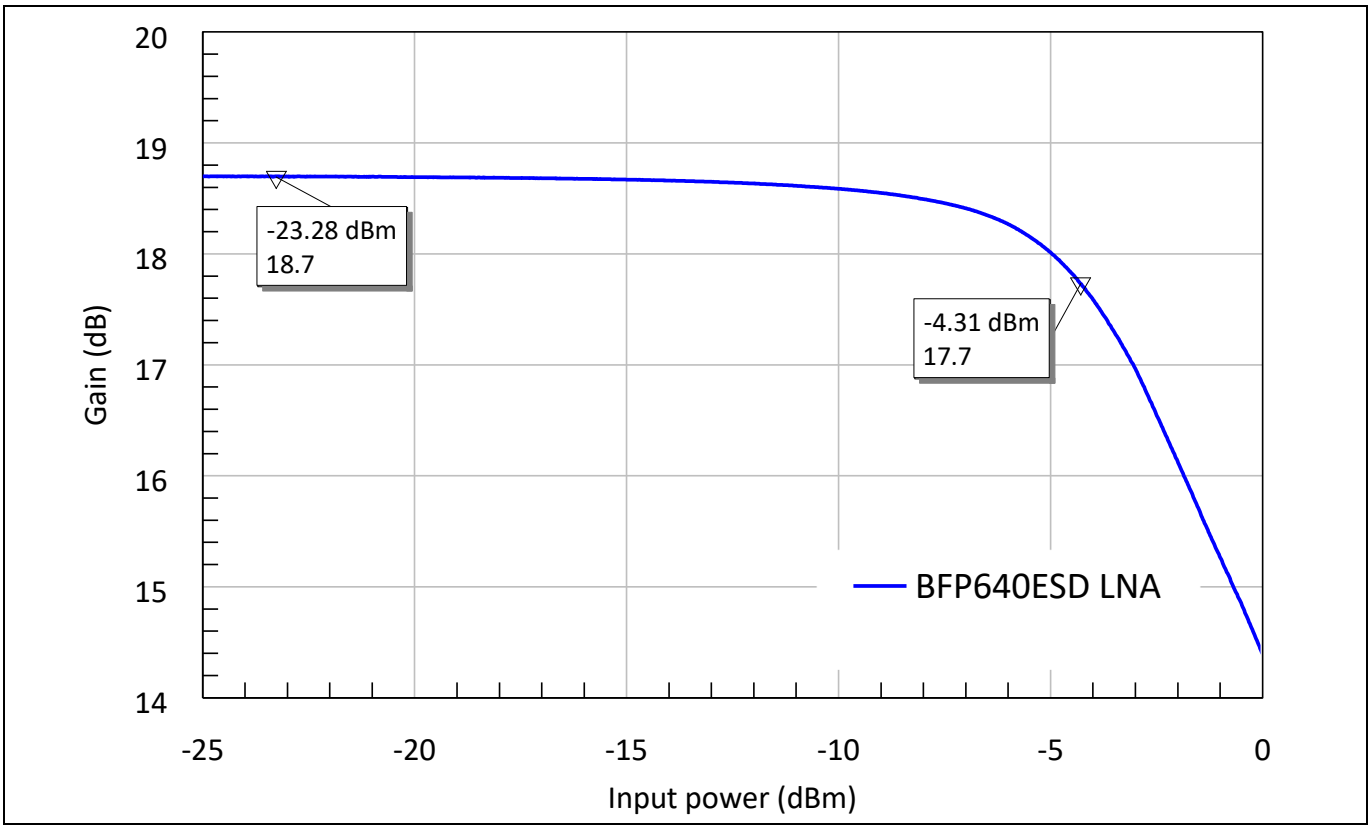

Figure 23 **Input 1-dB compression point measurement of the SDARS active antenna 2nd stage LNA with BFP640ESD transistor**

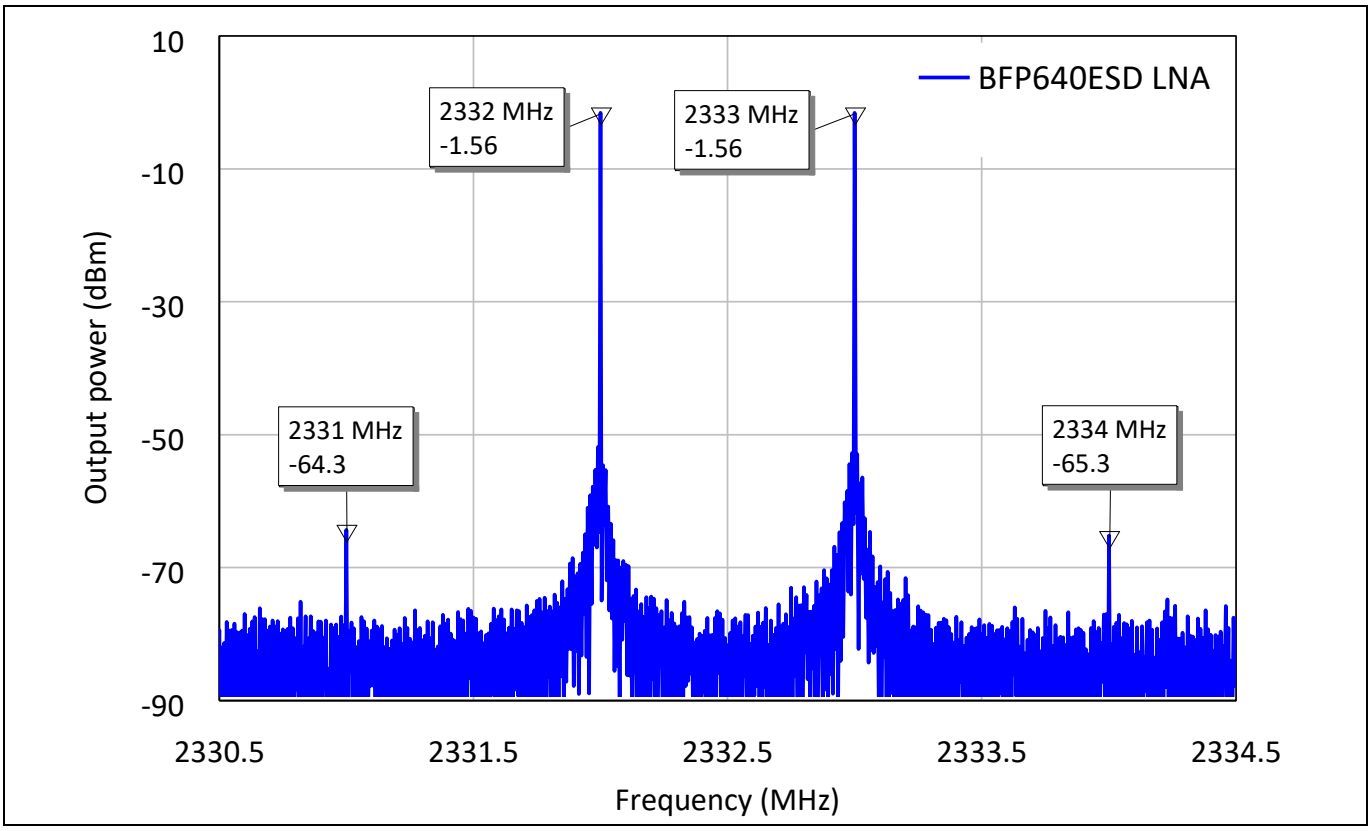

Figure 24 **3rd order Intermodulation distortion measurement of the SDARS active antenna 2nd stage LNA with BFP640ESD**

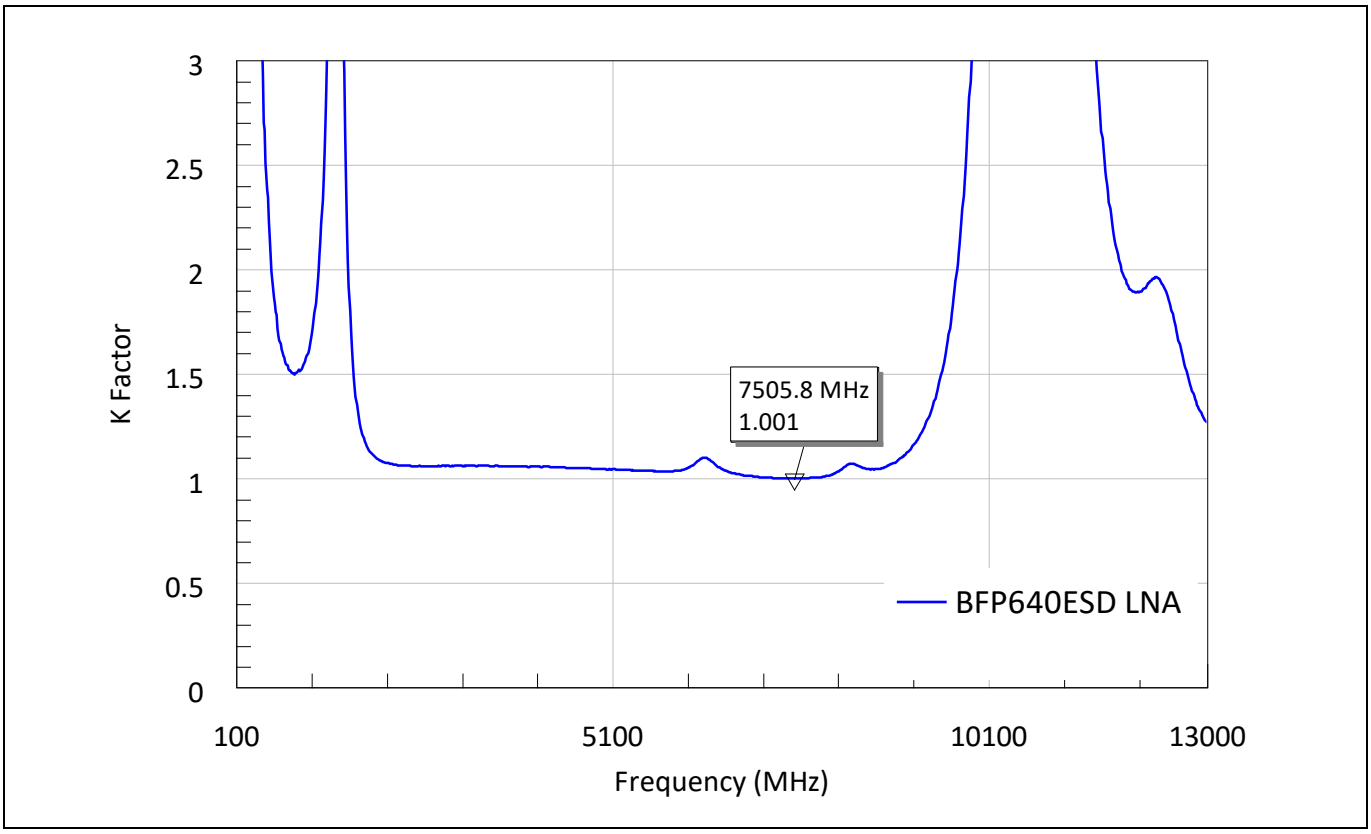

Figure 25 **Stability K factor plot of the SDARS active antenna 2nd stage LNA with BFP640ESD transistor**

2.3 SDARS active antenna 3rd stage LNA

The LNA described in this section can be used for the active antenna 3rd stage LNA in the SDARS receiver which provides very high linearity.

2.3.1 Performance overview

The following table shows the performance of the SDARS active antenna 3rd stage LNA with RF low-noise bipolar transistor BFP450 or BFP650.

Table 5 Summary of measurement results for the SDARS active antenna 3rd stage LNA with BFP450 or BFP650

Parameter	Symbol	Value						Unit	Notes
Device		BFP450			BFP650				
Bias voltage	V_{CC}	3.3			3.3			V	
Bias current	I_{CC}	88.2			57.2			mA	
Frequency	f	2320	2332.5	2345	2320	2332.5	2345	MHz	
Gain	G	10.3	10.3	10.3	14.3	14.2	14.2	dB	
Noise figure	NF	2.6	2.6	2.6	1.2	1.2	1.2	dB	
Input return loss	RL_{in}	10.4	10.7	11.1	14.8	14.6	14.4	dB	
Output return loss	RL_{out}	16	16.2	16.3	12.3	12	11.7	dB	
Reverse isolation	ISO_{rev}	16.4	16.4	16.3	18.3	18.3	18.3	dB	
Output 1-dB compression point	OP_{1dB}	17.81			17.37			dBm	Measured at 2332.5 MHz
Output third-order intercept point	OIP_3	32.78			30.2			dBm	P_{IN} = -10 dBm per tone f_1 = 2332 MHz f_2 = 2333 MHz
Stability	K	>1			>1				Measured from 100 MHz to 13 GHz

2.3.2 Schematic

The following figure presents the schematic of the SDARS active antenna 2nd stage LNA with BFP450 or BFP650. Emitter degeneration provides negative feedback to achieve the transistor impedance matching and low noise matching at the same time. In the LNA circuit, resistors R1 and R2 stand for transistor voltage and current bias, meanwhile, they form a negative DC feedback mechanism to stabilize the transistor bias points in various conditions. Capacitors C3, C4, and C5 serve as RF bypass. The transistor input matching can be achieved by C1, C2, C8, and L1. The output matching network is formed by C6, C7, R3, and L2. Resistor R3 also supports the improvement of circuit stability.

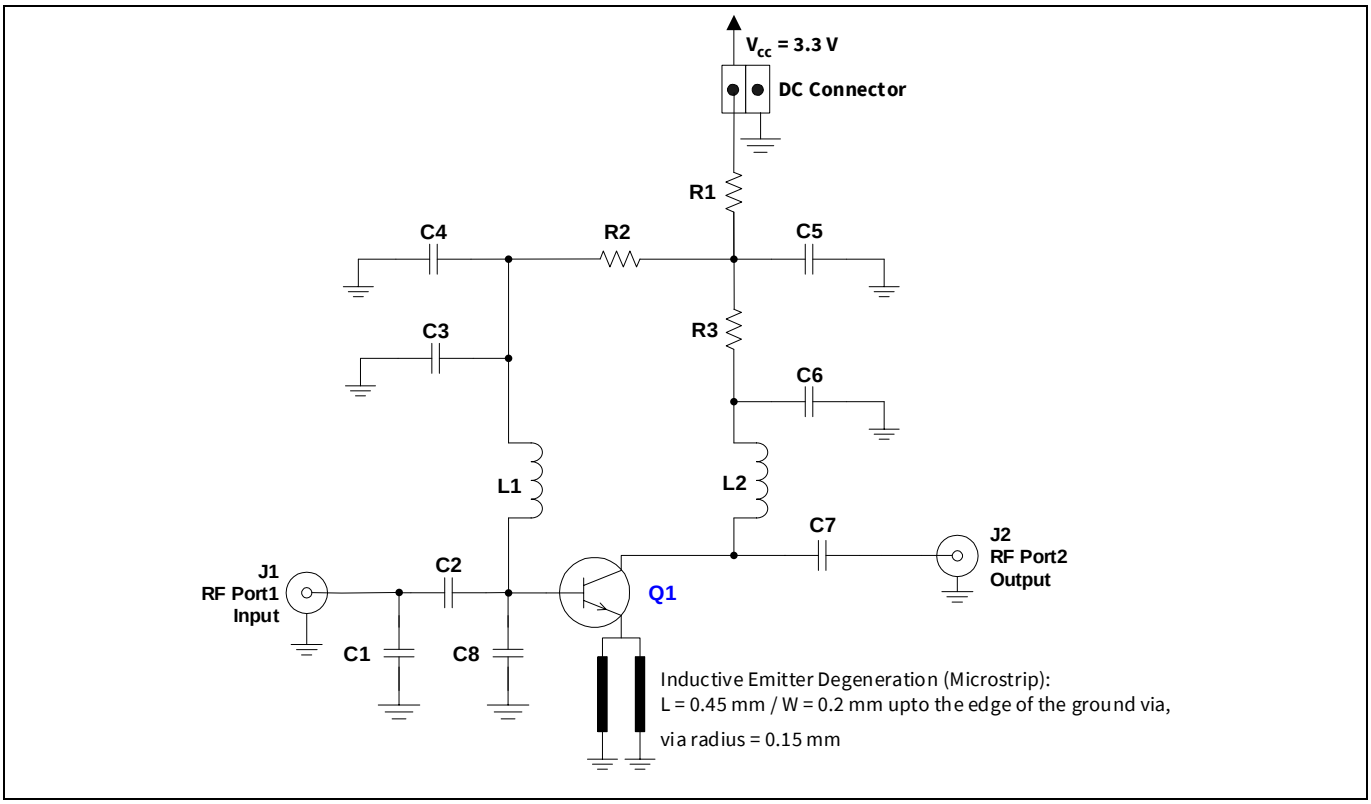

Figure 26 Schematic of the SDARS active antenna 3rd stage LNA s with BFP450 or BFP650

2.3.3 Bill of Materials (BOM)

Table 6 BOM of the SDARS active antenna 3rd stage LNAs with BFP450 or BFP650 transistor

Symbol	Value		Unit	Package	Manufacturer	Notes
Q1	BFP450	BFP650		SOT343	Infineon	BFP450-Si bipolar transistor and BFP650-SiGe: C low-noise transistor
C1	1	n.c.	pF	0402	Various	Input matching and DC blocking
C2	2.7		pF	0402	Various	Input matching and DC blocking
C3	8.2	8.2	pF	0402	Various	RF Decoupling
C4	220	220	nF	0402	Various	RF decoupling
C5	220	220	nF	0402	Various	RF decoupling
C6	8.2	8.2	pF	0402	Various	Output matching and stability improvement
C7	2.2	2.2	pF	0402	Various	Output matching and DC blocking
C8	n.c.[1)]	1	pF	0402	Various	Input matching and DC blocking
R1	4.3	5.1	Ω	0402	Various	DC biasing
R2	1.5	4.7	kΩ	0402	Various	Base DC biasing
R3	2.2	4.7	Ω	0402	Various	Low-frequency stability improvement
L1	12	12	nH	0402	Murata LQG	Input matching
L2	5.1	5.1	nH	0402	Murata LQG	Output matching

Note: 1) Not connected (n.c.).

2.3.4 Evaluation boards and PCB layout information

The evaluation board for the SDARS active antenna 3rd stage LNA with BFP450 and BFP650 transistor:

- PCB material: FR4
- PCB marking: M11118

The photo of the evaluation board for the SDARS active antenna 3rd stage LNA with BFP450 or BFP650 and the detailed description of the PCB stack are shown in the following figures.

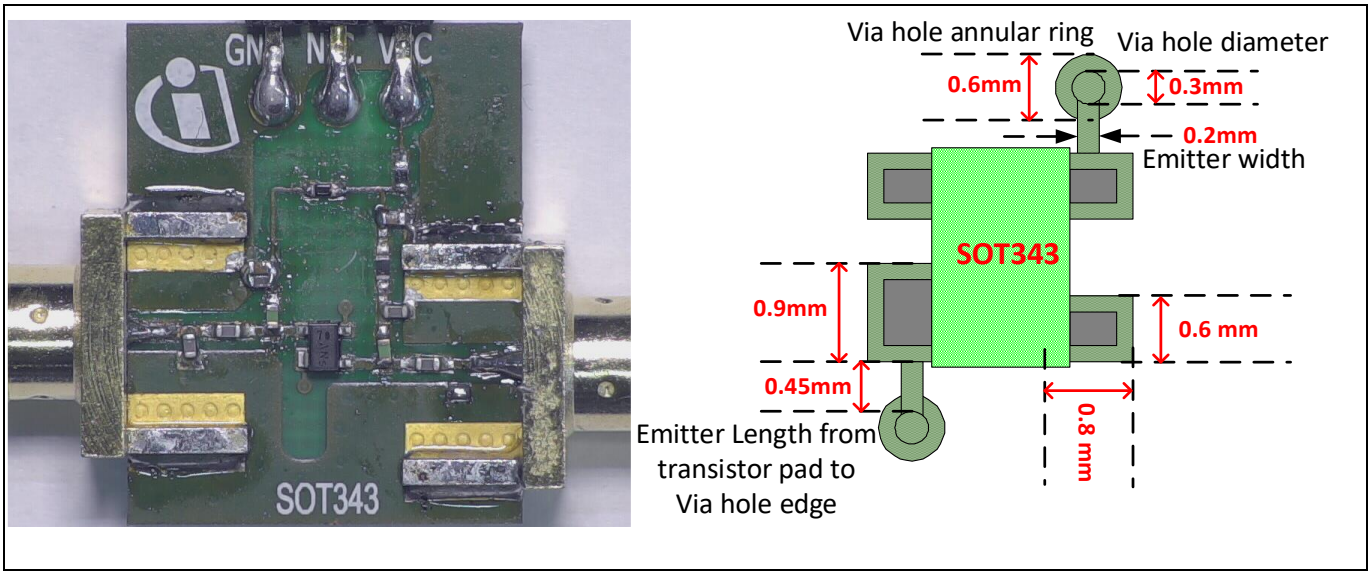

Figure 27 Photo of the evaluation board with the PCB marking M11118 (left) and emitter degeneration details (right)

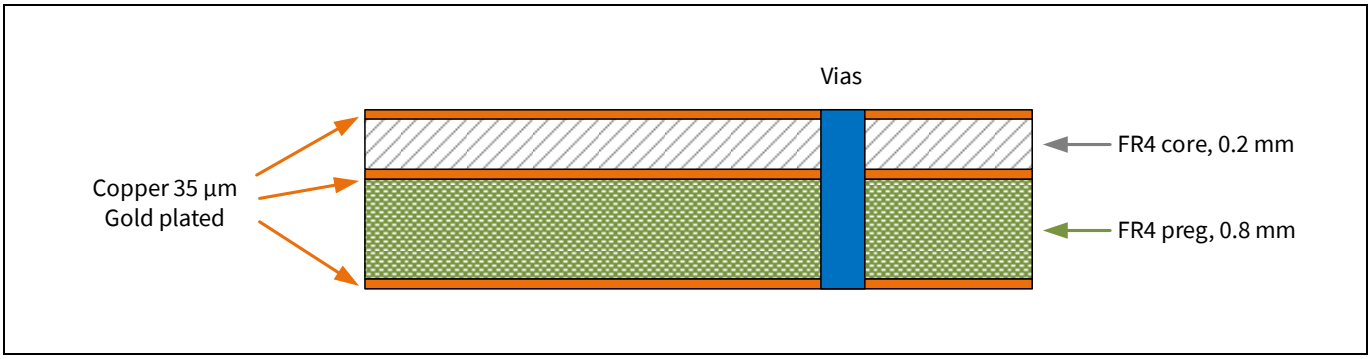

Figure 28 PCB stack information for the evaluation board with the PCB marking M11118

2.3.5 Measurement results of the SDARS active antenna 3rd stage LNA with BFP450 or BFP650 transistor[1)]

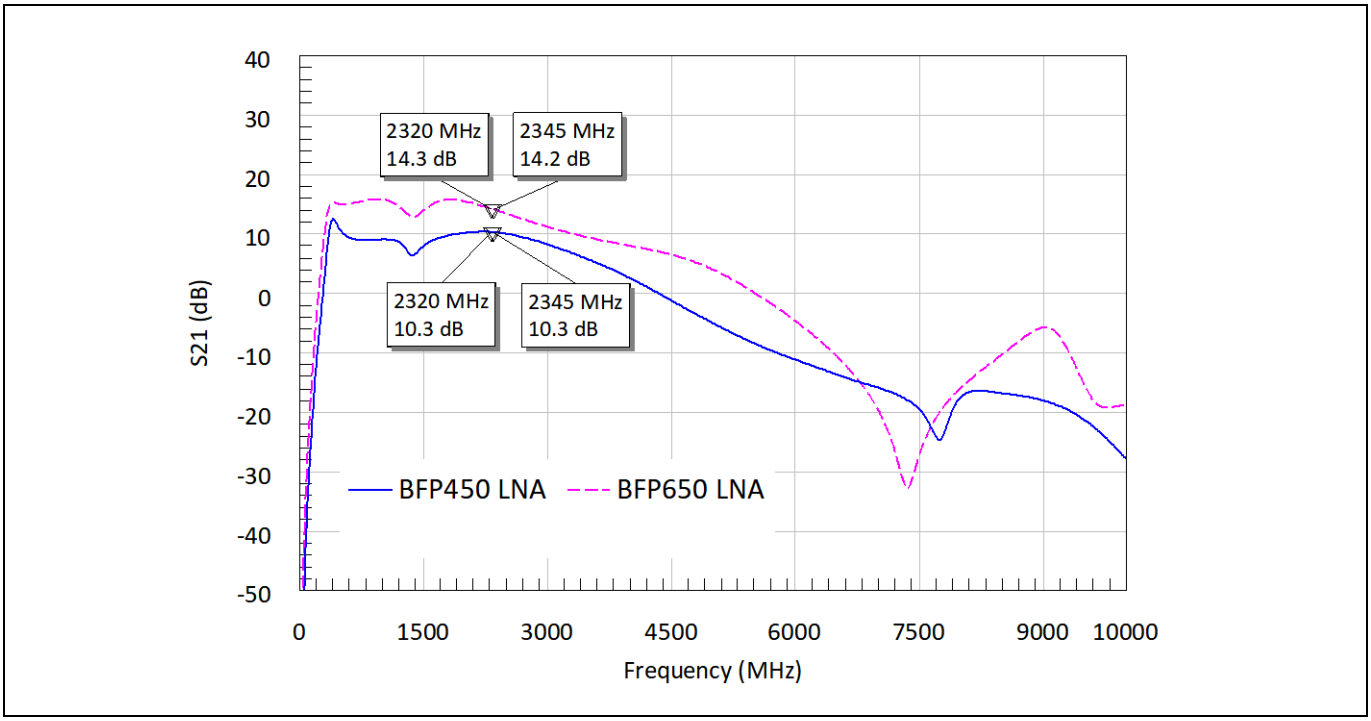

Figure 29 Small signal gain of the SDARS active antenna 3rd stage LNA with BFP450 or BFP650 transistor

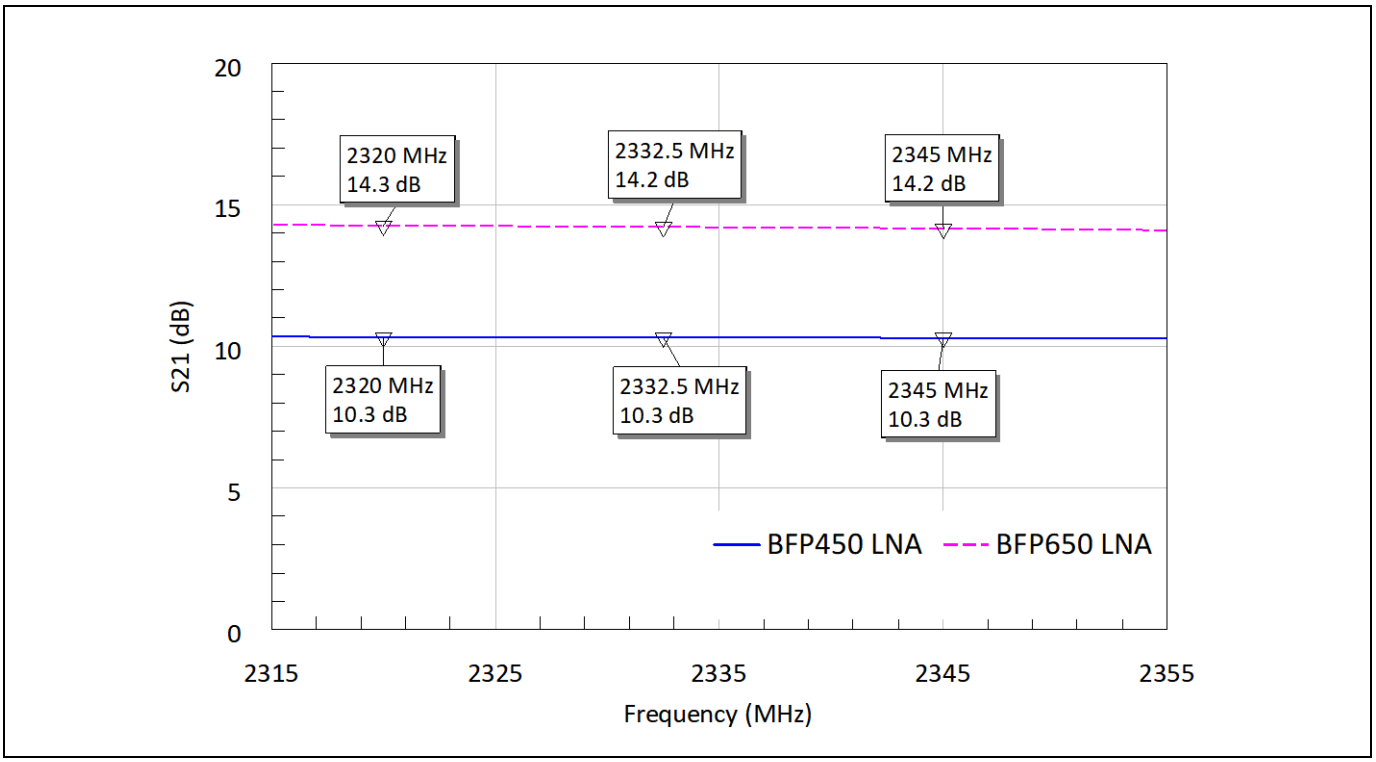

Figure 30 Small signal gain of the SDARS active antenna 3rd stage LNA with BFP450 or BFP650 transistor (detail view)

Note: 1) The graphs are generated with the AWR EDA software Microwave Office®.

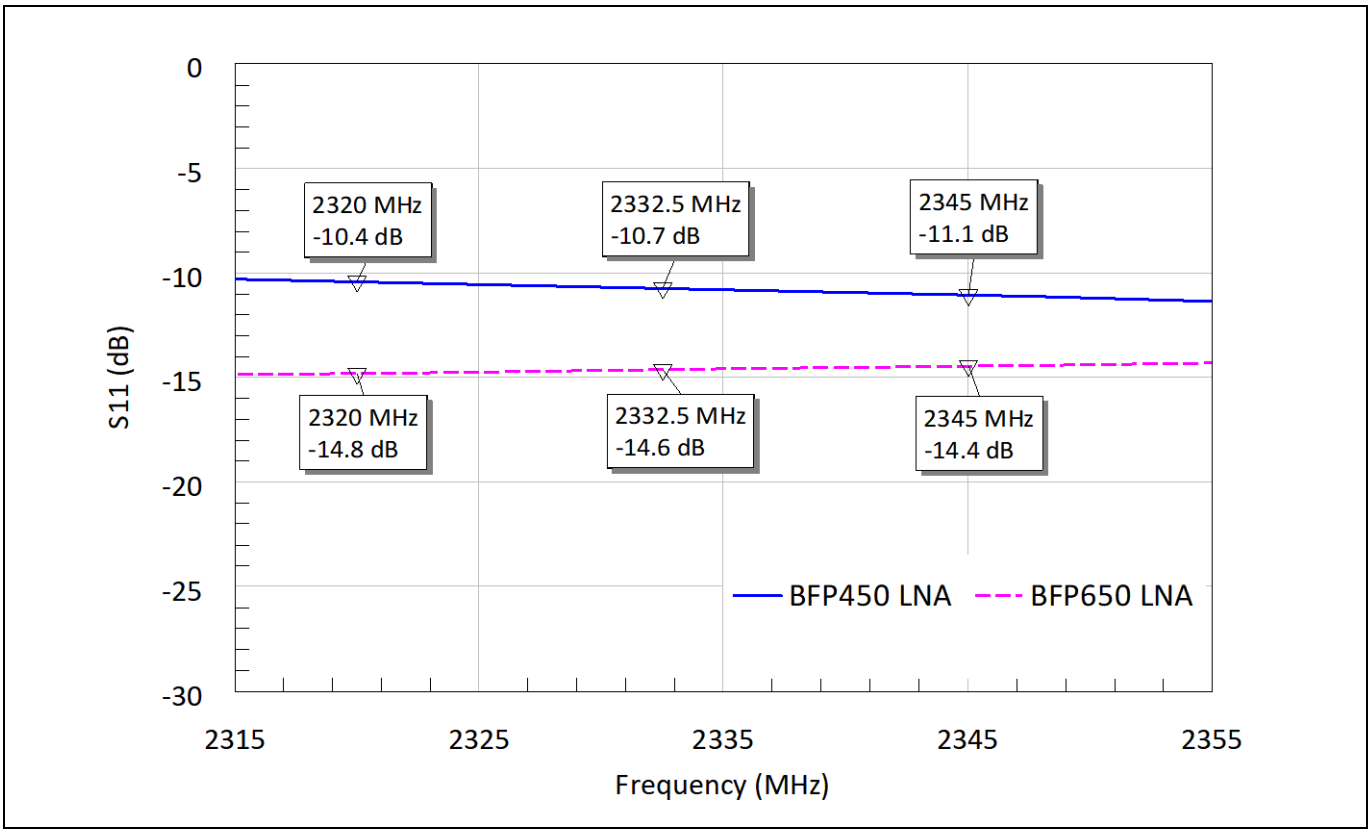

Figure 31 **Input return loss measurement of the SDARS active antenna 3rd stage LNA with BFP450 or BFP650 transistor**

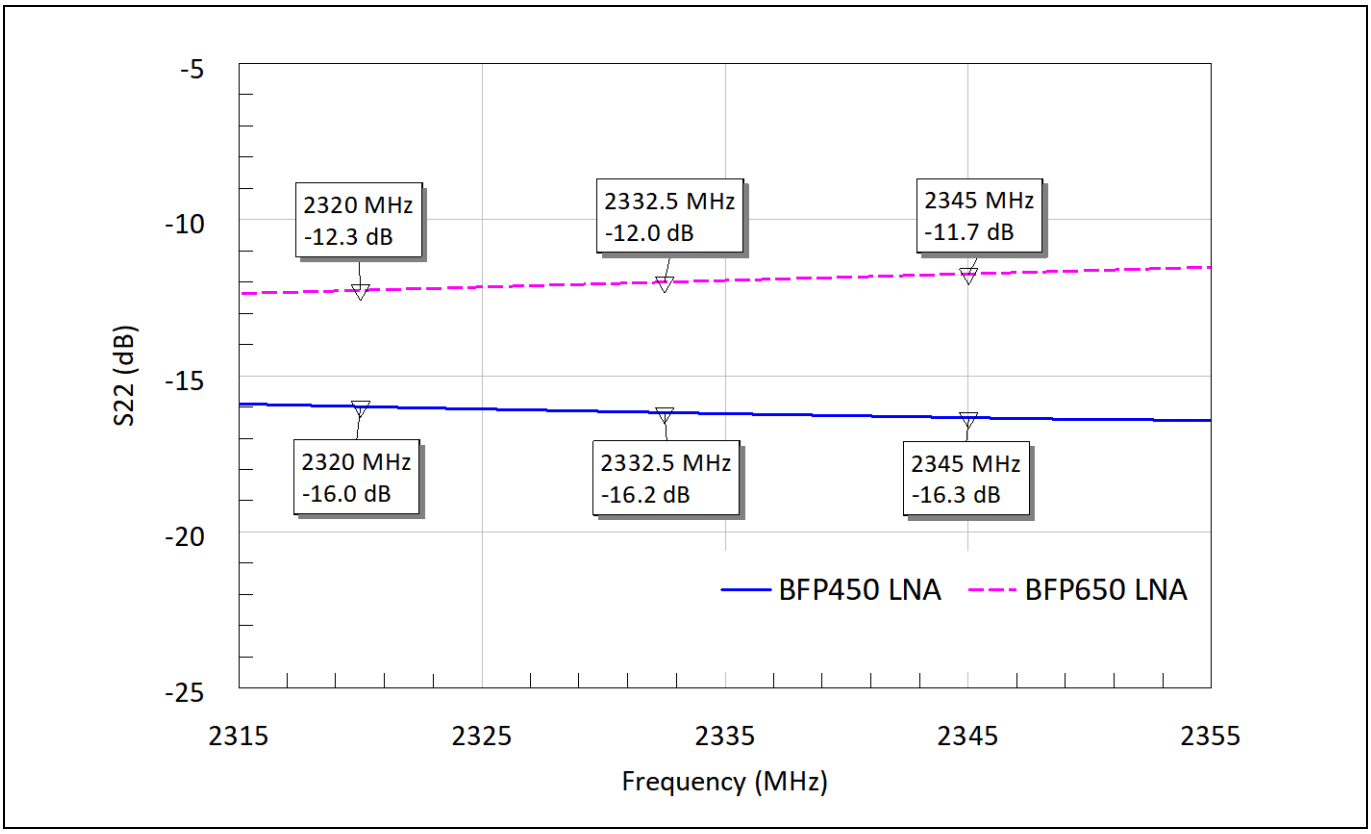

Figure 32 **Output return loss measurement of the SDARS active antenna 3rd stage LNA with BFP450 or BFP650 transistor**

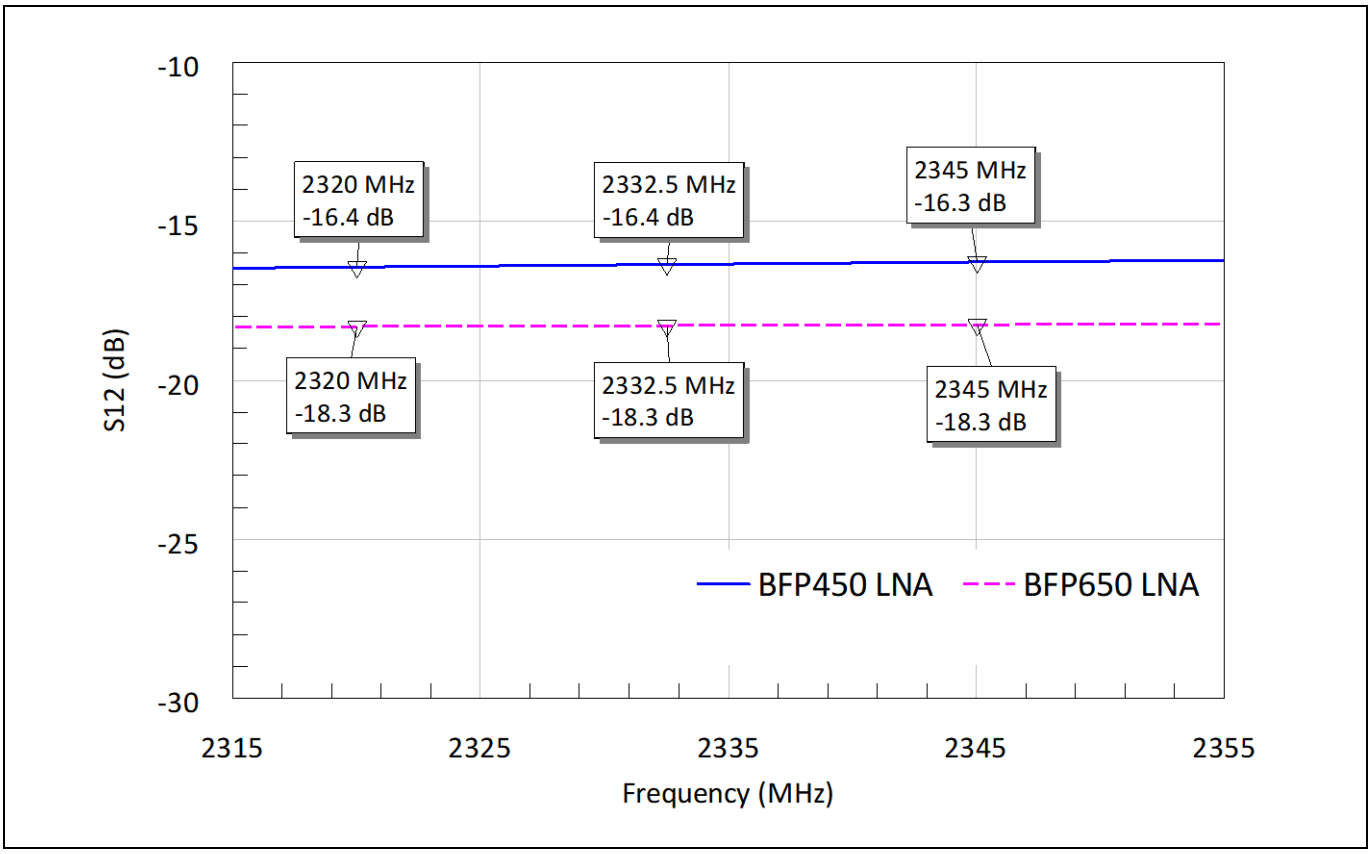

Figure 33 **Reverse isolation measurement of the SDARS active antenna 3rd stage LNA with BFP450 or BFP650 transistor**

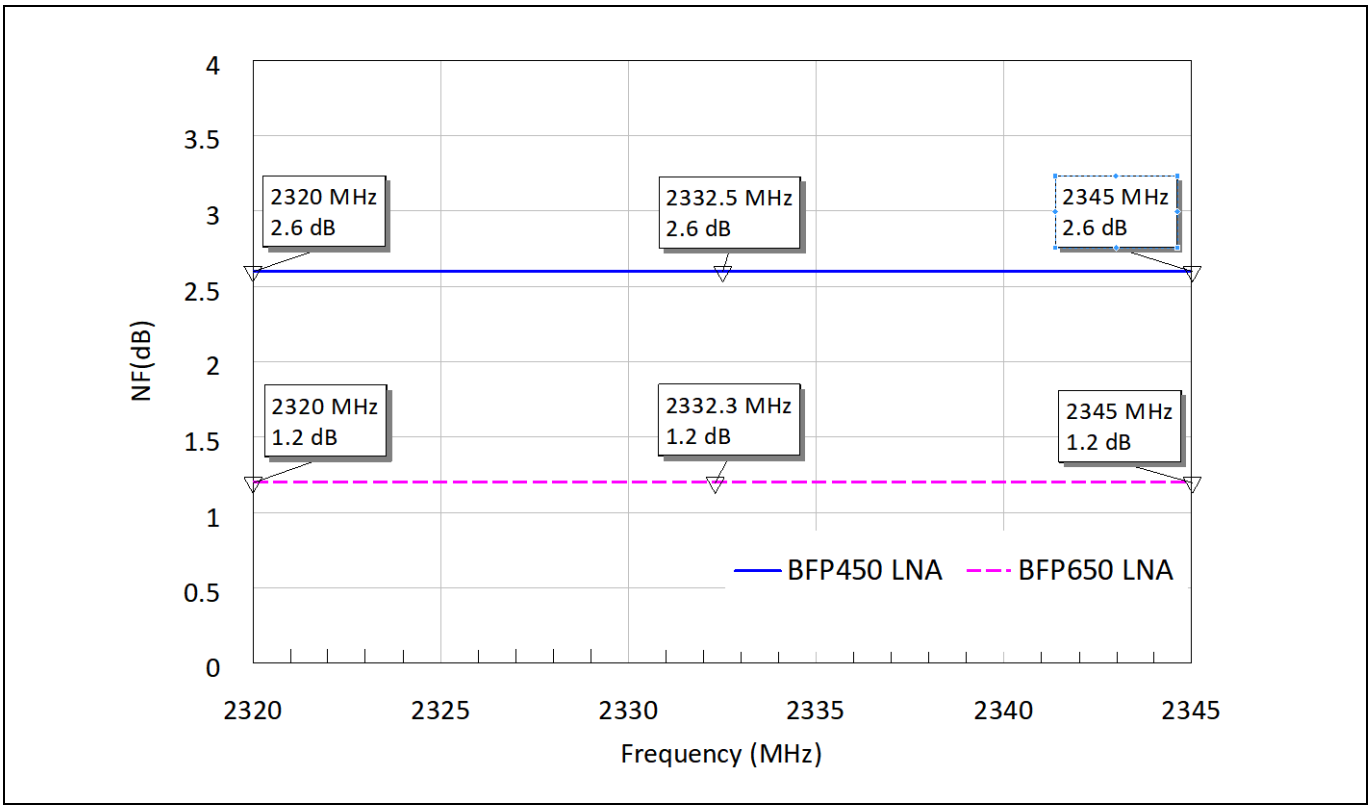

Figure 34 **Noise figure measurement of the SDARS active antenna 3rd stage LNA with BFP450 or BFP650 transistor**

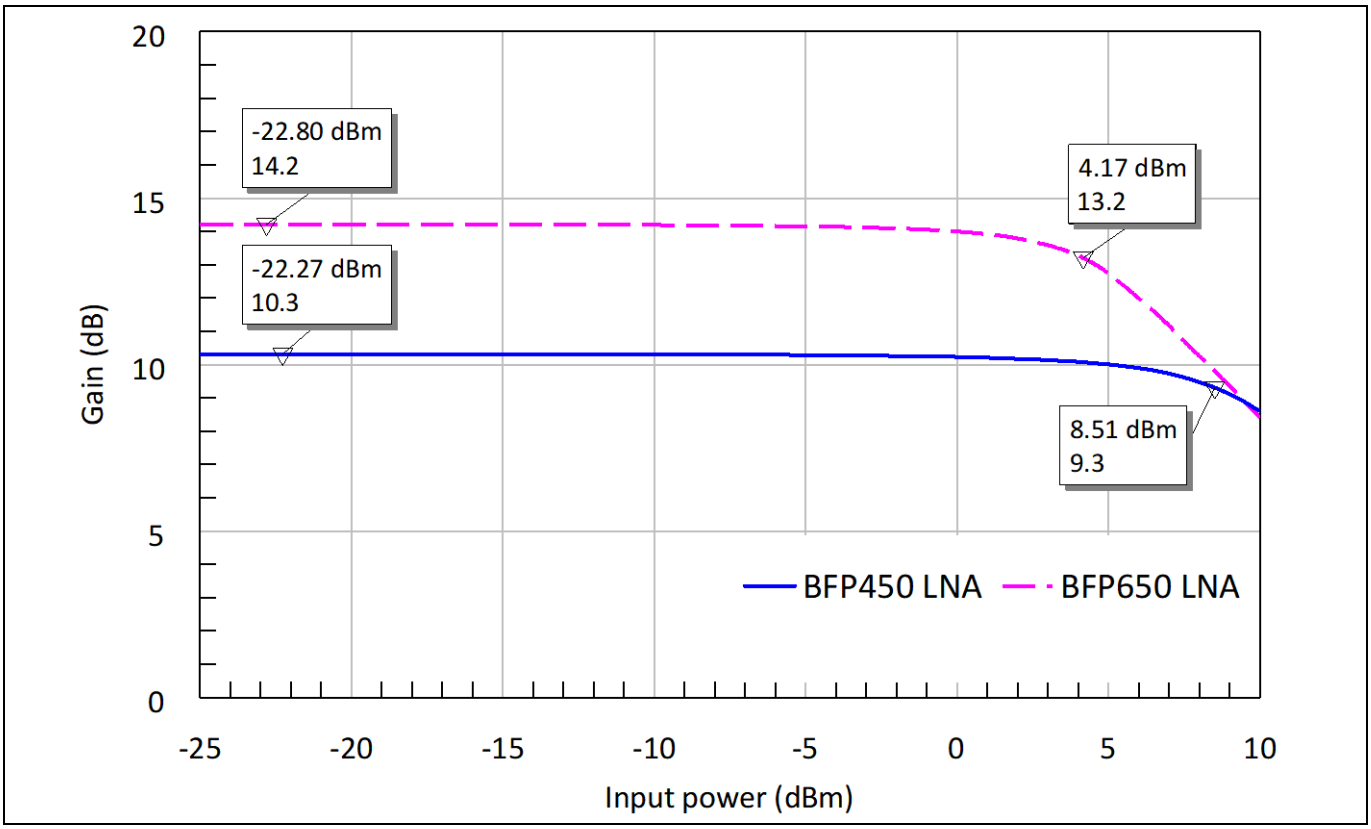

Figure 35 **Input 1-dB compression point measurement of the SDARS active antenna 3rd stage LNA with BFP450 or BFP650 transistor**

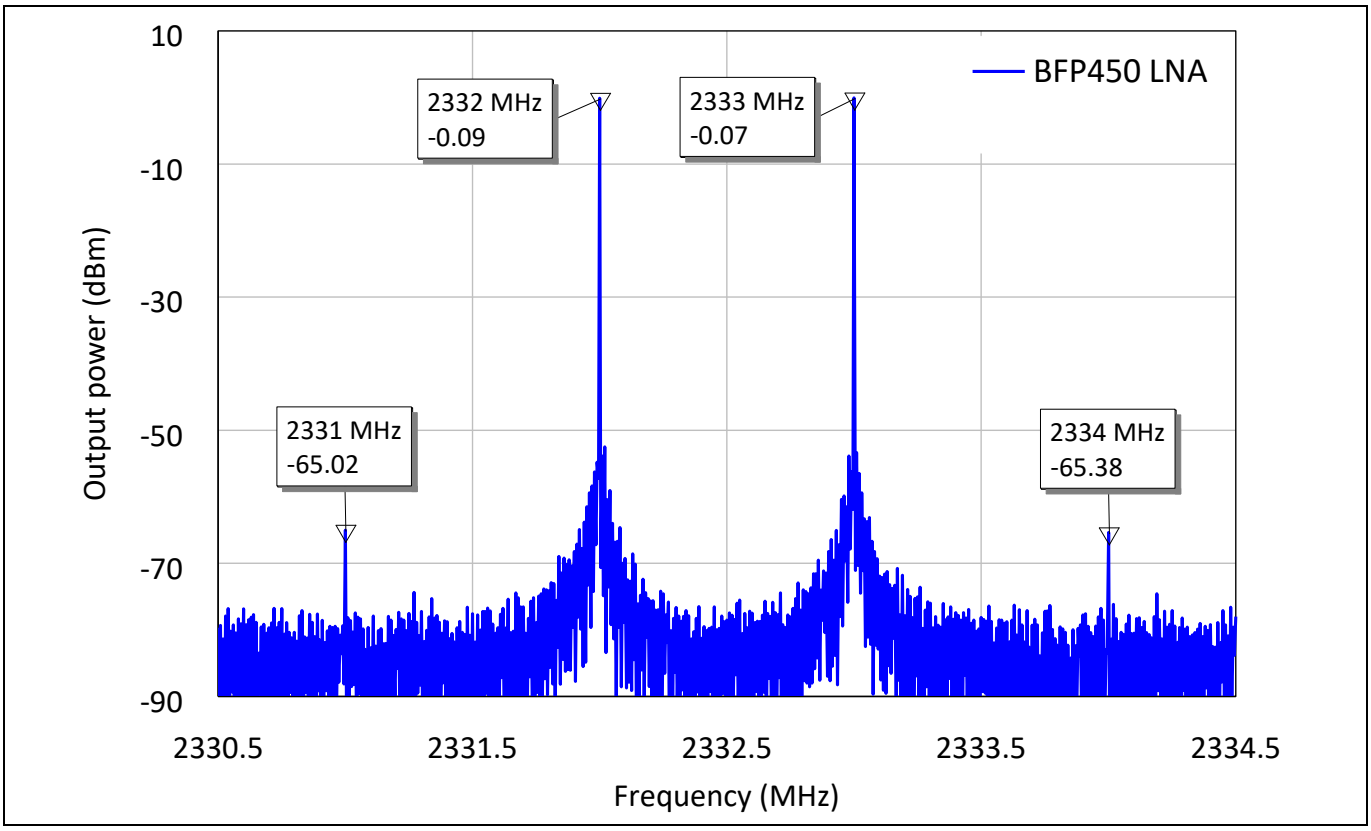

Figure 36 **3rd order Intermodulation distortion measurement of the SDARS active antenna 3rd stage LNA with BFP450**

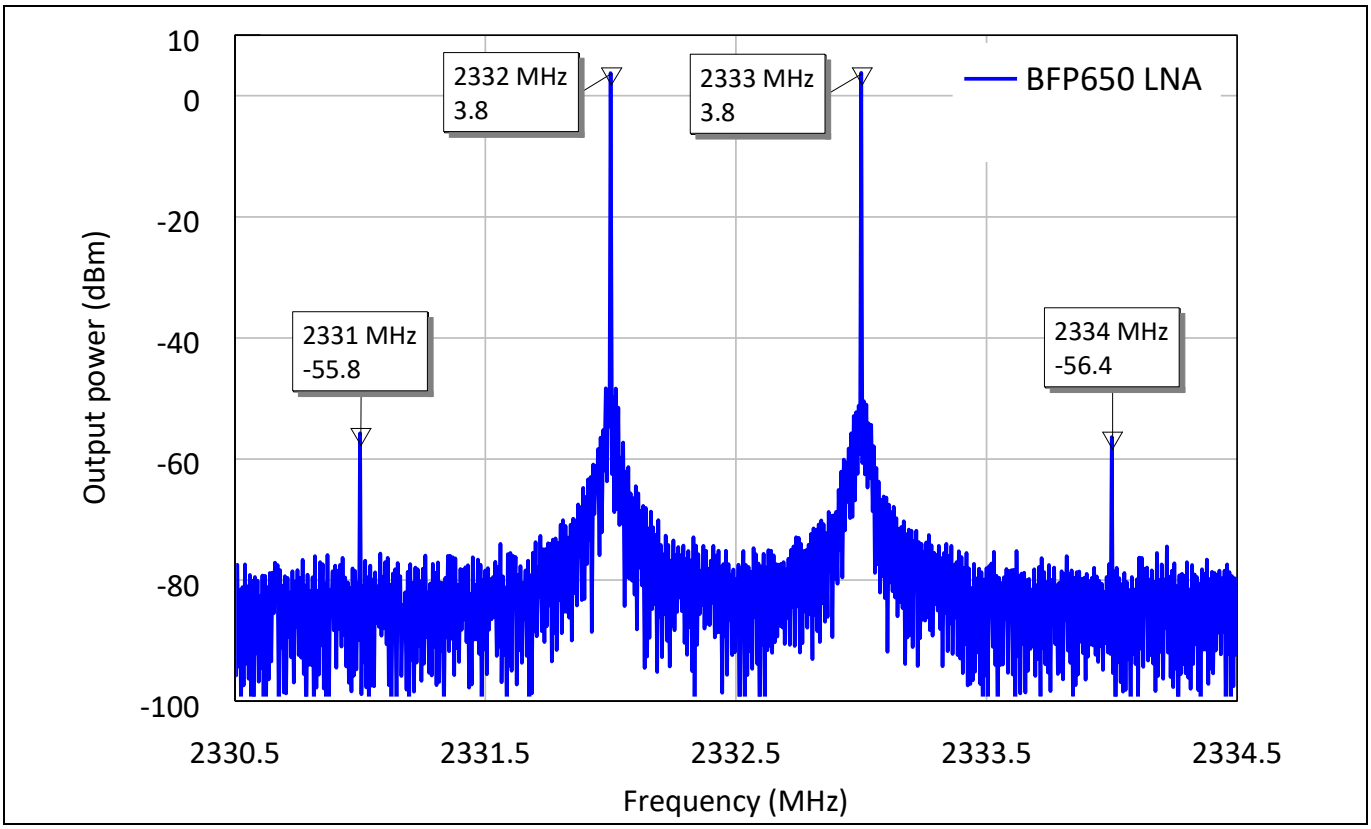

Figure 37 **3rd order Intermodulation distortion measurement of the SDARS active antenna 3rd stage LNA with BFP650**

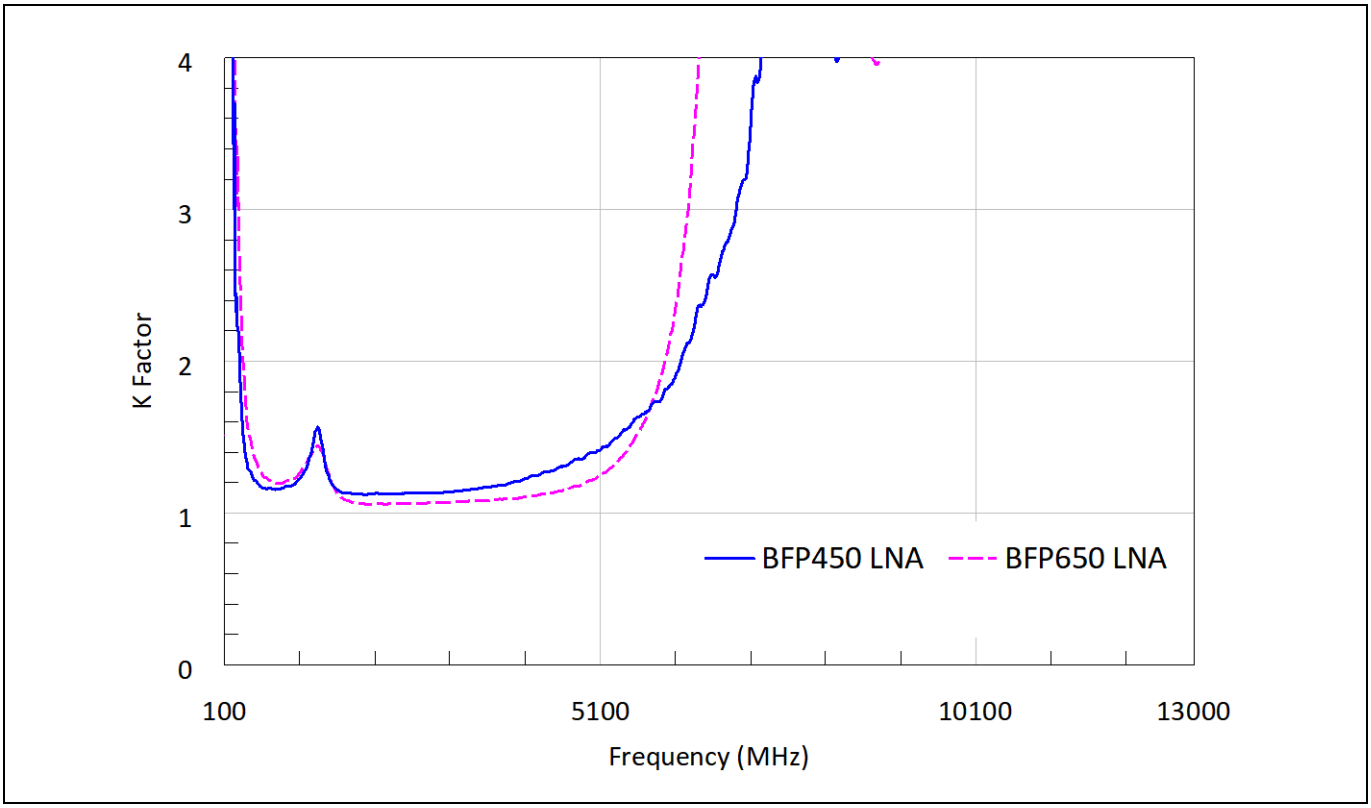

Figure 38 **Stability K factor plots of the SDARS active antenna 3rd stage LNA with BFP450 or BFP650 transistor**

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Document version	Date of release	Description of changes

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