Application Note

ANPS0027 - ICE2QS02G

Converter Design Using Quasi-resonant PWM Controller ICE2QS02G

Power Management & Supply

Never stop thinking.

Published by
Infineon Technologies AG
81726 Munich, Germany

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Title: ICE2QS02G Design Guide

Revision History:	**26 June 2008**	**V1.0**
Previous Version:	none	
Page	Subjects (major changes since last revision)	

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AN-PS0027

He Yi
Yi.he@infineon.com

Jeoh Meng Kiat
Mengkiat.jeoh@infineon.com

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1 Introduction

This application notes describes how to design quasi-resonant flyback converters using ICE2QS02G, which is a new Quasi-resonant PWM controller developed by Infineon Technologies. ICE2QS02G is specially designed for applications of switch mode power supplies used in LCD TV, colour TV, home audio systems, and printers, where an auxiliary converter is needed to provide power supplies of IC.

In this application note, an overview of quasi-resonant flyback converter will be given at first, followed by the introduction of ICE2QS02G functions and operations. Some application examples and hints will be given in the last past of this document.

2 Overview of quasi-resonant flyback converter

Figure 1 shows a typical application of ICE2QS02G in quasi-resonant flyback converter. In this converter, the mains input voltage is rectified by the diode bridge and then smoothed by the capacitor C_{bus} where the bus voltage V_{bus} is available. The transformer has one primary winding W_p, one or more secondary windings (here one secondary winding W_s), and one auxiliary winding W_a. When quasi-resonant control is used for the flyback converter, the typical waveforms are shown in Figure 2. The voltage from the auxiliary winding provides information about demagnetization of the power transformer, the information of input voltage and output voltage.

As shown in Figure 2, after switch-on of the power switch the voltage across the shunt resistor V_{CS} shows a spike caused by the discharging of the drain-source capacitor. After the spike, the voltage V_{CS} shows information about the real current through the main inductance of the transformer L_p. Once the measured current signal V_{CS} exceeds the maximum value determined by the feedback voltage V_{FB}, the power switch is turned off. During this on-time, a negative voltage proportional to the input bus voltage is generated across the auxiliary winding.

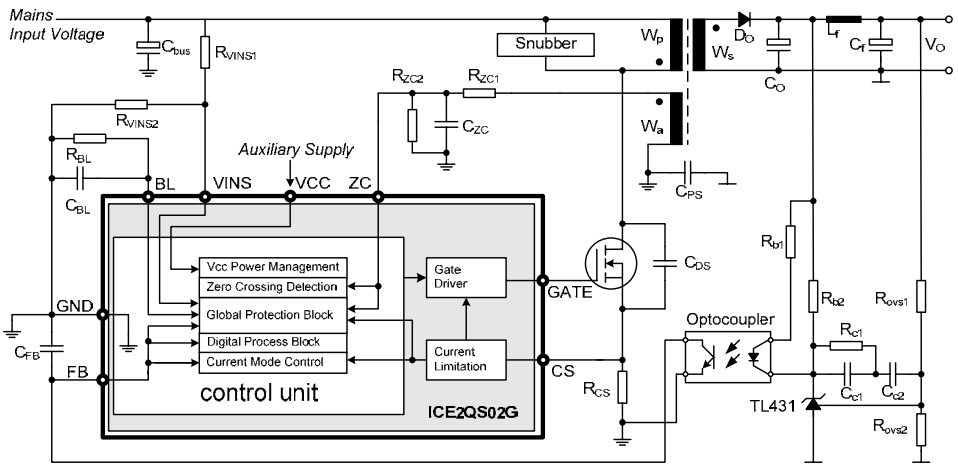

Figure 1 A Typical Application of ICE2QS02G

The drain-source voltage of the power switch v_{ds} will rise very fast after MOSFET is turned off. This is caused by the energy stored in the leakage inductance of the transformer. A snubber circuit, RCD in most cases, can be used to limit the maximum drain source voltage caused. After the oscillation 1, the drain-source voltage goes to its steady value. Here, the voltage v_{Refl} is the reflected value of the secondary voltage at the primary side of the transformer and is calculated as:

$$V_{Refl} = \frac{V_{out} + V_{do}}{n} \quad (1)$$

where n the turns ratio of the transformer, which is defined in this document as:

$$n = N_S/N_P \quad (2)$$

with N_p and N_s are the turns count of the primary and secondary winding, respectively.

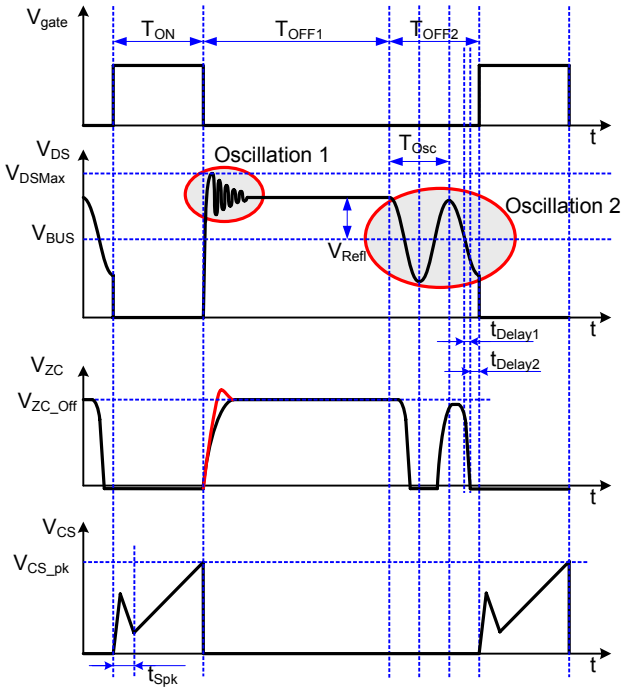

Figure 2 Key waveforms of a quasi-resonant flyback converter

After the oscillation 1 is damped, the drain-source voltage of the power switch shows a constant value of $v_{bus}+v_{Refl}$ until the transformer is fully demagnetized. This duration builds up the first portion of the off-time T_{OFF1}.

After the secondary side current falls to zero, the drains-source voltage of the power switch shows another oscillation (oscillation 2 in Figure 2, this is also mentioned as the main oscillation in this document). This oscillation happens in the circuit consisting of the equivalent main inductance of the transformer L_p and the capacitor across the drain-source (or drain-ground) terminal C_{DS}. The frequency of this oscillation is calculated as:

$$f_{OSC} = \frac{1}{2\pi\sqrt{L_P \cdot C_{DS}}} \quad (3)$$

The amplitude of this oscillation begins with a value of v_{Refl} and decreases exponentially with the elapsing time, which is determined by the losses factor of the resonant circuit. The first minimum of the drain voltage appears at the half of the oscillation period after the time t_4 and can be apporximated as:

$$V_{dsMin} = V_{bus} - V_{Refl} \quad (4)$$

In the quasi-resonant control, the power switch is switched on at the minimum of the drain-source voltage. From this kind of operation, the switching-on losses are minimized, and switching noise due to dv_{ds}/dt is reduced compared to a normal hard-switching flyback converter.

3 IC description

ICE2QS02G is a second generation quasi-resonant PWM controller optimized for off-line power supply applications such as LCD TV, audio and printers, where an auxiliary converter is used to provide IC power supply. The digital frequency reduction with decreasing load enables a quasi-resonant operation till very low load. As a result, the system efficiency is significantly improved compared to a free running quasi resonant converter implemented with maximum switching frequency limitation only.

In addition, numerous protection functions have been implemented in the IC to protect the system and customize the IC for the chosen applications. All of these make the ICE2QS02G an outstanding product for real quasi-resonant flyback converter in the market.

3.1 Main features

- Quasi-resonant operation
- Load dependent digital frequency reduction
- Built-in digital soft-start
- Cycle-by-cycle peak current limitation with built-in leading edge blanking time
- VCC undervoltage protection
- Mains undervoltage protection with adjustable hysteresis
- Foldback Point Correction with digitalized sensing and control circuits
- Over Load Protection with adjustable blanking time
- Adjustable restart time after Over Load Protection
- Adjustable output overvoltage protection with Latch mode
- Short-winding protection with Latch mode
- Maximum on time limitation
- Maximum switching period limitation

3.2 Pin layout

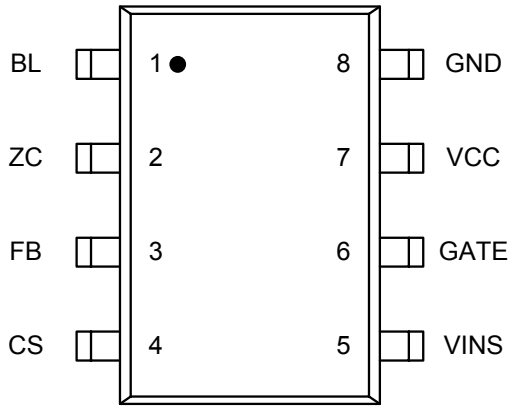

Figure 3 Pin configuration (top view)

3.3 Pin functions

3.3.1 BL (Adjustable Blanking Time)

By connecting a capacitor and a resistor in parallel between this pin and the ground, the blanking time for can be fully adjusted, as well as the restart time. This allows the system to face a sudden power surge for a short period of time without triggering the overload protection. Once the protection triggered, the IC will restart using the internal soft-start circuit, after a period of time fixed by the external resistance and capacitor.

3.3.2 ZC (Zero Crossing)

Three functions are incorporated at the ZC pin. First, during MOSFET off time, the de-magnetization of the transformer is detected when the ZC voltage falls below V_{ZCCT} (100mv). Second, after the MOSFET is turned off, an output overvoltage fault will be assumed if V_{ZC} is higher than V_{ZCOVP} (4.5V). Finally, during the MOSFET on time, a current depending on the bus voltage flows out of this pin. Information on this current is then used to adjust the maximum current limit. More details on this function are provided in Section 4.

3.3.3 FB (Feedback)

Usually, an external capacitor is connected to this pin to smooth the feedback voltage. Internally, this pin is connected to the PWM signal generator for switch-off determination (together with the current sensing signal), and to the digital signal processing for the frequency reduction with decreasing load during normal operation. Additionally, the openloop/overload protection is implemented by monitoring the voltage at this pin.

3.3.4 CS (Current Sensing)

This pin is connected to the shunt resistor for the primary current sensing, externally, and the PWM signal generator for switch-off determination (together with the feedback voltage), internally. Moreover, short-winding protection is realised by monitoring the V_{cs} voltage during on-time of the main power switch.

3.3.5 VINS (Input Voltage Sensing)

The voltage at this pin is used for Mains Undervoltage Protection. The protection is triggered, once V_{VINS} drops below 1.25V. For a stable operation, a hysteresis operation is ensured using an internal current source (See Section 3.5). When the V_{VINS} exceeds the hysteresis point, the system resumes its operation with a soft-start.

3.3.6 Gate (Gate drive output)

The GATE pin is the output of the internal driver stage, which has a rise time of 70ns and a fall time of 30ns when driving a 2.2nF capacitive load.

3.3.7 VCC (Power supply)

The VCC pin is the positive supply of the IC and should be connected to an external auxiliary supply.

3.3.8 GND (Ground)

This is the common ground of the controller.

4 Application information

4.1 IC power supply and soft start

This IC is designed for applications where an auxiliary converter will provide the IC power supply. ICE2QS02G starts operation if the voltage on VCC pin is higher than 12V. The VCC operation range for ICE2QS02G is from 11V to 25V. However, it is suggested that IC is supplied with a regulated dc power supply for better performance. At the same time, a small bypass filter capacitor (100nF typically) is suggested to be put between VCC and GND pins, as near as possible.

After IC supply voltage is higher than 12V, and if the voltage on VINS pin is higher than 1.25V, IC will start switch with a soft start. The soft start function is built inside the IC in a digital manner. During softstart, the peak current of the MOSFET is controlled by an internal voltage reference instead of the voltage on FB pin. The maximum voltage on CS pin for peak current control is increased step by step as shown in Figure 4. The maximum duration of softstart is 16ms with 4ms for each step.

During softstart, the over load protection function is disabled.

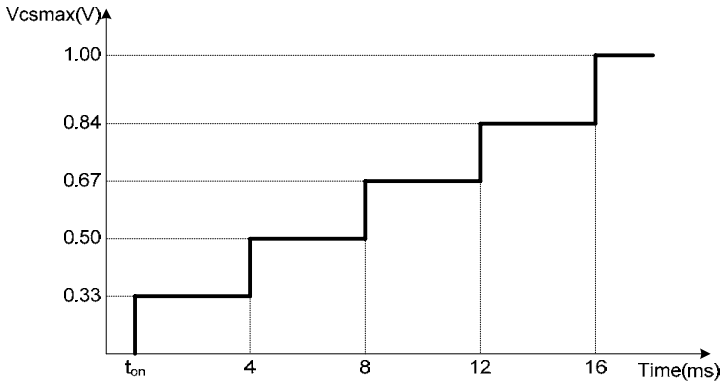

Figure 4 maximum current sense voltage during softstart

4.2 Current sense

The PWM comparator inside the IC has two inputs: one from current sense pin and the other from feedback voltage. Before being sent to the PWM comparator, there is an offset and operational gain on current sense voltage. In normal operation, the relationship between feedback voltage and maximum current sense votlage is determined by equation (5).

$$v_{FB} = G_{PWM} v_{CS\_pk} + V_{PWM} \quad (3)$$

The absolute maximum current sense voltage is 1V. Therefore, the current sense resistor can be chosen according to the maximum required peak current in the transformer as shown in (4).

$$R_{CS} = 1 / I_{pk\_p} \quad (4)$$

The design proceedure of quasi-resonant flyback transformer is shown in [2]. In addition, a leading edge blanking (LEB) is already built inside the current sense pin. The typical value of leading edge blanking time is 330ns, which can be thought as a minimum on time. In most cases, the normal RC filter to blocking the spike because of MOSFET turn-on is not needed. However, in some applications, adding this RC filter is helpful to improve the converter performance.

4.3 Feedback

Inside the IC, the feedback (FB) pin is connected to the 5V voltage source through a pull-up resistor R_{FB}. Outside the IC, this pin is connected to the collector of opto-coupler. Normally, a ceramic capacitor C_{FB}, 1nF for example, can be put between this pin and ground for smooting the signal.

Feedback voltage will be used for a few functions as following:

- It determines the maximum current voltage, equivalent to the transformer peak current.
- It determines the ZC counter value according to load condition
- It determines whether IC will start the over-load/open loop protection timer. In detail, IC will start the timer once the FB voltage is higher than 4.5V.

4.4 Zero crossing

The circuit components connected to zero crossing (ZC) pin include resistors R_{ZC1} and R_{ZC2} and capacitor C_{ZC}. The values of three components shall be chosen so that the three functions combined to this pin will perform as designed.

At first, the ratio between R_{ZC1} and R_{ZC2} is chosen first to set the trigger level of output overvoltage protection. Assuming the protection level of output voltage is V_{O_OVP}, the turns of auxiliary winding is Na and the turns of secondary output winding is Ns, the ratio is calculated as

$$\frac{R_{ZC2}}{R_{ZC1}+R_{ZC2}} < V_{ZCOVP}\frac{N_S}{V_O N_a} \tag{5}$$

In (5), V_{ZCOVP} is the trigger level of output overvoltage protection which can be found in product datasheet.

Secondly, as shown in Figure 2, there are two delay times for detection of the zero crossing and turn on of the MOSFET. The delay time t_{Delay1} is the delay from the drain-source voltage cross the bus voltage to the ZC voltage follows below 50mV. This delay time can be adjusted through changing C_{ZC}. The second one, t_{Delay2}, is the delay time from ZC voltage follows below 50mV to the MOSFET is turned on. This second delay time is determined by IC internal circuit and cannot be changed. Therefore, the capacitance C_{ZC} is chosen to adjust the delay time t_{Delay1} MOSFET is justed turned on at the valley point of drain-source voltage. This is normally done through experiment.

Next, there is a foldback point correction integrated in this pin. This function is to decrease the peak current limit on current sense pin so that the maximum output power of the converter will not increase when the input voltage increases. This is done through sensing the current flowing out from ZC pin when MOSFET is turned on.

When the main power switch is turned on, the negative voltage on auxiliary winding can be calculated as

$$V_{aux} = -V_{BUS}\frac{N_a}{N_P} \tag{6}$$

Inside ZC pin, there is a clamping circuit so that the ZC pin voltage is kept at nearly zero. Therefore, the current flowing out from ZC pin at this moment is

$$I_{ZC\_ON} = \frac{V_{BUS}N_a}{R_{ZC1}N_P} \tag{7}$$

The threshold in ZC pin to start the foldback point correction is I_{ZC} = 0.5 mA. Therefore, R_{ZC1} can be chosen so that

$$R_{ZC1} = \frac{V_{BUS\_S}N_a}{0.5mA * N_P} \tag{8}$$

In (8), V_{BUS_S} is the voltage from which the maximum output power is desired to be maintained at constant level. The corresponding maximum current sense voltage in relation to the ZC current is shown in Figure 5.

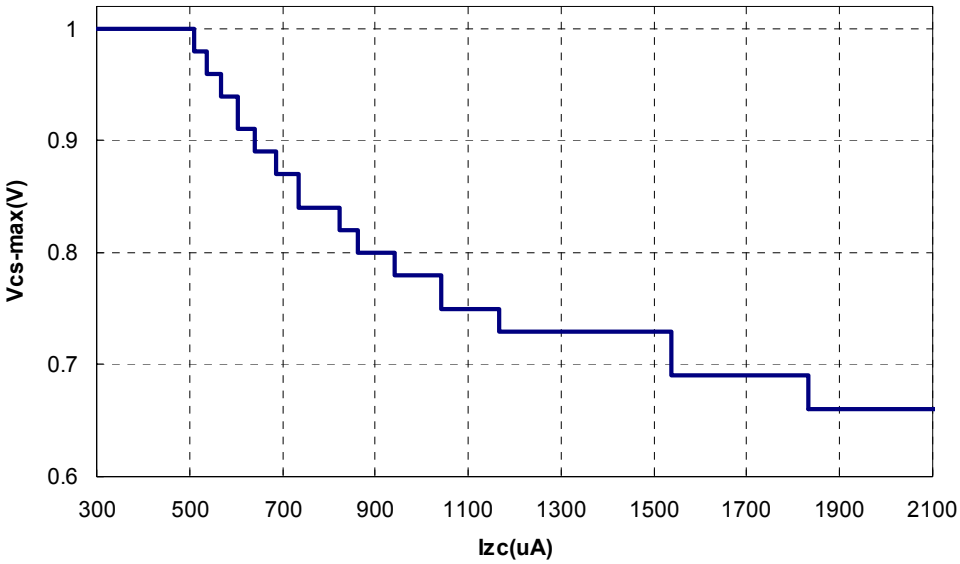

Figure 5 Maximum current sense limit versus ZC current during MOSFET on-state

In addition, as shown in Figure 2, an overshoot is possible on ZC voltages when MOSFET is turned off. This is because of the oscillation 1 on drain voltage, shown in Figure 2 may be coupled to the auxiliary winding. Therefore, the capacitance C_{ZC} and ratio can be adjusted to obtain the trade off between the output overvoltage protection accuracy and the valley switching performace.

Furthermore, to avoid mis-triggerring of ZC detection just after MOSFET is turned off, a ring suppression time is provided. The ring suppression time is 2.5 µs typically if V_{ZC} is higher than 0.7V and it is 25 µs typically if V_{ZC} is lower than 0.7V. During the ring suppression time, IC can not be turned on again. Therefore, the ring suppression time can also be thought as a minimum off time.

4.5 Input voltage sense

The VINS pin is used to receive bus voltage information. The outside connection of this pin is shown in Figure 6. When the input voltage is minimum required value, IC stops switch and enters into mains undervoltage protection. When the input voltage is higher than another threshold, IC will resume switch with a soft-start. To prevent IC from entering and leaving protection frequently, a hysteresis is provided by adding a current source I_{VINS} inside the IC, which is shown in Figure 6.

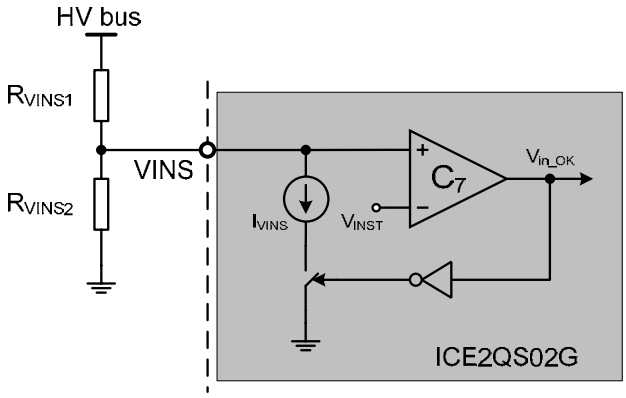

Figure 6 Input voltage sense on VINS pin

If the desired on and off bus voltages are V_{BUS_on} and V_{BUS_off}, the resistors can be chosen as follows. At first, the ratio of two resistors is obtained from (9).

$$V_{BUS-off} = V_{INST} \frac{R_{VINS1} + R_{VINS2}}{R_{VINS2}} \quad (9)$$

Next, the hysteresis between on and off voltage determines the R_{VINS1} according to (10).

$$R_{VINS1} = \frac{V_{BUS-on} - V_{BUS\_off}}{I_{VINS}} \quad (10)$$

With given R_{VINS1}, R_{VINS2} can be obtained from (9). In fact, there is production tolerance on current I_{VINS}, please consider the max/min value when choosing R_{VINS1}. If the noise on VINS pin is too large, a ceramic capacitor of 100nF can be put across the VINS and GND pins. The capacitor should be put near the IC as much as possible.

4.6 Blanking time

A capacitor C_{BL} and a resistor R_{BL} are connected to BL pin. This can be used to adjust the blanking time for overload protection and the blanking time from IC stops switching to it restarts again. The internal connection in BL pin and FB pin is shown in Figure 7.

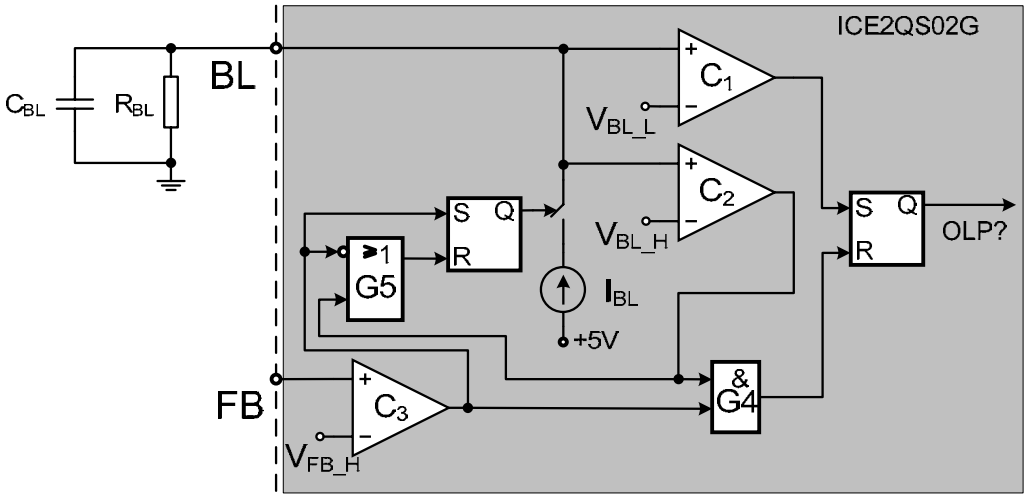

Figure 7 Blanking time setting

In case of over load or open loop mode, the FB voltage will rise higher than V_{FB_H}. Once FB voltage is higher than V_{FB_H}, IC will turn on the current source I_{BL}. The capacitor C_{BL} will be charged up. The time for charging C_{BL} to V_{BL_H} determines the overload protection blanking time. Considering the influence of R_{BL}, the over-load blanking time can be calculated as

$$T_{OLP\_BL} = -R_{BL} C_{BL} * \ln(1 - \frac{V_{BL\_H}}{I_{BL} * R_{BL}}) \quad (11)$$

After the over-load/open-loop protection is triggered, IC will stop the switch and turn-off I_{BL} at the same time. As a result, C_{BL} is slowly discharged by R_{BL}. Once the voltage on BL pin falls below V_{BLL}, IC will start another soft-start. The time for C_{BL} being discharged from V_{BL_H} to V_{BL_L} determines the auto-restart time. It is shown in (12)

$$T_{OLP\_R} = -R_{BL} C_{BL} \ln(\frac{V_{BL\_L}}{V_{BL\_H}}) \quad (12)$$

4.7 Gate drive

Inside Gate pin, a totem-drive circuit is integrated. The gate drive voltage is 10V, which is enough for most of the available MOSFET. In case of a 2.2nF load capacitance, the typically values of rise time and fall time are 70ns and 30ns, respectively. In practice, a gate resistor can be used to adjust the turn-on speed of the MOSFET. In addition, to accelerate the turn off speed, the gate resistor can be anti-paralleled with an ultra-

fast diode like 1N4148. To avoid the oscillation during turn-off of the MOSFET, it is suggested that the loop area of the driver, through gate resistor and MOSFET gate, source and back to IC ground should be as small as possible.

4.8 Others

For quasi-resonant flyback converters, it is possible that the operation frequency goes too low, which normally resulted in audible noise. To prevent it, in ICE2QS02G, a maximum on time and maximum switching period is provided.

The maximum on time in ICE2QS02G is 30 µs typically. If the gate is maintained on for 30 µs, IC will turn off the gate regardless of the current sense voltage.

When the MOSFET is off and IC can not detect enough number of ZC to turn on the MOSFET, IC will turn on the MOSFET when the maximum switching period, 50 µs typically, is reached. Please note that even a non-zero ZC pin voltage can not prevent IC from turning on the MOSFET. Therefore, during soft start, a CCM operation of the converter can be expected.

5 Typical application circuit

An 80W evaluation board with ICE2QS02G is also available. The detailed information can be found in [3]. The application circuit is shown in Figure 8.

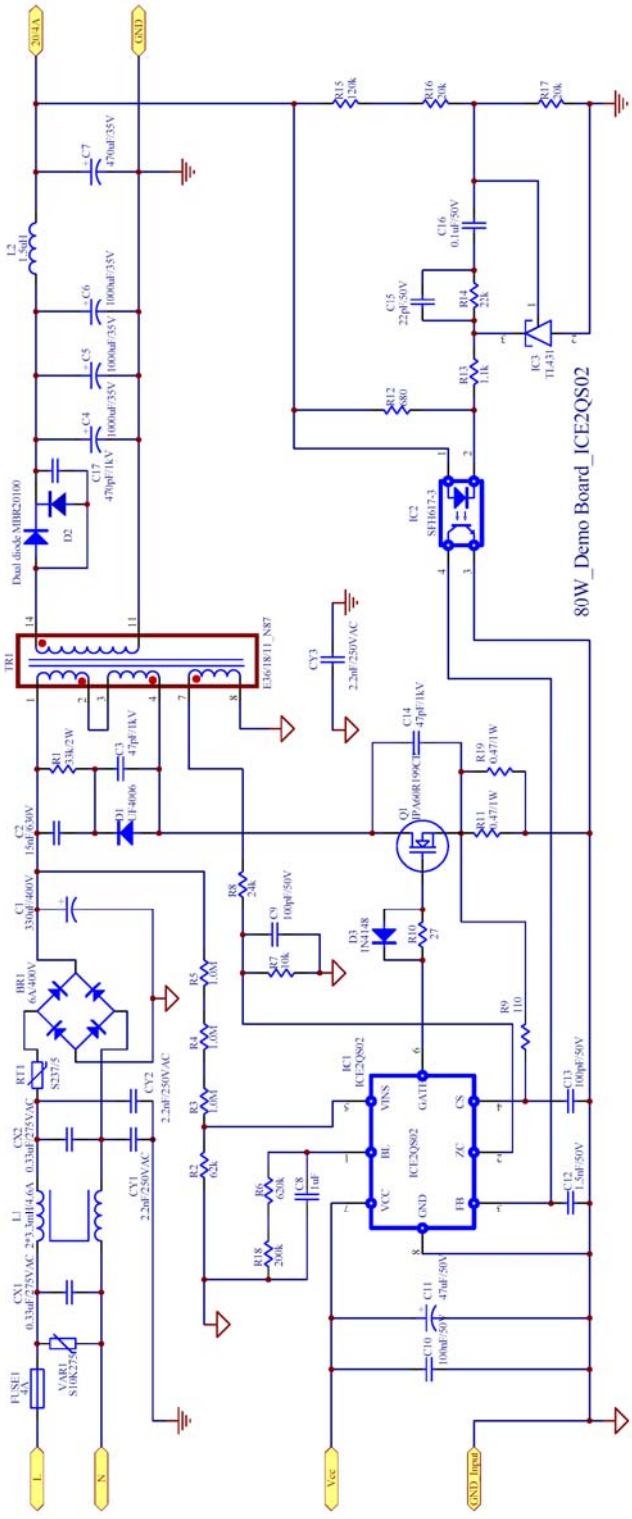

Figure 8 Schematic of the 80W evalulation board with ICE2QS02G

6 References

[1] ICE2QS02G, product datasheet, Infineon Technologies, 2008

[2] Converter design using the quasi-resonant PWM controller ICE2QS01, application notes, Infineon Technologies, 2006

[3] 80W Evaluation Board with Quasi-Resonant PWM Controller ICE2QS02G, AN-EVALQRS-ICE2QS02G-80W, Infineon Technologies, 2008