Design Guide for Boost Type CCM PFC with ICE3PCSxx

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Page	Subjects (major changes since last revision)
Page 17	Maximum switching frequency changed to 100kHz
Figure 13	Maximum switching frequency changed to 100kHz

Design Guide for Boost Type CCM PFC with ICE3PCS0xG

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Abstract

ICE3PCS01/02/03G are the 3rd generation of Continuous Conduction Mode (CCM) PFC controllers, which employ BiCMOS technology and digital control voltage loop. The IC control scheme does not need the direct sine-wave sensing reference signal from the AC mains compared to the conventional PFC solution. Average current control is implemented to achieve the unity power factor. In this application note, the design process for the boost PFC with ICE3PCS0XG is presented and the design details for a 300W output power PFC with the universal input voltage range of 85~265VAC are included.

1 Introduction

The pin layout of ICE3PCS01G, ICE3PCS02G and ICE3PCS03G is shown in Figure 1.

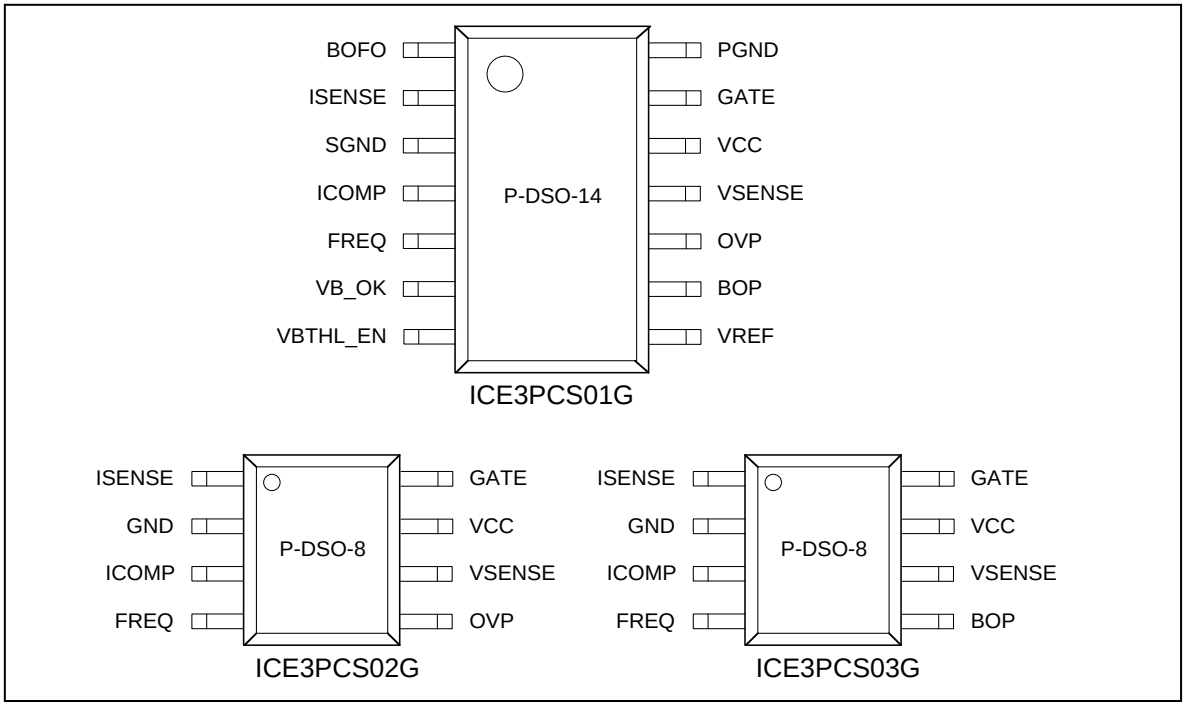

Figure 1 Pin Layout of ICE3PCS01G, ICE3PCS02G and ICE3PCS03G

In the 3rd generation CCM PFC controller, ICE3PCS01G has 14 pins with the best performance in efficiency and protections. This IC introduce a few new features such as -0.2V peak current limit, boost follower mode, 5V voltage regulator supply up to 5mA and IC can be disable using external signal.

ICE3PCS02G and ICE3PCS03G are dedicated for applications requiring less pin count and simpler functions. From the pin layout, it can be seen that most of pins in ICE3PCS02G are the same as ICE3PCS03G except Pin 5. In ICE3PCS02G, Pin 5 is to set the second over voltage protection. However, for ICE3PCS03G, Pin 5 is for AC brown out detection. The typical application circuits of ICE3PCS01G, ICE3PCS02G and ICE3PCS03G are shown in Figure 2, Figure 3 and Figure 4 respectively.

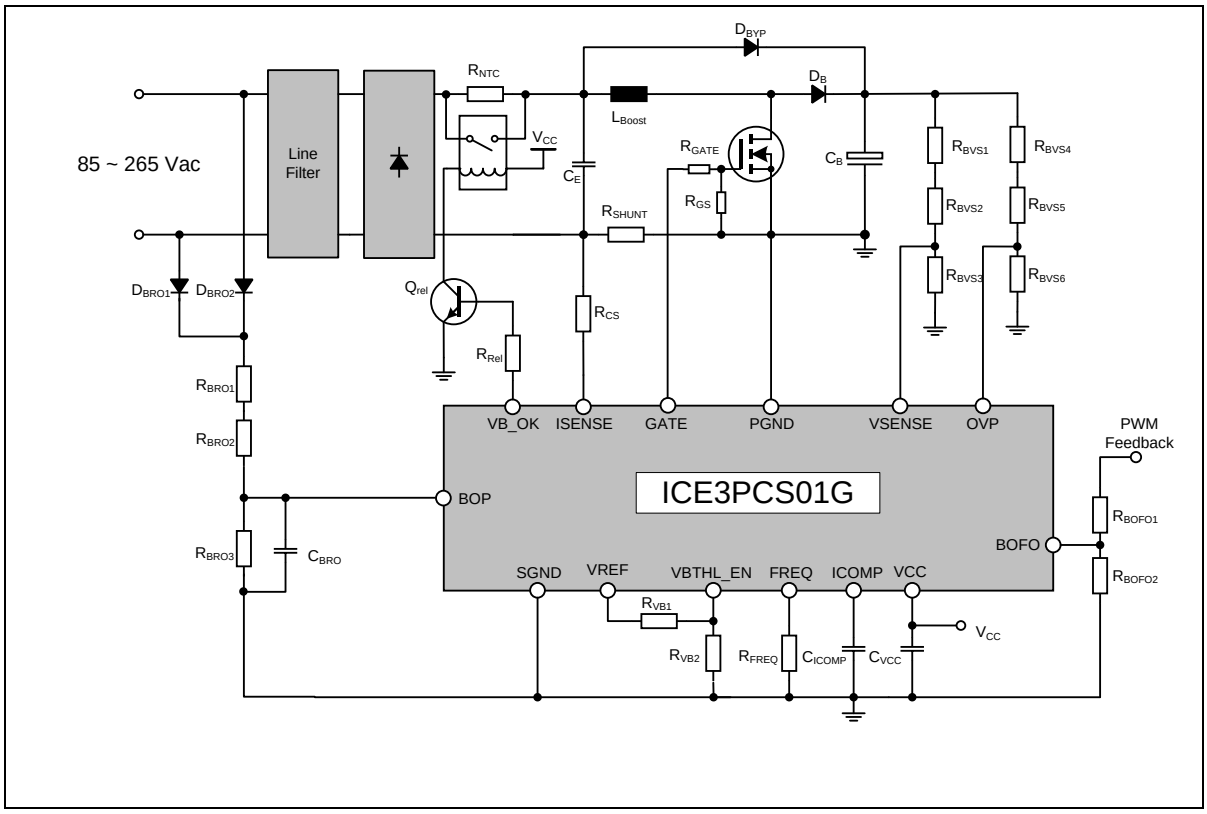

Figure 2 Typical application circuit of ICE3PCS01G

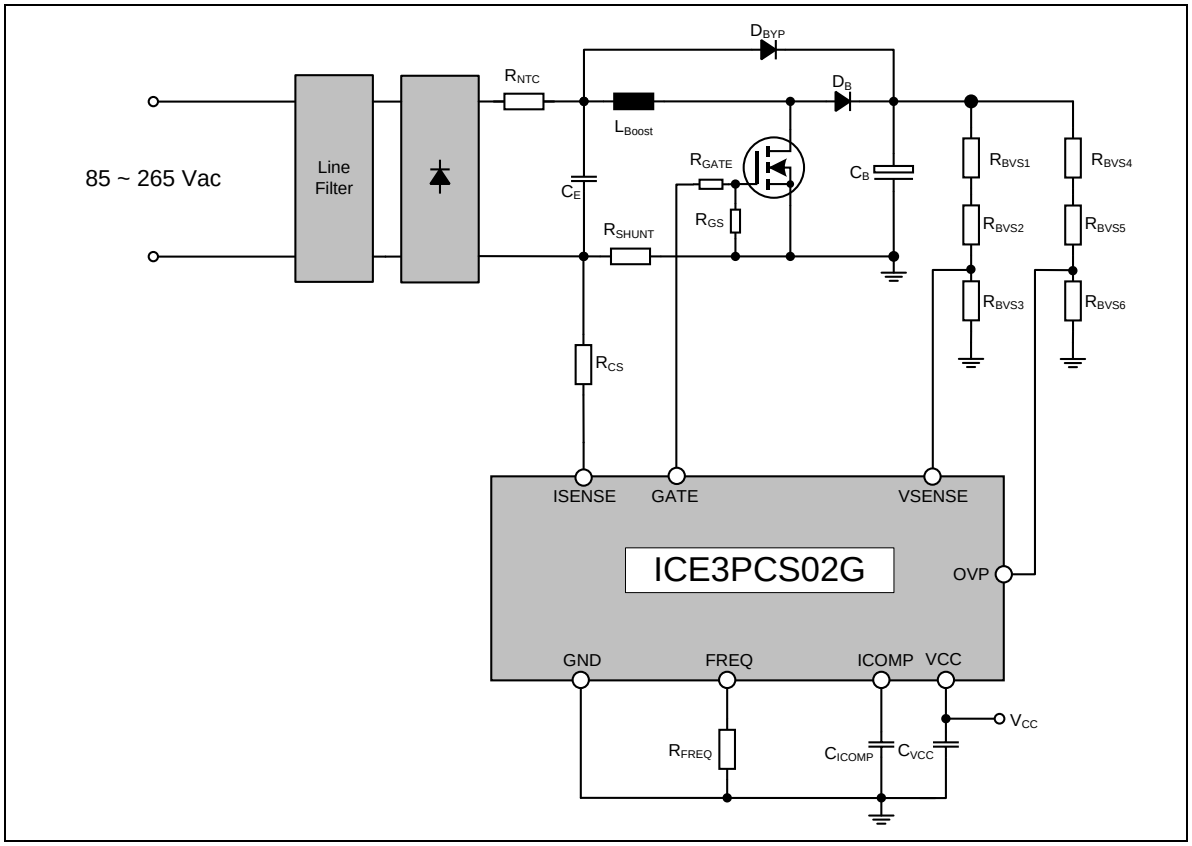

Figure 3 Typical application circuit of ICE3PCS02G

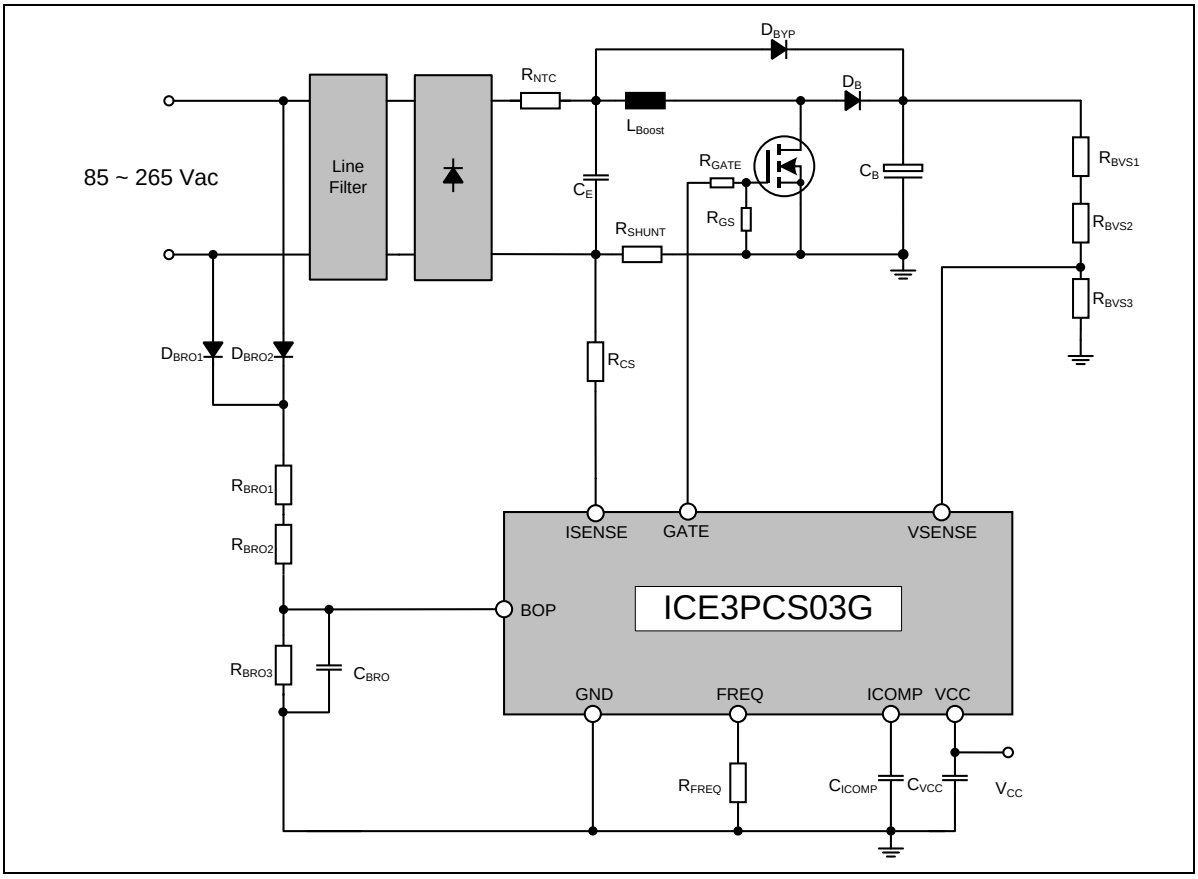

Figure 4 Typical application circuit of ICE3PCS03G

2 Boost PFC design with ICE3PCS0XG

2.1 Target specification

The fundamental electrical data of the circuit are the input voltage range, V_{IN}, the output power, P_{OUT}, the output voltage, V_{OUT}, the operating switching frequency, f_{SW} and the value of the high frequency ripple of the AC line current, I_{ripple}. Table 1 shows the relevant values for the system calculated in this Application Note. The efficiency at rated output power Pout is estimated to 95 % over the complete input voltage range.

Input voltage	85VAC~265VAC
Input frequency	50Hz~60Hz
Output voltage and current	400VDC, 0.75A
Output power	300W
Efficiency	>95%
Switching Frequency	65kHz
Maximum Ambient temperature around PFC	70ºC

Table 1 Design parameter for the proposed design

2.2 Bridge rectifier

In order to obtain 300W output power at 85V minimum AC input voltage, the maximum input RMS current is:

$$I_{IN\_RMS} = \frac{P_{OUT}}{V_{IN\_MIN} \cdot \eta} = \frac{300}{85 \cdot 95\%} = 3.715A \quad (1)$$

And the sinusoidal peak value of AC current is:

$$I_{in\_pk} = \sqrt{2} \cdot I_{in\_RMS} = \sqrt{2} \cdot 3.715A = 5.25A \quad (2)$$

For these values a bridge rectifier with an average current capability of 6A or higher is a good choice. Please note here, that due to a power dissipation of approximately,

$$P_{BR} = 2 \cdot V_F \cdot I_{in\_RMS} = 2 \cdot 1V \cdot 3.715A = 7.43W \quad (3)$$

The rectifier bridge should be connected to an appropriate heatsink. Assuming a maximum junction temperature T_{Jmax} of 125°C, a maximum ambient temperature T_{Amax} of 70°C, the thermal junction-to-case R_{thJC} of approximate 2.5 K/W and the thermal case to heatsink R_{thCHS} of approximate 1K/W, the heatsink could have a maximum thermal resistance of:

$$R_{thHS\_BR} = \frac{T_{J\max} - T_{A\max}}{P_{BR}} - R_{thJC} - R_{thCHS} = \frac{125 - 70}{7.43} - 2.5 - 1 = 3.9K/W \quad (4)$$

2.3 Power MOSFET and Gate Drive Circuit

Due to the switch mode operation, the loss is only valid during the on-time of the MOSFET. The duty cycle of the transistor in boost converters operating in CCM at minimum AC input RMS voltage is:

$$D_{on} = 1 - \frac{V_{in\_\min}}{V_{out}} = 1 - \frac{85}{400} = 0.7875 \quad (5)$$

Since rms-values have the same effect on a system as DC-values, it is possible to calculate a characteristic duty cycle for the rms-value. Therefore, the on-state loss of the MOSFET in CCM-mode at a junction-temperature of 125°C is:

$$P_{cond} = I_{in\_RMS}{}^2 \cdot D_{on} \cdot R_{dson(125°C)} \quad (6)$$

The MOSFET switching loss can be estimated as:

$$P_{turn\_on/off} = \frac{1}{6} \cdot V_{ds} \cdot I_{drain} \cdot \frac{T_{on/off}}{T_{SW}} \quad (7)$$

For 300W design, if IPP60R199CP is used, the conduction loss is:

$$P_{cond} = 3.92^2 \cdot 0.782 \cdot 0.42 = 5.05W$$

Assume the switching current is about 6A, so the switching loss is:

$$P_{turn\_on} = \frac{1}{6} \cdot \left(\sqrt{2} \cdot 85\right) \cdot 6A \cdot \frac{30ns}{14.9us}$$
$$P_{turn\_on} = 0.242W$$
$$P_{turn\_off} = \frac{1}{6} \cdot \left(\sqrt{2} \cdot 85\right) \cdot 6A \cdot \frac{25ns}{14.9us}$$
$$P_{turn\_off} = 0.202W$$

The total loss is:

$$P_{MOS\_total} = P_{cond} + P_{SW} = 5.494W \quad (8)$$

The required heatsink for the MOSFET is:

$$R_{thHS\_MOS} = \frac{T_{JA\max}}{P_{MOS\_total}} - R_{thJC\_MOS} - R_{thCHS} = \frac{125-70}{5.0623W} - 0.6 - 1 = 9.26K/W \quad (9)$$

R_{thCHS} is the R_{th} of the insulation pad between MOSFET and heatsink.

Gate drive resistance is used to drive MOSFET as fast as possible but also keep dv/dt within EMI specification. In this 300W example, 3.3Ω gate resistor is chosen for IPP60R199CP MOSFET.

Beside gate drive resistance, a 10kΩ resistor is also commonly connected between MOSFET gate and source to discharge gate capacitor.

2.4 Boost Diode

The boost diode D1 has big influence on the system's performance due to the reverse recovery behaviour. So the Ultra-fast diode with very low t_{rr} and Q_{rr} is necessary to reduce the switching loss. The new diode technology of silicon carbide (SiC) Schottky shows its outstanding performance with almost no reverse recovery behaviour. The switching loss due to the boost diode can be ignored with SiC Schottky diode. Only conduction loss is calculated as below.

$$P_{diode} = V_F \cdot I_{in\_RMS} \cdot (1 - D_{on}) = 2V \cdot 3.715A \cdot (1 - 0.7875) = 1.58W \quad (10)$$

To decide the current rating of a SiC diode, there is a rule of thumb - the SiC diode can handle output power P_{OUT} of 100W to 120W in a CCM-PFC-system per one rated ampere. For example, the IDH04S60C from Infineon Technologies is rated at a continous forward current, I_F = 4 A, so it is capable for a system of P_{OUT} = 4*100W = 400W system in minimum. Therefore, this diode should be suitable for the proposed design.
The required heatsink for boost diode is:

$$R_{thHS\_diode} = \frac{T_{J\max} - T_{A\max}}{P_{diode}} - R_{thJC\_diode} - R_{thCHS} = \frac{125-70}{1.58} - 4.1 - 1 = 29.72K/W \quad (11)$$

The SiC boost diodes often have a poor surge current handling capability. Therefore a so called bypass diode is necessary such as the diode D3 as Figure 5. For the proposed system, 1N5408 is suitable.

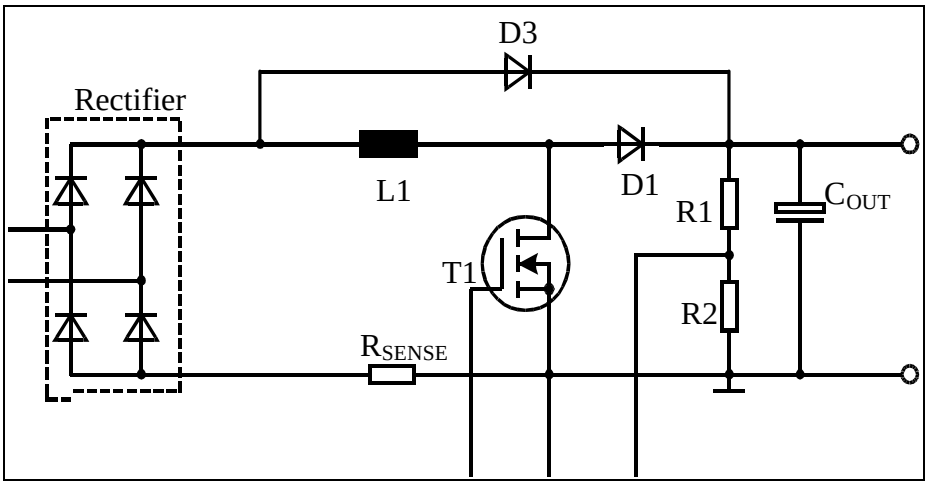

Figure 5 inrush current bypass diode

2.5 Boost inductor

The peak current that the inductor must carry is the peak line current at the lowest input voltage plus the high frequency ripple current. The high frequency ripple current peak to peak, I_{HF}, can be related to maximum input power and minmum input voltage as equation below.

$$I_{HF} = k \cdot \sqrt{2} \cdot \frac{P_{IN\_MAX}}{V_{IN\_MIN}} \tag{12}$$

Where, k must be kept reasonably small, and is usually optimized in the range of 15% to 40% for cost effective design based on the current magnetic component status. If k is too high, the larger AC input filter is required to filter out this ripple noise. If k is too low, the value of the inductance is too large and leads to big size of the magnetic core.

For example, we choose k = 40%, then:

$$I_{HF} = 40\% \cdot \sqrt{2} \cdot \frac{\left(\frac{300}{95\%}\right)}{85} = 2.1A$$

The peak current passing through inductor is:

$$I_{L\_pk} = I_{in\_peak} + \frac{I_{HF}}{2} = 5.25 + \frac{2.1}{2} = 6.3A \tag{13}$$

The boost choke inductance must be

$$L_{boost} \geq \frac{D \cdot (1-D) \cdot V_{out}}{I_{HF} \cdot f_{SW}} \tag{14}$$

D=0.5 will generate the maximum value for the above equation.

$$L_{boost} \geq \frac{0.5 \cdot (1-0.5) \cdot 400V}{2.1A \cdot 65kHz} = 732.6\mu H$$

The magnetic core of the boost choke can be either magnetic powder or ferrite material.

The copper loss of the winding wire can be calculated on I_{in_RMS}.

$$P_{L\_boost} = I_{in\_RMS}^{2} \cdot R_{L\_boost} \tag{15}$$

Select the proper wire type to fullfil the loss and thermal requirement for the choke.

2.6 AC line current filter

As decribed in section 2.5, there is high frequency ripple current peak to peak I_{HF} passing through boost choke. This ripple will also go into AC line power network. The current filter is necessary to reduce the amplitude of high frequency current component. The filtering circuit consists of a capacitor and an inductor as shown in Figure 6.

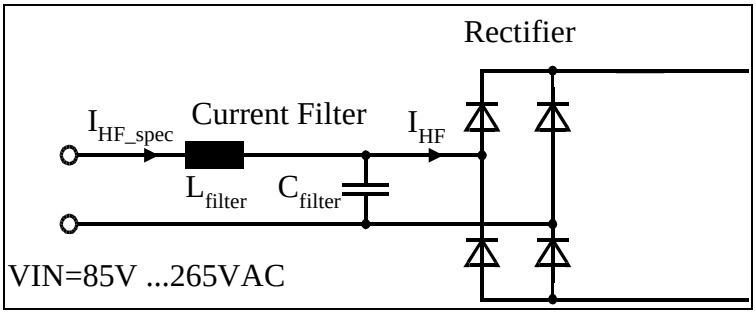

Figure 6 AC line current filter

The required L_{filter} is:

$$L_{filter} \geq \frac{\frac{I_{HF}}{I_{HF\_spec}} + 1}{(2\pi f_{SW})^2 C_{filter}} \tag{16}$$

Normally there is one EMI X2 capacitor which can act as C_{filter}. In this example, if we define I_{HF_spec} as 0.2A peak to peak and asumming X2 capacitances 0.68μF, then:

$$L_{filter} \geq \frac{\frac{2.1A}{0.2A} + 1}{(2\pi \cdot 65kHz)^2 \cdot 0.68\mu F} = 102\mu H$$

The leakage inductance of EMI common mode choke can be used for current filter. If the leakage inductance is large enough, no need to add the additional differential mode inductor for filtering. Otherwise, a current filter choke is necessary. The calculation method for the current filter choke is the same as for boost choke.

2.7 Boost Output Bulk Capacitance

The bulk capacitance has to fullfil two requirements, output double line frequency ripple and holdup time.

2.7.1 Output double line frequency ripple limit.

The inherent PFC always presents 2*f_L ripple. The amplitude of ripple voltage is dependant on output current and bulk capacitance as below.

$$C_{out} \geq \frac{I_{out}}{\pi \cdot 2 * f_L \cdot V_{out\_ripple\_pp}} \tag{17}$$

Where, I_{out} is the PFC output current, $V_{out\_ripple\_pp}$ is the output voltage ripple (peak to peak), and f_L is the AC line frequency.

Please note that ICE3PCxG has enhance dynamic block which is active when Vout exceed ±5% of regulated level. The enchance dynamic block should be designed to work only during load or line change. During steady state with constant load, enhance dynamic block should not be triggered, otherwise THD will be deteriorated. That means the target $V_{out\_ripple\_pp}$ must be lower than 10% of V_{out}. For this example, Vout=400VDC, then $V_{out\_ripple\_pp}$ must be lower than 40V. If we define $V_{out\_ripple\_pp}$=12V, then

$$C_{out} \geq \frac{0.75A}{\pi \cdot 2 \cdot 50Hz \cdot 12V} = 199\mu F \tag{18}$$

2.7.2 Holdup time requirement

After the PFC stage, there is commonly a PWM stage to provide isolated DC output for end user. Some applications, especially computing, have the holdup time requirement. It means that PWM stage should be able to provide the isolated output even if AC input voltage become zero for a short holdup time. The common specification for this holdup time is 20ms. If minimum input voltage for PWM stage is defined as 250VDC, then the bulk capacitance will be:

$$C_{out} \geq \frac{2 \cdot P_{out} \cdot t_{holdup}}{V_{out}^{\ 2} - V_{out\_\min}^{\ 2}} = \frac{2 \cdot 300W \cdot 20ms}{390^2 - 250^2} = 134\mu F \tag{19}$$

The final C_{out} capacitance should be higher value calculated from the above two requirements. So, 220µF is choosen for C9.

2.8 Current Sense Resistor

The current sense resistance is calculated based on the IC peak current limitation (PCL) protection carried by boost choke.

When the Isense signal reaches the PCL threshold, IC's gate switching will shut down. Finally the boost choke current is limited. According to IC datasheet, PCL threshold is -0.2V for ICE3PCS01G and -0.4V for ICE3PCS02/3G. So the current sense resistor for ICE3PCS01G should be:

$$R_{SHUNT} \leq \frac{0.2V}{I_{L\_pk}} = \frac{0.2V}{6.3A} = 0.0317\Omega \tag{20}$$

And the current sense resistor for ICE3PCS02/03G should be:

$$R_{SHUNT} \le \frac{0.4V}{I_{L\_pk}} = \frac{0.4V}{6.3A} = 0.063\Omega \quad (21)$$

So, 0.03Ω for ICE3PCS01G and 0.06Ω for ICE3PCS02/03G is choosen for respective R_{SHUNT}.

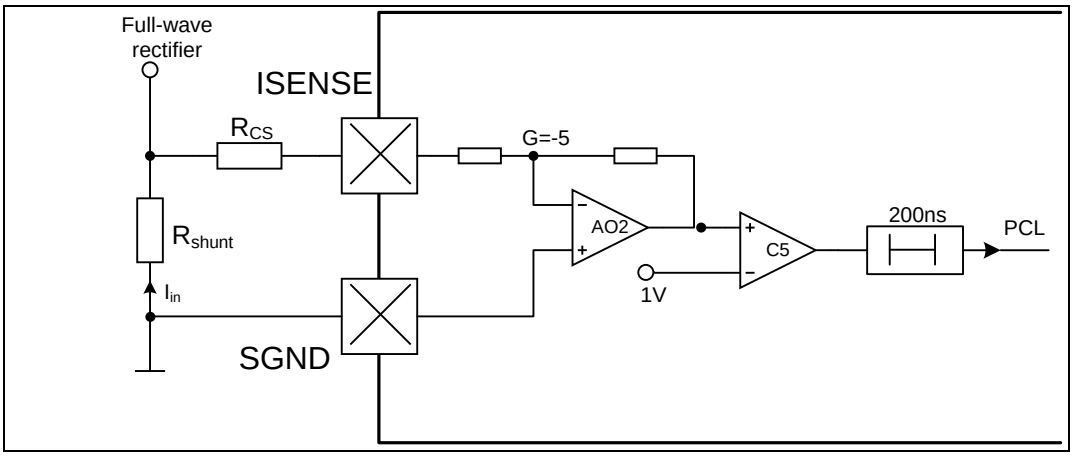

Figure 7 Peak Current Limitation ICE3PCS01G

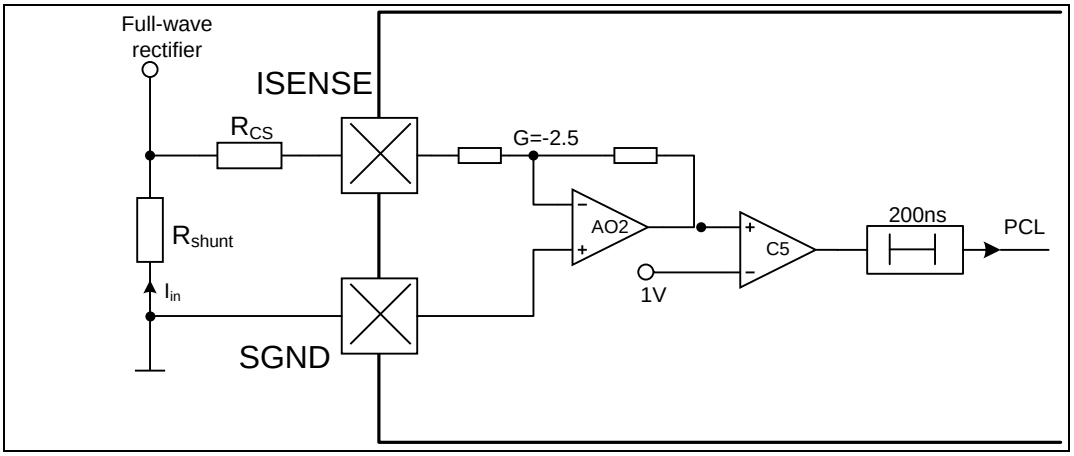

Figure 8 Peak Current Limitation ICE3PCS02/03G

According to Figure 2, Figure 3 and Figure 4, the transistor current as well as the diode current flows through R_{SHUNT}. That means when AC input voltage appear, a large negative voltage drop at R_{SHUNT} will be observed. This will induce large inrush current therefore it is necessary to limit the current into pin ISENSE which is realized with resistor R_{CS}. A value of R_{CS} = 68Ω is sufficient for this resistor.

2.9 Output voltage sensing divider

The output voltage is set with the voltage divider represented by $R_{BVS1/2}$ and R_{BVS3} in Figure 2, Figure 3 and Figure 4. In Figure 9 shows the simplified circuit at VSENSE pin with R3 as the internal impedance due to the bias current.

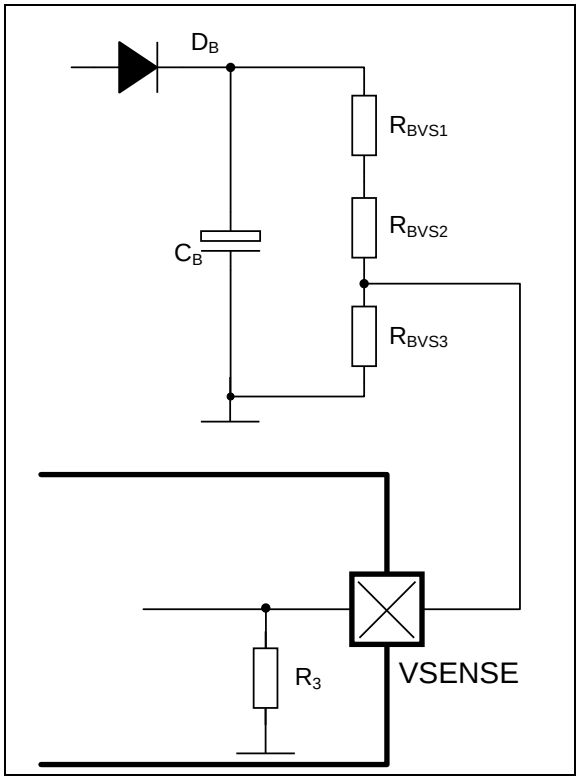

Figure 9 Simplified circuit at Vsense pin

Due to the variation of the bias current, IVSENSE from 0A ~1μA (from ICE3PCS0XG datasheet), the internal impedance R3 is variable from 2.5V/1uA=2.5Mohm (when IVSENSE=1μA) to ∞ (infinity when IVSENSE=0), which affects the accuracy of the bus voltage. The IC internal reference voltage for voltage sensing is 2.5V typical.

Therefore, the maximum to the bias current value of the resistors $R_{BVS1/2}$ and R_{BVS3} can be decided based on the two specifications:

1. The bias current.
2. The maximum allowable bulk voltage variation due to bias current.

For ICE3PCS0XG,

$$V_{BULK} = \frac{R_{BVS3} + R_{BVS1/2}}{R_{BVS3}} \times 2.5 \text{ (when } I_{VSENSE}=0) \quad (22)$$

$$V_{BULK} = \frac{R_{BVS3} // R_3 + R_{BVS1/2}}{R_{BVS3} // R_3} \times 2.5 \text{ (when } I_{VSENSE} \neq 0)$$

If we assume $R_{BVS1/2} = kR_{BVS3}$, and bus voltage variation caused is $\triangle V_{BULK}$, then:

$$\Delta V_{BULK} = \frac{R_{BVS3} // R_3 + R_{BVS1/2}}{R_{BVS3} // R_3} \times 2.5 - \frac{R_{BVS3} + R_{VBS1/2}}{R_{VBS3}} \times 2.5$$

$$\Delta V_{BULK} = 2.5 \cdot k \cdot \frac{R_{BVS3}}{R_3} \quad (23)$$

From (23), we get:

$$R_{BVS3} = \frac{\Delta V_{BULK} \cdot R_3}{2.5 \cdot k}$$

Here is an example. For ICE3PCS0XG, if V_{BULK}=400V, and the allowable bus voltage variation caused is 2%, $\Delta V_{BULK} = 400 \times 0.02 = 8V$, then k can be calculated from (22), $k = \frac{R_{BVS1/2}}{R_{BVS3}} = 160$, and R_{BVS3}=20.6kΩ (this resistor value is obtain from boost follower section using formula (28)),

$$R_{BVS1/2} = k \cdot R_{BVS3} = 160 \times 20.6k\Omega = 3.3M\Omega$$

It is recommended to take resistor values with a tolerance of 1% for $R_{BVS1/2}$ and R_{BVS3} and due to the voltage stress of $R_{BVS1/2}$, it is recommended to split this value into few resistors in series.

2.10 Second Over Voltage Protection (OVP2)

This function is only available in ICE3PCS01/02G. This second over voltage protection, OVP2, is provided in case that the first over voltage protection, OVP1, fails due to aging or incorrect resistor connected to the pin VSENSE. This is implemented by sensing the voltage at pin OVP is higher than 2.5V is shown in Figure 10, the IC will immediately turn off the gate, thereby preventing damage to bus capacitor.

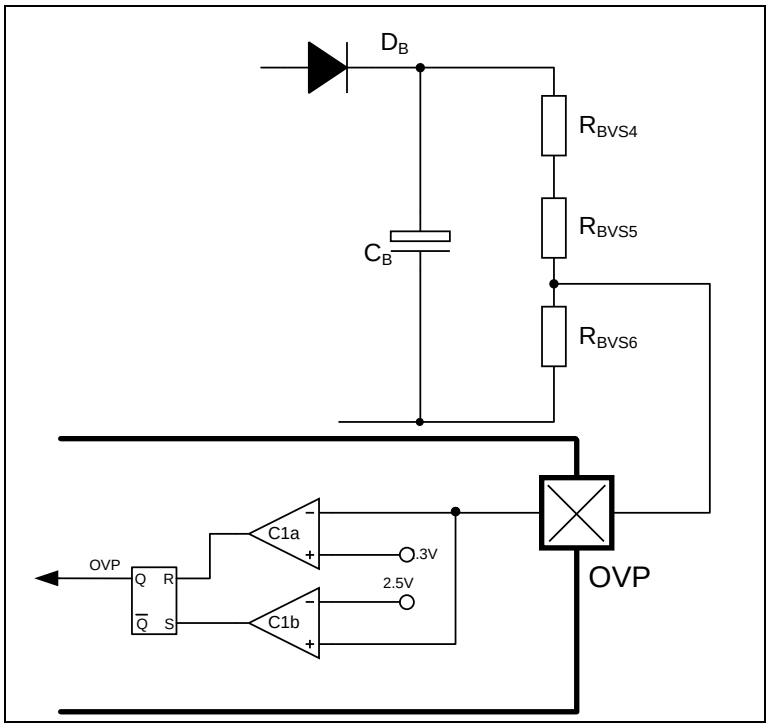

Figure 10 Second Over Voltage Protection block diagram

For ICE3PCS01G; when the bulk voltage drops out of the hysteresis, the IC can be latched further or begin auto softstart. These two protection modes are distinguished through detecting the external equivalent resistance connecting to pin VBTHL_EN after VCC is higher than UVLO threshold shown in Figure 11.

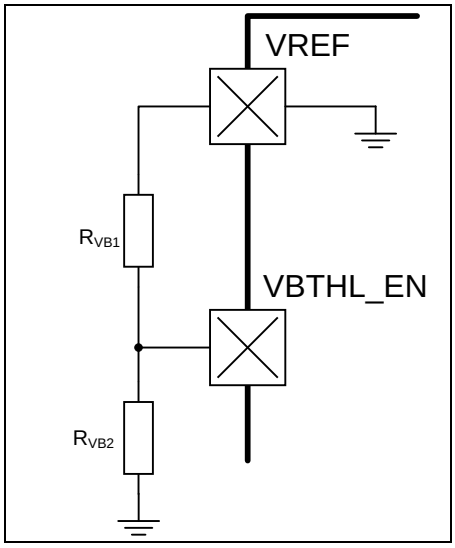

Figure 11 OVP2 mode setting

If the equivalent resistance is higher than 100kΩ the IC selects latch mode for second OVP, otherwise auto soft-start mode. Note that during the OVP2 mode selection, voltage at pin VREF is 0V shown in Figure 11.

So the equivalent resistance at pin VBTHL_EN:

$$R_{Equivalent} = \frac{1}{\frac{1}{R_{VB1}} + \frac{1}{R_{VB2}}} \tag{24}$$

In normal operation the trigger level of OVP2 should be designed higher than the first OVP. However in the condition of mains transient overshoot the bulk voltage may be pulled up to the peak value of mains that is higher than the threshold of OVP1 and OVP2. In this case the OVP1 and OVP2 are triggered in the same time the IC will shut down the gate drive until bulk voltage falls out of the two protection hysteresis, then resume the gate drive again.

Condition	Default Mode	Alternative Mode
	$R_{Equivalent}$<100kΩ	$R_{Equivalent}$ >100kΩ
OVP2 detected after OVP1 detected	Gate disable (IC resumes regulation as soon as OVP2 is not detected anymore)	
OVP2 detected without OVP1 detected	Gate disable The IC auto softstart as soon as OVP2 is not detected anymore	Gate disable IC latched until next UVLO

Table 2 OVP2 Mode Selection and Respone

In ICE3PCS02G, when the bulk voltage drops out of the hyterisis, the IC will begin auto softstart.

2.11 VBTHL_EN

The pin VBTHL_EN is only available in ICE3PCS01G. The pin VBTHL_EN defines the OVP2 mode selection and the threshold to trigger the low level at pin VB_OK which can be adjustable externally shown in Figure 12.

Assume R_{VB1}=330kΩ and R_{VB2}=200kΩ. During normal operation, the voltage at pin VBTHL_EN:

$$V_{VBTHL\_EN} = \frac{R_{VB2}}{R_{VB1} + R_{VB2}} \cdot 5V$$

$$V_{VBTHL\_EN} = \frac{200k\Omega}{330k\Omega + 200k\Omega} \cdot 5V$$

$$V_{VBTHL\_EN} = 1.89V$$

So, if the voltage at pin VSENSE is lower than 1.89V, pin VB_OK signal will pull low.

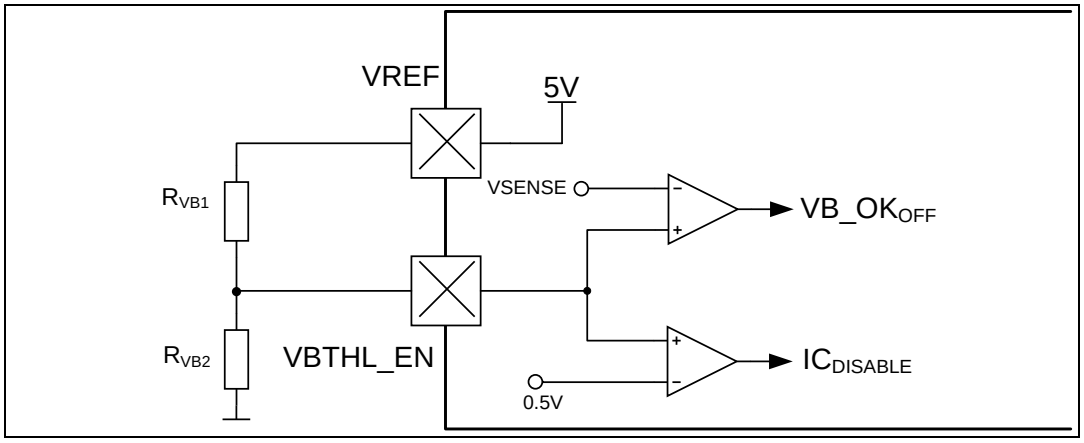

Figure 12 Resistor-frequency characteristic

When pin VBTHL_EN is pulled down externally lower than 0.5V, IC will enters into standby mode and most of the function blocks are turned off. When the disable signal is released the IC recovers by soft-start.

2.12 Frequency setting

The switching frequency can be adjusted between 50kHz~100kHz by external resistance at pin FREQ. The typical curve for switching frequency Vs. R_{FREQ} resistance is shown in Figure 13. The R_{FREQ} programs a current which controls the oscillator.

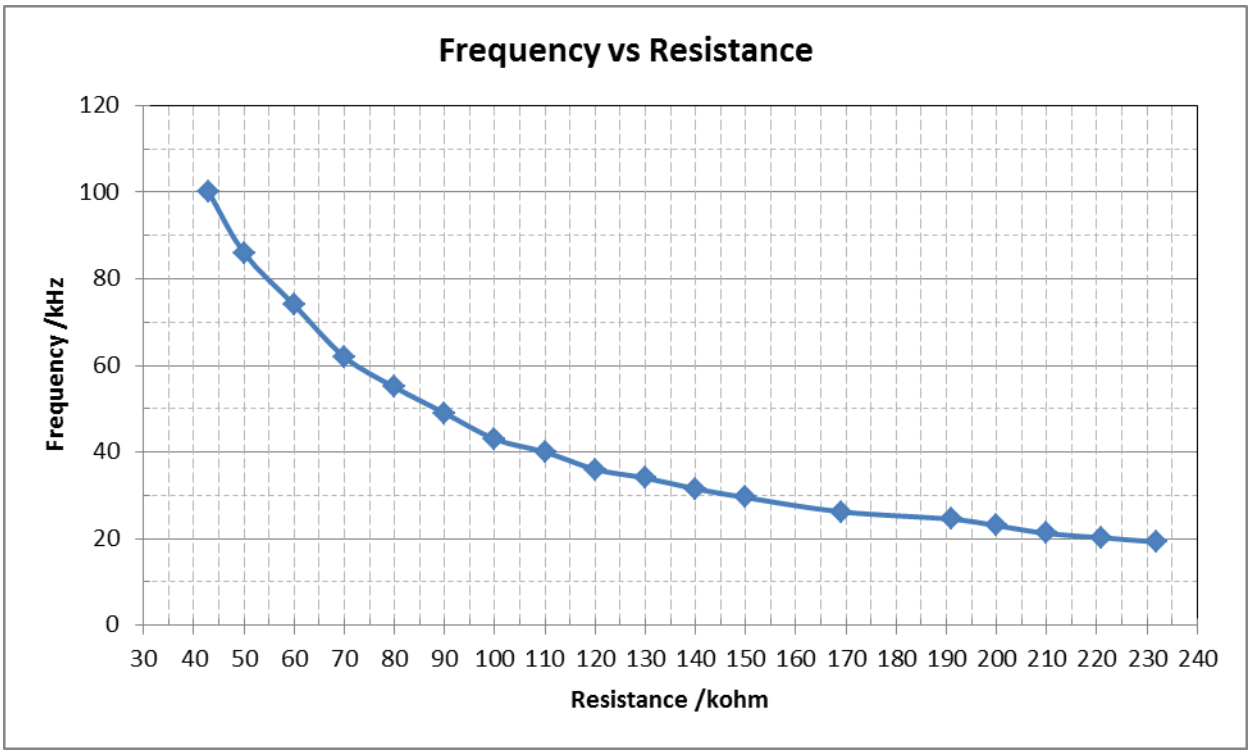

Figure 13 Resistor-frequency characteristic

2.13 Synchronous Frequency

After choosing the switching frequency for the PFC converter, R_{FREQ} is set. For synchronization, R_{SYN} has to be calculated with the information of R_{FREQ} and the synchronous clock high voltage, V_X. A diode is added in to prevent current flowing through R_{SYN} when there is no synchronous clock.

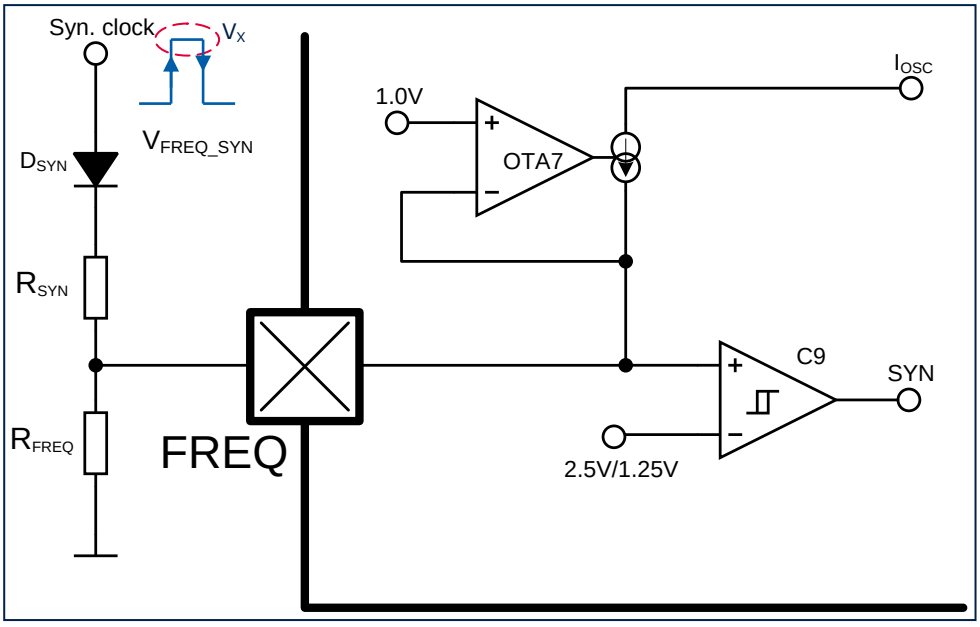

Figure 14 Frequency setting and synchronization

If we want the voltage at pin FREQ (V_{FREQ_SYN}) to be 5V when synchronous clock is high, V_X and now we are able to calculate R_{SYN} with the formula below:

$$R_{SYN} = \frac{R_{FREQ}}{\left\{\frac{5}{V_X - 0.7V}\right\}} - R_{FREQ} \quad (25)$$

$$R_{SYN} = \frac{68K}{\left\{\frac{5}{15 - 0.7V}\right\}} - 68K$$

$$R_{SYN} = 126.5k\Omega$$

130kΩ is selected for R_{SYN}.

2.14 Brown-Out Protection (BOP)

Brown-out protection (BOP) function is available for ICE3PCS01G and ICE3PCS03G. BOP occurs when the input voltage VAC falls below the minimum input voltage of the design (i.e. 85V for universal input voltage range) and the VCC has not entered into the VCCUVLO level yet. For a system without input brown out protection, the boost converter will increasingly draw a higher current from the mains at a given output power which may exceed the maximum design values of the input current and lead to overheat of MOSFET and boost diode. ICE3PCS01G and ICE3PCS03G provides a BOP feature whereby it senses directly the input voltage for Input Brown-Out condition via an external resistor/capacitor/diode network as shown in Figure 15. This network provides a filtered value of V_{IN} which turns the IC on when the voltage at BOP is more than 1.25V. The IC enters into the standby mode and gate is off when when voltage at pin BOP goes below 1.0V. The hysteresis prevents the system to oscillate between normal and standby mode.

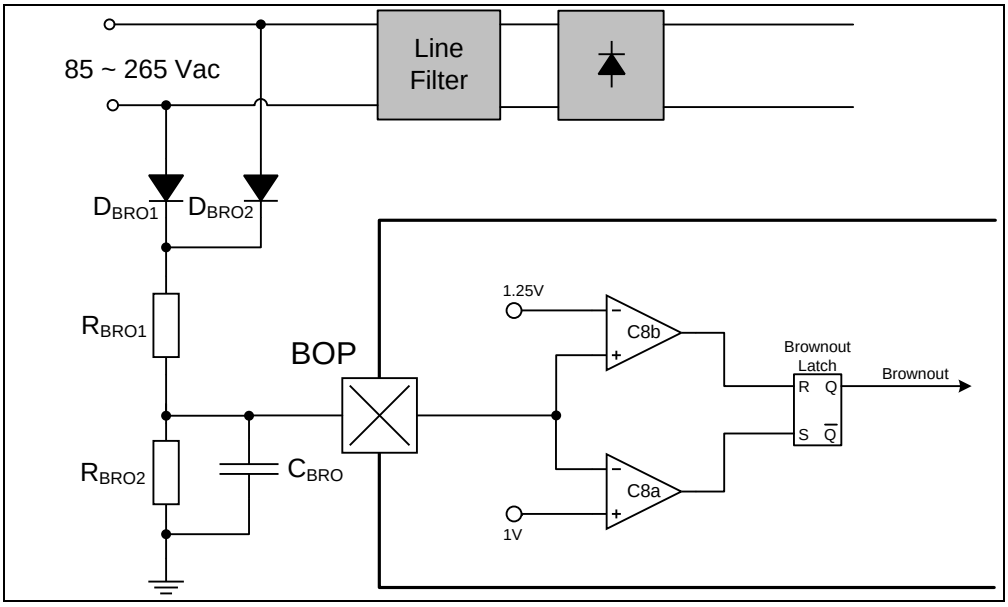

Figure 15 Block diagram Brown out Protection

Because of the high input impedence of comparator of C8a and C8b, R_{BRO1} can be high ohmic resistance to reduce the loss. From the datasheet, the bias current on V_{IN} pin is 0.5μA maximum. In order to have the design consistence, the current passing through R_{BRO1} and R_{BRO2} has to be much higher than this bias current, for example 8μA. Then R6 is:

$$R_{BRO2} = \frac{1V}{8uA} = 125k\Omega$$

130kΩ is selected for R_{BRO2}.

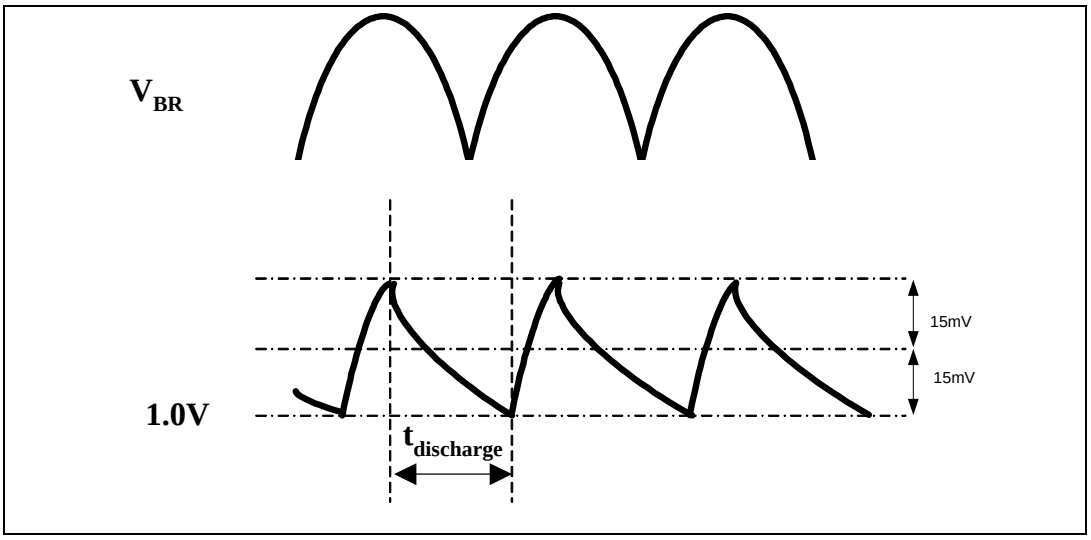

Figure 16 Timing diagram of BOP Pin when IC enters brown-out shutdown

If the bottom level of the ripple voltage touches 1.0V, PFC is in standby mode and gate is off. The datasheet shows the IC has tolerance ±2% or ±20mV detection in ripple voltage defines PFC brown out off. Therefore C_{BRO} is used to modulate the ripple at the pin BOP to achieve smaller than 30mV.

$$(V_{ripple}) \cdot e^{-\frac{t_{discharge}}{R_6 C_4}} = 1.0V \tag{26}$$

Assuming $t_{discharge}$ is equal to half cycle time of line frequency, ie. $t_{discharge} = \frac{1}{2 f_L}$, then:

$$C_4 = \left(2 \cdot f_L \cdot R_6 \cdot \ln \frac{V_{ripple}}{1.0V} \right)^{-1}$$

$$C_4 = \left(2 \cdot 50Hz \cdot 130k\Omega \cdot \ln \frac{1.03V}{1.0V} \right)^{-1} = 2.602\mu F$$

So, C_{BRO} of 3uF is chosen.

RBRO1 is selcted by:

$$R_{BRO1} = \frac{\sqrt{2} \cdot V_{AC\_on} - 0.7V - 1.25V}{1.25V} \cdot R_{BRO2} \tag{27}$$

Where, V_{AC_on} is the minimum AC input voltage (RMS) to start PFC, for example 70VAC.

$$R_{BRO1} = \frac{\sqrt{2} \cdot 70V - 0.7V - 1.25V}{1.25V} \cdot 130k\Omega = 10.09M\Omega$$

Due to the voltage stress of R_{BRO1}, it is recommended to split this value into few resistors in series.

2.15 Boost Follower Mode

The IC provides adjustable lower bulk voltage in case of low line input and light output power. The low line condition is determined when pin BOP voltage is less than 2.3V. Pin BOFO is connected to PWM feedback voltage through a voltage divider, representing the output power. The light load condition is determined when pin BOFO voltage is less than 0.5V. Once these two conditions are met in the same time, a 20µA current source is flowing out of pin VSENSE so that the bulk voltage should be reduced to a lower level in order to keep the VSENSE voltage same as the internal reference 2.5V as shown in Figure 17.

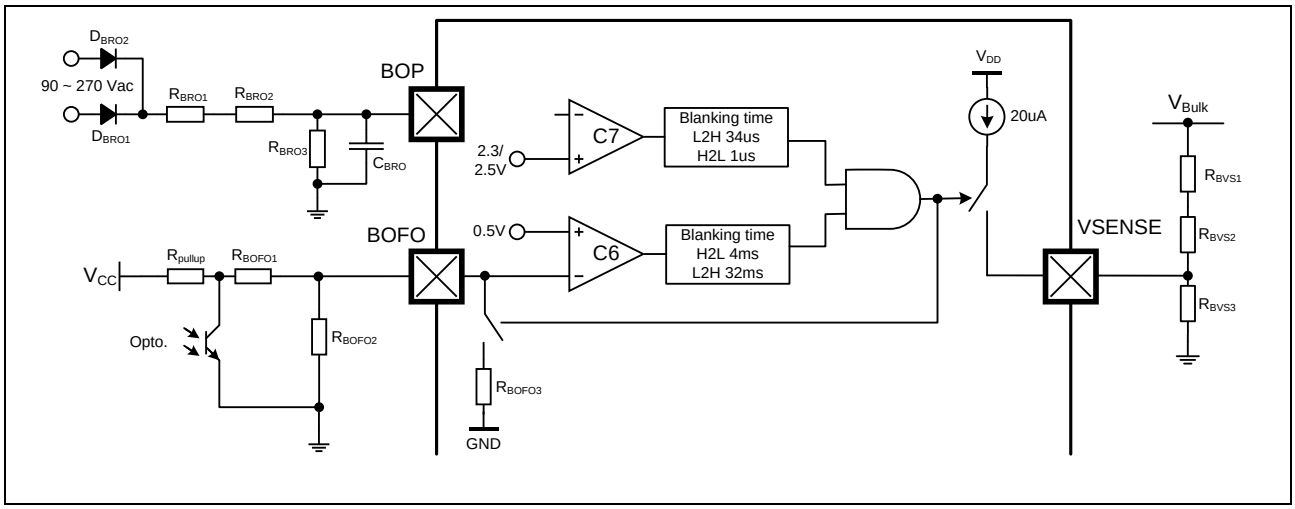

Figure 17 Boost Follower Function

The reduced bulk voltage can be designed by upper side resistance of voltage divider from pin VSENSE. Thus the low side resistance is designed by the voltage divider ratio from the reference 2.5V to the rated bulk voltage.

The boost follower feature will be disabled internally during PFC soft-start in order to prevent bulk voltage oscillation due to the unstable PWM feedback voltage. This feature can also be disabled externally by pulling up pin BOFO higher than 0.5V continuously.

The bulk voltage level during boost follower mode is defined by R_{BVS3}. Below is the simplified formula:

$$R_{BVS3} \approx \left\langle \left\{ 1 - \left[\frac{< BF'sBulkVoltage >}{BulkVoltage} \right] \right\} \times 2.5V \right\rangle / 20uA \quad (28)$$

BF's Bulk Voltage = bulk voltage level during boost follower mode

= 334V

Bulk Voltage = 400V

So, with the information above, we can now calculate R_{BVS3}.

$$R_{BVS3} \approx \left\langle \left\{ 1 - \left[\frac{334}{400} \right] \right\} \times 2.5V \right\rangle / 20uA$$

$$R_{BVS3} \approx 20.6k\Omega$$

An internal 300kW resistor will be paralleled with external low side resistor of BOFO pin to provide the adjustable hysteresis for PWM feedback voltage when boost follower is activated shown below in Figure 18.

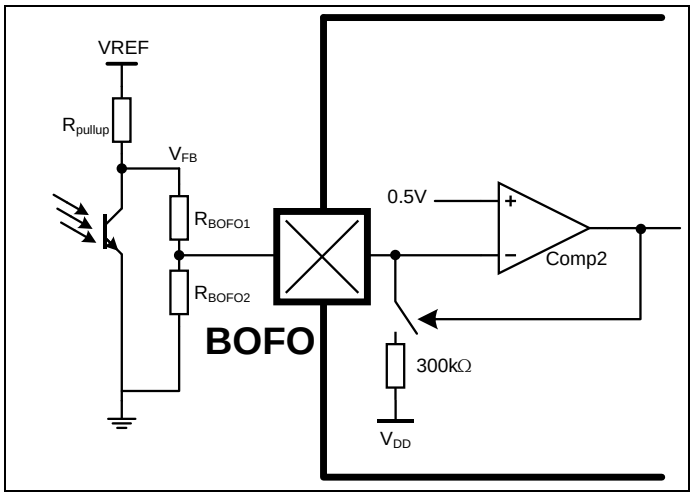

Figure 18 BOFO block diagram

Assume R_{BOFO1}=R_{BOFO2}=300kΩ, to activate the boost follower, voltage at V_{FB}:

$$V_{FB} = 0.5 \cdot \frac{R_{BOFO1} + R_{BOFO2}}{R_{BOFO2}} \tag{29}$$

$$V_{FB} = 1V$$

When boost follower is activate, the voltage at pin BOFO drop. This hysteresis is asjustable by changing the R_{BOFO2} resistor value. With current design where R_{BOFO1}=R_{BOFO2}=300kΩ. The new R_{BOFO2}:

$$R_{BOFO2} = 300k\Omega // 300k\Omega$$

$$R_{BOFO2} = 150k\Omega$$

The R_{BOFO2} become smaller when boost follower is activated. So the new voltage at pin BOFO:

$$V_{BOFO} = \frac{150k\Omega}{150k\Omega + 300k\Omega} \cdot 1V \tag{30}$$

$$V_{BOFO} = 0.33V$$

The pin BOFO hysteresis for boost follower mode = 0.5V – 0.33V

=0.17V

2.16 Current Averaging Circuit

IC sense the boost inductor current via shunt resistor, R_{SHUNT} as shown in Figure 2. The sensing signal is sent to ISENSE pin. As the voltage in Isense Pin is negative signal together with switching ripple, IC need to do signal averaging and convert the polarity to positive for following PWM modulation blocks. The output of averaging block is V_{icomp} voltage at ICOMP pin. The block diagram of current averaging block is shown in Figure 19.

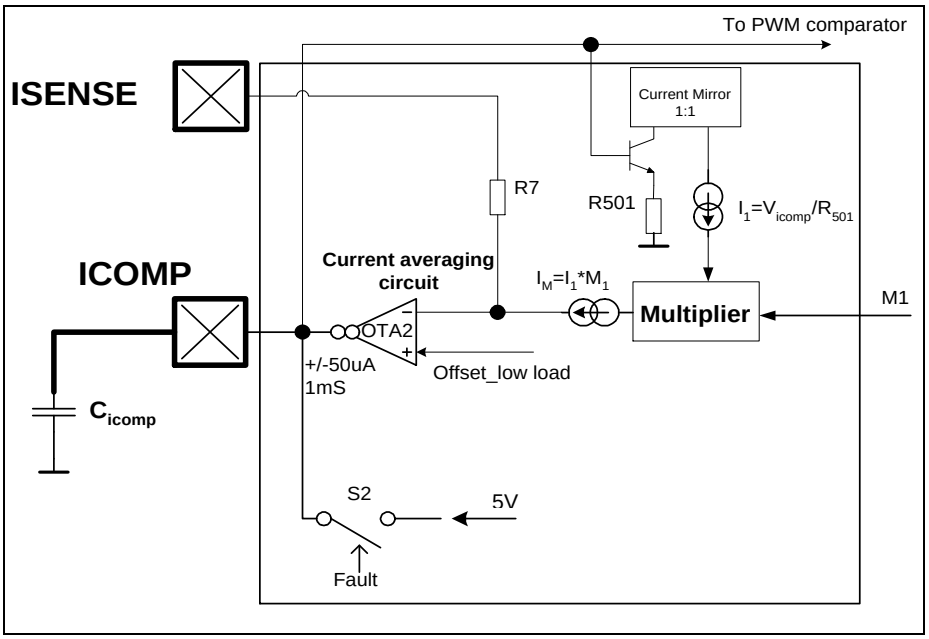

Figure 19 current averaging block diagram

The transfer function of averaging circuit block can be derived as below.

$$K_{AVE}(s) = \frac{V_{icomp}}{i_L} = \frac{\frac{K_1 R_{SHUNT}}{M_1}}{1 + s \cdot \frac{K_1 C_{icomp}}{M_1 g_{OTA2}}} \tag{31}$$

where, K_1 is a ratio between R501 and R7 which is equal to 4 (tolerance +/-2%), C_{icomp} is the capacitor at Icomp Pin, g_{OTA2} is the trans-conductance of the error amplifier of OTA2 for current averaging, typical 5.0mS as shown in Datasheet, M1 is the variable controlled by voltage loop (largest variable for M1 is M1=1).

The function of the averaging circuit is to filter out the switching current ripple. So the corner frequency of the averaging circuit f_{AVE} must be lower than the switching frequency f_{SW}. Assuming f_{AVE}=32kHz which is 2 times less than switching frequency 65kHz, then,

$$C_{icomp} \geq \frac{g_{OTA2} M_1}{K_1 \cdot 2\pi f_{AVE}}$$

$$C_{icomp} \geq \frac{(5mS)1}{4 \cdot 2\pi 32kHz}$$

$$C_{icomp} \geq 6.2nF$$

2.17 IC supply

The IC supply voltage operating range is 11V~25V.

There are two stages during IC turned on. First Vcc capacitor is charged from 0V to 7V, the IC internal regulator block starts to reset voltage at all external pins. The reset process will take about 10us. And then when Vcc voltage is charged to Vcc_on threshold, IC starts the soft start with gate switching. In the case of Vcc decoupling capacitance is too low such as 0.1uF, Vcc voltage may be charged up too fast and the time interval from Vcc=7V to Vcc_on is less than the reset time. Then the IC will not go through a proper soft start as the voltages at IC pins are not yet properly reset. To avoid such a problem, the delay circuitry is needed.

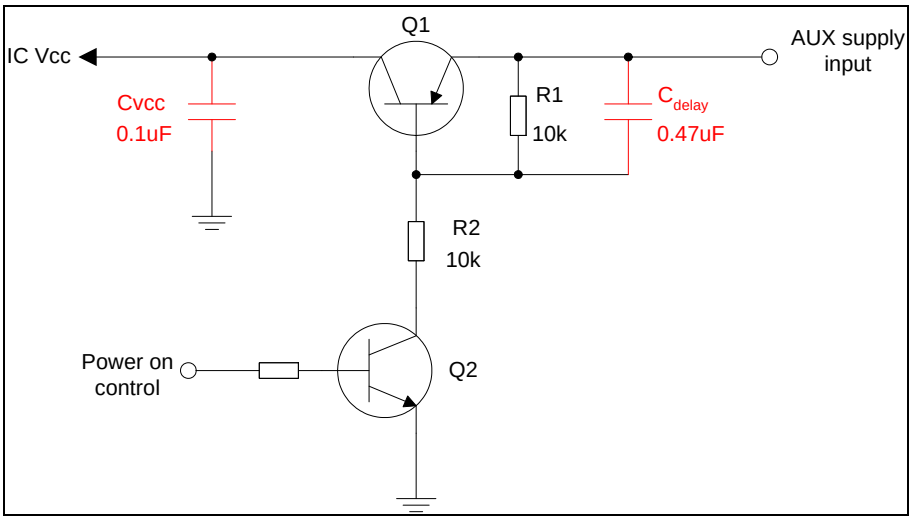

Figure 20 Vcc supply circuitry

Figure 20 is a typical circuitry to supply PFC controller. Q2 is NPN transistor and controlled by external "Power on" signal. When "Power on" signal is "high", Q2 is turned on provides base current for Q1. Q1 is turned on accordingly to supply auxiliary power to IC Vcc. The reset delay time is adjustable by changing the RC time constant of R1, R2 and C_{delay}. The recommended values are shown in Figure 20 as 10kΩ, 10kΩ and 0.47uF respectively.

The same reset process also happens during IC power down when Vcc is discharged from Vcc_off to 7V. The reset time for power down is around 200us. Because IC is in power down mode with very low current consumption, typically 650uA only, the required Vcc capacitance for power down reset can be calculated as:

$$C_{VCC} \geq \frac{I_{power\_down\_max} \cdot t_{reset}}{V_{cc\_off\_min} - V_{reset}} = \frac{650\mu A \cdot 200\mu s}{11V - 7V} = 32.5nF \quad (32)$$

So the common Vcc decoupling capacitance 0.1uF is enough for reset delay requirement.

3 PCB layout guide

In order to avoid crosstalk on the board between power and signal path, and to keep the IC GND pin as “clean” from noise as possible, the PCB layout for GND must be taken care of properly. Below are some suggestions for GND connections and together with Figure 21 below illustrates as a good example.

(1) Star connection rules for main power stage GND: the PCB tracks of MOSFET source, output load PGND, SGND, IC auxiliary supply GND and shunt resistor are separated and connected together at bulk capacitor negative Pin.

(2) Star connection rules for SGND: the IC external components which need to be connected to the SGND bus highlighted in red color. Such SGND bus is connected to IC SGND pin.

(3) Connection between main power stage GND and IC GND: in Figure 21, the single PCB track in pink color directly connects IC GND pins to power stage star connection point - bulk capacitor negative. This is to ensure that the voltage between ISENSE pin and SGND pin does not observe the switching rectangular noise current. The dark green and blue tracks denote for flowing paths of high frequency rectangular switching current.

(4) VCC decoupling capacitor C_{VCC}: the decoupling capacitor need to be placed close to IC VCC and GND pins as much as possible. The GND track of C_{VCC} (green color in Figure 21) should be connected at the point on the single PCB track connecting between IC SGND pin and PGND point so that the large gate charging current will not pass through the SGND bus.

(5) VSENSE capacitor C_{VSENSE}: to reduce noise in VSENSE pin, small capacitor up to 0.01uF can be added between VSENSE pin and SGND bus.

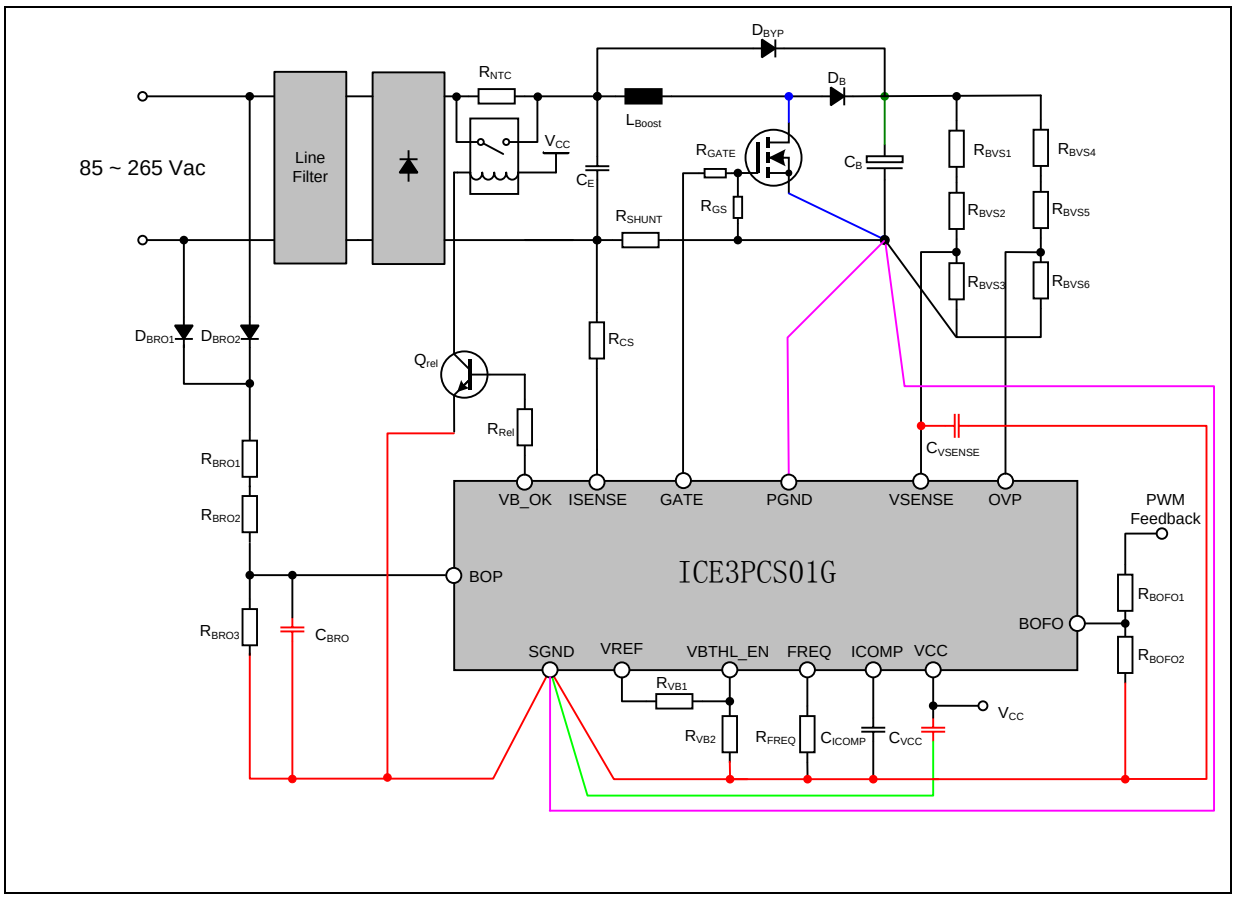

Figure 21 Good PCB layout illustration

References

[1] Infineon Technologies: ICE3PCS01G - Standalone Power Factor Correction Controller in Continuous Conduction Mode; Preliminary datasheet; Infineon Technologies; Munich; Germany; May. 2010.

[2] Infineon Technologies: ICE3PCS02G - Standalone Power Factor Correction (PFC) Controller in Continuous Conduction Mode (CCM) at Fixed Frequency, Preliminary datasheet; Infineon Technologies; Munich; Germany; May. 2010.

[3] Lim Teik Eng, Liu Jianwei, Li Dong, 300W CCM PFC Evaluation Board with ICE3PCS01G, CoolMOS™ and SiC Diode thinQ!™, Application note, Infineon Technologies, Munich, Germany, Aug. 2010.

[4] Luo Junyang, Liu Jianwei, Jeoh Meng Kiat, ICE2PCSxx Based Boost Type CCM PFC Design Guide - Control Loop Modeling, Application note, Infineon Technologies, Munich, Germany, May, 2008.