XDPL8220 – Digital PFC+Flyback Combo IC

XDP™ Digital Power

Design Guide of a High Performance AC/DC-DC Converter for LED Lighting

About this document

Scope and purpose

This document is a step-by-step guide for designing high-performance dual-stage digital PFC+Flyback AC-DC converter using the Infineon XDPL8220 controller for LED lighting applications. The document also describes parameter handling for typical use cases using the Infineon .dp Vision tool for the Infineon XDPL8220.

Intended audience

This document is intended for anyone wishing to design high-performance dual-stage digital PFC+Flyback AC/DC-DC converter for LED lighting based on the digital controller IC XDPL8220.

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1 Introduction

The digital controller IC XDPL8220 belongs to the Infineon XDP™ digital power family generation 2.0. It provides an independent PFC boost and Flyback dual stage control to achieve an output which combines a constant voltage (CV), constant current (CC) and limited Power (LP) for LED luminaires. The IC is available in a PG-DSO-16 package and supports wide features with only a minimum requirement of external components. The digital engine of the IC offers the possibility to configure operational parameters and protection modes, which helps to ease the design phase and allows a reduced number of hardware variants. Accurate primary side output voltage and current control eliminates a secondary side feedback loop.

This design guide provides detailed calculation of major power stage component values, as well as the setting of parameters for general functions and protection features. Useful tips on PCB layout are included to help the customers optimize their PCB design. Finally, the installation and usage of a General User Interface – .dp Vision is described to guide the customer to set parameters for the digital IC. The numeric values below are shown for the 50W reference board with universal input voltage.

1.1 Product Highlights

- Primary side controlled constant voltage (CV), constant current (CC) and limited power (LP) output
- High current accuracy output of typical +/- 2% across universal input voltage range (90 to 305VAC or 90 to 305VDC) and a factor three output voltage range till 48VDC.
- Multi-mode control (QR+DCM) ensures high power efficiency and low dimming output
- High power factor (PF >0.9) and low input current total harmonic distortion (iTHD < 15%) for load from 35% with advanced switching cycle modulation scheme
- Integrated startup cell ensures fast time to light and low power consumption
- Adaptive Temperature Protection
- Parameter configurability using graphic user interface .dp vision.

1.2 Design Features

- Universal AC input (90 - 305VAC) or DC input (90- 305VDC)
- Applicable power range of 30 W to 100 W
- Low Bill of Materials (BOM)

1.3 Target applications

- Electronic control gear (ECG) for LED luminaires (20 W to 100W)

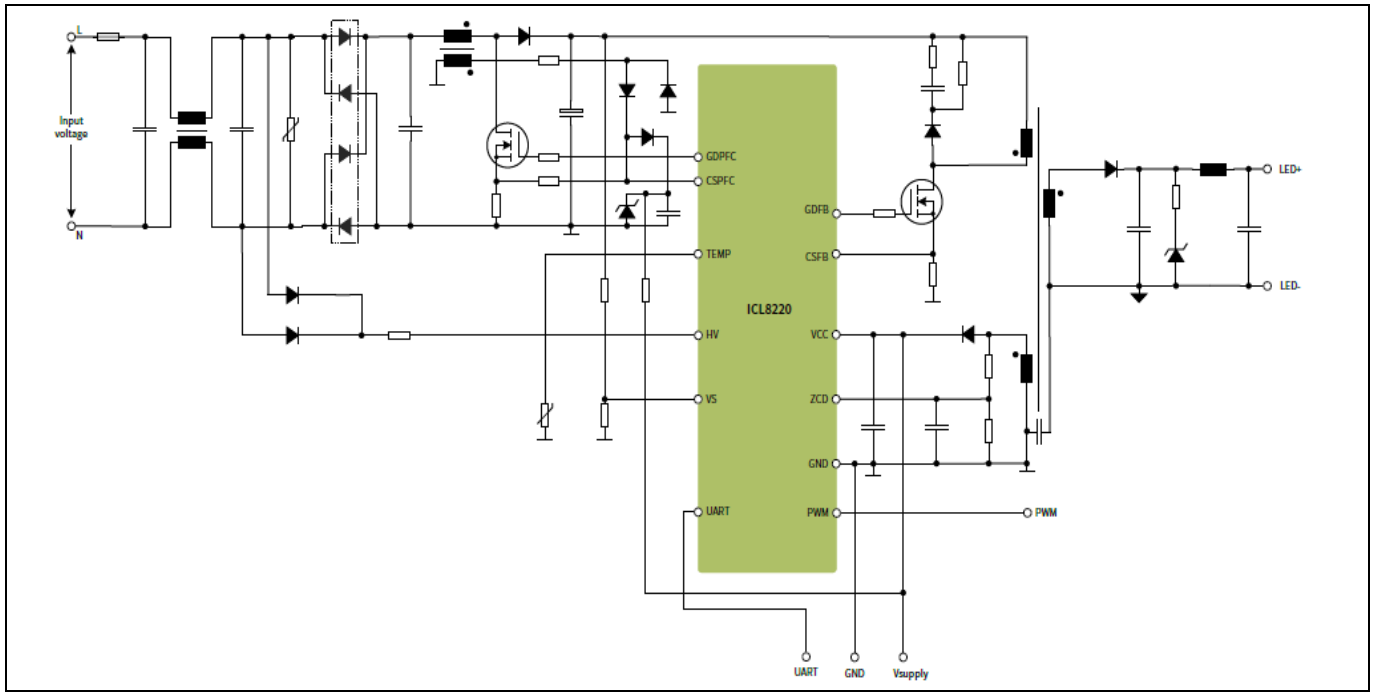
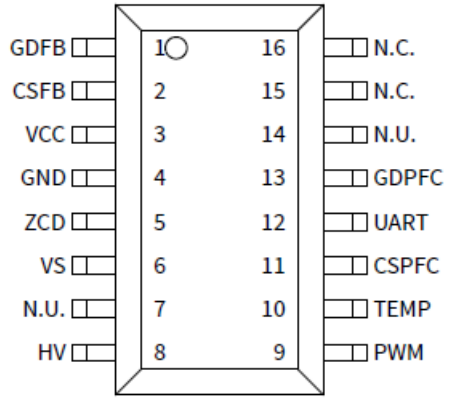


Figure 1 XDPL8220 Typical Application Schematic

1.4 Pin Configuration and Description

Pin assignments and basic pin description information are shown below.



PG-DSO-16(150mil)

Figure 2 Pin Configuration of XDPL8220

Table 1 Pin Definitions and Functions

Name	Pin	Type	Function
GDFB	1	O	**Flyback Gate Drive Output** Output for directly driving a power MOSFET of the Flyback converter via a resistor.
CSFB	2	I	**Flyback Current Sense Input** Connected to an external shunt resistor and the source of a power MOSFET of the Flyback converter.
VCC	3	I	**Positive Power Supply** IC power supply
GND	4	-	**Ground** IC Ground
ZCD	5	I	**Flyback Zero-crossing Detection** Connected to the Flyback auxiliary winding via a resistive divider for zero-crossing detection as well as primary side output voltage sensing for output regulation and backup bus voltage sensing for safety.
VS	6	I	**PFC Voltage Sense** Connected to DC bus via a resistive divider for the PFC boost converter output voltage sensing.
N.U.	7	-	**Not Used**
HV	8	I	**High Voltage Input** Connected to the AC mains via an external resistor. An internal 600V HV startup-cell is used to charge VCC initially. In addition, sampled high-voltage sensing is also used for AC/DC detection and brown-out.
PWM	9	I	**PWM Dimming** The PWM pin is used as a dimming input.
TEMP	10	I	**External Temperature Sensor** Connected to an external NTC resistor to sense the environment temperature.
CSPFC	11	I	**PFC Current Sensing** Connected to an external shunt resistor and the source of a power MOSFET of the PFC boost converter. Additionally, it is connected to the PFC aux winding for zero-crossing detection.
UART	12	I/O	**Universal Asynchronous Receiver Transmitter (UART) Communication** The UART pin is used for the UART interface to support parameterization.
GDPFC	13	O	**PFC Gate Drive Output** Output for directly driving a power MOSFET of the PFC boost converter via a resistor.
N.U.	14	-	**Not Used**
N.C.	15	-	**Not Connected**
N.C.	16	-	**Not Connected**

2 Hardware Design

The hardware design part provides detailed calculation of power component values as well as the setting of parameters of general functions and protection features for both PFC boost and Flyback converters. Useful tips on PCB layout are included to help the customers optimize their PCB design.

The design example used in this hardware design part is a 50W ECG reference design for LED lighting applications. The customer can easily apply their own target specifications and obtain the design parameters by themselves.

2.1 System Specification of a 50W ECG for LED Lighting Application

The system specification of a 50W ECG reference design for LED lighting applications is given as following:

Table 2 System Specification of a 50W ECG Reference Design

Parameter	Symbol	Target Value	Unit
50W ECG for LED Lighting Applications			
Nominal AC input voltage	V_{in_AC}	90 ~ 305	VAC
Nominal DC input voltage	V_{in_DC}	90 ~ 305	VDC
Output voltage	V_{OUT}	16 ~ 48	VDC
Output current	I_{OUT}	550 ~ 1500	mA
Output power	P_O	50	W
Power factor		> 0.9	
THD		< 15	%
Efficiency	η	89	%
PFC Boost Converter			
MOSFET maximum drain-source voltage	V_{DS_PFC}	600	VDC
Output power	P_{O_PFC}	55	W
Minimum switching frequency	f_{sw,min_PFC}	22	kHz
Flyback Converter			
Nominal input voltage	V_{DC}	460	VDC
Output power	P_O	50	W
Output overvoltage threshold	$V_{OUT,OV}$	53	VDC
MOSFET maximum drain-source voltage	V_{DS_FB}	800	VDC
Minimum switching frequency	$f_{sw,min}$	16	kHz

2.2 Schematic

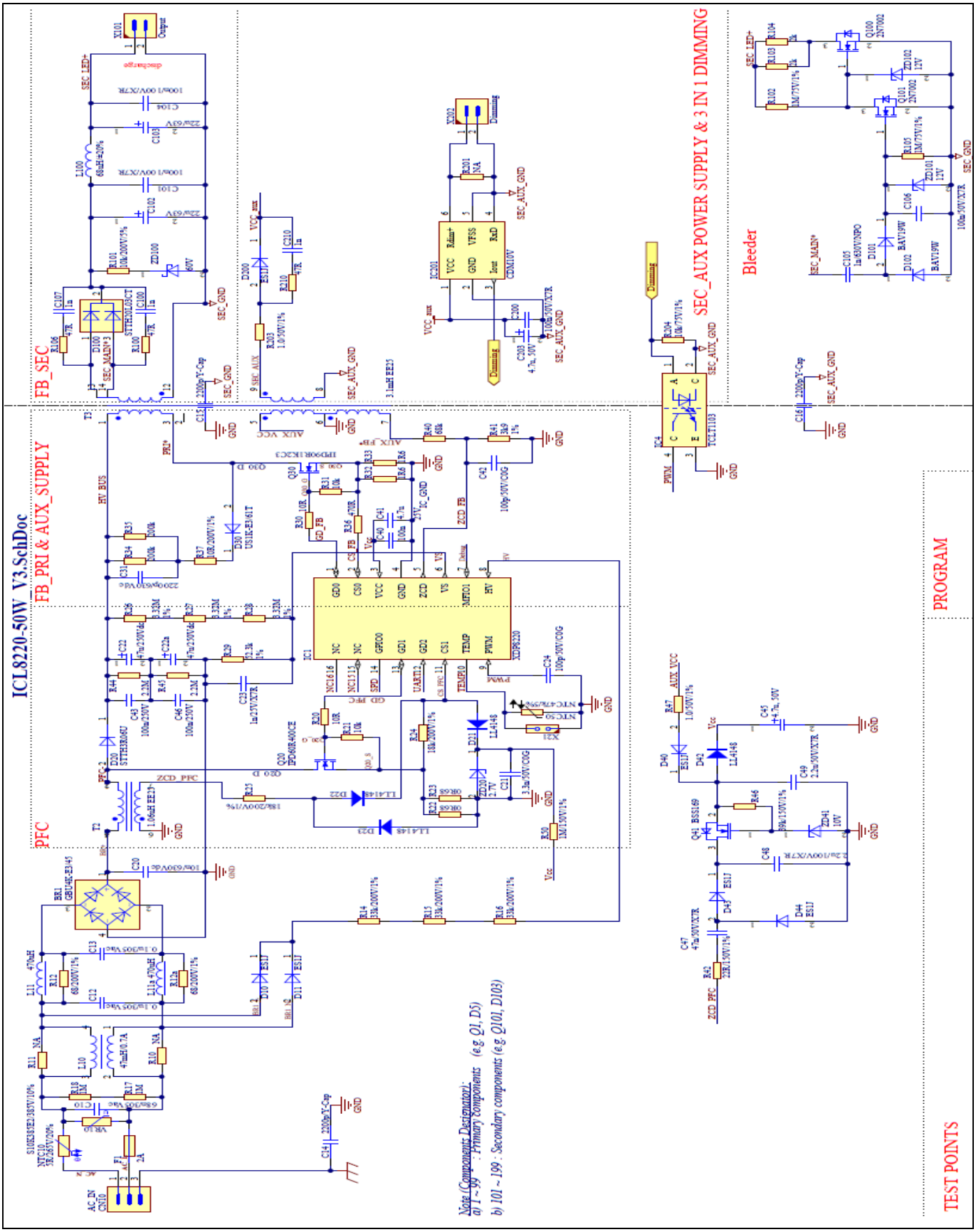


Figure 3 Schematic of a 50W ECG Reference Design

2.3 Bridge Rectifier

The bridge rectifier usually has the highest semiconductor power loss in the PFC boost converter. Using a higher rated current bridge rectifier can reduce the forward voltage drop, which reduces the total power dissipation at a small incremental cost. The total power loss is calculated using the average input current flowing through two of the bridge rectifying diodes if the forward voltage is assumed as 1V:

$$P_{loss\_BR} = I_{BR\_avg} * 2 * V_{F\_BR} = \frac{2\sqrt{2}}{\pi} * \frac{P_{O\_PFC\_max}}{V_{in\_rms\_min} * \eta_{PFC}} * 2 * V_{F\_BR} = 1.15\text{W}$$

With the value of power loss, an appropriate bridge rectifier based on its thermal characteristics should be selected.

2.4 Design the PFC Boost Converter

Power Factor Correction (PFC) shapes the input current of the power supply to be in synchronization with the mains voltage, in order to maximize the real power drawn from the mains. In a perfect PFC circuit, the input current follows the input voltage as a pure resistor, without any input current harmonics. In the ECG reference design, PFC is implemented as a boost converter which works in the Quasi-Resonant Mode (QRM) and Discontinuous Conduction Mode (DCM) with constant on-time control. The converter provides the following flyback stage a constant high DC voltage as input which reduces variations in the ECG output current (flicker) to a non-visible level. This chapter describes the methodology for designing the Multimode control (QRM+DCM) PFC Boost converter based on XDPL8220; including PFC boost inductor design, equations for power losses estimation, selection guide for power semiconductor devices and passive components.

2.4.1 Main PFC Boost Inductor

As the key magnetic component of the PFC boost converter, the boost inductor has the main function of energy storage. Its inductance is given as the following formula:

$$L_{PFC} = \frac{V_{in\_pk}^2 * (V_{bus} - V_{in\_pk}) * \eta_{PFC}}{4 * V_{bus} * P_{O\_PFC} * f_{PFC}}$$

Where:

- L_{PFC} -- Inductance of the PFC boost inductor
- V_{in_pk} -- Peak value of the input AC mains
- V_{bus} -- Bus voltage as the PFC output
- η_{PFC} -- Estimated power efficiency of the PFC boost converter
- P_{O_PFC} -- Output Power of the PFC boost converter
- f_{PFC} -- Operation switching frequency of the PFC boost inductor

In the 50W ECG reference design, the output of the PFC boost converter is chosen as 460V so that a high power factor is still guaranteed at the maximum AC/DC input. The minimum switching frequency limited at 22 kHz to avoid audible noise is controlled by XPDL8220 through “maximum switching period time-out” approach, which starts the next switching cycle when 45us of maximum switching period is reached. The detailed variables values are given in the following table:

Table 3 PFC Boost Converter Design Target Specification

PFC Boost Converter			
Parameter	**Symbol**	**Value**	**Unit**
Minimum AC/DC input voltage	$V_{in\_rms\_min}$	90	V

Minimum input peak value	$V_{in\_pk\_min}$	127	V
Maximum AC/DC input voltage	$V_{in\_rms\_max}$	305	V
Maximum input peak value	$V_{in\_pk\_max}$	431	V
Maximum PFC boost converter output power	$P_{O\_PFC\_max}$	55	W
Minimum switching frequency	f_{sw,min_PFC}	22	kHz
Estimated PFC boost converter power efficiency @ maximum AC input voltage	η_{PFC}	≤ 96	%
Nominal PFC boost converter output voltage	V_{bus}	460	V
Power Factor	PF	> 0.9	-

The maximum possible inductance is first calculated at the min and max AC input with full load and lowest switching frequency:

@ 90V AC input

$$L_{PFC\_90} = \frac{(90 * \sqrt{2})^2 * (460 - 90 * \sqrt{2}) * 0.96}{4 * 460 * 55 * 22 * 10^3} \approx 2.3mH$$

@ 277V AC input

$$L_{PFC\_305} = \frac{(277 * \sqrt{2})^2 * (460 - 277 * \sqrt{2}) * 0.96}{4 * 460 * 55 * 22 * 10^3} \approx 4.5mH$$

The proper inductance must be less than the smaller one of both.

$$L_{PFC} < min(L_{PFC_{90}}, L_{PFC_{305}}) = 2.3mH$$

To cover the worst cases like start-up and load transient, L_{PFC} =1mH is chosen as the PFC boost converter inductance.

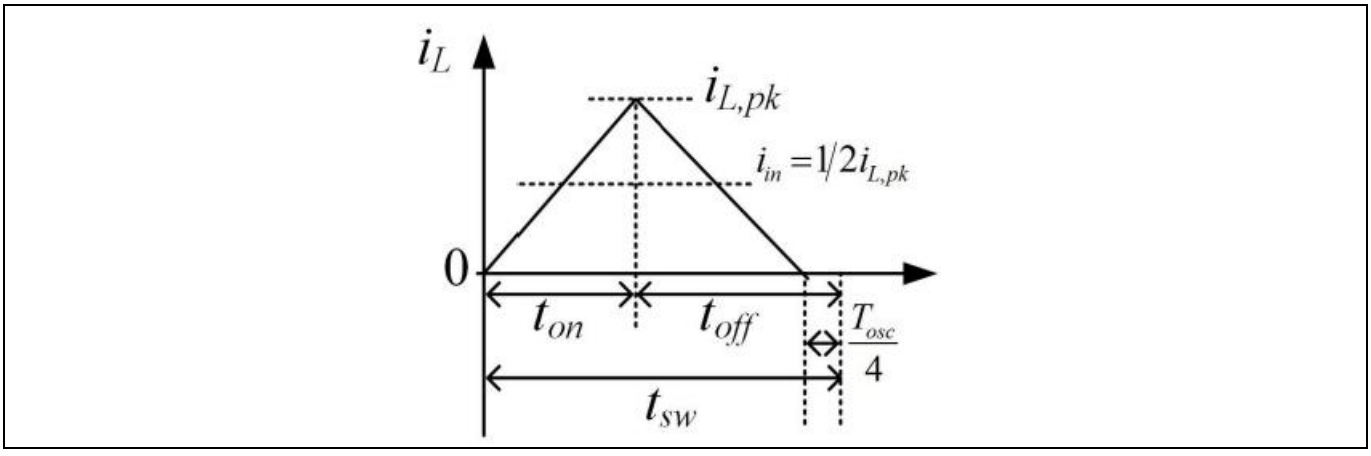


Figure 4 Boost Inductor Current Waveform in a Switching Cycle

From the Figure 4 above, other important parameters of the PFC boost converter can be obtained as following:

Maximum input current (RMS) happens at minimum AC input and maximum output power:

$$I_{in\_rms\_max} = \frac{P_{O\_PFC\_max}}{V_{in\_rms\_min} * \eta_{PFC}} = 0.64A$$

Maximum input peak current:

$$I_{in\_pk\_max} = \sqrt{2} * I_{in\_rms\_max} = \frac{\sqrt{2} * P_{O\_PFC\_max}}{V_{in\_rms\_min} * \eta_{PFC}} = 0.9A$$

Maximum inductor peak current:

$$I_{L,pk\_PFC\_max} = 2 * I_{in\_pk\_max} = 2\sqrt{2} * I_{in\_rms\_max} = \frac{\sqrt{2} * P_{O\_PFC\_max}}{V_{in\_rms\_min} * \eta_{PFC}} = 1.8A$$

Maximum on-time:

$$t_{on\_max} = \frac{L_{PFC} * I_{L,pk\_PFC\_max}}{V_{in\_pk\_min}} = 14.14\mu s$$

The off-time at minimum AC input and maximum output power:

$$t_{off} = \frac{L_{PFC} * I_{L,pk\_PFC\_max}}{V_{bus} - V_{in\_pk\_min}} = 5.41\mu s$$

If we ignore the T_{osc}, the lowest frequency for maximum output power is:

$$f_{PFC\_min} = \frac{1}{t_{on\_max} + t_{off}} = 51.12kHz$$

Maximum input current (RMS) during on-time:

$$I_{in,PFC\_on\_rms\_max} = 2 * I_{in\_rms\_max} * \sqrt{\frac{1}{3} * t_{on\_max} * f_{PFC\_min}} = 0.63A$$

Input current (RMS) during off-time:

$$I_{in,PFC\_off\_rms\_max} = 2 * I_{in\_rms\_max} * \sqrt{\frac{1}{3} * t_{off} * f_{PFC\_min}} = 0.39A$$

Maximum inductor current (RMS):

$$I_{L\_rms\_max} = \sqrt{I^2_{in,PFC\_on\_rms\_max} + I^2_{in,PFC\_off\_rms\_max}} = 0.74A$$

The other function of the PFC boost inductor is to detect the moment when the inductor current goes to zero (Zero-crossing Detection). This is realized by introducing an auxiliary winding additionally. To achieve the voltage at auxiliary winding below 50V while the maximum voltage across the PFC boost inductor primary winding is around 430V, a turns-ratio of 10:1 is recommended.

The important parameters of the PFC boost inductor are summarized in the following table:

Table 4 PFC Boost Inductor Design Parameters

PFC Boost Converter			
Parameter	**Symbol**	**Value**	**Unit**
Main Inductance of the PFC boost inductor	L_{PFC}	1000	µH
Minimum switching frequency	f_{PFC_min}	51.12	kHz
Maximum inductor peak current	I_{L,pk_PFC_max}	1.8	A

Maximum input current (RMS)	$I_{in\_rms\_max}$	0.64	A
Maximum input peak current	$I_{in\_pk\_max}$	0.9	A
Maximum inductor current (RMS)	$I_{L\_rms\_max}$	0.74	A
Maximum on-time	t_{on_max}	14.14	µs
Turns-ratio of primary to auxiliary winding	N_{p_PFC}/N_{a_PFC}	10:1	-

Based on the calculated specifications, the inductor can be constructed according to different design requirements like size, power efficiency and temperature etc. by selecting different bobbin and core. In order to avoid core saturation and achieve an optimized core loss, the flux density B_{max} is recommended not to exceed 0.3.

In the Infineon 50W ECG reference design, the PFC boost inductor is constructed by the Würth Electronic under part no. 750343252 as a design example. The specification sheet is given as following:

Table 5 Parameters of Würth Inductor 750343252

Parameter	Value	Unit
Inductance	1060	µH
Bobbin	PQ2016	-
Core material	TP4A or DMR44	-
Turns-ratio of primary to auxiliary winding	10 : 1	-
DC resistance primary winding	0.872	Ω
DC resistance auxiliary winding	0.175	Ω
Saturation current	1.85	A

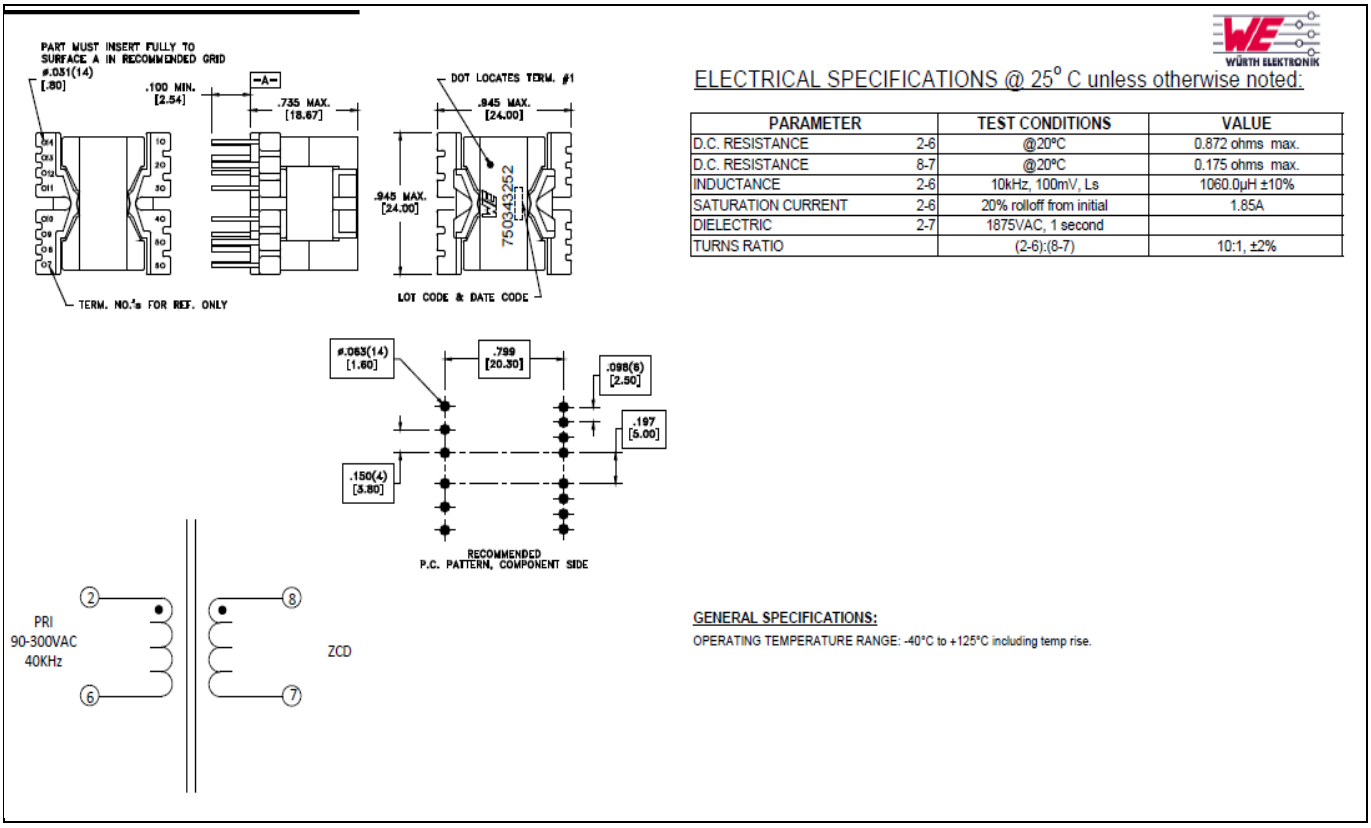


Figure 5 PFC Boost Inductor Specification Sheet

The maximum main inductor copper loss can be calculated based on the specification above as:

$$P_{loss\_L\_PFC} = I_{L\_rms\_max}^2 * R_{DC_{L_{PFC}}} = 0.48\text{W}$$

2.4.2 PFC Boost diode

Selection of the boost diode is a major design decision in the PFC boost converter and it is related to the converter efficiency. Following considerations should be taken into account:

- Reverse break down voltage

It must be chosen higher than the bus voltage with 20% margin. A 600V diode is suitable to be used.

- Average rectified forward current

It must be higher than the PFC boost converter output current. Using a diode with high current capability will be benefit to the power efficiency.

- Forward voltage

It is directly related to the power efficiency. So the forward voltage should be chosen as small as possible.

- Reverse recovery time

As the PFC boost converter works in the QRM+DCM mode, the PFC boost diode current goes into zero while the PFC MOSFET turns on. So there is no current commutation and thus no switching loss by reverse recovery. It is not necessary to choose an ultra-fast diode.

- Power loss

The only power loss is the conduction loss while the current flows through it. With a forward voltage of 1V assumed, the diode conduction loss can be calculated by:

$$P_{loss\_D\_PFC} = I_{D\_PFC\_avg} * V_{F\_D\_PFC} = \frac{P_{O\_PFC\_max}}{V_{bus}} * V_{F\_D\_PFC} = 0.12\text{W}$$

- Thermal characteristic

The important parameters for boost diode which used in the 50W ECG reference design are summarized in the following table:

Table 6 Boost Diode Design Parameters

Parameter	Symbol	Value	Unit
Maximum reverse voltage	$V_{RRM\_D\_PFC}$	600	V
Average rectified forward current	$I_{F\_D\_PFC}$	3	A
Forward voltage	$V_{F\_D\_PFC}$	1	V

2.4.3 PFC Power MOSFET

The selection of the PFC power MOSFET is based mainly on the break down voltage and the consideration of the MOSFET power dissipation. According to the operating bus voltage, a 600V MOSFET is suitable. In the QRM+DCM mode PFC boost converter, the overall MOSFET losses comprise:

- Conduction loss

These losses are frequency independent and do not scale significantly with frequency. It is calculated as following:

$$P_{con\_loss\_MOS\_PFC} = \left(\frac{I_{in,PFC\_on\_rms\_max}}{2}\right)^2 * R_{DS(ON)}$$

- Turn-on transition loss

As the converter works in the QRM+DCM mode, the turn-on transition loss caused by the magnetizing current can be ignored because the current rises from zero when a switching cycle starts. But to discharge the parasitic capacitors like C_{oss} and C_{can} through the MOSFET channel can cause significant turn-on transition loss. These losses occur every switching cycle and are thus frequency dependent.

- E_{oss} and $^1/_2 \cdot C_{can} \cdot V^2$ loss

As mentioned above, the energy stored in C_{can} and C_{oss} at the time of turn-on must be dissipated in the MOSFET channel and current sense resistor during the turn-on transition. The energy stored in any capacitor is fundamentally a function of the square of the voltage across it, and thus the E_{oss} and $½ \cdot C_{can} \cdot V^2$ losses can be very significant during high line conditions. These losses occur every switching cycle and are thus frequency dependent. To simplify the calculation, we assumed that the switching loss is approximately the half of the conduction loss:

$$P_{sw\_loss\_MOS\_PFC} = \frac{1}{2} * P_{con\_loss\_MOS\_PFC}$$

- Gate driver loss

These losses also scale linearly with frequency, but are generally a quite small contribution to the overall losses (at switching frequencies of below hundred kilohertz) and depend almost exclusively on the MOSFET Q_g (total gate-charge). The gate-driver power is typically dissipated in the external gate resistor and gate-driver itself and thus does not need to be considered in the thermal calculation of MOSFET.

In the 50W ECG reference design, the 650V Infineon MOSFET IPD60R400CE of CE family is used. With the $R_{DS(ON)}$ of 400mΩ, the total loss of the MOSFET is calculated as below:

$$P_{loss\_MOS\_PFC} = P_{sw\_loss\_MOS\_PFC} + P_{con\_loss\_MOS\_PFC} = 1.5 * P_{con\_loss\_MOS\_PFC} = 0.06W$$

The important parameters for PFC MOSFET are summarized in the following table:

Table 7 PFC MOSFET Design Parameters

Parameter	Symbol	Value	Unit
Break down voltage	$V_{BR\_DSS\_PFC}$	650	V
MOSFET on-resistance	$R_{DS(ON)}$	400	mΩ
PFC MOSFET conduction loss	$P_{loss\_MOS\_PFC\_con}$	0.04	W
PFC MOSFET switching loss	$P_{loss\_MOS\_PFC\_sw}$	0.02	W
PFC MOSFET total loss	$P_{loss\_MOS\_PFC}$	0.06	W

2.4.4 PFC MOSFET Gate Driver

The XDPL8220 PFC boost converter gate driver GDPFC offers following advanced features:

- Configurable charge current from 30 up to 118mA for turn-on slope optimization with dpVision tool
- Configurable gate voltage from 4.5 to up to V_{cc} - 0.5V

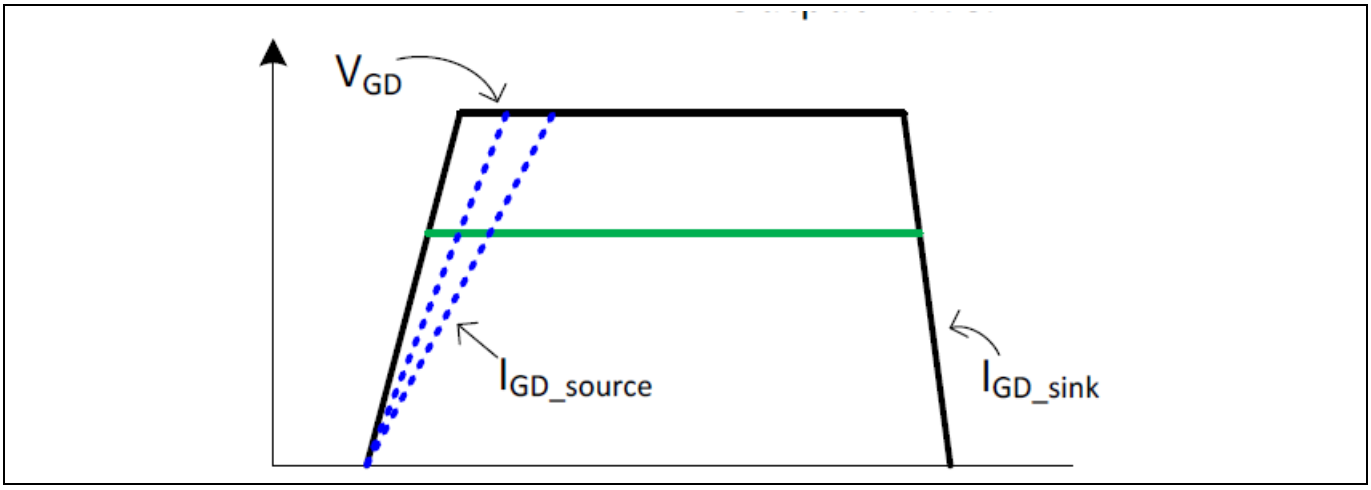


Figure 6 Configurable Gate Driver with Gate Voltage and Charge Current

Due to the configurable gate charge current and voltage, the external gate resistor should not be selected too high. A gate resistor of 10Ω should fit for most application cases. The soft turn on for improved EMI result is guaranteed by the configurable constant current gate charging. Following table shows the recommend range of the external gate resistor for a stable gate drive operation of different MOSFET:

Table 8 Recommended External Gate Resistor Value

Parameter	Symbol	Value		Unit
MOSFET Gate capacitance	C_g	1.0 ~2.0		nF
MOSFET gate source current	I_{gs}	100		mA
MOSFET gate source resistance	R_{gs}	10	100	kΩ
Recommended external gate resistor	R_g	5 ~ 20	15 ~ 25	Ω

2.4.5 PFC Current Sense and Zero-crossing Detection

The pin CSPFC of the XDPL8220 is used for two different purposes at the different moment in one switching cycle. During the on time of the PFC MOSFET, it is used as CS pin. The current sense of the PFC boost converter is used to limit the turn on time of the PFC MOSFET by sensing the peak current flowing through the MOSFET in order to protect it and also the boost inductor from the over-power situation. When the MOSFET is turned off, the pin is used as ZCD pin. The zero-crossing detection catches the moment when the boost inductor current goes to zero and the next switching cycle can be started so that the boost converter always works in the QRM or DCM mode with minimum switching loss.

As the Figure 7 shows below, when the PFC MOSFET turns on, the rectifier diode D_1 blocks the negative voltage drop across the PFC auxiliary winding so that the CSPFC pin is effectively connected only to the shunt resistor R_{CS_PFC} via the resistor R_{ZCD2_PFC} and thus only sees the peak current sense voltage signal. When the PFC MOSFET turns off, a positive voltage drop is forwarded by D_1. The CSPFC pin is connected effectively to a resistor divider R_{ZCD1_PFC} and R_{ZCD2_PFC}. A zener diode and a capacitor are necessary to clamp the pin voltage not higher than 3.3V. Another diode is required to decouple the current sensing signal from the clamping circuit.

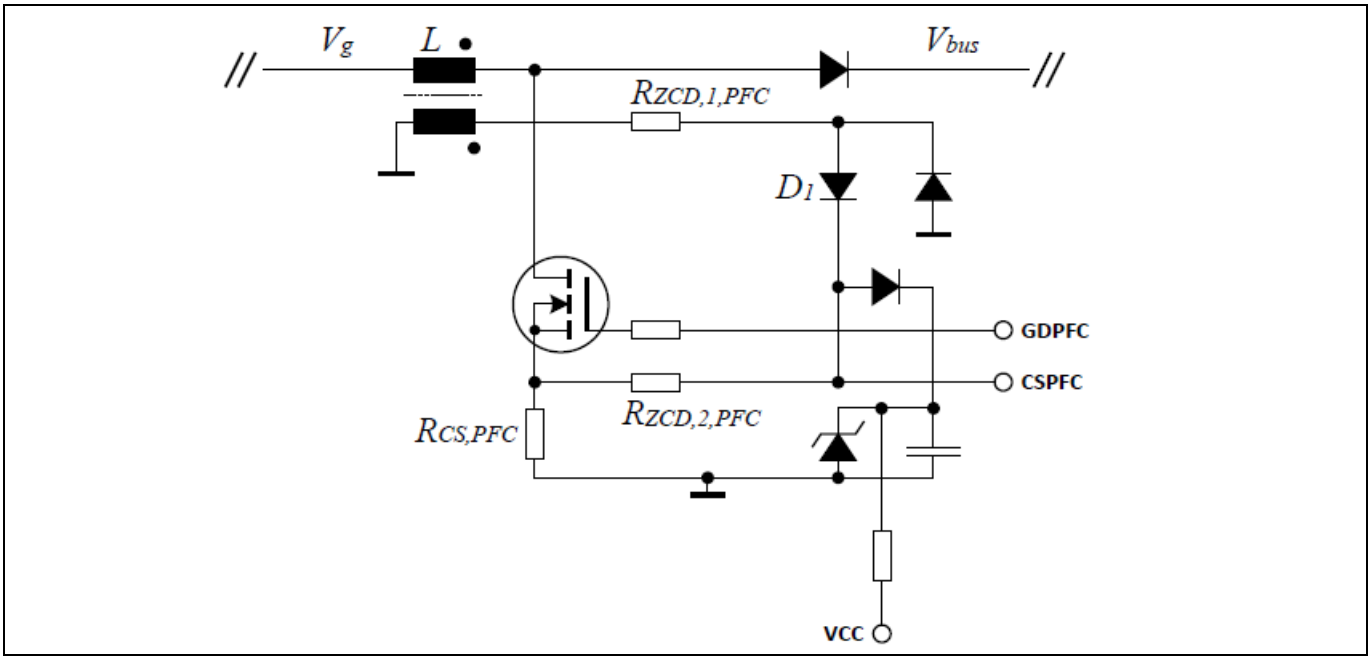


Figure 7 Schematic of Shared CS and ZCD Functions at Pin CSPFC

The important design parameters for bus voltage sensing are summarized in the following table:

Table 9 PFC Current Sense and ZCD Design Parameters

Parameter	Symbol	Value	Unit
Upper resistor of the PFC ZCD divider	R_{ZCD1_PFC}	18	kΩ
Lower resistor of the PFC ZCD divider	R_{ZCD2_PFC}	18	kΩ
PFC current sense resistor	R_{CS_PFC}	0.68//0.68=0.34	Ω

2.4.6 PFC Output Voltage Sense

As shown in the Figure 8 below, the bus voltage is measured at the ***VS*** pin of XDPL8220 through a resistor divider as the input of the bus voltage regulator to generate the PWM signal or offer the protection functions for the boost converter. It is strongly recommended to add a filter capacitor near the ***VS*** pin to filter the switching noise in order to get a precise and stable measurement result. The input pin ***VS*** has a very low leakage current so the intolerance can be ignored.

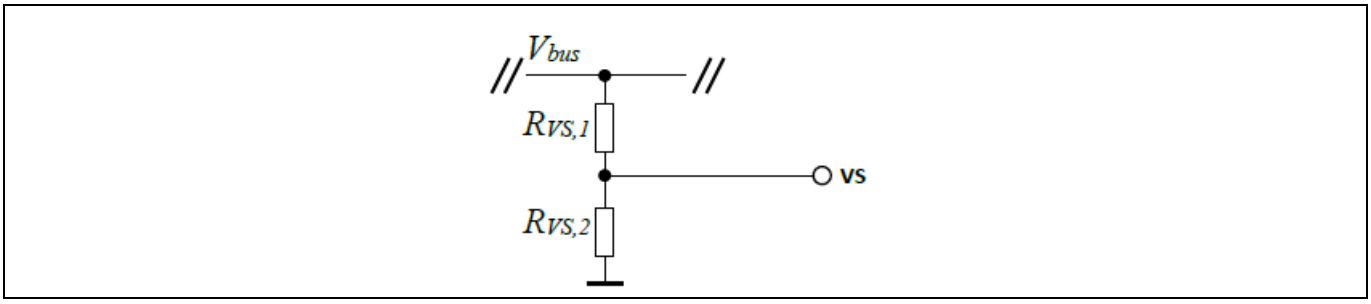


Figure 8 Bus Voltage measurement

In the XDPL8220, the ***VS*** pin is connected to an 8-Bit Analog-to-Digital Converter (ADC) which utilizes two voltage ranges for the bus voltage measurement results. This gives the advantage that on the one hand, the

whole voltage range started from 0V is monitored. On the other hand the operating range is sensed with a high resolution so that the regulation accuracy is guaranteed.

The wide voltage range from 0 to V_{REF} results in a low resolution. If the nominal operating bus voltage V_{bus} = 460V is assumed in the normal operation and mapped to V_{REF} by the resistor divider as recommended, then a 8-Bit ADC gives the range 0 ~ 460V a resolution of

$$Wide\ Range\ Resolution = \frac{V_{bus}}{256} \approx 1.8V/LSB$$

This range is used to monitor the start-up behavior or other failures.

The narrow voltage range from 5/6 V_{REF} to 7/6 V_{REF} gives a three times better resolution. If the nominal operating bus voltage V_{bus}= 460V is assumed and mapped to V_{REF}, then a 8-Bit ADC gives the range from 5/6*V_{bus}

= 383V to 7/6* V_{bus}= 536V a resolution of

$$Narrow\ Range\ Resolution = \frac{1}{3} * \frac{V_{bus}}{256} \approx 0.6V/LSB$$

So in the steady state operation, the high-resolution range is used to get an accurate bus voltage regulation.

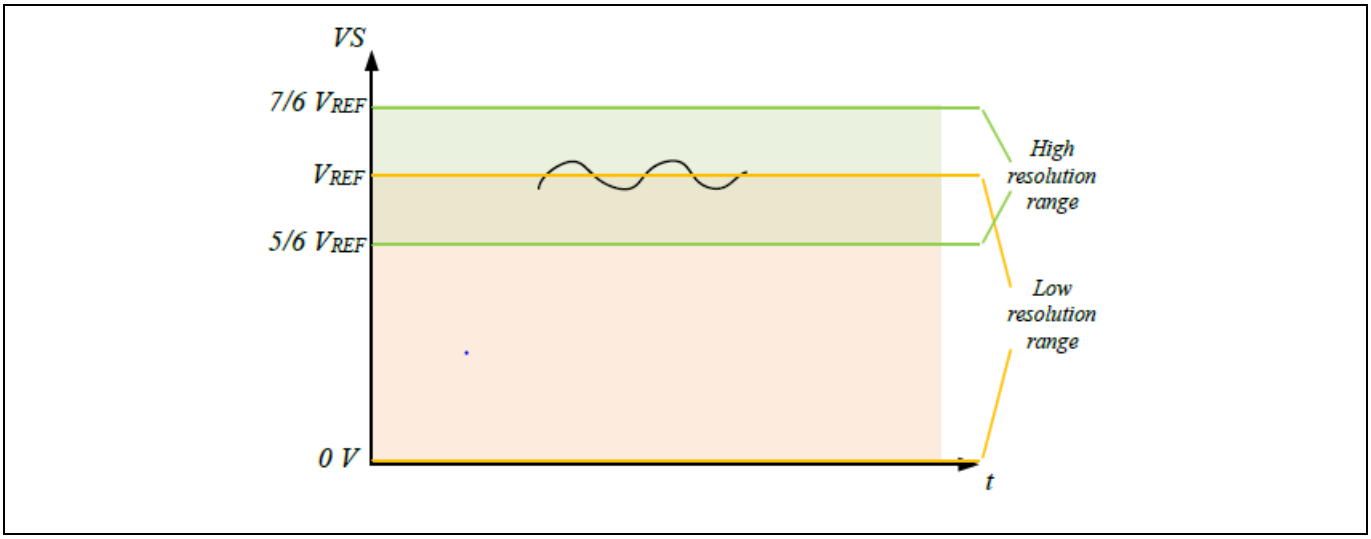


Figure 9 Two Different Bus Voltage Sensing Ranges

The calculation of the resistor divider is given as following if the V_{bus} = 460V is mapped to V_{REF}:

$$\frac{R_{VS1\_PFC}}{R_{VS2\_PFC}} = \frac{V_{bus} - V_{REF}}{V_{REF}} = 188.46$$

To reduce the inaccuracy caused by the resistor divider, it is necessary to select the bus voltage sensing resistors with a tolerance of less than 1%. In the 50W ECG reference design, to reduce the voltage stress, the upper resistor R_{VS1_PFC}consists of three resistors of each 3.32MΩ and the lower resistor R_{VS1_PFC} is selected as 52.3 kΩ.

The criteria to switch between these two ranges are as following if the tolerance of the resistors can be ignored:

- The PFC boost converter always starts in the narrow (high resolution) range
- In the narrow (high resolution) range, if the bus voltage V_{bus}< 406V then it will be switched to wide range
- In the wide (low resolution) range, if the bus voltage V_{bus}> 430V, then it will be switched to the narrow range

Note: *In order to reduce the switching noise coupled in the Bus voltage sense signal, a filter capacitor of 1nF is strongly recommended to be placed directly near the VS pin.*

The important design parameters for bus voltage sensing are summarized in the following table:

Table 10 Bus Voltage Sensing Design Parameters

Parameter	Symbol	Value	Unit
Nominal PFC boost converter output voltage	V_{bus}	460	V
XDPL8220 internal ADC reference voltage	V_{REF}	2.428	V
Bus voltage sensing divider ratio	R_{VS1_PFC} / R_{VS2_PFC}	188.46	-
Bus voltage sensing divider upper resistor	R_{VS1_PFC}	3.32 x 3	MΩ
Bus voltage sensing divider lower resistor	R_{VS2_PFC}	52.3	kΩ
Bus voltage sensing filter capacitor	C_{VS}	1	nF
Narrow (High Resolution) range	-	383 ~ 536	V
Resolution of narrow range	-	0.6	V/LSB
Wide (Low Resolution) range	-	0 ~ 460	V
Resolution of wide range	-	1.8	V/LSB

2.4.7 PFC Output Capacitor

The PFC bus capacitor can be calculated with the following formula if the ESR of the capacitor is small enough to be neglected and the peak to peak voltage ripple is selected as 20V:

$$C_{bus} = \frac{I_{out\_PFC\_max}}{2 * \pi * f_{line\_min} * V_{bus\_ripple\_pp}} = 20uF$$

With

$$I_{out\_PFC\_max} = \frac{P_{O\_PFC\_max}}{V_{bus}} = 0.12A$$

For voltage class, with consideration of over-voltage protection threshold, a 500V capacitor is necessary. But due to the price and size factors, it is reasonable to use two 250V rating capacitors in series. The ESR of the capacitor should be selected as small as possible and the allowed maximum ripple current should have enough margins. In the 50W ECG reference design, two capacitors of 47uF in series with low ESR are selected. To symmetrize the voltage stress on the two in series connected capacitors, an in parallel connected high ohmics resistor divider is recommended, which will increase the stand by power consumption lightly nevertheless.

The important parameters for the bus capacitor selection are summarized in the following table:

Table 11 Bus Capacitors Design Parameters

Parameter	Symbol	Value	Unit
Nominal PFC boost converter output voltage	V_{bus}	460	V
Maximum PFC boost converter output power	$P_{out\_PFC\_max}$	55	W
Bus voltage ripple (peak to peak)	$V_{bus\_ripple\_pp}$	20	V
AC input line frequency	f_{line}	45 ~ 66	Hz
PFC Bus capacitor	C_{bus}	22	µF

2.4.8 PFC Multi-Mode Control

The PFC boost converter regulates the output bus voltage through the calculated constant on-time:

$$t_{on\_PFC} = \frac{2 * P_{O\_PFC\_max} * L_{PFC}}{V_{in\_rms}^2 * \eta_{PFC}}$$

As shown from the formula above, when the inductance is fixed and the line input voltage is constant, the PFC on-time is only dependent on the converter output power. The output voltage is sensed and fed into the internal PIT1 regulator for on-time calculation. With the calculated on-time and by designed frequency law controlled off time, a switching cycle is then defined.

For PFC boost converter operating in the QRM (quasi resonant mode), the PFC MOSFET is turned on with constant on-time throughout the complete AC half cycle and the off-time is varying during the AC half cycle depending on the instantaneous input voltage applied. A new switching cycle starts after the inductor current reaches zero. It is ideal for full load operation, where the on-time is large. However, the on-time reduces at light load, resulting in very high switching frequency especially near the zero-crossings of the AC input. The high switching frequency increases the switching loss, resulting in poor efficiency at light load. Therefore the multi-mode control is implemented. The multimode PFC control can lower the switching frequency by adding an additional delay into each switching cycle through selecting further inductor current valleys to achieve QR2M and up to maximum QRM5 (configurable) operation. Figure 10 illustrates the QRM2 valley switching in multimode PFC control as an example.

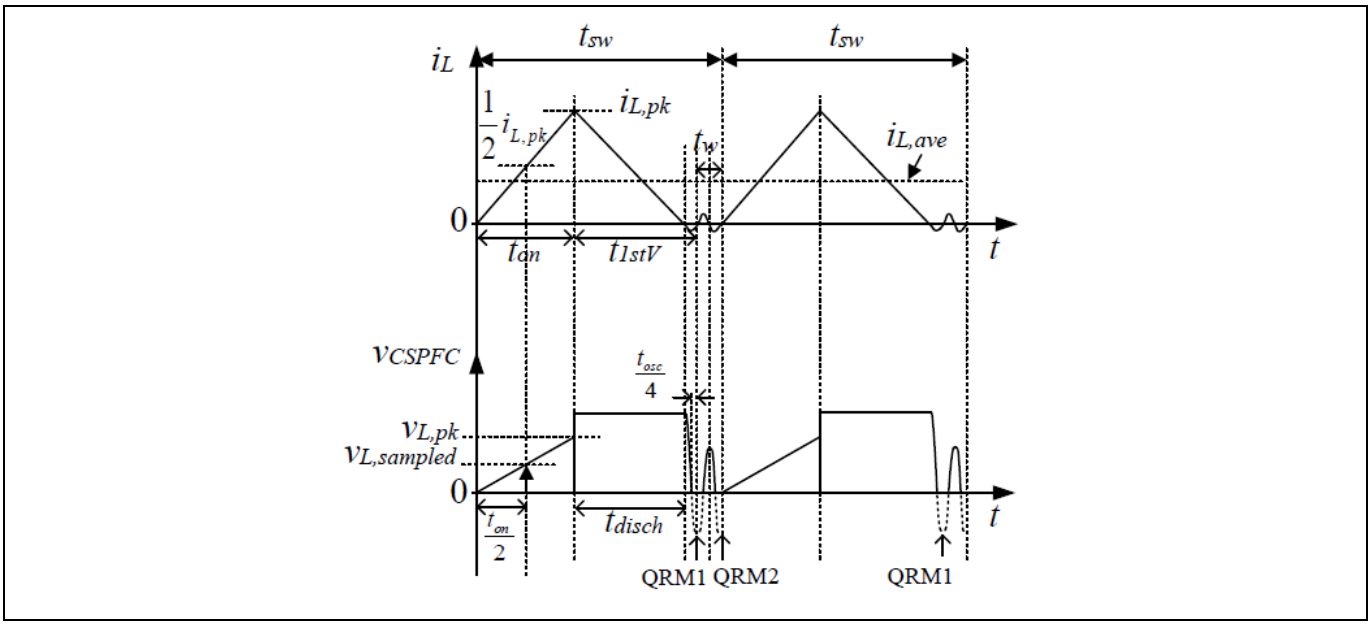


Figure 10 PFC Boost Multi-Mode Control with QRM2

The multi-mode control is defined in the frequency law, which consisting of a maximum switching frequency $f_{sw\_PFC\_max}$ and a minimum switching frequency $f_{sw\_PFC\_min}$ controls the valley selection (QRMn). In this way, the switching frequency is limited within the defined range and efficiency at light load can be improved. An illustration of the frequency law is shown in Figure 11.

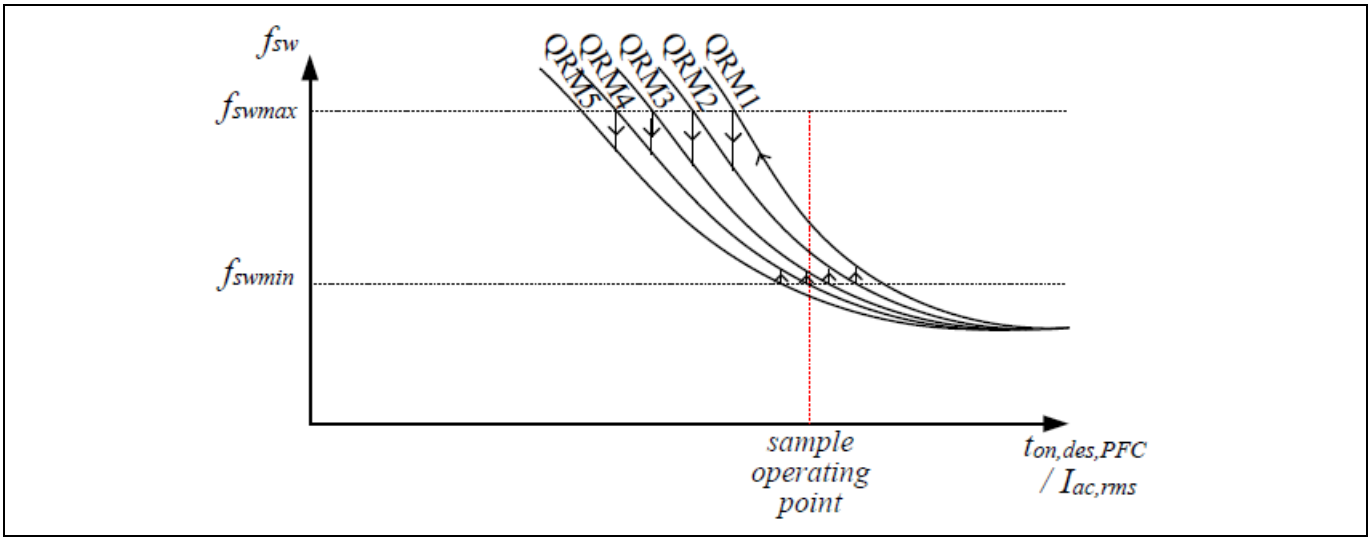


Figure 11 Frequency Law For Operating Mode

The important design parameters for multi-mode control are summarized in the following table:

Table 12 Input Voltage Sensing Design Parameters

Parameter	Symbol	Value	Unit
Maximum PFC boost converter switching frequency	$f_{sw\_max\_PFC}$	120	kHz
Minimum PFC boost converter switching frequency	$f_{sw\_min\_PFC}$	22	kHz
Maximum allowed valley	$N_{valley\_max\_PFC}$	5	-

2.4.9 PFC Start-Up Control

After the AC or DC voltage is applied at the input, the bus voltage is charged to $V_{bus\_start\_PFC}$. The V_{cc} capacitors are charged by the start-up cell till the voltage reaches the on threshold and then the XDPL8220 is active. The first thing that XDPL8220 will do after the activation is the start-up check: if the bus voltage is higher than the $V_{bus\_start\_PFC}$, the PFC boost converter will begin with the soft-start phase. After the threshold $V_{bus\_steady\_entry\_UV}$ is reached within the time $t_{start\_max\_PFC}$, the start-up phase is over and the controller is in the steady state operation till the operating bus voltage V_{bus_set} is established. If it is not the case, the PFC soft-start failure will be triggered. This is shown in the following figure 12:

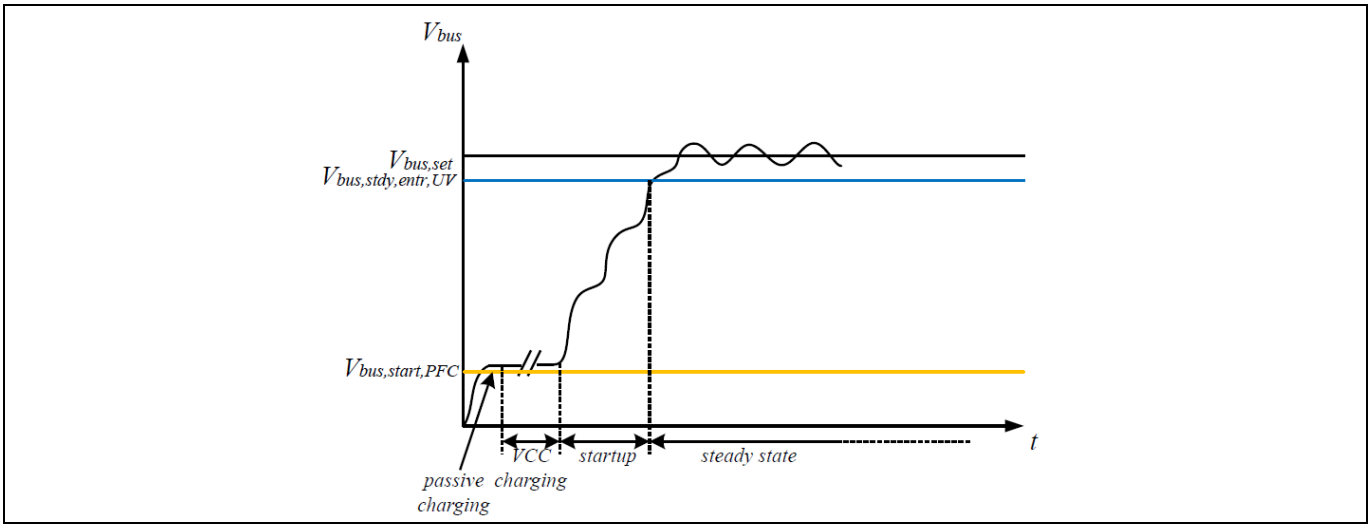


Figure 12 PFC Boost Converter Start-Up Control

The PIT1 regulator parameters used for the start-up and steady state may be different because of different requirements of the control loop. In the start-up phase, T1 regulator is inactive because a fast dynamic response is important in order to settle the bus voltage at the defined operation level as soon as possible so that the flyback stage can start quickly and take over the IC power supply. Furthermore, it also helps to reduce the time-to-light. On the contrary in the steady state phase, a slow loop response is suitable for the stable bus voltage regulation and T1 regulator is activated.

The important design parameters for PFC Boost Converter Start-up control are summarized in the table below:

Table 13 PFC Start-Up Design Parameters

Parameter	Symbol	Value	Unit
Voltage threshold to start PFC stage	$V_{bus\_start\_PFC}$	75	V
Voltage threshold for closed loop regulation	$V_{bus\_steady\_entry\_UV}$	448	V
Nominal PFC boost converter output voltage	V_{bus_set}	460	V
Proportional gain of PIT1 regulator in the start-up phase	SVP_{start_up}	4	-
Integral gain of PIT1 regulator in the start-up phase	SVI_{start_up}	7	-
Proportional gain of PIT1 regulator in the steady state phase	SVP_{steady_state}	4	-
Integral gain of PIT1 regulator in the steady state phase	SVI_{steady_state}	7	-
T1 filter gain in the steady state phase	SVT	6	-

2.4.10 Input Voltage Sensing

The rectified input voltage is measured through an external current limitation resistor R_{HV} at the HV pin as shown in the Figure 10. This path provides not only the input voltage sensing function, but also the power supply via the IC internal built HV start-up cell for XDPL8220 before the V_{cc} reaches the on-threshold.

The input voltage sensing distinguishes whether the AC or DC voltage is connected at input. Meanwhile, input voltage measurement provides the brown-in, brown-out and input over voltage protection. The threshold of each protection may be different for AC or DC input.

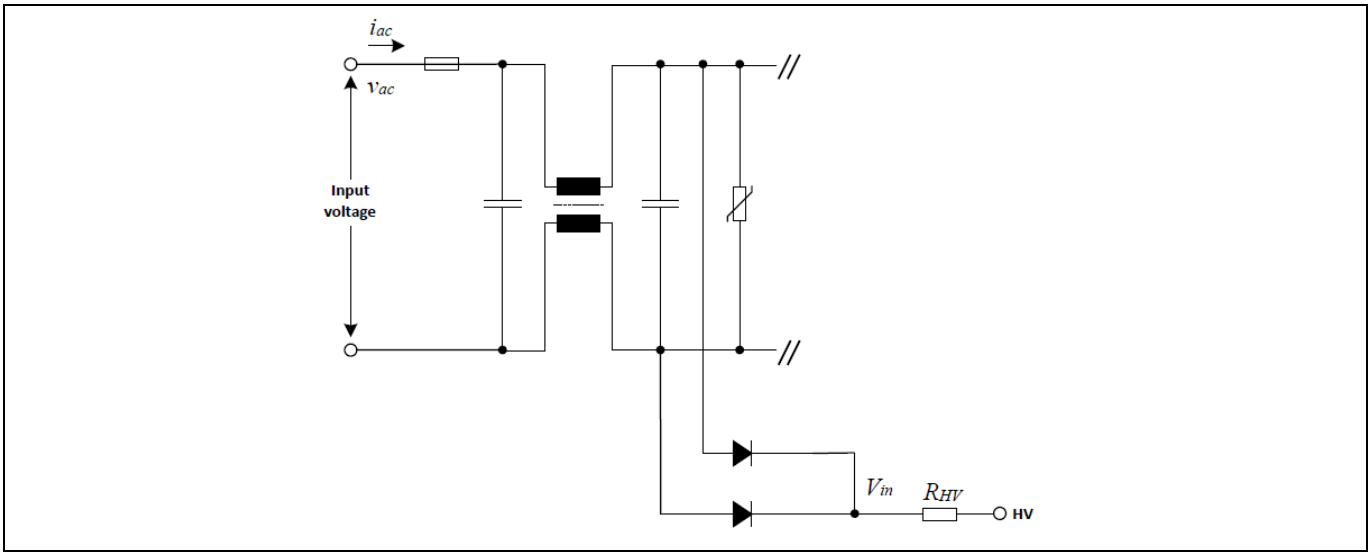


Figure 13 Input Voltage Sensing

To charge the V_{cc} capacitors through the IC internal start-up cell, the charge current must be limited not to over-power the start-up cell. The current limitation resistor R_{HV} must fulfill the following condition:

$$R_{HV} > \frac{\sqrt{2} * V_{in\_max\_rms}}{I_{HV\_max}} = 90k\Omega$$

Because of internal setup of the HV pin to measure the input precisely, it is mandatory to use the HV current limitation resistor R_{HV}= 99kΩ in order to limit the maximum HV pin current to 4.8mA. To reduce the voltage and power stress of the resistor, it is strongly recommended to split it into three 1206 resistors of each 33kΩ. To improve the accuracy of the measurement, resistors with tolerance less than 1% should be selected.

The important design parameters for input voltage sensing are summarized in the following table:

Table 14 Input Voltage Sensing Design Parameters

Parameter	Symbol	Value	Unit
Maximum AC input Voltage	$V_{in\_AC\_max\_rms}$	305	Vrms
Maximum DC input voltage	$V_{in\_DC\_max}$	305	V
Maximum current of start-up cell	I_{HV_max}	4.8	mA
HV current limitation resistor	R_{HV}	33x3=99	kΩ

2.4.11 PFC Protection Features

The digital controller XDPL8220 provides all around protections for both power components and input/output of the PFC boost converter. As illustrated below in the control state machine (Figure 14), the protections are active after the system enters the start-up checks state (when ***Vcc*** voltage reaches the on-threshold). While the start-up checks, the input/output are monitored before starts PFC to protect against possible under/over-voltage. After the system is in the soft-start state, more protections like over-current, over-power and CCM protection are also activated. An overview of which protection enabled in which operating state is given in the following table 15.

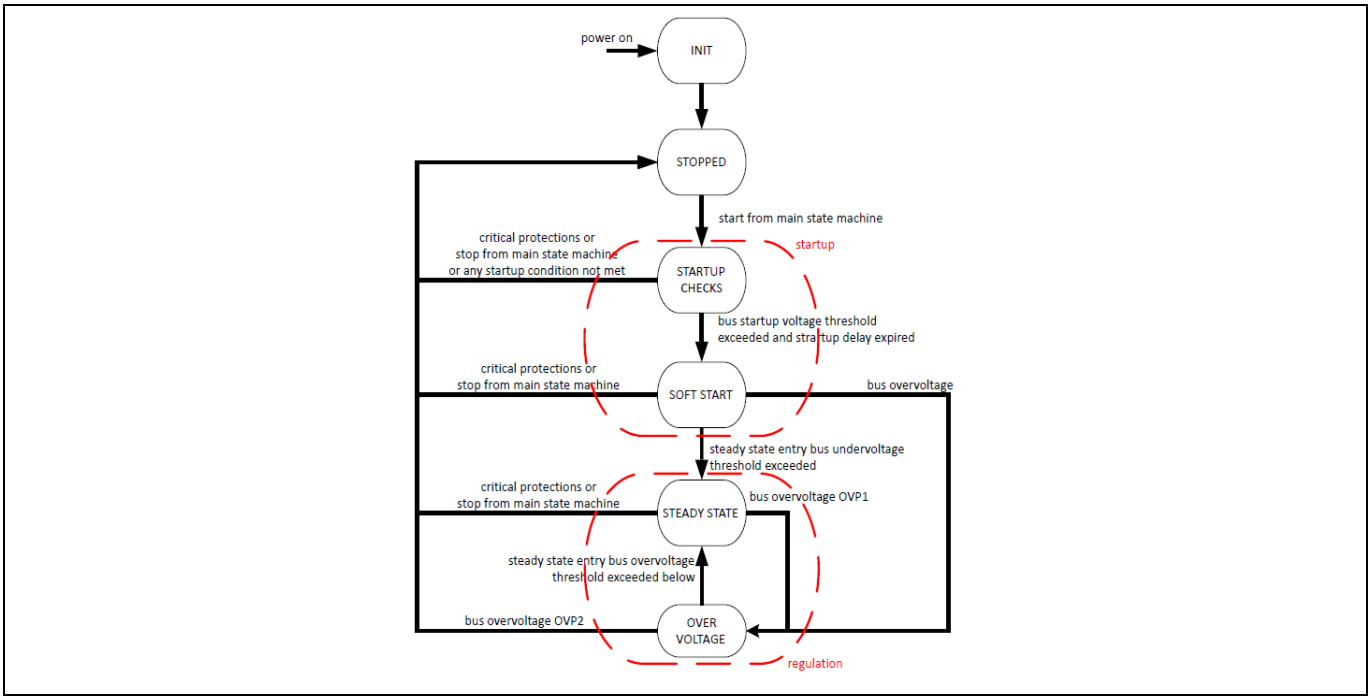


Figure 14 PFC Boost Converter Control State Machine

Table 15 PFC Protection States

Protection	Stopped	Soft-Start	SteadyState	Over Voltage
Bus Over Voltage Protection level 2 (OVP2)	Disabled	Enabled	Enabled	Enabled
Bus Under Voltage Protection	Disabled	Disabled	Enabled	Enabled
Input Over Voltage Protection	Disabled	Enabled	Enabled	Enabled
Input Under Voltage Protection	Disabled	Enabled	Enabled	Enabled
Over Current Protection level 2	Disabled	Enabled	Enabled	Enabled
Soft-Start Failure	Disabled	Enabled	Disabled	Disabled
CCM Protection	Disabled	Disabled	Enabled	Disabled

2.4.11.1 Bus Voltage Protection

The voltage at the ***VS*** pin which represents the bus voltage is monitored for the bus voltage protection.

Bus over-voltage protection is mandatory to protect the DC-link electrolytic capacitor, boost diode and MOSFET of the flyback converter. There are two different level protections defined:

- The OVP1 is part of the regulation loop and controlled by the firmware. When the OVP1 threshold V_{bus_OVP1} is continuously triggered beyond the configured blanking time $t_{blank\_bus\_OVP1}$, the PFC gate driver is stopped by the firmware. In this case, flyback converter should go on switching to help discharging the bus capacitor. The gate driver is only enabled again when the bus voltage falls below the level $V_{bus\_steady\_entry\_OV}$. No further protection action is necessary.
- The OVP2 in contrast is a hardware protection and the gate driver is disabled if the fixed OVP2 threshold V_{bus_OVP2} is triggered beyond the defined blanking time $t_{blank\_bus\_OVP2}$ and without any firmware delay. In this case, flyback converter will also stop working and XDPL8220 will enter the latch mode. The OVP2 threshold is defined as a ***VS*** pin voltage of 2.8V, which together with the bus voltage sense divider results in the corresponding voltage at the bus.
- Bus under-voltage protection is meaningful to prevent the flyback transformer from running into saturation. When the threshold V_{bus_UV} is continuously triggered beyond the configured blanking time $t_{blank\_bus\_UV}$, both PFC and flyback converter operations are stopped and XDPL8220 will enter the auto-restart mode. The different OVP thresholds are illustrated in the following figure 14:

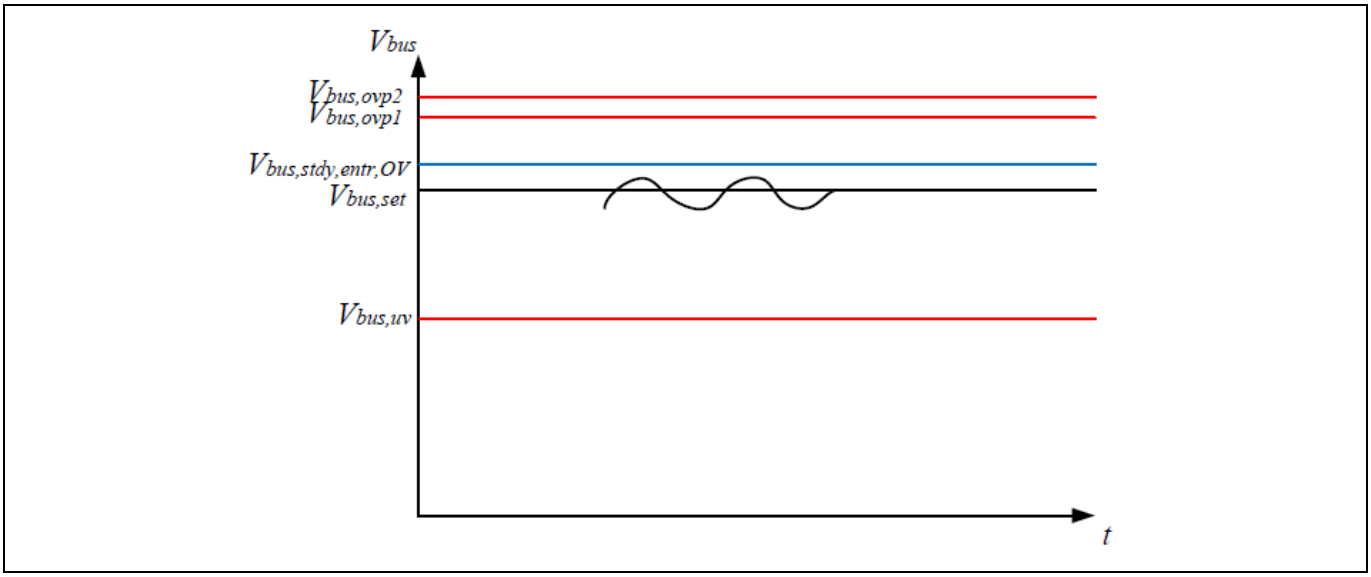


Figure 15 PFC Bus Voltage Protection Thresholds

The important design parameters for bus voltage protection are summarized in the table below:

Table 16 PFC Bus Voltage Protection Design Parameters

Parameter	Symbol	Value	Unit	Configurable
Bus over-voltage protection level 2 threshold	V_{bus_OVP2}	536	V	No
Blanking time for OVP2	$t_{blank\_bus\_OVP2}$	200	ns	Yes
Reaction OVP2	-	Latch	-	No
Bus over-voltage protection level 1 threshold	V_{bus_OVP1}	496	V	Yes
Blanking time for OVP1	$t_{blank\_bus\_OVP1}$	384	µs	Yes
Recovery threshold from OVP1	$V_{bus\_steady\_entry\_OV}$	472	V	Yes
Bus under-voltage protection threshold	V_{bus_UV}	300	V	Yes
Blanking time for under-voltage	$t_{blank\_bus\_UV}$	500	ms	Yes
Reaction bus under-voltage protection	-	Auto-Restart	-	Yes

2.4.11.2 Input Voltage Protection

Input voltage protection is realized by monitoring the voltage at the HV pin. After the XDPL8220 is active and before the PFC boost converter is started, the input voltage will be checked first. Only if the input RMS voltage is between the threshold $V_{in\_start\_min}$ and $V_{in\_start\_max}$, PFC will start. After this, input will be monitored continuously. If the input voltage touches the under-voltage or over-voltage threshold beyond the blanking time, XDPL8220 will enter the auto-restart mode.

The important design parameters for input voltage protection are summarized in the table below:

Table 17 PFC Input Voltage Protection Design Parameters

Parameter	Symbol	Value	Unit	Configurable
Minimum input voltage to start PFC Converter	$V_{in\_start\_min}$	90	Vrms	Yes
Maximum input voltage to start PFC Converter	$V_{in\_start\_max}$	277	Vrms	Yes
Input under-voltage protection during operation	V_{in_UV}	75	Vrms	Yes
Blanking time for input under-voltage	t_{vin_UV}	100	ms	Yes
Reaction input under-voltage protection	-	Auto-Restart	-	Yes
Input over-voltage protection during operation	V_{in_OV}	320	Vrms	Yes
Blanking time for input over-voltage	t_{vin_OV}	100	ms	Yes
Reaction input over-voltage protection	-	Auto-Restart	-	Yes

Note: *The thresholds listed in the table above are related to the selected **HV** resistor of 99kΩ. Different **HV** resistor will result in different thresholds.*

Note: *Due to the selected R_{HV}=99kΩ and the current limitation of 4.8mA into the **HV** pin, the maximum input voltage protection threshold is only till 277Vrms possible. For an extended threshold till 305Vrms, this input voltage protection should be disabled and the input over-voltage protection will be covered by the bus over-voltage protection.*

2.4.11.3 Over-Current Protection

The over-current protection is necessary to control the maximum current flowing through the PFC boost inductor and PFC MOSFET so that they are not over-powered. This is realized by monitoring the voltage across the PFC shunt resistor. If the voltage reaches the threshold and beyond the blanking time, PFC gate will be switched off. There are two level of the over-current protection:

- Over-current Protection level 1: by touching the threshold $V_{CS\_PFC\_OCP1}$ of the OCP1 beyond the blanking time $t_{blank\_OCP1\_PFC}$, PFC gate will be switched off and the next switching cycle will be started again after the zero-crossing signal is detected. No further action will be taken. This is a cycle by cycle power limitation.
- Over-current Protection level 2: by touching the threshold $V_{CS\_PFC\_OCP2}$ of the OCP2, both PFC and flyback gate drive will be switched off and XDPL8220 will enter the latch mode

The important design parameters for PFC over-current protection are summarized in the table below:

Table 18 PFC Over Current Design Parameters

Parameter	Symbol	Value	Unit	Configurable
PFC Over-current protection level 1 threshold	$V_{CS\_PFC\_OCP1}$	0.75	V	Yes
Blanking time for PFC OCP1	$t_{blank\_OCP1\_PFC}$	200	ns	Yes
PFC Over-current protection level 2 threshold	$V_{CS\_PFC\_OCP2}$	1.6	V	No
Blanking time for PFC OCP2	$t_{blank\_OCP2\_PFC}$	200	ns	Yes
Reaction to PFC OCP2	-	Latch	-	Yes

2.4.11.4 Soft-Start Failure

When the input voltage is very low or the output is over-loaded, the start-up time of the PFC boost converter is very long. In both cases, the protection is triggered and XDPL8220 will enter the auto-restart mode. The PFC soft-start time t_{start_PFC} is defined and monitored from the moment that PFC stage is started till the bus voltage reaches the threshold $V_{bus\_steady\_entry\_UV}$. If this time exceeds the maximum allowed PFC soft-start time $t_{start\_PFC\_max}$, protection will be triggered.

The important design parameters for soft-start failure are summarized in the table below:

Table 19 PFC Soft-Start Failure Design Parameters

Parameter	Symbol	Value	Unit	Configurable
Voltage threshold for start-up end	$V_{bus\_steady\_entry\_UV}$	448	V	Yes
Maximum allowed PFC soft-start time	$t_{start\_PFC\_max}$	400	ms	Yes
Reaction soft-start failure	-	Auto-Restart	-	Yes

2.4.11.5 CCM Protection

Continuous conduction mode (CCM) operation occurs when the magnetizing current does not decrease to zero before the next switching cycle starts. This happens usually when the difference of the bus voltage and input voltage is very small, which is the case of start-up or boost diode short. However, when the output is over-loaded or input voltage is too low, the inductor peak current will be very high and the demagnetizing of boost inductor cannot be operated completely, too. At start-up, the CCM operation is allowed for limited time but in other conditions, XDPL8220 must enter the protection mode.

The CCM operation is monitored at the PFC CS pin. When the ZCD signal does not come till the maximum switching period time-out happens, it will be treated as a CCM cycle. If the CCM operation happens beyond the blanking time $t_{blank\_CCM\_PFC}$, XDPL8220 will enter the auto-restart mode.

The important design parameters for CCM protection are summarized in the table below:

Table 20 PFC CCM Protection Design Parameters

Parameter	Symbol	Value	Unit	Configurable
Blanking time for PFC CCM operation	$t_{blank\_CCM\_PFC}$	500	µs	Yes
Reaction PFC CCM protection	-	Auto-Restart	-	Yes

2.5 Design the Flyback Converter

The flyback converter takes the PFC boost output DC voltage at the primary side and converts it to a configurable wide voltage range DC output with the programmable constant current at the secondary side. The controller XDPL8220 provides a primary side output voltage and current control without the secondary side external regulator components as this function is already fully integrated in the controller. This chapter describes the methodology for designing the Multimode control (QR+DCM) flyback converter based on XDPL8220; including the flyback transformer design, equations for power losses estimation, selection guide for power semiconductor devices and passive components. The design target specification for the 50W ECG reference design is given in the following table:

Table 21 Flyback Converter Design Target Specification

Flyback Converter			
Parameter	**Symbol**	**Value**	**Unit**
Minimum DC input voltage	V_{bus_min}	440	V
Nominal DC input voltage	V_{bus}	460	V
Maximum DC input voltage	V_{bus_max}	480	V
Maximum flybackconverter output power	P_{O_max}	50	W
Minimum switching frequency	$f_{sw\_FB\_min}$	40	kHz
Estimated flyback converter power efficiency	η_{FB}	< 93	%
Flyback converter output voltage	V_{out}	16 ~ 48	V
Flyback converter output over-voltage threshold	V_{out_OV}	53	V
Flyback converter output current	I_{out}	550 ~1500	mA
Maximum flyback MOSFET drain-source voltage	V_{DS_max}	800	V
Secondary diode forward voltage	V_F	1	V
Secondary diode voltage rating	V_{RRM}	400	V

2.5.1 Design the Flyback Transformer

For flyback converter, the transformer is the most important factor that determines the performance such as the efficiency, output regulation and EMI. Contrary to the normal transformer, the flyback transformer is inherently an inductor that provides energy storage, coupling and isolation for the flyback converter. In

the general transformer, the current flows in both the primary and secondary winding at the same time. However, in the flyback transformer, the current flows only in the primary winding while the energy in the core is charged and in the secondary winding while the energy in the core is discharged. Usually gap is introduced between the cores to increase the energy storage capacity. The general transformer design procedures are briefly described below:

2.5.1.1 Transformer Turns-Ratio

The transformer turns-ratio n decides not only the reflected voltage from the secondary side to the primary side, which affects the primary side flyback MOSFET selection, but also the maximum switching duty cycle D_{max} of the flyback converter.

A higher transformer turns-ratio steps down the voltage from input to output more, such that a higher duty cycle may be employed. The maximum duty cycle is exactly defined by the turns-ratio, since magnetizing time and demagnetizing time are functions of input voltage and reflected output voltage respectively. The duty cycle of the QR mode flyback can be calculated as following:

$$D = \frac{t_{on}}{t_{on} + t_{off}} = \frac{n * (V_{out} + V_F)}{V_{bus} + n * (V_{out} + V_F)}$$

This expression for D clearly approaches 1 asymptotically when n approaches ∞ (and 0 when n approaches 0). Nevertheless, a high turns-ratio means high reflected voltage from the secondary to primary side, which requires a higher MOSFET drain-source break down voltage. Therefore, the maximum transformer turns-ratio depends on the expected maximum input voltage and reflected output voltage, since the sum of the two determines the voltage stress across drain-source of primary side MOSFET during the demagnetization period like following:

$$V_{DS\_MOS\_FB} = V_{bus\_max} + n * V_{out\_max}$$

During turn-off of the primary side MOSFET, energy stored in leakage inductance will charge up the C_{oss} of the primary MOSFET causing an overvoltage spike to occur on top of the steady-state stress voltage. Depending on the leakage inductance value and the C_{oss} characteristics of the MOSFET employed, the snubber circuit can be tuned to guarantee operation within the voltage rating of the MOSFET, when employing a de-rating factor as is norm in the industry. In the 50W ECG reference design, 800V MOSFET is selected with a de-rating of 85% is assumed. So the maximum turns-ratio n_{max} is calculated as:

$$n \leq n_{max} = \frac{0.85 * V_{DS\_MOS\_FB} - V_{bus\_max}}{V_{out\_max}} = 4$$

A low transformer turns-ratio could be desirable for several reasons as well. One reason is the conduction losses on the output loop, since the primary peak current is defined independent of the transformer turns-ratio by the DCM Flyback power equation:

$$P_{out} = \frac{1}{2} * L_{FB} * i_{p\_pk}^2 * f_{FB} * \eta_{FB}$$

The output loop peak-current is the input peak current reflected across the transformer:

$$i_{s\_pk} = n * i_{p\_pk}$$

A smaller turns-ratio will reduce the secondary peak current and thus the conduction loss. One other reason could be the construction of the transformer itself. In order to get a strong coupling with accurate turns-ratio, there is a minimum practical limit to the number of physical turns on the output-side. With a minimum output winding turns-count and a maximum input winding turns-count, a practical upper limit to the transformer turns-ratio will also exist. With the electrical requirements known, the minimum transformer turns-ratio can be

found similarly as the maximum, but based on voltage rating for the desired output rectifier diode V_{RRM}. The steady state voltage stress across the diode is the sum of the transformer winding voltage and the output voltage, both of which have known maxima from previous calculations. The MOSFET voltage rating must adhere to de-rating criteria:

$$n \geq n_{min} = \frac{V_{bus\_max}}{0.8 * V_{RRM} - V_{out\_max}} = 2.52$$

Nevertheless, a very low turns-ratio leads to a low duty cycle or smaller on-time at light load. If this small on-time is not able to be output by the controller, then the burst mode is unavoidable. In the 50W ECG reference design, the turns-ratio is chosen as:

$$n = 3.9$$

2.5.1.2 Magnetizing Inductance

The magnetizing inductance scaling can be done in several ways. One such way would be to ensure that at least full power can be produced at lowest bus voltage while staying in QR operation.

As already described in the previous chapter, the maximum duty cycle occurs at minimum bus voltage and maximum output voltage:

$$D_{max} = \frac{n * V_{out\_max}}{V_{bus\_min} + n * V_{out\_max}} = 0.3$$

The maximum possible magnetizing inductance is then calculated as:

$$L_{P\_FB\_max} = \frac{V_{bus\_min}^2 * D_{max}^2 * \eta_{FB}}{2 * P_{O\_max} * f_{sw\_FB\_min}} = 4000\mu H$$

A larger inductance will increase the operating frequency thus causing more switching losses. Due to the wide range voltage output and relative small peak current, it is recommended to choose the inductance so that the switching frequency at maximum output voltage and full load is not higher than 60kHz. In the 50W reference design, the primary flyback main inductance is set as:

$$L_{P\_FB} = 3100\mu H$$

The maximum reflected voltage is:

$$V_{R\_max} = n * (V_{out\_max} + V_F) = 191V$$

The maximum switching frequency appears at maximum bus voltage, maximum output voltage and full load:

$$f_{sw\_FB\_max} = \frac{V_{bus\_max}^2 * D^2 * \eta_{FB}}{2 * P_{O\_max} * L_{P\_FB}} = 56kHz$$

The maximum primary peak current appears at minimum bus voltage, maximum output current and full load:

$$I_{p\_pk\_max} = \sqrt{\frac{2 * P_{O\_max}}{L_{P\_FB} * \eta_{FB} * f_{sw\_FB}}} = 1.05A$$

The maximum on-time happens at minimum bus voltage, maximum output current and full load:

$$t_{on\_max} = \frac{L_{P\_FB} * i_{p\_pk\_max}}{V_{bus\_min}} = 7.38\mu s$$

The maximum primary RMS current is:

$$I_{p\_RMS\_max} = I_{p\_pk\_max} * \sqrt{\frac{D}{3}} = 0.29A$$

The maximum primary DC current is:

$$I_{p\_DC\_max} = \frac{1}{2} * I_{p\_pk\_max} * \mathrm{D} = 0.12\mathrm{A}$$

The maximum primary AC current is:

$$I_{p\_AC\_max} = \sqrt{I_{p\_RMS\_max}^2 - I_{p\_DC\_max}^2} = 0.26A$$

The maximum secondary peak current is:

$$I_{s\_pk\_max} = n * I_{p\_pk\_max} = 4.1A$$

The maximum secondary RMS current is

$$I_{s\_RMS\_max} = I_{s\_pk\_max} * \sqrt{\frac{1-D}{3}} = 2.07A$$

The maximum secondary DC current is:

$$I_{s\_DC\_max} = \frac{1}{2} * I_{s\_pk\_max} * (1 - \mathrm{D}) = 1.57\mathrm{A}$$

The maximum secondary AC current is:

$$I_{s\_AC\_max} = \sqrt{I_{s\_RMS\_max}^2 - I_{s\_DC\_max}^2} = 1.35A$$

2.5.1.3 Transformer Winding Turns

After the primary main inductance is determined and the maximum primary peak current is calculated, the turns of each winding of the flyback transformer can be calculated after the selection of the proper core. In the 50W reference design, the EE25 core with an effective area Ae of 52.5mm^2 is selected. With the assumption of the saturation flux density $\boldsymbol{B_{sat}}$ of 0.3, the minimum primary turns to avoid core saturation can be calculated as following:

$$N_p = N_{p\_min} = \frac{L_p * I_{p\_pk\_max}}{B_{sat} * A_e} \approx 206\ turns$$

The secondary turns is calculated as:

$$N_s = \frac{N_p}{n} \approx 52\ turns$$

The primary auxiliary winding is separated to two parts. One is the forward winding which provides the power for the controller XDPL8220. This ensures the precision of the primary side regulation. As this winding operates

in the forward mode, so the winding voltage is proportional to the bus voltage when the flyback MOSFET is turned on and independent from the output voltage. To make sure that the winding voltage is between 12V and 22V according to the Vcc voltage range, the turns-ratio of the primary to the primary aux forward winding is:

$$\frac{N_p}{N_{p\_aux\_FWD}} \approx 28$$

The other winding is used to sense the output voltage and the secondary side current zero-crossing moment from the primary side. As this winding operates in the flyback mode, so the winding voltage is proportional to the output voltage. The turns-ratio of the primary to the primary ZCD winding is:

$$\frac{N_p}{N_{p\_aux\_ZCD}} \approx 4.94$$

Another winding, which provides the power for the dimming circuit, is also operated in the forward mode so that the winding voltage is independent from the output voltage. To make sure that the winding voltage is between 12V and 22V, the turns-ratio of the primary to the secondary aux forward winding is:

$$\frac{N_p}{N_{s\_aux\_FWD}} \approx 28$$

The important parameters of the flyback transformer are summarized in the following table:

Table 22 Flyback Transformer Design Parameters

Parameter	Symbol	Value	Unit
Primary main inductance of the flyback transformer	L_{p_FB}	3100	µH
Turns-ratio from primary to secondary winding	N_p/N_s	3.9	-
Turns-ratio from primary to primary aux forward winding	$N_p/N_{p\_aux\_FWD}$	28	-
Turns-ratio from primary to primary ZCD winding	N_p/N_{p_ZCD}	4.94	-
Turns-ratio from primary to secondary aux forward winding	$N_p/N_{s\_aux\_FWD}$	28	-
Maximum duty cycle	D_{max}	0.3	-
Maximum primary peak current	$I_{p\_pk\_max}$	1.05	A
Maximum primary RMS current	$I_{p\_RMS\_max}$	0.29	A
Maximum secondary peak current	$I_{s\_pk\_max}$	4.1	A
Maximum secondary RMS current	$I_{s\_RMS\_max}$	2.06	A
Maximum on-time	t_{on_max}	7.38	µs
Maximum switching frequency	$f_{sw\_FB\_max}$	56	kHz

Based on the above calculated specifications, the flyback transformer can be constructed according to different design requirements like size, power efficiency and temperature etc. by selecting different bobbin and core. In order to avoid core saturation and achieve an optimized core loss, the flux density B_{max} is recommended not to exceed 0.3.

In the Infineon 50W ECG reference design, the flyback transformer is constructed by the Würth Electronic under part no. 750343127-Rev01 as a design example. The specification sheet is given as following:

Table 23 Parameters of Würth Inductor 750343127-Rev01

Parameter	Value	Unit
Inductance	3100	µH

Parameter	Value	Unit
Bobbin	EE25	-
Core material	TP4A or DMR44, N87 equivalent	-
Turns-ratio from primary to secondary winding	3.9:1	-
Turns-ratio from primary to primary aux forward winding	28:1	-
Turns-ratio from primary to primary ZCD winding	4.94:1	-
Turns-ratio from primary to secondary aux forward winding	28:1	-
DC resistance primary winding	4	Ω
DC resistance secondary winding	2	Ω
Cross section of the EE25 core	52.5	mm^2
Volume of the EE25 core	2970.92	mm^3

The maximum primary side DC conduction loss can be calculated as:

$$P_{loss\_p\_FB} = I_{p\_rms\_max}^2 * R_{DC\_p\_FB} = 0.34\text{W}$$

The maximum secondary side DC conduction loss can be calculated as:

$$P_{loss\_s\_FB} = I_{s\_rms\_max}^2 * R_{DC\_p\_FB} = 0.55\text{W}$$

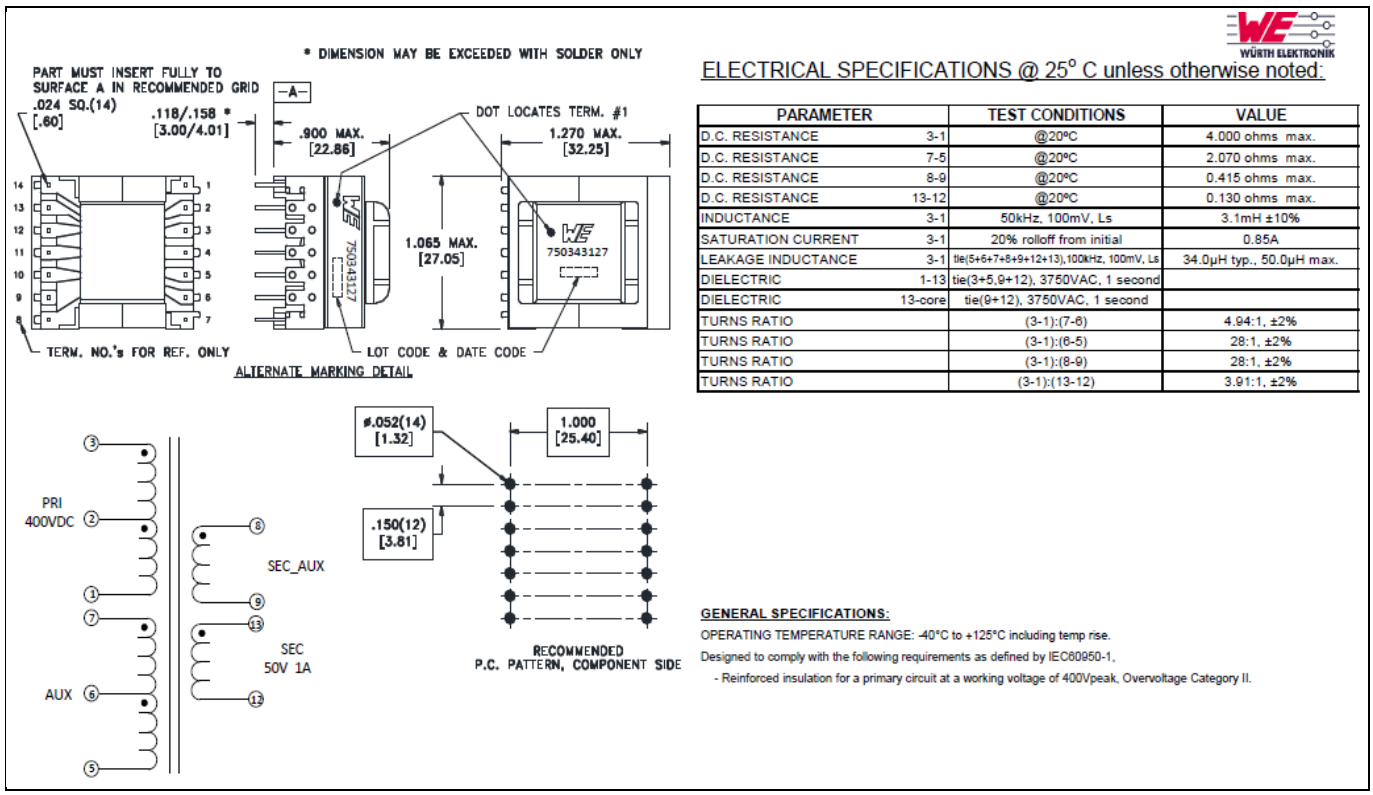


Figure 16 Flyback transformer Specification Sheet

The core loss can be looked up in the following figure with the operating frequency and the AC flux density.

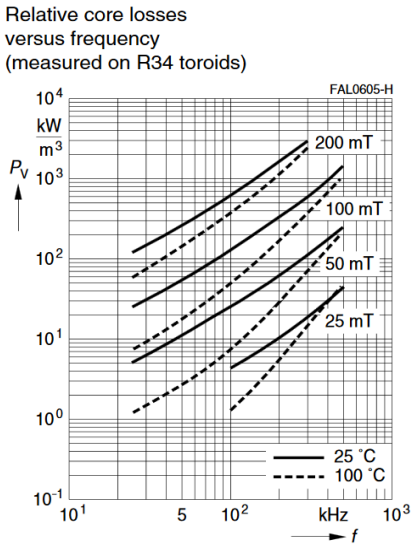


Figure 17 Relative core losses of the N87 Material

2.5.2 Flyback Primary Power MOSFET

The selection of the flyback primary side power MOSFET is based mainly on the break down voltage and the consideration of the MOSFET power dissipation. As already mentioned in the previous chapter, an 800V MOSFET is used in the reference design. In the QR+DCM mode flyback converter, the overall MOSFET losses comprise:

- Conduction loss

These losses are frequency independent and do not scale significantly with frequency. It is calculated as following:

$$P_{con\_loss\_MOS\_FB} = I_{p\_RMS\_max}^2 * R_{DS(ON)}$$

Due to the high bus voltage, the primary RMS current is quite low. It is recommended to use a MOSFET with a relative high $R_{DS(on)}$ but smaller C_{oss}.

- Turn-on transition loss

As the converter works in the QR+DCM mode, the turn-on transition loss caused by the magnetizing current can be ignored because the current rises from zero when a switching cycle starts. But to discharge the parasitic capacitors like C_{oss} and C_{can} through the MOSFET channel can cause significant turn-on transition loss. These losses occur every switching cycle and are thus frequency dependent.

- E_{oss} and $^1/_2 \cdot Ccan \cdot V^2$ **loss**

As mentioned above, the energy stored in C_{oss} and C_{can} at the time of turn-on must be dissipated in the MOSFET channel and current sense resistor during the turn-on transition. The energy stored in any capacitor is fundamentally a function of the square of the voltage across it, and thus the E_{oss} and $^1/_2 \cdot Ccan \cdot V^2$ **loss** can be very significant during high line conditions. These losses occur every switching cycle and are thus frequency dependent. To simplify the calculation, we assumed that the switching loss is approximately the same as the conduction loss:

$$P_{sw\_loss\_MOS\_FB} = P_{con\_loss\_MOS\_FB}$$

- Gate driver loss

These losses also scale linearly with frequency, but are generally a quite small contribution to the overall losses (at switching frequencies of a few hundred kilohertz and below) and depend almost exclusively on the MOSFET Q_g (total gate-charge). The gate-driver power is typically dissipated in the external gate resistor and gate-driver itself and thus does not need to be considered in the thermal calculation of MOSFET.

In the 50W ECG reference design, the 800 Infineon MOSFET IPD80R1K4P7 of the P7 family is used. With the $R_{DS(ON)}$ of 1.4Ω, the total loss of the MOSFET is calculated as below:

$$P_{loss\_MOS\_FB} = P_{sw\_loss\_MOS\_FB} + P_{con\_loss\_MOS\_FB} = 2 * P_{con\_loss\_MOS\_FB} = 0.2W$$

The important parameters for PFC MOSFET are summarized in the following table:

Table 24 PFC MOSFET Design Parameters

Parameter	Symbol	Value	Unit
Flyback MOSFET break down voltage	$V_{BR\_DSS\_FB}$	800	V
Flyback MOSFET on-resistance	$R_{DS(ON)}$	1400	mΩ
Flyback MOSFET conduction loss	$P_{loss\_MOS\_FB\_con}$	0.1	W
Flyback MOSFET switching loss	$P_{loss\_MOS\_FB\_sw}$	0.1	W
Flyback MOSFET total loss	$P_{loss\_MOS\_FB}$	0.2	W

2.5.3 Flyback Primary snubber

When the flyback power MOSFET is turned off, there is a high voltage spike on the drain due to the transformer leakage inductance and the C_{oss} of the MOSFET. This excessive voltage may lead to an avalanche break down and damage the MOSFET. Therefore, it is necessary to use an additional RCD snubber network to clamp the voltage spike in order to protect the power MOSFET.

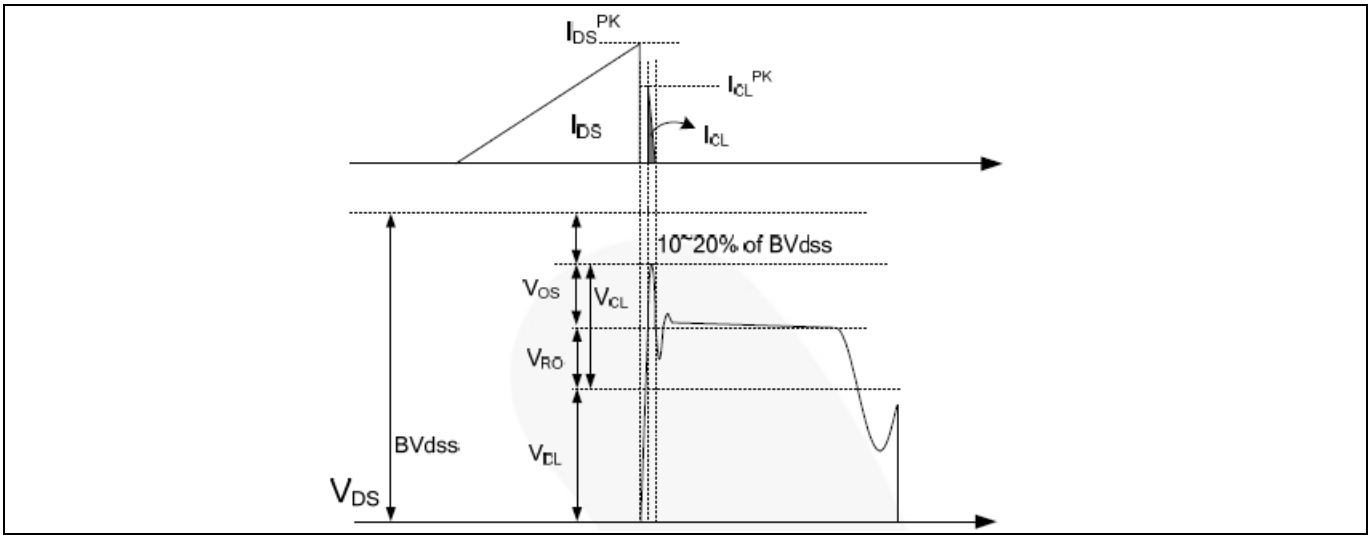


Figure 18 MOSFET Drain-Source Voltage and Snubber Capacitor Voltage

The RCD snubber network limit the high voltage spike by absorbing the current in the leakage inductance by turning on the snubber diode once the MOSFET drain voltage exceeds a certain voltage limit. The voltage over-shoot V_{os_FB} limited by the RCD snubber is related to the power dissipation in the clamping network. Setting the voltage overshoot too low can lead to severe power dissipation in the clamping circuit. For reasonable clamping circuit design, voltage over-shoot V_{os_FB} is typically 1~2 times the reflected output voltage.

It is typical to have a margin of 10~20% of the breakdown voltage for maximum MOSFET voltage stress. The maximum voltage stress of the MOSFET is given as:

$$V_{DS\_stress\_FB} = V_{bus\_OVP1} + V_{R\_max} + V_{OS\_FB} < 0.9 * V_{BR\_DSS\_FB}$$

So the voltage overshoot is:

$$V_{OS\_FB} < 0.9 * V_{BR\_DSS\_FB} - V_{bus\_OVP1} - V_{R\_max}$$

The peak current of the clamping network is:

$$I_{pk\_sn\_FB} = \sqrt{I_{p\_pk}^2 - \frac{C_{oss} * V_{OS\_FB}^2}{L_{leak\_FB}}}$$

The leakage inductance measured with an LCR meter tends to be larger than the actual effective leakage inductance. Moreover, the effective output capacitance of the MOSFET is difficult to measure. The best way to obtain these parameters correctly is to use the drain voltage waveform. Since L_{p_FB} can be measured with an LCR meter, C_{oss} and L_{LeaK_FB} can be calculated from the measured resonant period. The power dissipation in the clamping circuit is obtained as:

$$P_{loss\_sn\_FB} = \frac{1}{2} * f_{sw\_FB} * L_{leak\_FB} * I_{pk\_sn\_FB}^2 * \frac{V_R + V_{OS\_FB}}{V_{OS\_FB}}$$

Then the clamping circuit resistor is calculated as:

$$R_{sn\_FB} = \frac{(V_R + V_{OS\_FB})^2}{P_{loss\_sn\_FB}}$$

In order to reduce the power stress of the snubber resistor, it is recommended to separate the resistor to two parallel connected resistors. The actual drain voltage can be lower than the design due to the loss of stray resistance of inductor and capacitor. The resistor value can be adjusted after the power supply is actually built. The voltage rating of the snubber diode should be higher than the MOSFET drain-source break down voltage. Usually, an ultra-fast diode with 1A current rating is used for the snubber network. To allow less than 40 V ripple on the clamping capacitor voltage, the clamping capacitor should be calculated as:

$$C_{sn\_FB} \geq \frac{V_R + V_{OS\_FB}}{\Delta V_{sn} * R_{sn\_FB} * f_{sw\_FB}}$$

2.5.4 Flyback Secondary Rectifier Diode

The rectifier diode at the secondary side is selected mainly according to the voltage and current ratings. Because the flyback converter works either in QR or in DCM mode, so there is no reverse recovery requirement of the diode and an ultra-fast is thus not necessary. The maximum reverse voltage of the diode is given as:

$$V_{RRM\_D\_sec} \geq 1.25 * (\frac{V_{bus\_OVP2}}{n} + V_{out\_OV}) = 235V$$

The maximum average forward current of the rectifier diode is given as:

$$I_{F\_D\_sec} \geq 1.5 * I_{s\_RMS\_max} = 3.1A$$

The forward voltage of the rectifier diode is directly related to the power efficiency. So the forward voltage should be chosen as small as possible. With an assumption of the forward voltage of 1V, the maximum conduction loss of the diode is calculated as:

$$P_{loss\_D\_sec} = I_{out\_max} * V_{F\_D\_sec} = 1.5\text{W}$$

The important parameters for secondary rectifier diode which used in the 50W ECG reference design are summarized in the following table:

Table 25 Flyback Secondary Rectifier Diode Design Parameters

Parameter	Symbol	Value	Unit
Maximum reverse voltage	$V_{RRM\_D\_sec}$	300	V
Average rectified forward current	$I_{F\_D\_sec}$	2x10	A
Forward voltage	$V_{F\_D\_sec}$	0.9	V

2.5.5 Flyback Secondary Snubber

When the primary-side MOSFET is turned on, severe voltage oscillation occurs across the secondary-side diode, as shown in Figure 19. This is caused by the oscillation between the diode parasitic capacitance $C_{D\_sec\_FB}$ and transformer secondary side leakage inductance $L_{leak\_sec\_FB}$. To reduce the oscillation, an RC snubber is typically used, as shown in the following figure:

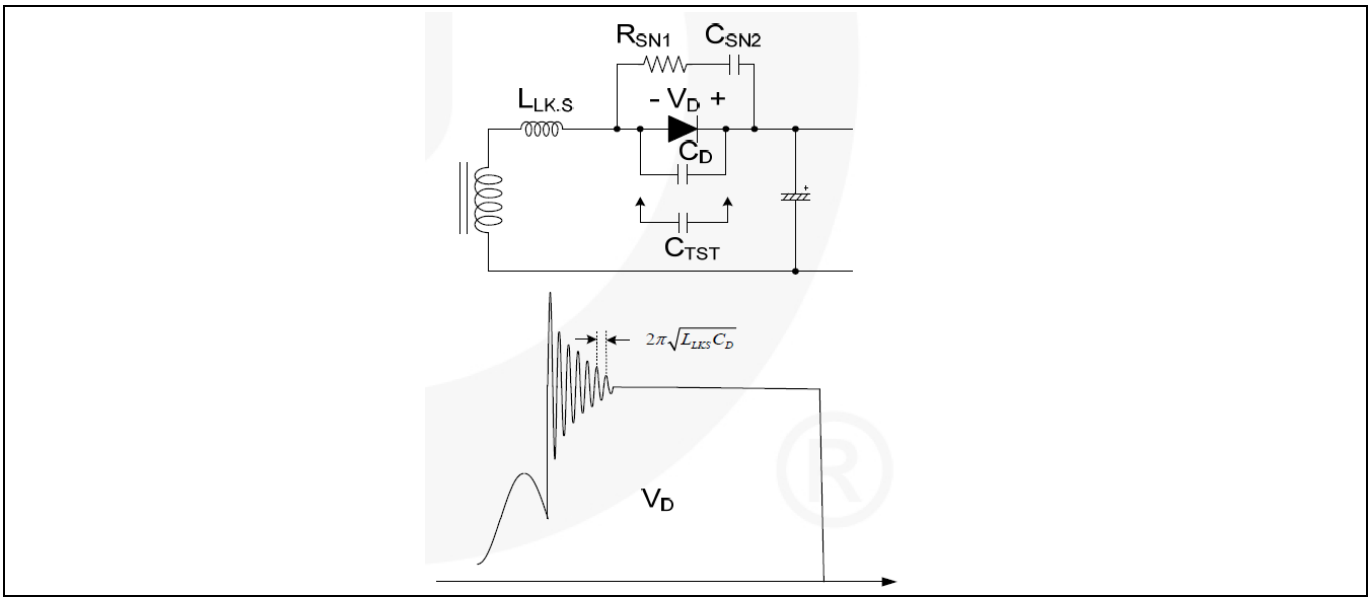


Figure 19 Secondary Rectifier Diode Voltage Waveform

The-secondary side leakage inductance and the diode parasitic capacitance are difficult to measure with an LCR meter. The best way is to use a test capacitor across the diode. First, measure the natural resonance period $T_{res\_D\_sec}$ without to connect anything to the diode. Then, add a test capacitor across the diode C_{test} such that the test resonance period $T_{res\_D\_sec\_test}$ becomes about twice its original value and measure the test resonance period. With the measured $T_{res\_D\_sec}$, $T_{res\_D\_sec\_test}$, and C_{test}, the resonance parameters can be calculated as:

$$C_{D\_sec\_FB} = \frac{C_{test}}{\left(\frac{T_{res\_D\_sec\_test}}{T_{res\_D\_sec}}\right)^2 - 1}$$

$$L_{leak\_sec\_FB} = \left(\frac{T_{res\_D\_sec}}{2\pi}\right)^2 * \frac{1}{C_{D\_sec\_FB}}$$

Then the snubber circuit parameters can be calculated as following:

$$R_{sn\_D\_sec} = \sqrt{\frac{L_{leak\_sec\_FB}}{C_{D\_sec\_FB}}}$$

$$C_{sn\_D\_sec} = 2.5 * C_{D\_sec\_FB}$$

If the voltage rating of the secondary rectifier diode is selected high enough to provide enough margins, then the snubber circuit can be saved for a better power efficiency.

2.5.6 Flyback Secondary Output Capacitor

Output capacitance will need to be selected carefully in order to meet the LED ripple current. It represents a trade-off between LED ripple current and BOM cost that the designer has to meet. In addition, the capacitor has to be able to handle the ripple current through it. As a rule of thumb, the total output capacitors should be able to handle at least 2.5 times the max LED DC current at maximum temperature.

The ripple current of the output capacitor is obtained as:

$$\Delta I_{out\_cap} = \sqrt{I_{s\_RMS}^2 - I_{out}^2}$$

The ripple current should be smaller than the ripple current specification of the capacitor. The voltage ripple on the output is given by:

$$\Delta V_{out} = \frac{I_{out} * D_{max}}{C_{out} * f_{sw\_FB}} + \frac{I_{p\_pk\_FB} * V_R * R_{C_{out}}}{V_{out} + V_{F\_D\_sec}}$$

Where R_c is the effective series resistance (ESR) of the output capacitor.

Sometimes it is impossible to meet the ripple specification with a single output capacitor due to the high ESR of the electrolytic capacitor. Then, additional LC filter stages (post filter) can be used. When using the post filters, be careful not to place the corner frequency too low. Too low a corner frequency may make the system unstable or limit the control bandwidth. It is typical to set the corner frequency of the post filter at around 1/10~1/5 of the switching frequency.

2.5.7 Flyback Zero-crossing Detection Divider

The digital controller XDPL8220 provides primary side flyback converter control of output current and output voltage. No external feedback components are necessary for the current control as the primary side regulation control loop is fully integrated. This primary side control feature is realized through the ZCD pin of XDPL8220, which has three functions:

- Output voltage measurement:

The output voltage is determined by measuring the reflected output voltage on the auxiliary winding of the flyback transformer. A resistor divider adapts the voltage to the operating range of the ZCD pin. The voltage measured at the ZCD pin is calculated:

$$V_{ZCD} = (V_{out} - V_{F\_D\_sec}) * \frac{N_{p\_ZCD}}{N_s} * \frac{R_{ZCDL\_FB}}{R_{ZCDH\_FB} + R_{ZCDL\_FB}}$$

The measurement range of the ZCD pin is from 0V to 2.66V. To ensure that the maximum bus voltage and output voltage can be measured at the pin, following relation must be fulfilled:

$$R_{ZCDH\_FB} > \frac{V_{bus\_OVP1} * \frac{N_{p\_ZCD}}{N_p} - V_{ZCD\_clamp} * \frac{V_{out\_OV}}{V_{ZCD\_max}} * \frac{N_{p\_ZCD}}{N_s}}{I_{ZCD\_clamp\_max}} = 30k\Omega$$

where

- V_{bus_OVP1} is the bus over voltage protection level 1 threshold
- V_{out_OV} is the output overvoltage threshold
- V_{ZCD_clamp} = 0.2 V (refer to the XDPL8220 datasheet)
- V_{ZCD_max} = 2.66 V is the upper measurement range (refer to the XDPL8220 datasheet)
- $I_{ZCD\_clamp\_max}$ = 3.2 mA (refer to the XDPL8220 datasheet)

In the 50W ECG reference design, R_{ZCDH_FB} = 68KΩ is selected to have enough margin and low power loss for a better standby power consumption. Then the lower resistor of the divider should fulfill the following relation:

$$R_{ZCDL\_FB} < \frac{R_{ZCDH\_FB} * V_{ZCD\_max}}{V_{out\_OV} * \frac{N_{p\_ZCD}}{N_s} - V_{ZCD\_max}} = 4.7k\Omega$$

R_{ZCDL_FB} = 3.9KΩ is selected. To ensure the output voltage measurement accuracy, it is strongly recommended that both resistors should have at least 1% intolerance or less.

Attention*: *Please note that the demagnetizing time has to be longer than 2.0 µs to ensure that the reflected output voltage can be sensed correctly at the ZCD pin.

- Bus voltage measurement:

As already described above, the bus voltage is monitored when the flyback MOSFET is turned on. The resistor divider adapts the negative voltage to the operating range of the ZCD pin. This second measurement path is required to protect against component failures in the VS measurement path (open loop protection for the PFC stage).

- Zero-crossing Detection:

Zero-crossing detection is to catch the moment, when the transformer is completely demagnetized and the secondary current decreases to zero. It is necessary for the QR and DCM mode. Meanwhile, it is used to realize the valley switching, which reduces the switching loss of the flyback MOSFET.

In order to filter the noise spike at the ZCD pin so that there is no switching cycle triggered unwanted, it is recommended to use a 100pF ceramic capacitor directly near the pin. As the capacitance of such ceramic capacitors varies with temperature, a C0G/NP0 ceramic capacitor is more suitable.

Note: *The filter capacitor at the ZCD pin is not used to delay the MOSFET turning on to realize the valley switching. This is done in the XDPL8220 internally.*

The important parameters for designing the zero-crossing divider are summarized in the following table:

Table 26 Zero-crossing Detection Divider Design Parameters

Parameter	Symbol	Value	Unit
ZCD pin voltage measurement range	V_{ZCD}	0 ~ 2.66	V
Upper resistor of the ZCD divider	R_{ZCDH_FB}	68	kΩ
Lower resistor of the ZCD divider	R_{ZCDL_FB}	3.9	kΩ
Filter capacitor at the ZCD pin	C_{ZCD}	100	pF

2.5.8 Flyback Current Sense

As the flyback converter operates in the peak current control mode, the power is transferred from the primary to the secondary side with cycle by cycle current limitation. This peak current control mode compensates the bus voltage ripple automatically which contributes to the minimization of the secondary current output variation. The primary peak current is determined by sensing the voltage V_{CS} at the CS pin which is connected via a RC-filter to the current sensing shunt resistor. The output current I_{out} will then be calculated based on the output diode conduction time and the switching period.

The recommended operating voltage range at the CS pin is 0 V to slightly lower than 1.2 V. According to the calculated maximum primary peak current which calculated in the previous chapter, the shunt resistor must follow:

$$R_{cs\_FB} < \frac{1.2}{I_{p\_pk\_max}} = 1.14\Omega$$

For a lower power consumption, R_{cs_FB} = 0.8Ω is selected. To reduce the power stress of the shunt resistor, two parallel connected resistors of 1.6Ω are used. For the control accuracy, resistors with intolerance less than 1% must be used. The power dissipation of each resistor is then calculated as:

$$P_{loss\_CS\_FB} = \frac{1}{2} * I_{p\_RMS}^2 * R_{cs\_FB}$$

In order to filter the voltage spike so that the peak current control is not triggered by wrong, there is a leading edge blanking time built inside the controller. Besides, an external filter is recommended as well. In the 50W ECG design, a RC-filter is used with $R_{flt\_cs\_FB}$ = 470Ω and $C_{flt\_cs\_FB}$ = 330pF. The capacitor should be placed directly near the ***CS*** pin.

The important parameters for designing the current sense resistor are summarized in the following table:

Table 27 Flyback Converter Current Sense Design Parameters

Parameter	Symbol	Value	Unit
Flyback current sense pin voltage measurement range	V_{cs_FB}	0 ~ 1.2	V
Flyback current sense shunt resistor	R_{cs_FB}	1.6//1.6 = 0.8	Ω
Flyback current sense filter resistor	$R_{flt\_CS\_FB}$	470	Ω
Flyback current sense filter capacitor	$C_{flt\_CS\_FB}$	330	pF

2.5.9 Flyback Output Control Scheme

The XDPL8220 includes three different control schemes for a CC (constant current), CV (constant voltage) or LP (limited power) output. Different use cases require the controller to operate according to different operation schemes:

- In the case of typical LED strings, the forward voltage of the LED string determines the output voltage of the driver. XDPL8220 operates in CC and drives a constant output current I_{out_full} to the load. The forward voltage of the connected LED string has to be below a configurable maximum value V_{out_set}.
- In the case of LED loads including a power stage (e.g. Infineon BCR linear regulators or Infineon DC/DC buck ILD2111), XDPL8220 operates in CV, ensuring a constant voltage V_{out_set} to the load. The total output current drawn by the load has to be below a configurable maximum value I_{out_full}.

- In the case of a high output current set-point I_{out_full} and an overly long LED string which exceeds the configurable power limit P_{out_set}, XDPL8220 operates in LP to ensure that the power limit of the driver is not exceeded. The controller reduces the output current automatically, ensuring light output without any interruption even for overly long LED strings. The forward voltage of the connected LED string has to be below a configurable maximum value V_{out_set}.

For every update of the control loop, the control scheme is selected on the basis of the current operation conditions (output voltage V_{out} and output current I_{out}) and their distance to the three limiting set-points (V_{out_set}, P_{out_set} and I_{out_full}):

- For CC schemes, the internal reference current I_{out_full} is weighted according to thermal management and a dimming curve to yield I_{out_set}. The calculated output current I_{out} is compared with the weighted reference current I_{out_set} to generate an error signal for the output current.
- For CV schemes, the sensed output voltage V_{out} at the ZCD pin is compared to a reference voltage V_{out_set} to generate an error signal for the output voltage.
- For LP schemes, the output current is limited to a maximum of $I_{out\_set} = P_{out\_set} / V_{out}$.

Out of these three schemes, for each step the most critical error is selected (see Figure 20):

1. If any set-point is exceeded, the largest error for power decrease is selected to bring the controller back to the desired operating point as quickly as possible.

2. If the current operating conditions are below all three set-points, the smallest error for power increase is selected to avoid overshooting any set-point.

The selected error signal is fed into a compensator to control the gate driver switching parameters (i.e. duty-cycle and frequency) for the power MOSFET of the Flyback converter.

In dimming cases, the output current set-point I_{out_set} is located between I_{out_min} and I_{out_full} and varies according to the sensed PWM duty cycle D_{DIM}. Dimming can be visualized by moving the vertical line for the output current set-point in Figure 20 from right to left.

Note: *An operation in limited power mode can cause dimmer dead-travel until the controller enters constant current mode.*

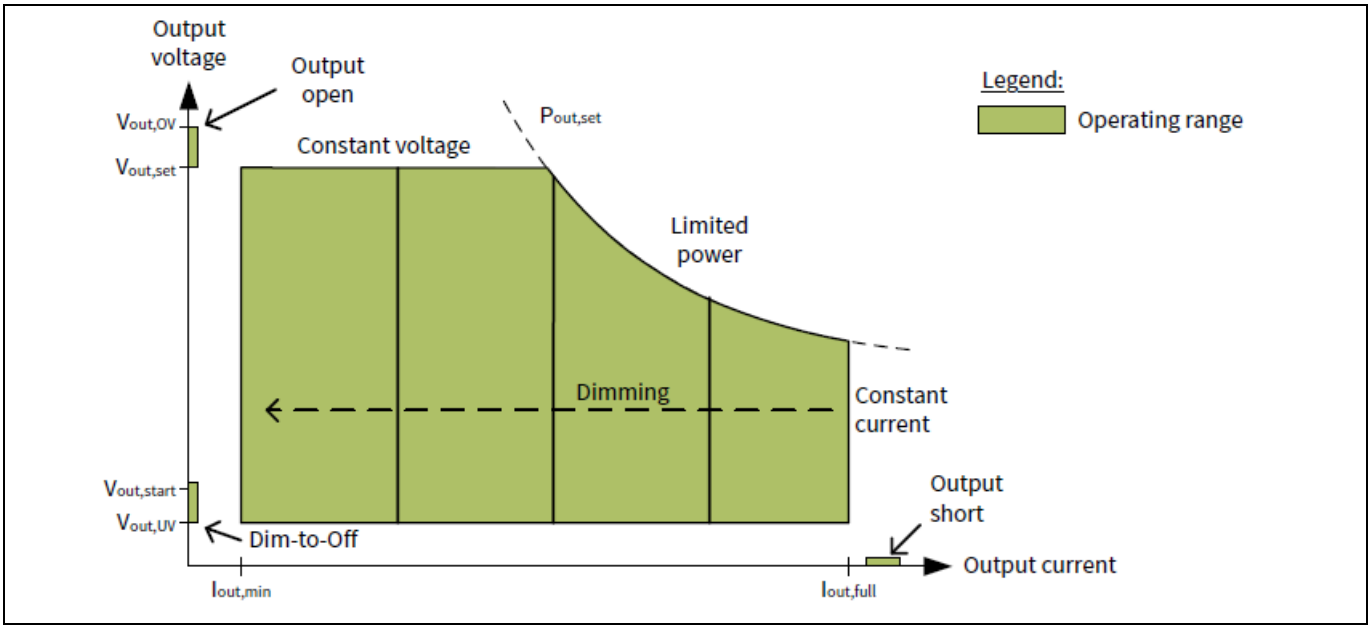


Figure 20 Secondary Rectifier Diode Voltage Waveform

Attention: One or more of the output control schemes can be deactivated by configuration of the set-points. Some examples are given below:

- The LP scheme is not active for $P_{out\_set} > V_{out\_set} * I_{out\_full}$. For such a configuration, the controller will only select between a CC and CV scheme.
- The CV scheme is not active for $V_{out\_set} = V_{out\_OV}$ as the output overvoltage protection will be triggered.
- The CC scheme is not active for $I_{out\_full} = I_{out\_OC}$ as the output overcurrent protection will be triggered.

The important parameters to set up the flyback converter output are summarized in the following table:

Table 28 Flyback Converter Output Set-Up Design Parameters

Parameter	Symbol	Value	Unit
Flyback No-dimmed output current	I_{out_full}	1500	mA
Flyback output voltage set-point	V_{out_set}	50	V
Flyback output power limitation set-point	P_{out_set}	50	W

2.5.10 Flyback Multi-Mode Control

The control loop of XDPL8220 uses two different switching modes as shown in the following Figure 21. QRM1 is optimized for high efficiency at high loads while DCM is used in light load conditions.

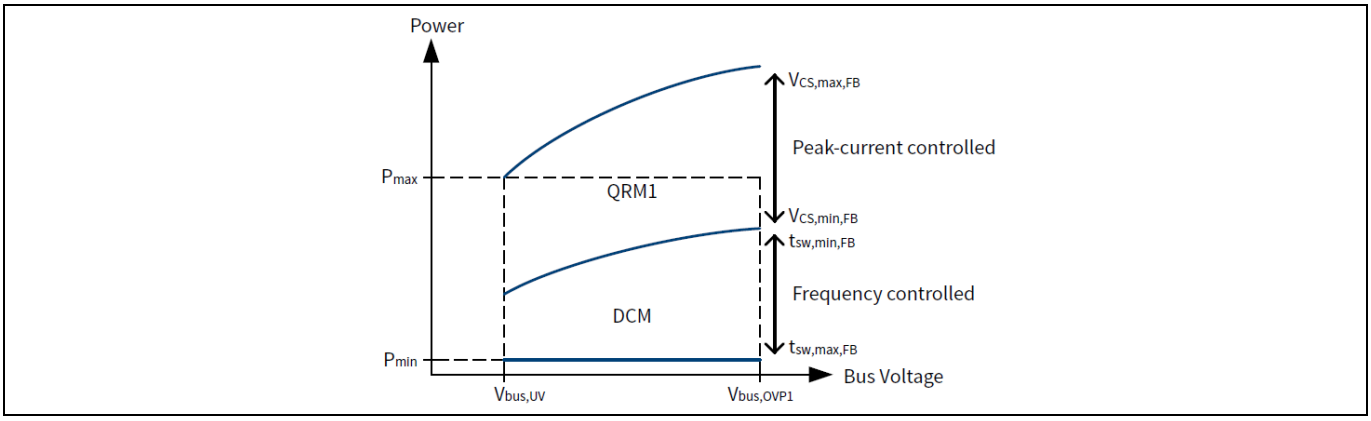


Figure 21 Flyback Multi-Mode Control

- QRM1: This mode maximizes the efficiency by switching on the 1st valley of the ZCD signal. This ensures zero current switching with a minimum of switching losses. The power is controlled by regulating the primary peak current.
- DCM: This mode is used if the peak current limit reaches its minimum value $V_{CS\_min\_FB}$. To allow lower output power, the controller extends the switching period later than the 1st valley.

The minimum primary peak current $I_{p\_pk\_min}$ is restricted by:

$$I_{p\_pk\_min} = t_{off\_min} * \frac{N_p}{N_s} * \frac{V_{out\_OV}}{L_{p\_FB}} = 0.15A$$

And the mode change from QRM1 to DCM happens if the CS pin voltage:

$$V_{CS\_\min\_FB} \le I_{p\_pk\_min} * R_{CS\_FB} = 0.12V$$

The minimum power is limited by the transformer primary inductance L_{p_FB}, the minimum switching frequency $f_{sw\_min\_FB}$ and the minimum primary peak current $I_{p\_pk\_min}$:

$$P_{O\_\min} = \frac{1}{2} * L_{p_{FB}} * I^2_{p\_pk\_min} * f_{sw\_\min\_FB} = 0.58W$$

The important parameters to set up the flyback converter multi-mode control scheme are summarized in the following table:

Table 29 Flyback Converter Multi-Mode Set-Up Design Parameters

Parameter	Symbol	Value	Unit
Flyback minimum primary peak current	$I_{p\_pk\_min}$	0.15	A
Flyback minimum CS voltage for the QR1 and DCM mode change	$V_{CS\_min\_FB}$	0.12	V
Flyback minimum output power	P_{O_min}	0.58	W

Note: *If the load drops below the minimum load of P_{O_min}, the output voltage will rise up to the output overvoltage threshold V_{out_ov} and trigger the protection. An auto-restart can be used to keep the output voltage close to V_{out_ov} until the load increases again.*

2.5.11 Flyback Start-Up Control

After the bus voltage reaches the threshold $V_{bus\_start\_FB}$ for the flyback converter to start-up, the controller XDPL8220 initiates a soft-start for the flyback converter to minimize the switching stress for the flyback power MOSFET and secondary rectifier diode.

As shown in the following Figure 22, after the start-up check, the flyback converter starts with switching frequency $f_{sw\_start\_FB}$ and the cycle-by-cycle current limit is increased in steps of V_{CS_step} with a configurable duration $t_{softstart}$ for each step. After the final limit level $V_{CS\_max\_start\_FB}$ has been reached, the output will be charged until the minimum output voltage V_{out_start} has been reached. At this condition, the Continuous Conduction Mode (CCM) as well as the output under-voltage protections are activated and the control loop takes over. The starting point for the control loop is to operate in DCM at lowest switching frequency and shortest on-time. These switching parameters avoid any overshoot of output current for short LED string in dimmed conditions.

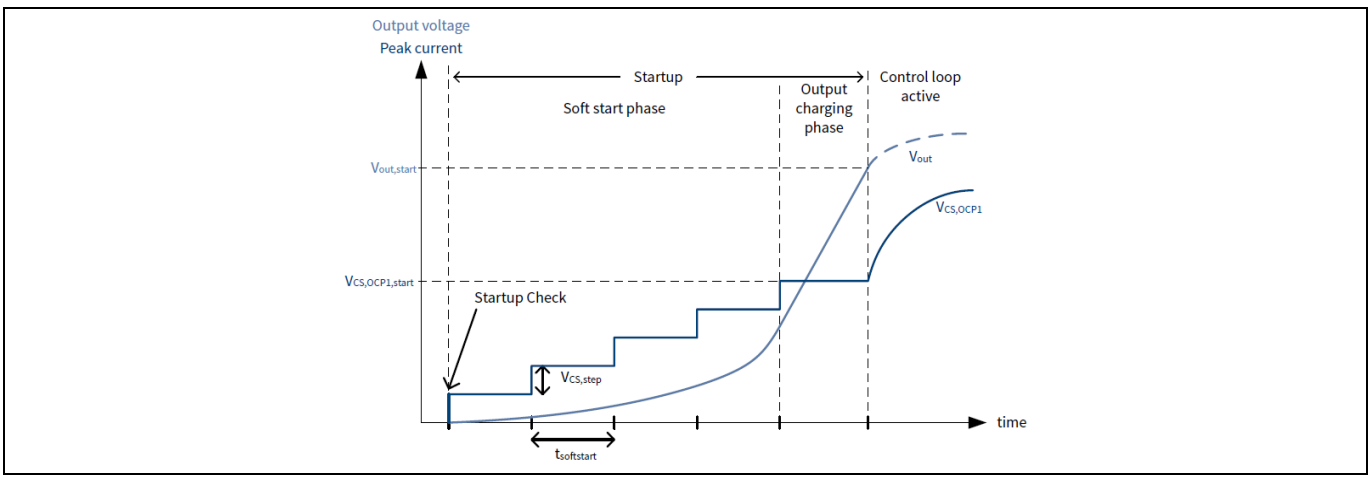


Figure 22 Flyback Start-Up Control

The important parameters to set up the flyback converter start-up control are summarized in the following table:

Table 30 Flyback Converter Multi-Mode Set-Up Design Parameters

Parameter	Symbol	Value	Unit
Bus voltage threshold for the flyback stage start-up	$V_{bus\_start\_FB}$	460	V
Flyback soft-start switching frequency	$f_{sw\_start\_FB}$	20	kHz
Flyback soft-start peak current limit changing step	V_{CS_step}	0.1	V
Flyback peak current limit threshold to end the soft-start phase and enter output charging phase	$V_{CS\_max\_start\_FB}$	0.6	V
Flyback soft-start time duration of each step	$t_{softstart}$	0.5	ms
Flyback output voltage threshold for control loop to take over the regulation	V_{out_start}	12.5	V

2.5.12 Flyback Protection Features

Protections ensure the operation of the controller under restricted conditions. Protections are triggered if fault conditions are present longer than the blanking time configured for each protection. The controller will react to a triggered protection as configured. The following table defines which protections are enabled or disabled with respect to the state of the stages described in the last chapter:

Table 31 Flyback Protection States

Protection	Stopped	Start-Up	Regulation
Flyback primary over-current level 2 protection	Disabled	Enabled	Enabled
Flyback output under-voltage protection at startup	Disabled	Enabled	Disabled
Flyback output under-voltage protection during operation	Disabled	Disabled	Enabled
Flyback output over-voltage protection	Disabled	Enabled	Enabled
Flyback output over-current protection	Disabled	Enabled	Enabled
Flyback output over-power protection	Disabled	Enabled	Enabled
Flyback CCM protection	Disabled	Disabled	Enabled
Flyback soft-start failure	Disabled	Enabled	Disabled

2.5.12.1 Flyback Primary Over-Current Protection

The primary side overcurrent protection implemented in hardware covers fault conditions like a short in the transformer primary winding or an open CS pin. The primary side current is compared to a configurable overcurrent protection threshold V_{CS_OCP2}. If the threshold is exceeded for longer than the blanking time $t_{blank\_OCP2\_FB}$, the protection will be triggered. The flyback gate driver will be disabled at once by hardware and PFC stage is disabled, too by the firmware. After then, XDPL8220 will enter the latch mode.

The important design parameters for primary over-current protection are summarized in the table below:

Table 32 Flyback Primary Over-Current Protection Design Parameters

Parameter	Symbol	Value	Unit	Configurable
Flyback OCP level 2 threshold	V_{CS_OCP2}	1.6	V	No
Blanking time for flyback OCP2	$t_{blank\_CP2\_FB}$	250	ns	No
Reaction for flyback OCP2	-	Latch	-	No

2.5.12.2 Flyback Output Under-Voltage Protection

In the case of a short in the output, the output voltage may drop to a very low level. Detection of the under-voltage of the output is realized by measurement using the ZCD pin. The output voltage is compared to a configurable under-voltage protection threshold V_{out_UV}. If the threshold is exceeded for longer than the blanking time $t_{blank\_out\_UV}$, the protection will be triggered. Both PFC and flyback stages are disabled and XDPL8220 will enter auto-restart mode.

Output under-voltage protection is disabled during startup. The startup threshold V_{out_start} has to be configured higher than the under-voltage threshold to allow undershoots. This occurs especially for resistive loads.

The important design parameters for output under-voltage protection are summarized in the table below:

Table 33 Flyback Output Under-Voltage Protection Design Parameters

Parameter	Symbol	Value	Unit	Configurable
Flyback under-voltage protection threshold	V_{out_UV}	8	V	Yes
Blanking time for output under-voltage protection	$t_{blank\_out\_UV}$	1	ms	Yes
Reaction for output under-voltage protection	-	Auto-Restart	-	Yes

2.5.12.3 Flyback Output Over-Voltage Protection

In case of an open output, the output voltage may rise to a high level. The Overvoltage detection of the output is provided by measurement at the ZCD pin. The output voltage is compared to a configurable overvoltage protection threshold V_{out_OV}. If the threshold is exceeded for longer than the blanking time $t_{blank\_out\_OV}$, the protection will be triggered. Both PFC and flyback stages are disabled and XDPL8220 will enter auto-restart mode.

Note: *The blanking time $t_{blank\_Vout\_OV}$ should be set to the minimum value to minimize overshoots of the output voltage above the protection threshold.*

Note: *This protection is usually triggered if the output is open or the output load drops below the minimum load P_{min}.*

The important design parameters for output over-voltage protection are summarized in the table below:

Table 34 Flyback Output Over-Voltage Protection Design Parameters

Parameter	Symbol	Value	Unit	Configurable
Flyback over-voltage protection threshold	V_{out_OV}	53	V	Yes
Blanking time for output over-voltage protection	$t_{blank\_out\_OV}$	0.2	ms	Yes

Parameter	Symbol	Value	Unit	Configurable
Reaction for output over-voltage protection	-	Auto-Restart	-	Yes

In addition to the output over-voltage provides by the XDPL8220 from the primary side, there are also two other analog hardware protection features necessary against the output over-voltage:

- To protect the secondary output capacitors, a zener diode with a current limitation resistor will clamp the output voltage under the voltage rating of the output capacitor.
- An active bleeder at the secondary side will discharge the output capacitor continuously if the flyback converter is in the auto-restart or latch mode.

2.5.12.4 Flyback Output Over-Current Protection

Overcurrent detection in the output current is provided on the basis of the calculated output current. The calculated output current is compared to a configurable overcurrent protection threshold I_{out_OC}. If the threshold is exceeded for longer than the blanking time $t_{blank\_out\_OC}$, the protection will be triggered. Both PFC and flyback stages are disabled and XDPL8220 will enter auto-restart mode.

Table 35 Flyback Output Over-Current Protection Design Parameters

Parameter	Symbol	Value	Unit	Configurable
Flyback over-current protection threshold	I_{out_OC}	1600	mA	Yes
Blanking time for output over-voltage protection	$t_{blank\_out\_OC}$	1	ms	Yes
Reaction for output over-voltage protection	-	Auto-Restart	-	Yes

2.5.12.5 Flyback Output Over-Power Protection

Overpower detection of the output power is provided on the basis of the calculated output power. The calculated output power is compared to a configurable overpower protection threshold P_{out_OP}. If the threshold is exceeded for longer than the blanking time $t_{blank\_out\_OP}$, the protection will be triggered. Both PFC and flyback stages are disabled and XDPL8220 will enter auto-restart mode.

Table 36 Flyback Output Over-Current Protection Design Parameters

Parameter	Symbol	Value	Unit	Configurable
Flyback over-current protection threshold	P_{out_OP}	52	W	Yes
Blanking time for output over-voltage protection	$t_{blank\_out\_OP}$	1	ms	Yes
Reaction for output over-voltage protection	-	Auto-Restart	-	Yes

2.5.12.6 Flyback CCM Protection

Continuous conduction mode (CCM) operation occurs when the magnetizing current does not decrease to zero before the next switching cycle starts. This happens usually in the soft-start phase or when the output voltage is shorted. However, when the output is over-loaded or bus voltage is too low, the inductor peak current will be very high and the demagnetizing of the flyback transformer cannot be operated completely, too. In the soft-start phase, the CCM operation is allowed for limited time but in other conditions, XDPL8220 must enter the protection mode.

The CCM operation is monitored at the flyback ZCD pin. When the ZCD signal does not come till the maximum switching period time-out happens, it will be treated as a CCM cycle. If the CCM operation happens beyond the blanking time $t_{blank\_CCM\_FB}$, both PFC and flyback stages are disabled and XDPL8220 will enter auto-restart mode.

The important design parameters for flyback CCM protection are summarized in the table below:

Table 37 PFC CCM Protection Design Parameters

Parameter	Symbol	Value	Unit	Configurable
Blanking time for PFC CCM operation	$t_{blank\_CCM\_FB}$	1	ms	Yes
Reaction PFC CCM protection	-	Auto-Restart	-	Yes

2.5.12.7 Soft-start Failure

When the bus voltage is very low or the output is over-loaded/shorted, the start-up time of the flyback converter is very long. In both cases, the protection is triggered and XDPL8220 will enter the auto-restart mode. The flyback soft-start time is monitored from the moment that the bus voltage reaches threshold to start flyback converter till the secondary output voltage reaches the threshold V_{out_start}. If this time exceeds the defined maximum allowed flyback soft-start time $t_{start\_max\_FB}$, protection will be triggered. Both PFC and flyback stages are disabled and XDPL8220 will enter auto-restart mode.

The important design parameters for flyback soft-start failure are summarized in the table below:

Table 38 PFC Soft-Start Failure Design Parameters

Parameter	Symbol	Value	Unit	Configurable
Voltage threshold for flyback soft-start end	V_{out_start}	12.5	V	Yes
Maximum allowed flyback soft-start time	$t_{start\_max\_FB}$	30	ms	Yes
Reaction flyback soft-start failure	-	Auto-Restart	-	Yes

2.6 Design the Power Supply for XDPL8220

The power supply for the controller XDPL8220 is provided by the capacitors connected to the V_{cc} pin. It is strongly recommended to use both electrolytic capacitor and ceramic capacitor parallel connected as V_{cc} capacitors. Due to its high capacitance, electrolytic capacitor is suitable as charge stores but has a bad AC coupling behavior. Ceramic capacitor in the contrary has an excellent AC decoupling effect but has a capacitance derating strongly dependent on voltage and temperature. There are three different way to charge the V_{cc} capacitors for power supply of XDPL8220:

- Start-up Cell

At every cold start, after the AC or DC is applied at input, the V_{cc} capacitors are charged by the start-up cell before the V_{cc} reaches the on-threshold. The start-up cell is connected through the HV pin to the rectified AC or DC input. After the XDPL8220 is active, the start-up cell is switched off. The charging current is dependent on the RMS value of the input voltage. Using AC input as example, the maximum charge current through the start-up cell happens at maximum AC input:

$$I_{charge\_max} = \frac{\sqrt{2} * V_{in\_max\_rms}}{R_{HV}} = 3.95mA$$

And the minimum charge current through the start-up cell happens at minimum AC input:

$$I_{charge\_min} = \frac{\sqrt{2} * V_{in\_min\_rms}}{R_{HV}} = 1.29mA$$

- PFC auxiliary winding

When the XDPL8220 is active, the start-up cell will be switched off. After the input AC/DC detection, XDPL8220 will start PFC boost converter. The V_{cc} capacitors can be then charged by the PFC auxiliary winding. Due to the slowly increased voltage difference across the PFC boost inductor in the start-up phase, the charging current is very limited at the beginning. It is recommended to use a charge pump together with a linear regulator for the power supply. The linear regulator ensures that the V_{cc} is under the over-voltage threshold and the zener diode can be so selected that later when the flyback converter is active, the PFC auxiliary winding power supply can be disabled.

If an average IC power consumption of 8mA is assumed and the V_{cc} must be hold higher than the off-threshold for 15ms without any power supply due to the PFC input check, the V_{cc} capacitors must fulfill following requirement:

$$C_{Vcc} > \frac{I_{IC\_avg\_startup}}{V_{VCC\_on\_min} - V_{VCC\_off}} * 15ms = 9.2\mu F$$

- Flyback auxiliary winding

After the bus voltage is boosted to the threshold to start flyback converter, the charging of V_{cc} capacitors should be taken over by the flyback auxiliary winding. The flyback auxiliary winding operates in the forward mode so the winding voltage is dependent only on the fixed bus voltage and almost constant. In comparison to the flyback mode operation, the advantages are obviously: no linear regulator is required due to the wide output voltage range and the influence on the accuracy of the primary side regulation is also minimized.

With the winding turns-ratio $N_p/N_{p\_aux\_FWD}$ of 28:1 and the voltage drop 1V of the rectifier diode, the V_{cc} voltage is around 15V. The zener diode of the linear regulator for PFC auxiliary winding power supply should be selected as 12V so that the PFC power supply is disabled after flyback converter is active.

In the 50W ECG reference design, there are 3 V_{cc} capacitors of 9.5 µF all together connected parallel directly to the V_{cc} pin. One electrolytic capacitor of 4.7µF and two ceramic capacitors: 4.7 µF and 100nF. The ceramic capacitors should be placed directly near the V_{cc} pin. At the start-up, the maximum time to charge these capacitors to the V_{cc} on-threshold is:

$$t_{HV\_charge} = C_{Vcc} * \frac{V_{VCC\_on\_max}}{I_{HV\_min}} = 162ms$$

With a start-up time 50ms of PFC and 30ms start-up time for flyback, the time-to-light can be controlled within 250ms as following calculated:

$$time\_to\_light = t_{HV\_charge} + t_{startup\_PFC} + t_{startup\_FB} = 242ms$$

The important parameters for designing the power supply for XDPL8220 are summarized in the following table:

Table 39 Power Supply for XDPL8220 Design Parameters

Parameter	Symbol	Value	Unit
Minimum AC input Voltage	$V_{in\_AC\_min\_rms}$	90	Vrms
Maximum AC input voltage	$V_{in\_AC\_min\_rms}$	277	Vrms

Parameter	Symbol	Value	Unit
Maximum V_{cc} on threshold	$V_{Vcc\_on\_max}$	22	V
Minimum V_{cc} on threshold	$V_{Vcc\_on\_min}$	20.5	V
V_{cc} off threshold	V_{Vcc_off}	6	V
HV current limitation resistor	R_{HV}	33x3=99	kΩ
V_{cc} capacitor	C_{Vcc}	4.7+4.7+0.1=9.5	µF

2.7 Design the Active bleeder

Output bleeder circuitry is necessary to discharge the remaining electrical charge stored in the output capacitor when the LEDs are disconnected. In the case of Dim-to-off, output bleeder helps to keep the output voltage under the LEDs forward voltage so that there is no light.

The active bleeder consists of three mainly parts: charge pump, two MOSFET switches and discharge resistor. As the schematic shows below in the figure 23, if the flyback converter is in the normal operation, the charge pump will charge the capacitor ***C106*** continuously and the MOSFET ***Q101*** is on and ***Q100*** is off. There is no discharge of the output capacitor. If the flyback converter is in the auto-restart or latch mode, capacitor C106 will be discharged so the MOSFET ***Q101*** is off and ***Q100*** is on. The output capacitor is discharged. The discharge resistors ***R103*** and ***R104*** decides the discharge current and the discharge resistor ***R105*** for capacitor C106 decides how long after the no-switching of the flyback converter the discharge should begin.

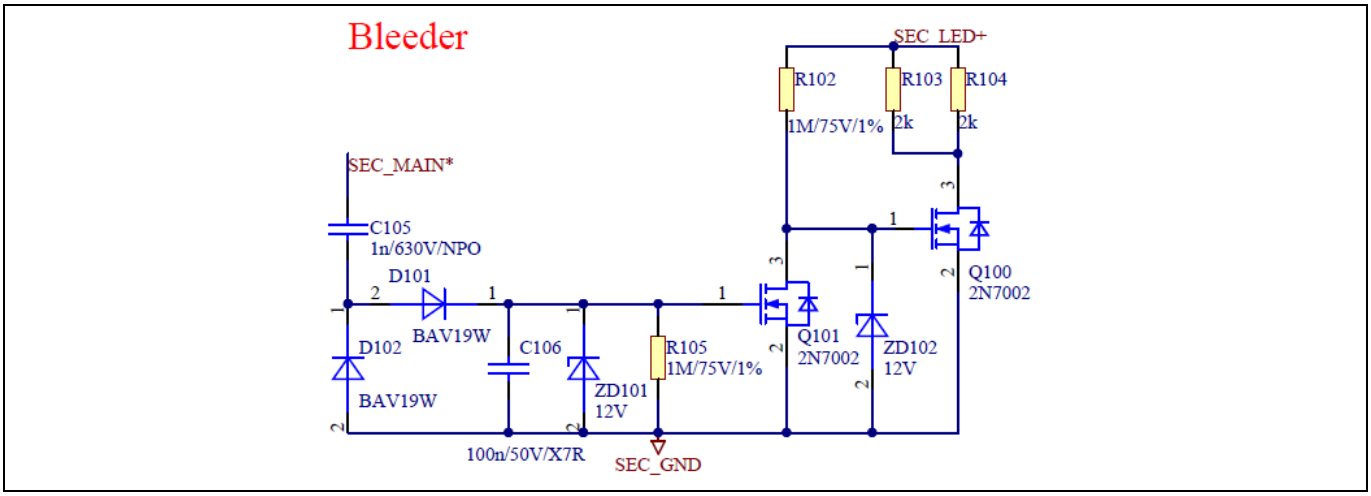


Figure 23 Active Bleeder Reference Design Schematic

2.8 Design the Adaptive Temperature Protection

XDPL8220 offers adaptive temperature protection using internal and/or external temperature sensors. This feature reduces the output current according to temperature to protect the load and driver against over-temperature.

Whenever the temperature T_{hot} is exceeded, the current is gradually reduced from the maximum current I_{out_full} to the minimum current I_{out_red} with the programmed current changing step I_{out_step} and time step T_{step}, as shown in Figure 24. If the temperature drops below T_{hot}, the output current is increased again. This allows the controller to ensure operation at or below a temperature of T_{hot}.

If a reduction down to a minimum current I_{out_red} is not able to compensate for any continued increase in temperature, over-temperature protection is then triggered if $T_{critical}$ is exceeded and XDPL8220 will enter auto-restart mode. After the temperature decreases to the safe level of T_{start}, the system will go back to the normal operation again.

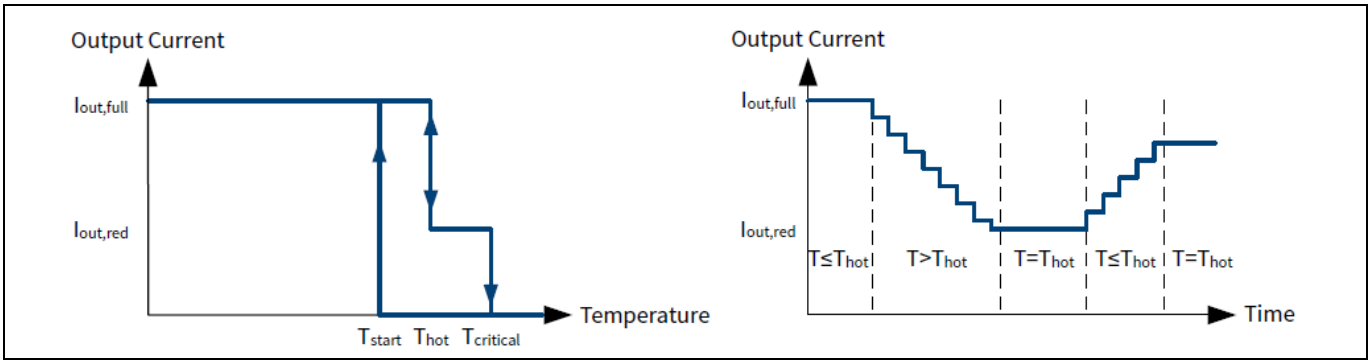


Figure 24 Adaptive Temperature Protection

Note: *Please note that the internal temperature sensor can only protect external components which have sufficient thermal coupling to XDPL8220. The external temperature sensor can be used to protect the temperature of external components (e.g. power MOSFETs or LED engine).*

If an external NTC resistor is connected at the temp pin, the temperature threshold will be converted correspondingly to the NTC resistor value.

The important parameters for designing the adaptive temperature protection for XDPL8220 are summarized in the following table:

Table 40 Power Supply for XDPL8220 Design Parameters

Parameter	Symbol	Value	Unit
Internal temperature threshold to trigger the internal over-temperature protection	$T_{critical}$	110	°C
Internal temperature threshold to activate the adaptive temperature protection	T_{hot}	100	°C
Temperature threshold for normal operation	T_{start}	90	°C
Time step to reduce the output current in the adaptive temperature protection	t_{step}	2	s
Minimum output current level in the in the adaptive temperature protection	I_{out_red}	200	mA
Current step to reduce the output current in the adaptive temperature protection	I_{out_step}	5	mA
External NTC resistor value threshold to trigger the external over-temperature protection	$R_{NTC\_critical}$	1657	Ω
External NTC resistor value threshold to activate the adaptive temperature protection	R_{NTC_hot}	2293	Ω
Reaction internal over-temperature protection	-	Auto-Restart	configurable
Reaction external over-temperature protection	-	Auto-Restart	configurable

2.9 Design the Dimming Interface

As the dimming signal input interface, the PWM pin is used to sense the duty cycle of the applied PWM signal to determine the output current level. The XDPL8220 can be configured to use either a linear or a quadratic dimming curve. Either normal or inverted dimming curves can be selected.

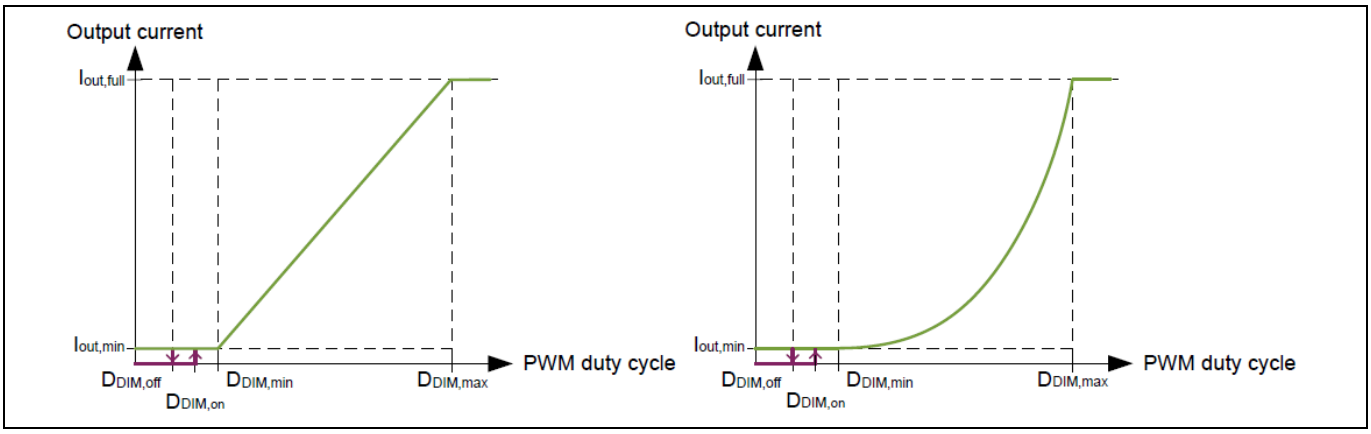


Figure 25 Configurable Dimming Curves

Figure 25 shows the relationship of the PWM duty cycle to the output current target value. Configurable levels D_{DIM_min} and D_{DIM_max} ensure that the minimum current I_{out_min} and maximum current I_{out_full} can always be achieved, thereby making the application robust against component tolerances.
Using the optional Dim-to-Off feature, the light output can be stopped without removal of input voltage. In Dim-to-off, the controller will enter auto-restart operation to minimize power consumption. The auto-restart recharges the output voltage to a minimum output voltage of V_{out_start} to measure the PWM duty cycle. With this feature, the output voltage can be maintained in a specific range by configuration of the startup voltage $V_{out,start}$ and auto-restart time t_{AR}, and by dimensioning of an active or passive output bleeder. If V_{out_start} is configured to be low enough than the minimum forward voltage of the LED string, the LEDs will show no light in this state.

Note: *Either an active or passive output bleeder is required to allow the controller to maintain the output voltage if the Dim-to-Off feature is enabled. Dim-to-Off is entered if the PWM duty cycle exceeds the configurable threshold $D_{DIM,off}$ (see purple line in Figure 25). As soon as the duty cycle exceeds D_{DIM_on}, the controller will start to continuously regulate output voltage or output current again.*

The important parameters for designing the dimming interface of XDPL8220 are summarized in the following table:

Table 41 Dimming Interface of XDPL8220 Design Parameters

Parameter	Symbol	Value	Unit
Dimming curve	-	Linear/Quadratic	-
Dimming curve direction	-	Normal/Inverted	-
Duty cycle threshold to enter Dim-to-off state	D_{DIM_off}	5	%
Duty cycle threshold to leave Dim-to-off state	D_{DIM_on}	7	%
Maximum duty cycle for the full output current	D_{DIM_max}	95	%
Minimum duty cycle for the minimum output current	D_{DIM_min}	10	%
Minimum output current	I_{out_min}	48	mA

2.10 PCB Layout Guidelines

Printed Circuit Board (PCB) layout and design are very important for switching power supplies where the voltage and current change with high ***dv/dt*** and ***di/dt***. Good PCB layout minimizes excessive EMI and prevents the power supply from being disrupted during surge / ESD tests. AS XDPL8220 combines the PFC boost and flyback in one controller, to prevent the interference of these two stages plays also a very critical role in the PCB layout. The following guidelines are recommended for layout designs:

2.10.1 Star connection of grounding

A good grounding of XDPL8220 is proven to minimize the risk of mutual interference among signals:

- The electrolytic PFC bulk cap ground is taken as the system ground reference at primary side. The other power ground of PFC stage, flyback main stage, MOSFET/Diode heatsink and EMI return ground should have separated connections to this system ground reference point in a star structure with preferably thick and short traces.
- The second ground reference is the ground of the XDPL8220 V_{CC} electrolytic capacitor which should be placed close to the IC. The flyback auxiliary winding ground is treated as power ground and should be connected to this second ground reference directly with a preferably thick and short trace.
- The V_{CC} electrolytic capacitor ground should be connected to the PFC bulk cap ground directly with a preferably thick and short trace.
- The ground of the XDPL8220 should be first connected to the V_{CC} ceramic capacitors ground and then to the V_{CC} electrolytic capacitor ground with a preferably short and thick PCB track.
- All ground connections of small signals like ***CS***, ***ZCD***, ***PWM*** and ***UART*** around the controller XDPL8220 should be connected to the V_{CC} ceramic capacitors ground with preferably short traces in a star structure.

2.10.2 Filtering capacitors of XDPL8220

Generally, filtering capacitors are used to suppress the high frequency noises which could cause interference or ground shifting when entering IC controller and will trigger some protections unwanted. These capacitors are usually made from ceramic and must be placed very close to the XDPL8220 and the ground of them must be connected to the IC ground as short as possible.

- V_{CC} filter capacitor: 100nF recommended
- PFC ***VS*** filter capacitor: 1nF recommended
- Flyback ***ZCD*** filter capacitor: 100pF recommended
- Flyback ***CS*** filter capacitor: 330pF recommended
- ***PWM*** filter capacitor: 100pF recommended
- An optional 100nF high-frequency-and-high-voltage bypass capacitor is recommended to be mounted in parallel with the PFC bulk capacitor, and close to the PFC MOSFET and PFC diode, to suppress EMI.

2.10.3 PFC Voltage Sense Circuit

The design and layout of the PFC voltage sense circuit play a critical role for the PFC boost stage operation, or over-voltage protection could be triggered unwanted by wrong layout. The trace of the sensing divider must be as short as possible and must be routed as far as possible from the PFC and flyback MOSFET. The filter capacitor of 1nF is mandatory and must be placed directly at the pin.

2.10.4 Minimum Current Loop

Minimized power and gate current loop areas reduce the radiated EMI noise and interference to the other signal traces.

- The PFC and flyback power current flowing loop area should be minimized as small as possible.
- The gate current of PFC and flyback stage should be minimized as small as possible and if allowed, the gate current should has its own ground trace back to the XDPL8220 ground instead of using the power ground traces.

2.10.5 Other Layout Considerations

- It is suggested that the track to ***HV*** pin shall be kept away from other small signal tracks. The distance is better to be more than 3mm.
- Keep distance of small signal tracks from MOSFET drain trace of at least 4mm.
- Any PCB track with high current should be designed as short and wide as possible to reduce the parasitic inductance like traces through the MOSFET Drain-Source and shunt resistors.
- The ground traces should be designed as wide as possible and better as area if possible. This helps also increase the immunity to noise.
- The PFC and flyback MOSFET drain tracks should be designed to areas and as large as possible if SMD packages are used. These areas are used as heat sink and spread the heat dissipated by the MOSFETs.
- An ESD protection diode is recommended to be designed for the UART pin as it may be touchable through the programming connector.

Revision History

Major changes since the last revision

Page or Reference	Description of change

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