Design guide for dual-stage PFC+LLC LED driver using ICL5102

Design guide
Revision 1.0

About this document

Scope and purpose

This document describes the procedure to design a dual-stage PFC+LLC offline LED driver using ICL5102 step by step based on the ICL5102 130 W Constant Current (CC) board.

Intended audience

This document is intended for anyone who needs to design an AC-DC offline LED driver with ICL5102 for dual-stage PFC+LLC control.

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Introduction

1 Introduction

The ICL5102 is a highly integrated multi-mode (Critical Conduction Mode – CrCM and Discontinuous Conduction Mode – DCM) Power Factor Correction (PFC) and resonant Half-Bridge (HB) combination controller. The integration of PFC and HB into a single controller enables reduction of external components and optimizes performance by harmonized operation of the two stages.

The two-stage approach divides the PFC responsibilities from the output current regulation functions. This ensures low variation in the output voltage and current and allows for low Total Harmonic Distortion (THD), high Power Factor (PF) and a greater ability to withstand AC-line perturbations. The multi-mode operation of the PFC converter provides excellent efficiency over the whole load range.

1.1 Product highlights

- PFC controller with CrCM and DCM
- Resonant HB controller with fixed or variable switching frequency control
- Maximum 500 KHz HB switching frequency and soft-start frequency up to 1.3 MHz
- BM of HB controller with power limitation ensures low standby power of less than 300 mW in dim-to-off condition
- THD optimization ensures low harmonic distortion (THD less than 10 percent) down to 30 percent nominal load

1.2 Design features

- Supports universal AC input voltage (90 to 305 V\textsubscript{rms}) nominal
- Excellent system efficiency up to 94 percent
- Applicable power range up to 350 W

1.3 Target applications

- Offline AC-DC LED drivers for commercial and industrial lighting up to 350 W
- High-density AC-DC power supply

Figure 1 shows a typical LED driver application using ICL5102 with PFC+LCC topology.
Introduction

Figure 1  ICL5102 typical application with PFC+LCC topology

1.4 Pin configuration and description

ICL5102 pin assignments and basic pin descriptions are shown in Figure 2 and Table 1.

![Pinning of ICL5102](image)

**Figure 2** Pinning of ICL5102

<table>
<thead>
<tr>
<th>Name</th>
<th>Pin</th>
<th>Type</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>LSGD</td>
<td>1</td>
<td>O</td>
<td>HB Low-Side (LS) gate driver</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Output for directly driving the HB LS MOSFET via a resistor</td>
</tr>
<tr>
<td>LSCS</td>
<td>2</td>
<td>I</td>
<td>HB Current Sense (CS)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Connected to an external shunt resistor and the source of the HB LS MOSFET</td>
</tr>
<tr>
<td>Vcc</td>
<td>3</td>
<td>I</td>
<td>Positive power supply</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>IC power supply</td>
</tr>
<tr>
<td>GND</td>
<td>4</td>
<td>-</td>
<td>Ground</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>IC ground</td>
</tr>
<tr>
<td>PFCGD</td>
<td>5</td>
<td>O</td>
<td>PFC gate driver</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Output for directly driving the PFC MOSFET via a resistor</td>
</tr>
<tr>
<td>PFCCS</td>
<td>6</td>
<td>I</td>
<td>PFC CS</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Connected to an external shunt resistor and the source of the PFC MOSFET</td>
</tr>
<tr>
<td>PFCZCD</td>
<td>7</td>
<td>I</td>
<td>PFC Zero-Crossing Detection (ZCD)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Connected to the PFC auxiliary winding via a resistor for PFC inductor current ZCD</td>
</tr>
<tr>
<td>PFCVS</td>
<td>8</td>
<td>I</td>
<td>PFC bus voltage sense</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Connected to a high-impedance resistor divider from the PFC controller output for bus voltage sensing</td>
</tr>
<tr>
<td>RF</td>
<td>9</td>
<td>I</td>
<td>HB minimum switching frequency setting</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Connected via an external resistor to GND for HB minimum switching frequency setting</td>
</tr>
<tr>
<td>BM</td>
<td>10</td>
<td>I</td>
<td>BM enter/exit setting</td>
</tr>
</tbody>
</table>
Introduction

<table>
<thead>
<tr>
<th>Name</th>
<th>Pin</th>
<th>Type</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>OTP</td>
<td>11</td>
<td>I</td>
<td>Over-Temperature Protection (OTP) Connected to an external Negative Temperature Coefficient (NTC) thermistor for external OTP</td>
</tr>
<tr>
<td>BO</td>
<td>12</td>
<td>I</td>
<td>Brown-in/out detection Connected to the rectified input voltage via an external resistor for input brown-in/out detection</td>
</tr>
<tr>
<td>OVP</td>
<td>13</td>
<td>I</td>
<td>Output Over-Voltage Protection (OVP) Connected to the HB auxiliary winding via a resistor divider and diode for OVP of the secondary output voltage</td>
</tr>
<tr>
<td>HSGND</td>
<td>14</td>
<td>-</td>
<td>High-Side (HS) ground Ground for floating HS driver of HB</td>
</tr>
<tr>
<td>HSVCC</td>
<td>15</td>
<td>I</td>
<td>HS Vcc power supply Power supply of the HS floating driver of HB, supplied via bootstrap circuit</td>
</tr>
<tr>
<td>HSGD</td>
<td>16</td>
<td>O</td>
<td>HS floating gate driver Output for directly driving the HB floating HS MOSFET via a resistor</td>
</tr>
</tbody>
</table>

The ICL5102 pin connection schematic is shown in Figure 3.

![ICL5102 pin connection schematic](image)

Figure 3  ICL5102 pin connection
Design specification

The design example used in this design guide is a 130 W CC mode reference design for direct driving of LED lighting applications based on the LLC topology. The customer can easily apply their own target specifications according to this example and obtain the design parameters by themselves.

2.1 System specification of a 130 W PFC+LLC reference design for LED lighting applications

The system specification of the ICL5102 130 W CC reference design for LED lighting applications is given in Table 2.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Target value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>General input/output specification</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Nominal input AC voltage</td>
<td>( V_{IN,\text{nom}} )</td>
<td>90 – 305</td>
<td>( V_{\text{RMS}} )</td>
</tr>
<tr>
<td>Line frequency</td>
<td>( f_{AC,\text{line}} )</td>
<td>47 – 63</td>
<td>Hz</td>
</tr>
<tr>
<td>Nominal output voltage</td>
<td>( V_{OUT} )</td>
<td>38 – 76</td>
<td>( V_{\text{DC}} )</td>
</tr>
<tr>
<td>Nominal output current</td>
<td>( I_{OUT,\text{nom}} )</td>
<td>1.75</td>
<td>A</td>
</tr>
<tr>
<td>Minimum output current</td>
<td>( I_{OUT,\text{min}} )</td>
<td>75</td>
<td>mA</td>
</tr>
<tr>
<td>Nominal output power</td>
<td>( P_{O,\text{nom}} )</td>
<td>130</td>
<td>W</td>
</tr>
<tr>
<td>Power factor</td>
<td>PF</td>
<td>More than 0.9</td>
<td></td>
</tr>
<tr>
<td>THD</td>
<td>( i\text{THD} )</td>
<td>Less than 10</td>
<td>%</td>
</tr>
<tr>
<td>Power efficiency</td>
<td>( \eta )</td>
<td>Less than 92</td>
<td>%</td>
</tr>
<tr>
<td>Maximum standby power at no load</td>
<td>( P_{O,\text{STB,max}} )</td>
<td>300</td>
<td>mW</td>
</tr>
<tr>
<td>Maximum time to light at 90 V AC</td>
<td>( t_{T2L} )</td>
<td>350</td>
<td>ms</td>
</tr>
<tr>
<td><strong>Protections</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Brown-out threshold</td>
<td>( V_{IN,\text{BO}} )</td>
<td>71</td>
<td>( V_{\text{RMS}} )</td>
</tr>
<tr>
<td>Brown-in threshold</td>
<td>( V_{IN,\text{BI}} )</td>
<td>90</td>
<td>( V_{\text{RMS}} )</td>
</tr>
<tr>
<td>Maximum output over-voltage threshold</td>
<td>( V_{OUT,\text{OVP}} )</td>
<td>90</td>
<td>( V_{\text{DC}} )</td>
</tr>
<tr>
<td>OTP threshold</td>
<td>( T_{OTP} )</td>
<td>85</td>
<td>°C</td>
</tr>
<tr>
<td><strong>Standard compliance</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Harmonics</td>
<td>–</td>
<td>EN61000-3-2 Class-C</td>
<td>–</td>
</tr>
<tr>
<td>EMI</td>
<td>–</td>
<td>EN55015</td>
<td>–</td>
</tr>
<tr>
<td>Safety</td>
<td>–</td>
<td>EN61347-2-13</td>
<td>–</td>
</tr>
<tr>
<td><strong>Board dimensions</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Size</td>
<td>( L \times H \times B )</td>
<td>178 x 52 x 32</td>
<td>mm</td>
</tr>
</tbody>
</table>
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Design specification

2.2 Schematic

The schematic of the ICL5102 130 W reference design for LED lighting applications is given in Figure 4.

Figure 4  ICL5102 130 W reference design schematic
PFC boost converter design

3 PFC boost converter design

PFC shapes the input current of the power supply to be in synchronization with the mains voltage, in order to maximize the real power drawn from the mains. In a perfect PFC circuit, the input current follows the input voltage as a pure resistor, without any input current harmonics. In the ICL5102 130 W reference design, PFC is implemented as a boost converter, which works in CrCM and DCM with constant on-time control to provide a constant high DC voltage for the HB control.

The design specification of the PFC boost converter is given in Table 3.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Minimum AC input voltage</td>
<td>( V_{IN_{\text{min}}} )</td>
<td>90</td>
<td>( V_{\text{RMS}} )</td>
</tr>
<tr>
<td>Minimum AC input peak voltage</td>
<td>( V_{IN_{\text{pk},\text{min}}} )</td>
<td>127</td>
<td>( V_{\text{RMS}} )</td>
</tr>
<tr>
<td>Maximum AC input voltage</td>
<td>( V_{IN_{\text{max}}} )</td>
<td>305</td>
<td>( V_{\text{RMS}} )</td>
</tr>
<tr>
<td>Maximum AC input peak voltage</td>
<td>( V_{IN_{\text{pk},\text{max}}} )</td>
<td>431</td>
<td>( V_{\text{RMS}} )</td>
</tr>
<tr>
<td>AC-line frequency</td>
<td>( f_{\text{AC_line}} )</td>
<td>47  ~  63</td>
<td>Hz</td>
</tr>
<tr>
<td>Maximum PFC output power</td>
<td>( P_{PFC_{\text{out,\text{max}}} )</td>
<td>145</td>
<td>W</td>
</tr>
<tr>
<td>Minimum PFC bus voltage</td>
<td>( V_{bus_{\text{min}}} )</td>
<td>400</td>
<td>V</td>
</tr>
<tr>
<td>Nominal PFC bus voltage</td>
<td>( V_{bus} )</td>
<td>450</td>
<td>V</td>
</tr>
<tr>
<td>PFC OVP level 1</td>
<td>( V_{bus_{\text{OVP1}}} )</td>
<td>71</td>
<td>( V_{\text{RMS}} )</td>
</tr>
<tr>
<td>Brown-out threshold</td>
<td>( V_{IN_{\text{BO}}} )</td>
<td>90</td>
<td>( V_{\text{RMS}} )</td>
</tr>
<tr>
<td>Brown-in threshold</td>
<td>( V_{IN_{\text{BI}}} )</td>
<td>90</td>
<td>( V_{\text{RMS}} )</td>
</tr>
<tr>
<td>Minimum PFC switching frequency</td>
<td>( f_{PFC_{\text{min}}} )</td>
<td>35</td>
<td>KHz</td>
</tr>
<tr>
<td>Estimated PFC efficiency</td>
<td>( \eta_{PFC} )</td>
<td>Less than or equal to 96</td>
<td>%</td>
</tr>
</tbody>
</table>

### 3.1 Main PFC boost inductor

As the key magnetic component of the PFC boost converter, the boost inductor has the main function of energy storage. Its inductance is given as the following formula:

\[
L_{PFC} = \frac{V_{IN_{\text{pk}}}^2 \times (V_{bus} - V_{IN_{\text{pk}}}) \times \eta_{PFC}}{4 \times V_{bus} \times P_{PFC_{\text{out}}} \times f_{PFC}}
\]

Where:
- \( L_{PFC} \) – inductance of the PFC boost inductor
- \( V_{IN_{\text{pk}}} \) – peak value of the input AC mains
- \( V_{bus} \) – bus voltage as the PFC output
- \( \eta_{PFC} \) – estimated power efficiency of the PFC boost converter
- \( P_{PFC_{\text{out}}} \) – output power of the PFC boost converter
- \( f_{PFC} \) – operation switching frequency of the PFC boost inductor

The maximum possible inductance should be calculated at both lowest (input brown-out threshold) and highest possible input voltage (input over-voltage threshold) with full load and minimum switching frequency.
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PFC boost converter design

At $V_{IN_{\text{min}}}=71\,\text{V}_{\text{RMS}}$:

$$L_{\text{PFC},71} = \frac{(71 \times \sqrt{2})^2 \times (450 - 71 \times \sqrt{2}) \times 0.96}{4 \times 450 \times 145 \times 35 \times 10^3} \approx 370.3\,\mu\text{H}$$

At $V_{IN_{\text{max}}}=305\,\text{V}_{\text{RMS}}$:

$$L_{\text{PFC},305} = \frac{(305 \times \sqrt{2})^2 \times (450 - 305 \times \sqrt{2}) \times 0.96}{4 \times 450 \times 145 \times 35 \times 10^3} \approx 366.1\,\mu\text{H}$$

The suitable inductance must be less than the smaller one of both.

$$L_{\text{PFC}} < \min(L_{\text{PFC},71}, L_{\text{PFC},305})$$

Other considerations regarding PFC choke inductance:

- The selected PFC inductance must be small enough to cover the maximum output power at the minimum input (e.g. to cover the brown-in/out feature).
- Bigger PFC inductance has the advantage at light load in comparison to smaller inductance due to longer on-time. This ensures smaller minimum output power in DCM when the LED load is small (e.g. 1 percent dimming) and avoids unwanted bus voltage ripples due to the limited minimum on-time of the IC controller.
- For the maximum output power, bigger PFC inductance has longer on-time and lower switching frequency. It must be guaranteed that these two parameters are still within the limit of ICL5102.
- Bigger PFC inductance leads to bigger choke size and more winding turns, which cause more winding loss. In contrast, smaller inductance has a smaller size and fewer winding turns but higher frequency, which could lead to more switching loss.

In the reference design, $L_{\text{PFC}} = 0.36\,\text{mH}$ is chosen to avoid magnetic saturation in all worst cases like start-up and load transient. After the PFC choke inductance is fixed, the choke relevant parameters can be calculated as follows with the assumption of the boundary conduction mode operation.

Maximum input current (RMS) happens at minimum AC input and maximum output power:

$$I_{\text{in}_{\text{rms,max}}} = \frac{P_{O_{\text{PFC,max}}}}{V_{IN_{BO}} \times t_{\text{PFC}}} = 2.12\,\text{A}$$

Maximum input peak current:

$$I_{\text{in}_{\text{pk,max}}} = \sqrt{2} \times I_{\text{in}_{\text{rms,max}}} = 3.0\,\text{A}$$

Maximum inductor peak current:

$$I_{L_{\text{pk,PFC,max}}} = 2 \times I_{\text{in}_{\text{pk,max}}} = 6.0\,\text{A}$$

![Figure 5](design-guide.png)

**Figure 5**  
Boost inductor current waveform in a switching cycle
PFC boost converter design

According to Figure 5, other important parameters of the PFC boost converter can be calculated as follows.

Maximum on-time:

\[ t_{on,max} = \frac{L_{PFC} \times I_{L,pk,PFC,max}}{\sqrt{2} \times V_{IN,BO}} = 21.5 \, \mu s \]

If \( T_{osc} = 1.5 \, \mu s \) is assumed, off-time at minimum AC input and maximum output power:

\[ t_{off} = \frac{L_{PFC} \times I_{L,pk,PFC,max}}{V_{bus} - \sqrt{2} \times V_{IN,BO}} + 0.5 \times T_{osc} = 6.92 \, \mu s \]

The lowest frequency for maximum output power of PFC converter in QRM:

\[ f_{PFC,min} = \frac{1}{t_{on,max} + t_{off}} = 35.2 \, kHz \]

Maximum current (RMS) through the PFC inductor during on-time:

\[ I_{L,PFC,\text{on},\text{rms},\text{max}} = I_{L,pk,PFC,max} \times \sqrt{\frac{1}{3} \times t_{on,max} \times f_{PFC,min}} = 3.0 \, A \]

Maximum current (RMS) through the PFC inductor during off-time:

\[ I_{L,PFC,\text{off},\text{rms},\text{max}} = I_{L,pk,PFC,max} \times \sqrt{\frac{1}{3} \times t_{off} \times f_{PFC,min}} = 1.71 \, A \]

Thus the maximum PFC inductor current (RMS):

\[ I_{L,\text{rms},\text{max}} = \sqrt{I_{L,PFC,\text{on},\text{rms},\text{max}}^2 + I_{L,PFC,\text{off},\text{rms},\text{max}}^2} = 3.45 \, A \]

To realize the ZCD of the inductor current for the CrCM switching, an additional auxiliary winding is introduced in the PFC inductor. The turns ratio of the main and auxiliary winding decides the amplitude of the oscillation at the PFCZCD pin. So that the comparator for the ZCD works correctly, the oscillation amplitude at the PFCZCD pin for ZCD must exceed \( V_{PFCZCDTHRH_{\text{max}}} = 1.6 \, V \). The turns ratio is calculated as:

\[ \frac{N_{p,PFC}}{N_{a,PFC}} < \frac{V_{bus} - V_{in, pk, max}}{1.6V} = 11.68 \]

The important parameters of the PFC boost inductor are summarized in Table 4.

**Table 4** PFC boost inductor design parameters

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Main inductance of the PFC boost inductor</td>
<td>( L_{PFC} )</td>
<td>360 ( \mu H )</td>
<td></td>
</tr>
<tr>
<td>Minimum switching frequency in QRM</td>
<td>( f_{PFC,min} )</td>
<td>35.2 ( kHz )</td>
<td></td>
</tr>
<tr>
<td>Maximum inductor peak current</td>
<td>( I_{L,pk,PFC,max} )</td>
<td>6 ( A )</td>
<td></td>
</tr>
<tr>
<td>Maximum input current (RMS)</td>
<td>( I_{in,rms,max} )</td>
<td>2.12 ( A )</td>
<td></td>
</tr>
<tr>
<td>Maximum input peak current</td>
<td>( I_{in, pk, max} )</td>
<td>3 ( A )</td>
<td></td>
</tr>
<tr>
<td>Maximum inductor current (RMS)</td>
<td>( I_{L,\text{rms},\text{max}} )</td>
<td>3.45 ( A )</td>
<td></td>
</tr>
<tr>
<td>Maximum on-time</td>
<td>( t_{on,max} )</td>
<td>21.5 ( \mu s )</td>
<td></td>
</tr>
<tr>
<td>Turns ratio of primary to auxiliary winding</td>
<td>( \frac{N_{p,PFC}}{N_{a,PFC}} )</td>
<td>9:1</td>
<td></td>
</tr>
</tbody>
</table>

Based on the calculated specifications above, the inductor can be constructed according to different design requirements such as size, power efficiency and temperature by selecting different bobbin and core materials. In order to avoid core saturation and achieve an optimized core loss, the flux density \( B_{\text{max}} \) is recommended not to exceed 0.3.
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**PFC boost converter design**

In the ICL5102 130 W CC reference design, the PFC boost inductor is constructed by Würth Electronik under part no. 750343180 as a design example. The specification sheet is given as shown in Figure 6 and Table 5.

![Würth PFC inductor 750343180](image)

**Figure 6**  
Würth PFC inductor 750343180

**Table 5  Parameters of Würth PFC inductor 750343180**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Inductance</td>
<td>360</td>
<td>µH</td>
</tr>
<tr>
<td>Bobbin</td>
<td>PQ2620</td>
<td>–</td>
</tr>
<tr>
<td>Core material</td>
<td>TP4A or DMR44</td>
<td>–</td>
</tr>
<tr>
<td>Turns ratio of primary to auxiliary winding</td>
<td>9.18</td>
<td>–</td>
</tr>
<tr>
<td>DC resistance primary winding</td>
<td>0.18</td>
<td>Ω</td>
</tr>
<tr>
<td>DC resistance auxiliary winding</td>
<td>0.25</td>
<td>Ω</td>
</tr>
<tr>
<td>Saturation current</td>
<td>7.2</td>
<td>A</td>
</tr>
</tbody>
</table>

**3.2 Input bridge rectifier**

The bridge rectifier usually has the highest semiconductor power loss in the LED driver. The following considerations must be taken into account for a proper selection.

- Maximum recurrent peak reverse voltage/DC blocking voltage:

Must be chosen to be higher than the peak of the maximum input voltage with at least 20 percent margin:

\[
V_{BR, RRM} > 1.2 \times V_{IN, pk, max} = 518 \text{ V}
\]

- Maximum rectified average forward current:

The maximum rectified average forward current is calculated as:

\[
I_{BR, avg, max} = \frac{2\sqrt{2}}{\pi} \times \frac{P_{O, PFC, max}}{V_{INBO} \times \eta_{PFC}} = 1.91 \text{ A}
\]
PFC boost converter design

Using a bridge rectifier with a higher rated current can reduce the forward voltage drop, which reduces the total power dissipation at a small incremental cost.

- Peak surge forward current

The peak surge forward current must be chosen to cover the maximum surge current requirement.

- Forward voltage

This is directly related to the power efficiency; the forward voltage should be chosen to be as small as possible.

- Maximum power loss

The total maximum power loss is calculated using the maximum average input current flowing through two of the bridge rectifying diodes if the forward voltage is assumed as 1 V:

\[
P_{BR\_loss\_max} = I_{BR\_avg\_max} \times 2 \times V_{BR\_F} = 3.83 \text{ W}
\]

- Maximum diode temperature rise without heatsink

Assuming the thermal resistance of the bridge rectifier is \( R_{TH\_JA} = 21^\circ \text{C/W} \) (e.g. according to GBU80M), the maximum temperature rise of the diode without heatsink can be calculated as:

\[
\Delta T_{BR\_max} = R_{TH\_JA} \times P_{BR\_loss\_max} = 80.43 ^\circ \text{C}
\]

The important parameters for the bridge rectifier used in the 130 W reference design are summarized in Table 6.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Maximum reverse voltage</td>
<td>( V_{BR_RMM} )</td>
<td>1000</td>
<td>V</td>
</tr>
<tr>
<td>Average rectified forward current</td>
<td>( I_{BR_avg} )</td>
<td>8</td>
<td>A</td>
</tr>
<tr>
<td>Forward voltage</td>
<td>( V_{BR_F} )</td>
<td>1</td>
<td>V</td>
</tr>
</tbody>
</table>

### 3.3 PFC boost diode

The selection of the boost diode is a major decision in the PFC boost converter design, and it is related to the converter efficiency. The following considerations should be taken into account:

- Reverse breakdown voltage

It must be chosen to be higher than the bus voltage with at least 20 percent margin:

\[
V_{RRM\_D\_PFC} > 1.2 \times V_{bus\_OV\_P1} = 594 \text{ V}
\]

A 600 V diode is suitable here in the 130 W reference design.

- Average rectified forward current

It must be higher than the maximum average PFC diode current, calculated as follows:

\[
I_{D\_PFC\_avg\_max} = \frac{\sqrt{3}}{2} \times I_{L\_PFC\_off\_rms\_max} = 1.05 \text{ A}
\]

Using a diode with high current capability will benefit the power efficiency.
PFC boost converter design

- Forward voltage

This is directly related to the power efficiency. So the forward voltage should be chosen to be as small as possible.

- Reverse recovery time

As the PFC boost converter is controlled by ICL5102 in the QRM+DCM mode, the PFC boost diode current goes back to zero while the PFC MOSFET turns on. So there is no current commutation between the PFC diode and MOSFET and thus no switching loss by reverse recovery. It is not necessary to choose an ultra-fast diode.

- Power loss

The only power loss that should be considered is conduction loss. With a forward voltage of 0.5 V assumed, the diode conduction loss can be calculated as follows:

\[ P_{\text{loss, D_PFC}} = I_{D,\text{PFC,avg, max}} \times V_{F,\text{D_PFC}} = 0.525 \text{ W} \]

- Thermal characteristics

With the thermal resistance of the diode \( R_{\text{D_PFC,TH,JA}} \) and ambient temperature \( T_A \), the PFC diode temperature without heatsink is calculated as:

\[ T_{D,\text{PFC}} = P_{\text{loss, D_PFC}} \times R_{D,\text{PFC,TH,JA}} + T_A \]

The important parameters for the boost diode used in the 130 W reference design are summarized in Table 7.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Maximum reverse voltage</td>
<td>( V_{\text{RRM, D_PFC}} )</td>
<td>600</td>
<td>V</td>
</tr>
<tr>
<td>Average rectified forward current</td>
<td>( I_{F,\text{D_PFC}} )</td>
<td>4</td>
<td>A</td>
</tr>
<tr>
<td>Forward voltage</td>
<td>( V_{F,\text{D_PFC}} )</td>
<td>0.5</td>
<td>V</td>
</tr>
</tbody>
</table>

### 3.3.1 PFC power MOSFET

The selection of the PFC power MOSFET is based mainly on the consideration of the drain-source breakdown voltage and the power dissipation.

- Drain-source breakdown voltage

According to the operating bus voltage, the breakdown voltage should be chosen as:

\[ V_{(BR)DSS} > 1.2 \times V_{\text{bus, OVP}} = 594 \text{ V} \]

A 600 V MOSFET would be suitable; for applications with enhanced surge protection, higher breakdown voltage should be selected.

- Continuous drain current

The maximum continuous drain current is calculated as:

\[ I_{D,\text{MOS, PFC, max}} = 3 \times I_{L,\text{PFC, on, rms, max}} = 6.33 \text{ A} \]

- Conduction loss
Design guide for dual-stage PFC+LLC LED driver using ICL5102

PFC boost converter design

These losses are frequency independent and do not scale significantly with frequency. This is calculated as follows:

\[ P_{\text{con,loss,MOS,PFC}} = \left( \frac{I_{\text{L,PFC, on, rms, max}}}{2} \right)^2 \cdot R_{\text{DS(ON)}} \]

- Turn-on transition loss

As the converter works in QRM+DCM mode, the turn-on transition loss caused by the magnetizing current can be ignored because the current rises from zero when a switching cycle starts. But to discharge the parasitic capacitors like \( C_{\text{oss}} \) (MOSFET output capacitance) and \( C_{\text{DS,total}} \) (total parasitic drain-source equivalent capacitance) through the MOSFET channel can cause significant turn-on transition loss. These losses occur every switching cycle and are thus frequency dependent.

- \( E_{\text{oss}} \) and \( \frac{1}{2} \cdot C_{\text{DS,total}} \cdot V^2 \) loss

The energy stored in \( C_{\text{DS,total}} \) and \( C_{\text{oss}} \) at the time of turn-on must be dissipated in the MOSFET channel and CS resistor during the turn-on transition. These losses are fundamentally a function of the square of the voltage across it, and can be very significant during high-line conditions. They occur every switching cycle and are thus frequency dependent. To simplify the calculation, we assumed that the switching loss is approximately half of the conduction loss:

\[ P_{\text{sw,loss,MOS,PFC}} = \frac{1}{2} \cdot P_{\text{con,loss,MOS,PFC}} \]

- Gate driver loss

These losses also scale linearly with frequency, but are generally quite a small contribution to the overall losses (at switching frequencies of below 100 kHz) and depend almost exclusively on the MOSFET \( Q_g \) (total gate charge). The gate driver power is typically dissipated in the external gate resistor and the gate driver itself and thus does not need to be considered in the thermal calculation of the MOSFET.

In the 130 W reference design, two 600 V Infineon MOSFETs IPD60R400CE of CE family are used in parallel to minimize the power dissipation. With the \( R_{\text{DS(ON)}} \) of 200 m\( \Omega \), the maximum total loss of each MOSFET is calculated as below:

\[ P_{\text{loss,MOS,PFC,max}} = 0.5 \cdot (P_{\text{sw,loss,MOS,PFC}} + P_{\text{con,loss,MOS,PFC}}) = 0.75 \cdot P_{\text{con,loss,MOS,PFC}} = 0.96 \text{ W} \]

The maximum temperature rise of each MOSFET without heatsink is:

\[ \Delta T_{\text{MOS,PFC,max}} = R_{\text{TH,JA}} \cdot P_{\text{loss,MOS,PFC,max}} = 76.8 \text{ °C} \]

The important parameters for PFC MOSFETs are summarized in Table 8.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Breakdown voltage</td>
<td>( V_{\text{BR,DSS,PFC}} )</td>
<td>650</td>
<td>V</td>
</tr>
<tr>
<td>MOSFET on-resistance</td>
<td>( R_{\text{DS(ON)}} )</td>
<td>400/400 = 200</td>
<td>m( \Omega )</td>
</tr>
<tr>
<td>Maximum PFC MOSFET conduction loss</td>
<td>( P_{\text{loss,MOS,PFC,con}} )</td>
<td>1.93</td>
<td>W</td>
</tr>
</tbody>
</table>
3.3.2 PFC CS

To design the PFC CS shunt resistor, the following condition must be complied with:

\[ I_{L,pk_{PFC\_max}} \cdot R_{CSPFC} < V_{OCP1\_PFC\_min} = 0.95 \, V \]

and:

\[ R_{CSPFC} < \frac{0.95 \, V}{I_{L,pk_{PFC\_max}}} = 0.22 \, \Omega \]

The value of the CS resistor is chosen to be 0.2 \( \Omega \) with five resistors of 1 \( \Omega \) connected in parallel. This splits the power dissipation and reduces the thermal stress. The maximum power loss of each shunt resistor is:

\[ P_{loss\_shunt_{PFC\_max}} = 0.2 \cdot I_{PFC\_on\_rms\_max}^2 \cdot R_{CSPFC} = 0.2 \cdot 2.11A^2 \cdot 0.2 = 0.18 \, W \]

This should be considered while selecting the proper shunt resistor type.

The important design parameters for bus voltage sensing are summarized in Table 9.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>PFC OCP1 maximum operating range</td>
<td>( V_{OCP1_PFC_min} )</td>
<td>0.95</td>
<td>V</td>
</tr>
<tr>
<td>PFC CS resistor</td>
<td>( R_{CSPFC} )</td>
<td>0.2</td>
<td>( \Omega )</td>
</tr>
</tbody>
</table>

3.3.3 PFC bus voltage sense

As shown in Figure 7, the bus voltage is measured at the PFCVS pin of ICL5102 through a resistor divider. This measurement is used as the input of the PFC output voltage regulator to generate the PWM control signal for the PFC MOSFET and offers protection functions for the PFC boost converter. It is strongly recommended to add a filter capacitor near the VS pin to filter the switching noise in order to get a precise and stable measurement result. The VS pin has a very low leakage current so the intolerance can be ignored.

The calculation of the resistor divider is given as follows when the \( V_{bus} = 450 \, V \) is mapped to \( V_{PFCVSCREF} = 2.5 \, V \).

\[ \frac{R_{VS1\_PFC}}{R_{VS2\_PFC}} = \frac{V_{bus} - V_{PFCVSCREF}}{V_{PFCVSCREF}} = 179 \]

To reduce the inaccuracy caused by the resistor divider, it is necessary to select the bus voltage sensing resistors with a tolerance of 1 percent or less. In the 130 W reference design, to reduce the voltage stress, the
PFC boost converter design

upper resistor $R_{V51,PFC}$ consists of three resistors each of 1.5 MΩ, and the lower resistor $R_{V51,PFC}$ is selected as 24.9 kΩ.

Note: In order to reduce the switching noise coupled in the bus voltage sense signal, a filter capacitor of 1 nF is strongly recommended to be placed directly near the PFCVS pin.

The important design parameters for bus voltage sensing are summarized in Table 10.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Nominal PFC boost converter output voltage</td>
<td>$V_{bus}$</td>
<td>450</td>
<td>V</td>
</tr>
<tr>
<td>ICL5102 PFCVS pin reference voltage</td>
<td>$V_{REF}$</td>
<td>2.5</td>
<td>V</td>
</tr>
<tr>
<td>Bus voltage sensing divider upper resistor</td>
<td>$R_{V51,PFC}$</td>
<td>1.5 x 3</td>
<td>MΩ</td>
</tr>
<tr>
<td>Bus voltage sensing divider lower resistor</td>
<td>$R_{V52,PFC}$</td>
<td>24.9</td>
<td>kΩ</td>
</tr>
<tr>
<td>Bus voltage sensing filter capacitor</td>
<td>$C_{VS}$</td>
<td>1</td>
<td>nF</td>
</tr>
</tbody>
</table>

3.3.4 PFC output capacitor

The PFC bus capacitor can be calculated with the following formula if the ESR of the capacitor is small enough to be neglected and the peak-to-peak voltage ripple is selected as 20 V. Please note that the tolerance of 20 percent of the capacitance needs to be taken into account as well.

$$C_{bus} = \frac{I_{out,PFC,\text{max}}}{2 \cdot \pi \cdot f_{\text{line, min}} \cdot V_{bus,\text{ripple, pp}}} \cdot 1.2 = 46 \, \mu F$$

With:

$$I_{out,PFC,\text{max}} = \frac{P_{O,PFC,\text{max}}}{V_{bus}} = 0.24 A$$

Regarding the voltage rating with consideration for the OVP threshold, a 500 V capacitor is necessary. The ESR of the capacitor should be selected to be as small as possible, and the allowed maximum ripple current should have enough margin. In the 130 W reference design, one 500 V capacitor of 56 µF with low ESR is selected.

The important parameters for the bus capacitor selection are summarized in the following table.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Nominal PFC boost converter output voltage</td>
<td>$V_{bus}$</td>
<td>450</td>
<td>V</td>
</tr>
<tr>
<td>Maximum PFC boost converter output power</td>
<td>$P_{out,PFC,\text{max}}$</td>
<td>130</td>
<td>W</td>
</tr>
<tr>
<td>Bus voltage ripple (peak to peak)</td>
<td>$V_{bus,\text{ripple, pp}}$</td>
<td>20</td>
<td>V</td>
</tr>
<tr>
<td>AC input line frequency</td>
<td>$f_{\text{line}}$</td>
<td>45 ~ 66</td>
<td>Hz</td>
</tr>
<tr>
<td>PFC bus capacitor</td>
<td>$C_{bus}$</td>
<td>56</td>
<td>µF</td>
</tr>
</tbody>
</table>

3.3.5 Input voltage sensing and brown-in/out

The rectified input voltage is sensed through an external resistor divider which consists of $R_{BO1}$ and $R_{BO2}$ at the BO pin as shown in Figure 8. This input voltage sensing function enables the AC input brown-in/out to provide the under-voltage protection for the LED driver.
PFC boost converter design

It is strongly recommended to add a high-voltage capacitor $C_{BO1}$ directly after the rectification diodes $D_{BO1}$ and $D_{BO1}$ so that the peak value of AC input is measured, which is not dependent on the load condition. Without the capacitor $C_{BO1}$, the equalized AC input mean value is sensed at the BO pin, which shifts according to the load. Thus the brown-in/out threshold is different under different load conditions.

![Figure 8 Input voltage sensing](image)

At the initial start-up (AC plug-in), the voltage at the BO pin must typically exceed $V_{BO} = 1.4$ V to enable brown-in. During normal operation, brown-out is detected when the voltage at the BO pin drops below typically $V_{BO} = 1.2$ V for longer than 50 ms. ICL5102 will stop both PFC and HB switching and enter auto-restart. Normal system operation recovers if the voltage at the BO pin is above 1.4 V again.

The ratio of the divider is calculated as follows:

$$\frac{R_{BO1}}{R_{BO2}} = \frac{1.414 \cdot V_{IN,BO} - V_{D,BO} - V_{BO,\text{out}_{\text{min}}}}{V_{BO,\text{out}_{\text{min}}}} = 86$$

With $V_{BO,\text{out}_{\text{min}}} = 1.14$ V from ICL5102 datasheet Table 16, brown-in threshold $V_{IN,\text{BI}} = 71$ V and $V_{D,BO} = 0.7$ V.

In the ICL5102 130 W CC reference design, $R_{BO1} = 6600$ k$\Omega$ is selected. To reduce the voltage and power stress of the resistor, it is strongly recommended to split it into three 1206 resistors of 2200 k$\Omega$ each. To improve the accuracy of the measurement, resistors with tolerance of less than 1 percent should be selected. According to the divider ratio calculated previously, $R_{BO2} = 76.8$ k$\Omega$ is selected.

The brown-in voltage can be calculated after $R_{BO1}$ and $R_{BO2}$ are fixed:

$$V_{IN,\text{BI}} = \frac{86 \cdot V_{BO,\text{in}_{\text{max}}} + V_{D,BO} + V_{BO,\text{in}_{\text{max}}}}{1.414} = 90$$ V

The important design parameters for input voltage sensing are summarized in Table 12.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Brown-out threshold</td>
<td>$V_{IN,BO}$</td>
<td>71</td>
<td>$V_{\text{RMS}}$</td>
</tr>
<tr>
<td>Brown-in threshold</td>
<td>$V_{IN,\text{BI}}$</td>
<td>90</td>
<td>$V_{\text{RMS}}$</td>
</tr>
</tbody>
</table>
**PFC boost converter design**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>BO pin divider upper resistor</td>
<td>$R_{BO1}$</td>
<td>6600</td>
<td>kΩ</td>
</tr>
<tr>
<td>BO pin divider lower resistor</td>
<td>$R_{BO2}$</td>
<td>76.8</td>
<td>kΩ</td>
</tr>
</tbody>
</table>

### 3.3.6 THD optimization

The input AC current becomes most distorted in the area when zero-crossing of AC input voltage occurs. In order to ensure the sinusoidal current waveform in this area, the ICL5102 extends the PFC on-time dynamically up to twice PFC maximum on-time according to the instantaneous value of the input voltage amplitude. The detection of AC input voltage zero-crossing is realized through the PFC auxiliary winding. When the voltage across the PFC auxiliary winding after the PFC MOSFET turns on reaches the minimum value, AC zero-crossing is detected. The concept of THD correction is shown in Figure 9.

![PFC THD correction](image)

To adjust the on-time enlargement, an external resistor between the PFC choke auxiliary winding and PFCZCD pin is required, as shown in Figure 10. When the PFC MOSFET turns on, the input voltage is measured according to the current flowing out of the PFCZCD pin. A smaller current means AC input is in the area A (see Figure 9), which requires an enlargement of the PFC on-time. Generally, the smaller the current flowing out of the PFCZCD pin is, the bigger the PFC on-time enlargement. The value of the resistor should be selected so that the current is limited between $I_{ZCD} = 500 \mu A \sim 1.2 \ mA$. 
Design guide for dual-stage PFC+LLC LED driver using ICL5102

PFC boost converter design

![Diagram of PFC boost converter design]

**Figure 10** PFC THD optimization via an external resistor

The following formula shows the calculation of the connected ZCD resistor value with the assumption that $I_{ZCD,\text{max}} = 1.2$ mA flows out of the PFCZCD pin at maximum AC-line input:

$$R_{ZCD} = 1.414 \times \frac{V_{IN,\text{max}}}{N_{P,\text{PFC}} / N_{A,\text{PFC}} \times I_{ZCD,\text{max}}} = 39.9 \text{ k}\Omega$$

The THD performance can be optimized by varying the resistor value around 40 kΩ.

**Note:** There is a trade-off between improvement in PF and reduction of THD. However, trying to achieve harmonic-free current may bring harmonics into the voltage and thus a lower PF. On the other hand, any attempt at PF unity by the usual methods will result in a non-sinusoidal current, which increases THD.
4 HB LLC resonant converter design

A resonant HB converter has many advantages, such as high efficiency, high power density and low EMI. ICL5102 provides independent control of the resonant HB converter (e.g. LLC or LCC topology) for Constant Voltage (CV) or CC output. It supports both fixed and variable switching frequency control.

The following sections provide the HB converter design guidelines using ICL5102 based on LLC topology with a secondary-side regulated CC control.

The design specification for the 130 W LLC CC reference design is given in the following table.

Table 13 LLC converter design specification

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Minimum DC input voltage</td>
<td>( V_{\text{bus_min}} )</td>
<td>400</td>
<td>V</td>
</tr>
<tr>
<td>Nominal DC input voltage</td>
<td>( V_{\text{bus}} )</td>
<td>450</td>
<td>V</td>
</tr>
<tr>
<td>Maximum DC input voltage</td>
<td>( V_{\text{bus_max}} )</td>
<td>490</td>
<td>V</td>
</tr>
<tr>
<td>Maximum LLC converter output power</td>
<td>( P_{O_{\text{max}}} )</td>
<td>130</td>
<td>W</td>
</tr>
<tr>
<td>Estimated LLC converter power efficiency</td>
<td>( \eta_{\text{FB}} )</td>
<td>Less than 96</td>
<td>%</td>
</tr>
<tr>
<td>LLC converter maximum output voltage</td>
<td>( V_{\text{out_max}} )</td>
<td>76</td>
<td>V</td>
</tr>
<tr>
<td>LLC converter maximum output voltage</td>
<td>( V_{\text{out_min}} )</td>
<td>38</td>
<td>V</td>
</tr>
<tr>
<td>LLC converter maximum output current</td>
<td>( I_{\text{out_max}} )</td>
<td>1750</td>
<td>mA</td>
</tr>
<tr>
<td>LLC converter output current</td>
<td>( I_{\text{out_min}} )</td>
<td>75</td>
<td>mA</td>
</tr>
<tr>
<td>LLC converter resonant frequency</td>
<td>( f_r )</td>
<td>100</td>
<td>kHz</td>
</tr>
<tr>
<td>Primary-side switching bridge topology</td>
<td>–</td>
<td>HB</td>
<td>–</td>
</tr>
<tr>
<td>Secondary-side rectifier topology</td>
<td>–</td>
<td>Full-Bridge (FB) rectifier</td>
<td>–</td>
</tr>
</tbody>
</table>

On the primary side, the HB is used as a switching bridge because ICL5102 is a HB controller. On the secondary side, a FB rectifier is preferred due to the high voltage and low current output characteristics. The design target is to achieve Zero Voltage Switching (ZVS) on the primary side and Zero Current Switching (ZCS) on the secondary side for the entire load range for optimized power efficiency and low-EMI performance.

4.1 LLC resonant tank design

Due to the non-linear nature of the resonant LLC topology, the following calculations of resonant tank are based on the First Harmonic Approximation (FHA). Furthermore, to simplify the design of the LLC transformer, an external resonant inductor is used.

4.1.1 Transformer turns ratio

According to the characteristics of the HB LLC converter with FB rectifier, the converter gain can be calculated as:

\[
\text{LLC Converter Gain} = \frac{V_{\text{out}} + 2 \times V_{F_D}}{V_{\text{bus}}} = 0.5 \times \text{Resonant Tank Gain} \times \text{Transformer Turns Ratio} \ (N_s/N_p)
\]

When the LLC converter operates at a frequency equal to the resonant frequency, the resonant tank gain is 1 when using an individual core for the series inductor. So the transformer turns ratio can be expressed as:

\[
n = \frac{N_p}{N_s} = \frac{V_{\text{bus}}}{2 \times (V_{\text{out}} + 2 \times V_{F_D})}
\]
Design guide for dual-stage PFC+LLC LED driver using ICL5102

HB LLC resonant converter design
It is recommended to operate the LLC tank below resonant frequency (boost mode operation) for CC output. To ensure this for the widest load range, the minimum output voltage with maximum bus voltage as a working point is selected as LLC resonant operation to decide the transformer turns ratio:

\[ n = \frac{N_p}{N_s} = \frac{V_{bus,max}}{2 \times (V_{out,min} + 2 \times V_{F,D})} = 6.22 \]

4.1.2 LLC resonant tank gain
After the transformer turns ratio is defined, the resonant tank voltage gain \( M_{LLC} \) can be summarized as:
- Unit gain \( M_{LLC} = 1 \) for maximum bus voltage and lowest output voltage
- Minimum gain \( M_{LLC.min} = M_{LLC} = 1 \)
- Maximum gain \( M_{LLC.max} \) for minimum bus voltage and highest output voltage

\[ M_{LLC.max} = \frac{n \times 2 \times (V_{out,max} + 2 \times V_{F,D})}{V_{bus,min}} = 2.4 \]

4.1.3 Selecting the \( m \) value
The ratio of total primary inductance to resonant inductance is defined as the \( m \) value as follows:

\[ m = \frac{L_p + L_m}{L_r} \]

Lower values of \( m \) can achieve higher boost gain and provide more flexible control and regulation, which is valuable in applications with wide input voltage range. Nevertheless, low values of \( m \) mean smaller magnetizing inductance \( L_m \), and therefore higher magnetizing peak-to-peak current ripple, causing increased circulating energy and conduction losses.

For the 130 W LLC CC reference design, a reasonable initial value of \( m = 8 \) is first selected. Later, by few iterations, the \( m \) value can still be optimized as long as the maximum gain requirement for all load conditions can still be achieved.

4.1.4 Selecting the maximum quality factor value \( Q_{max} \)
Quality factor is dependent on the load and defined as:

\[ Q = \sqrt{\frac{L_p}{L_r}} \frac{1}{R_{ac}} \]

Heavy load conditions operate at high \( Q \) values while lighter loads have lower \( Q \) values. It is important to set a value for the \( Q_{max} \) associated with the maximum load point.

By using the ICL5102 LLC calculation tool, the analysis can be simplified. The peak gains are obtained and depicted in Figure 11, which shows how the peak gain (attainable maximum gain) varies with \( Q \) for different \( m \) values. It appears that higher peak gain can be obtained by reducing \( m \) or \( Q \) values. With a given resonant frequency and \( Q \) value, decreasing \( m \) means reducing the magnetizing inductance, which results in increased circulating current. There is a trade-off between the available gain range and conduction loss.

With the maximum gain \( M_{LLC,max} \) and defined \( m \) value, the maximum quality factor is achieved through the curve:

\[ Q_{max} = 0.17 \]
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HB LLC resonant converter design

4.1.5 Equivalent reflected resistance $R_{ac}$

FHA eliminates non-linearity and generates an equivalent resonant circuit, as shown in Figure 12. The input square wave voltage is replaced with first harmonic of the voltage square wave, while the secondary section with rectifier and load is replaced by equivalent load $R_{ac}$, which is calculated at full load as:

$$R_{ac} = \frac{8}{\pi^2} * n^2 * \frac{(V_{out,max} + 2 * V_{FD})}{I_{out,max}} = 1388 \Omega$$

4.1.6 LLC resonant tank calculation

After the values of $m$, $Q_{max}$ and $R_{ac}$ are obtained, the value of the resonant capacitor can be calculated as:
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\[ C_r = \frac{1}{2 \pi Q_{max} f_r R_{ac}} = 6.74 \text{nF} \]

To reduce the size of the resonant choke, a bigger resonant capacitor is selected for the 130 W reference design as:

\[ C_r = 11.5 \text{nF} \]

In order to reduce the start-up inrush current and the ripple current in normal operation through the resonant capacitor, one resonant capacitor can be split into two capacitors with standard values (one to the DC bus, the other to the ground). This helps to obtain the available capacitor values, too.

\[ C_{r1} = 6.8 \text{nF} \]
\[ C_{r2} = 4.7 \text{nF} \]

The inductance of the resonant choke is calculated as:

\[ L_r = \frac{1}{4 \pi^2 C_r f_r^2} = 220 \mu\text{H} \]

The main inductance of the LLC transformer \( L_p \) is calculated as:

\[ L_p = m L_r = 1760 \mu\text{H} \]

The magnetizing inductance \( L_m \) is calculated as:

\[ L_m = L_p - L_r = 1540 \mu\text{H} \]

The equivalent leakage inductance due to HB can be approximately estimated as:

\[ L_{leak} = 0.5 \times 8\% \times L_m = 60 \mu\text{H} \]

So the inductance of the separated resonant choke is calculated as:

\[ L_{r,ext} = L_r - L_{leak} = 160 \mu\text{H} \]

4.1.7 Verification of the LLC resonant tank parameters

After all resonant tank parameters are decided, the working points of all corner cases must recalculated to ensure that the LLC resonant design target is still fulfilled.

Resonant frequency:

\[ f_r = \frac{1}{2 \pi \sqrt{L_r C_r}} = 100.1 \text{kHz} \]
\[ f_p = \frac{1}{2 \pi \sqrt{L_p C_r}} = 35.3 \text{kHz} \]

Quality factor:

\[ Q = \frac{L_r}{R_{ac}} = 0.1 \]

Ratio of total primary inductance to resonant inductance:

\[ m = \frac{L_r + L_m}{L_r} = 8 \]
HB LLC resonant converter design

4.1.8 Achieving ZVS of the LLC converter

To ensure high power efficiency of the LLC converter, ZVS must be guaranteed for all input and load conditions. There are two main considerations to achieve ZVS.

- Operating regions of the LLC converter
  As long as the converter switches at higher than resonant frequencies \( f_r \), it always runs in ZVS mode. When the converter is switching between the resonant frequencies \( f_r \) and \( f_p \), the load condition (Quality Factor, \( Q \)) determines whether the converter operates in ZVS mode or not. Under normal operating conditions, the LLC resonant converter operates at slightly higher than the resonant frequency \( f_r \), which is optimal for high efficiency.

- MOSFET output capacitance
  The resonant inductor current must be high enough to discharge the voltage of effective capacitance appearing in parallel with drain-sources of the power MOSFETs. A major part of this capacitance is the MOSFET output capacitance.

- Dead-time
  Dead-time is required to completely discharge the effective capacitance appearing in parallel with drain-sources of the power MOSFETs to realize the ZVS operation in worst-case conditions applied to the converter.

The four most common waveforms and solutions for ZVS are shown in Figure 13, where modification of the circuit for optimal efficiency can be carried out according to the instructions given. Figure 13 (a) illustrates the perfect ZVS diagram. In Figure 13 (b), \( V_{DS} \) cannot fully discharge to 0 V before the control signal \( V_{GS} \) is sent, thus it is recommended to reduce the magnetizing inductance value in the transformer, and slightly increase the dead-time or replace the power MOSFET with a higher \( R_{DS(ON)} \). In Figure 13 (c), the power MOSFET achieves ZVS, but the inductance current is insufficient to continually forward bias the body diode; thus it is recommended to slightly reduce dead-time. ZVS is achieved in Figure 13 (d), but the excessive dead-time results in reduced efficiency; thus, it is recommended to reduce dead-time.

![Figure 13 Waveforms for ZVS power MOSFET and solutions](image)

After the turns ratio and inductance of the main transformer have been confirmed, the design parameters of the transformer can be obtained.

4.2 LLC main transformer design

After the turns ratio and inductance of the main transformer have been confirmed, the design parameters of the transformer can be obtained.
**HB LLC resonant converter design**

With selected secondary turns:

\[ N_s = 6 \text{ turns} \]

The primary turns can be calculated as:

\[ N_p = n \times N_s = 38.7 \approx 40 \text{ turns} \]

In order to provide the \( V_{cc} \) power supply for ICL5102, an auxiliary winding is introduced. The turns ratio is calculated as if the \( V_{cc} = 15 \text{ V} \) is assumed:

\[ n_a = \frac{N_p}{N_a} = \frac{V_{bus}}{2 \times (V_{cc} + V_{F,D})} = 14.33 \]

The auxiliary turns can be calculated as:

\[ N_a = N_p \times n_a = 2.79 \approx 3 \text{ turns} \]

According to the following gain curves from different load conditions from the ICL5102 LLC design tool, the LLC converter minimum switching frequency at maximum gain can be obtained as:

\[ f_{\text{min}} = 44.7 \text{ kHz} \]

![Gain vs. Frequency](image)

**Figure 14**  Gain vs. frequency for different load conditions

The RMS current on the primary side through the resonant tank can be calculated as:

\[ I_{L,p,\text{rms}} = \frac{1}{n} \sqrt{\left( \frac{\pi \times I_{out,\text{max}}}{2 \times \sqrt{2} \times n} \right)^2 + \left( \frac{n \times (V_{out,\text{max}} + 2 \times V_{F,D})}{4 \times \sqrt{2} \times f_r \times (L_p - L_r)} \right)^2} = 0.73 \text{ A} \]

The primary peak current through the resonant tank can be calculated as:

\[ I_{L,p,\text{peak}} = \sqrt{2} \times I_{L,p,\text{rms}} = 1.03 \text{ A} \]

In the ICL5102 130 W CC reference design, the LLC external resonant inductor is constructed by Würth Electronik under part no. 750342805 as a design example. The specification sheet is given in Table 14.

**Table 14  Parameters of Würth inductor 750342805**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Inductance</td>
<td>160</td>
<td>µH</td>
</tr>
</tbody>
</table>

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HB LLC resonant converter design

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>DC resistance</td>
<td>0.33</td>
<td>Ω</td>
</tr>
<tr>
<td>Saturation current</td>
<td>3.5</td>
<td>A</td>
</tr>
</tbody>
</table>

The LLC main transformer is constructed by Würth Electronik under part no. **750342886** as a design example. The specification sheet is given in Table 15.

**Table 15** Parameters of Würth inductor 750342886

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Main inductance</td>
<td>1500</td>
<td>µH</td>
</tr>
<tr>
<td>Leakage inductance</td>
<td>47</td>
<td>µH</td>
</tr>
<tr>
<td>Turns ratio N_p/N_s</td>
<td>6.67</td>
<td>–</td>
</tr>
</tbody>
</table>
### HB LLC resonant converter design

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Turns ratio $N_p/N_a$</td>
<td>15</td>
<td>–</td>
</tr>
<tr>
<td>DC resistance primary main winding</td>
<td>0.33</td>
<td>Ω</td>
</tr>
<tr>
<td>DC resistance secondary output winding</td>
<td>0.054</td>
<td>Ω</td>
</tr>
<tr>
<td>Saturation current</td>
<td>2</td>
<td>A</td>
</tr>
</tbody>
</table>

### 4.3 HB primary MOSFET selection

The selection of the HB primary power MOSFET is based mainly on the consideration of the drain-source breakdown voltage and the power dissipation.

- **Drain-source breakdown voltage**

According to the operating bus voltage, the breakdown voltage should be chosen as:

\[ V_{(BR)\text{DSS}} > 1.2 \times V_{\text{bus,OV1}} = 594 \text{ V} \]

A 600 V MOSFET would be suitable; for applications with enhanced surge protection, higher breakdown voltage should be selected.

- **Conduction loss**

These losses are frequency independent and do not scale significantly with frequency. This is calculated as follows:

\[ P_{\text{con,loss,MOS,HB}} = (I_{L,p,\text{rms}})^2 \times R_{DS(ON)} = 0.21 \text{ W} \]

In the 130 W reference design, two 600 V Infineon MOSFETs IPD60R400CE of CE family are used for HS and LS. With the $R_{DS(ON)}$ of 290mΩ, the maximum total loss of each MOSFETs is calculated as below:

\[ P_{\text{loss,MOS,HB,max}} = 1.5 \times P_{\text{con,loss,MOS,PFC}} = 0.315 \text{ W} \]

The maximum temperature rise of each MOSFET without heatsink is:

\[ \Delta T_{\text{MOS,PFC,max}} = R_{\text{TH,JA}} \times P_{\text{loss,MOS,HB,max}} = 25.2 ^\circ \text{C} \]

The important parameters for HB MOSFETs are summarized in **Table 16**.

### Table 16 PFC MOSFET design parameters

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Breakdown voltage</td>
<td>$V_{BR,\text{DSS,HB}}$</td>
<td>650</td>
<td>V</td>
</tr>
<tr>
<td>MOSFET on-resistance</td>
<td>$R_{DS(\text{ON})}$</td>
<td>400</td>
<td>mΩ</td>
</tr>
<tr>
<td>Maximum PFC MOSFET conduction loss</td>
<td>$P_{\text{loss,MOS,HB,con}}$</td>
<td>0.315</td>
<td>W</td>
</tr>
</tbody>
</table>

### 4.4 HB low-side CS resistor selection

The LS CS resistor is connected to the ICL5102 LSCS pin and the source of the HB LS MOSFET in order to protect the HB converter from over-current. The capacitive mode protection and the self-adaptive dead-time are also implemented with the CS function at the LSCS pin.
HB LLC resonant converter design

According to the datasheet, there are two over-current protection levels. The LS CS resistor value can be calculated according to the over-current protection level 1 as following:

\[ R_{LCS} < \frac{V_{HB, OCP1, min}}{I_{p, p, peak}} = 0.71 \, \Omega \]

In the ICL5102 130 W reference design, \( R_{LCS} = 0.5 \, \Omega \) is chosen. In order to achieve the precise resistor value and minimize the power dissipation, the CS resistor is split to three parallel connected resistors of 1.2 \( \Omega \) / 1.2 \( \Omega \) / 1.5 \( \Omega \).

To enable the power limitation function in BM, a resistor \( R_{PL} \) between the LCS pin and the CS resistor is required, as shown in Figure 17.

![Figure 17](image)

**Figure 17** ICL5102 BM power limitation

In BM, during burst phase, the ICL5102 HB controller turns on with a switching frequency of \( f_{HB, BM} \) and steadily decreases it to \( f_{HB, max} \) to initialize a soft-on (see ICL5102 datasheet). After soft-on, the switching frequency continues to decrease to \( f_{HB, PL} \), which is set by the resistor \( R_{PL} \).

As shown in Figure 18, a reference threshold higher than 0 is set by the resistor \( R_{PL} \). ICL5102 will integrate the area above and below this threshold according to the voltage at the LSCS pin. The HB switching frequency will adjust itself (by increasing and decreasing) until \( f_{HB, PL} \) is reached so that the integration of area B is the same as area A1 and area A2. By changing the \( R_{PL} \) resistor value, the switching frequency \( f_{HB, PL} \) is set and thus the transferred power in BM. The recommended value of the resistor \( R_{PL} \) is between 200 \( \Omega \) and 1000 \( \Omega \).

![Figure 18](image)

**Figure 18** Threshold set by \( R_{PL} \) for limited power transfer in the BM

In order to filter the voltage spike at the LSCS pin so that the over-current protection is not wrongly triggered, an external filter consisting of \( R_{PL} \) and a small capacitor of some pF is recommended. The capacitor should be placed near the LSCS pin.

### 4.5 HB secondary rectifier diode selection

For the selection of the secondary rectifier diode, the following considerations should be taken into account:

- Reverse breakdown voltage
HB LLC resonant converter design

As the FB rectifier network is used on the secondary side, the diode voltage stress should be the same as the output voltage. However, due to the leakage inductance of the LLC transformer, the rectifier diodes could experience much higher voltage peak, thus a factor 2 margin should be taken into account:

\[ V_{RRM,D,sec} > 2 \times \left( V_{out,max} + V_{F,D,sec} \right) = 155 \, V \]

- Maximum RMS current

The maximum RMS current flowing through each rectifier diode is calculated as:

\[ I_{D,sec,\text{rms,max}} = \frac{\pi}{4} \times I_{out,max} = 1.37 \, A \]

Using a diode with high current capability will benefit the power efficiency.

- Forward voltage

This is directly related to the power efficiency, so the forward voltage should be chosen to be as small as possible.

- Reverse recovery time

As hard commutation of the rectifier diode cannot always be prevented, it’s better to choose an ultra-fast recovery diode.

- Power loss

The only power loss that should be considered is conduction loss. With a forward voltage of 0.5 V assumed, the diode conduction loss can be calculated as follows:

\[ P_{loss,D,sec} = I_{D,sec,\text{rms,max}} \times V_{F,D,sec} = 0.7 \, W \]

- Thermal characteristics

With the thermal resistance of the diode and ambient temperature \( T_a \), the secondary rectifier diode temperature without heatsink is calculated as:

\[ T_{D,sec} = P_{loss,D,sec} \times R_{D,sec,TH JA} + T_a \]

The important parameters for the boost diode used in the 130 W reference design are summarized in Table 17.

<table>
<thead>
<tr>
<th>Table 17</th>
<th>Secondary rectifier diode design parameters</th>
</tr>
</thead>
<tbody>
<tr>
<td>Parameter</td>
<td>Symbol</td>
</tr>
<tr>
<td>Maximum reverse voltage</td>
<td>( V_{RRM,D,sec} )</td>
</tr>
<tr>
<td>Average rectified forward current</td>
<td>( I_{F,D,sec} )</td>
</tr>
<tr>
<td>Forward voltage</td>
<td>( V_{F,D,sec} )</td>
</tr>
</tbody>
</table>

4.6 HB secondary output capacitor

The ripple current flowing through the output capacitor is given as:

\[ I_{cap,sec,\text{rms,max}} = \sqrt{\left( \frac{\pi}{2} \times I_{out,max} \right)^2 - I_{out,max}^2} = 0.84 \, A \]

The output current ripple is defined as 2 percent of the maximum output current:

\[ I_{out,ripple} = 2\% \times I_{out,max} = 0.035 \, A \]
HB LLC resonant converter design

The output voltage ripple is defined as 1 percent of the maximum output voltage:

$$V_{out\_ripple} = 1\% \times V_{out\_max} = 0.76 \, V$$

The equivalent serial resistance of the output capacitor is given as:

$$ESR = \frac{V_{out\_ripple}}{2 \times I_{out\_ripple}} = 0.22 \, \Omega$$

The value of the output capacitor is then given as:

$$C_{out} = \frac{1}{4 \times \pi \times f_{line} \times \sqrt{\left(\frac{V_{out\_ripple}}{I_{out\_ripple}}\right)^2 - ESR^2}} = 80 \, \mu F$$

Sometimes it is impossible to meet the ripple specification with a single output capacitor due to the high ESR of the electrolytic capacitor. Then, additional LC filter stages (post filter) or more parallel capacitors (to reduce ESR) can be used. When using the post filters, be careful not to make the corner frequency too low. Too low a corner frequency may make the system unstable or limit the control bandwidth. It is typical to set the corner frequency of the post filter at around 1/10 ~ 1/5 of the switching frequency.

The important parameters for the output capacitor used in the 130 W reference design are summarized in Table 18.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Voltage rating</td>
<td>$V_{out_C_sec}$</td>
<td>100</td>
<td>V</td>
</tr>
<tr>
<td>Equivalent serial resistance</td>
<td>ESR</td>
<td>0.22</td>
<td>Ω</td>
</tr>
<tr>
<td>Output capacitor</td>
<td>$C_{out}$</td>
<td>220 // 220</td>
<td>μF</td>
</tr>
</tbody>
</table>

4.7 HB output regulation

In the ICL5102 130 W reference design, the HB LLC converter’s output regulation includes three parts: constant current regulation, constant voltage regulation and output current dimming:

- **Constant current regulation**
  
  In normal operation, the LLC converter provides a constant output current. The current regulation is realized through a PI regulator based on the operation amplifier LM358, as shown in Figure 19. The output current is measured through three parallel connected shunt resistors, R50, R51 and R52. These CS resistors must have high accuracy so that the current is regulated precisely. Output reference current is set through a divided voltage from either the auxiliary supply voltage or from the dimming voltage.

- **Output current dimming**
  
  Based on the constant current regulation, a 1 to 10 V dimmer is implemented and provides the current reference signal for the output current regulation. A secondary auxiliary winding with a linear regulator is designed to provide power supply for the dimming circuit.
In addition to the current regulation, a constant output voltage regulation by using TL431 to prevent LEDs lighting in the dim-to-off condition is implemented so that the output voltage is not charged higher than the lowest possible LED forward voltage. This is shown in Figure 20.

Once the dimmer brings the LED driver into the dim-to-off condition, the constant current regulator is then substituted by the constant output voltage regulator. ICL5102 will enter BM according to the output voltage regulation.
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HB LLC resonant converter design

4.8 Frequency setting

In order to close the regulation loop, the feedback signal from the secondary-side current regulation circuit through the optocoupler must be connected to ICL5102.

During normal operation, the ICL5102 HB controller uses CCO to determine the switching frequency. The switching frequency is determined by current $I_{RF}$ that flows out of the RF pin. The RF pin maintains a constant voltage of $V_{RF} = 2.5$ V. This voltage, together with the voltage at pin $V_{BM}$, resistors $R_{BM}$ and $R_{RF}$, and the optocoupler, defines the current flowing out of the RF pin as shown in the following formula and Figure 21:

$$I_{RF} = I_1 + I_2 = I_{BM} + I_{OP} + \frac{V_{RF}}{R_{RF}}$$

![Figure 21](ICL5102 RF pin current definition)

In order to determine the two resistors $R_{RF}$ and $R_{BM}$, the HB LLC converter minimum and maximum switching frequency are needed.

$$f_{min} = 41.6 \text{ kHz}$$
$$f_{max} = 260 \text{ kHz}$$

The CCO of the ICL5102 HB controller is defined linearly with the constant slew rate $C_{FC}$ as shown in Figure 22.

$$C_{FC} = 400 \text{ KHz/mA}$$

![Figure 22](CCO of ICL5102 in normal operation)

The calculation of the two resistors $R_{RF}$ and $R_{BM}$ is given below:
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\[ R_{RF} = C_{FC} \times \frac{15V}{f_{min} - f_{max}} = 212.76 \text{k}\Omega \]

\[ R_{BM} = C_{FC} \times \frac{1.5V}{f_{max} - f_{min}} = 2.71 \text{k}\Omega \]

Both resistor values are selected so that the ICL5102 130 W reference design does not enter BM in order to prevent the LED blinking. BM is only for standby in the dim-to-off operation.

4.9 Primary output OVP

ICL5102 provides another possibility for fast OVP on the primary side by sensing the winding voltage. This function is realized by connecting the OVP pin to the auxiliary winding of the HB transformer, as shown in Figure 23.

![Figure 23](image)

Figure 23 HB output OVP detection circuit

To decide the \( R_{OVP,1} \) and \( R_{OVP,2} \), the following formula can be used:

\[ \frac{R_{OVP,2}}{R_{OVP,1}} = \frac{V_{OVP,\text{ref}}}{V_{out,OVP} \times \frac{n}{n_{a}} - V_{F.D.Vcc} - V_{OVP,\text{ref}}} \]

If the primary output voltage level is defined as 90 V, the divider ratio can be obtained as:

\[ \frac{R_{OVP,2}}{R_{OVP,1}} = 15 \]
5 Power supply for ICL5102

The power supply for the controller ICL5102 is provided by the capacitors connected to the $V_{cc}$ pin. It is strongly recommended to use both an electrolytic capacitor and a ceramic capacitor parallel connected as $V_{cc}$ capacitors. Due to its high capacitance, an electrolytic capacitor is suitable as charge storage but has a bad AC coupling behavior. A ceramic capacitor on the other hand has an excellent AC decoupling effect, but has a capacitance derating strongly dependent on voltage and temperature.

The $V_{cc}$ capacitors can be charged either by high-voltage start-up circuit, by PFC auxiliary winding or by HB auxiliary winding according to different requirements and conditions. This is described in the following sections.

5.1 Power-up

At start-up, after the AC input is applied, the $V_{cc}$ capacitors must be charged by the high-voltage start-up circuit before the $V_{cc}$ reaches the on-threshold. The start-up circuit can be designed as illustrated in Figure 24.

![Figure 24: Vcc power supply from the start-up circuit](image)

The start-up circuit is connected to the rectified AC input after the bridge rectifier via the current limitation resistors R3, R4 and R5. Depletion MOSFET BSS126 is used so that the $V_{cc}$ charge function happens automatically as long as the $V_{cc}$ is under a certain threshold dependent on the customer’s design.

The charge current limited by the resistors R3, R4 and R5 is dependent on the time-to-light from the LED driver system requirement. Assuming the required time-to-light is 500 ms, the $V_{cc}$ capacitor is 220 $\mu$F, and PFC and HB start-up time are each 50 ms, the minimum charge current can be calculated as:

$$I_{V_{cc \_charge \_min}} = C_{V_{cc}} \cdot \frac{V_{V_{cc \_on \_max}}}{t_{time \_to \_light} - t_{PFC \_start} - t_{HB \_start}} = 12.2 \, mA$$

To ensure that this charge current can be provided at low-line input so that the time-to-light is under 500 ms, the current limitation resistor value is calculated as:
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Power supply for ICL5102

\[ R_{HV} = \sqrt{2} \times \frac{V_{in,\text{min},\text{rms}}}{I_{Vcc,\text{charge,\text{min}}} = 10 \, k\Omega} \]

And the maximum charge current at high-line input is:

\[ I_{Vcc,\text{charge,\text{max}}} = \frac{\sqrt{2} \times V_{in,\text{max},\text{rms}}}{R_{HV}} = 43 \, mA \]

It is strongly recommended to split the \( R_{HV} \) to three serial connected resistors as R3, R4 and R5 to minimize the power and voltage stress of each current limitation resistor.

5.2 Power supply during operation

After the \( V_{CC} \) on-threshold is reached, ICL5102 will start the first PFC stage to boost the bus voltage to \( V_{bus} = 450 \) V and then the HB stage begins to work. If there is no \( V_{CC} \) power supply from the PFC auxiliary winding, the \( V_{CC} \) high-voltage start-up circuit should stop working at the latest when the HB begins to work and the HB auxiliary winding will take over the charging of the \( V_{CC} \) capacitors. The start-up circuit can be disabled either by a certain \( V_{CC} \) voltage level or by the switching of the HB LS gate, as shown in Figure 24.

It is recommended to regulate the \( V_{CC} \) voltage not higher than 16 V, in order to reduce the power consumed by ICL5102 and avoid over-temperature. A reference circuit using a linear regulator for the \( V_{CC} \) power supply circuit is shown in Figure 25.

![Figure 25](linear_regulator.png)  
**Figure 25** Linear regulator for \( V_{CC} \) power supply

5.3 Power supply for high-side driver

Due to the floating ground of the HS gate driver of ICL5102, the power supply for HS is separated and realized through the bootstrap circuit. This is shown in Figure 26.

![Figure 26](bootstrap_circuit.png)  
**Figure 26** Bootstrap circuit for high-side power supply
Power supply for ICL5102

To optimize HB switching behavior during start-up and BM operation, the HS Vcc capacitor is targeted to reach its turn-on threshold within the first LS gate pulse. Thus, its capacitance can be calculated as:

\[ C_{HSVcc} < -\frac{0.5 \cdot T_{HB\_switching} + t_{dead\_time}}{\ln(1 - \frac{V_{HSVcc\_on}}{V_{cc} - V_{D\_BS}}) \cdot R_{HSVcc}} \]

Assuming the HB soft-start frequency begins with 300 kHz with 500 ns dead-time, HS Vcc on-threshold is maximum 11V, Vcc is 15 V, bootstrap diode forward voltage is 0.7 V, current limitation resistor is 10 \( \Omega \), the capacitor value is:

\[ C_{HSVcc} < 120nF \]

In the ICL5102 130 W reference design, a 100 nF capacitor is selected.

The diode in the bootstrap circuit must be a 600 V high-voltage one according to the bus voltage level. The reverse recovery speed must be ultra-fast.

5.4 Other considerations for ICL5102 power supply

In the dim-to-off condition, ICL5102 is working in BM. To ensure the power supply for ICL5102 so that the Vcc does not fall below the UVLO threshold, other auxiliary winding for the power supply such as PFC or external resonant inductor auxiliary windings could be taken into account.
6 OTP

ICL5102 provides OTP through an external connected NTC temperature sensor at the OTP pin. The source current out of the OTP pin is $I_{OTP} = 100 \text{ µA}$. The current generates a voltage drop on the connected NTC sensor. Once the voltage at the OTP pin decreases below $V_{OTP,\text{off}} = 625 \text{ mV}$ longer than the blanking time $t_{OTP,\text{blanking}} = 620 \mu\text{s}$ in normal operation, both PFC and HB stages stop switching and ICL5102HV will enter auto-restart. PFC and HB operations recover after the voltage at the OTP pin is higher than $V_{OTP,\text{start}} = 703 \text{ mV}$ for longer than $t_{OTP,\text{blanking}}$. This is shown in Figure 27.

![Figure 27 External OTP](image)

In order to trigger the OTP threshold, the connected NTC should have a resistor value:

$$R_{OTP,\text{off},\text{min}} = \frac{V_{OTP,\text{off},\text{min}}}{I_{OTP,\text{max}}} = 5.6 \text{ kΩ}$$

In order to recover from the OTP, the connected NTC should have a resistor value:

$$R_{OTP,\text{start},\text{max}} = \frac{V_{OTP,\text{start},\text{max}}}{I_{OTP,\text{min}}} = 7.8 \text{ kΩ}$$

With the calculated values, the NTC temperature sensors of EPCOS 8507 series are compared as in the example in Figure 28.

![Figure 28 Characteristics of EPCPS NTC 8507 series](image)
Design guide for dual-stage PFC+LLC LED driver using ICL5102

OTP

From the characteristics, 100 kΩ NTC is suitable and selected for the ICL5102 130 W reference design.

Additionally, to modify the resistance curve according to different requirements, serial or parallel resistors can be added to the NTC. Figure 29 shows examples of how to modify the characteristics of NTC.

![Diagram of NTC in Combination with Rs and Rp vs. Ambient Temperature](image)

Figure 29  Modified characteristics of EPCPS NTC 8507 series

It is recommended to place a good-quality ceramic capacitor close to the OTP pin to prevent mis-triggered OTP protection from noise.

To disable the external OTP, a resistor of 20 kΩ can be added at the OTP pin instead of the NTC to keep the voltage higher than $V_{OTP\_start} = 703$ mV.
ICL5102 operation flow chart

Operating FLOW Chart ICL5102

- **UVLO**
  - VCC < 9.0V
  - Icc < 90µA

- **Monitoring**
  - 9.0V < VCC < 16.3V
  - Icc < 100µA

- **Power-up**
  - Gate Drives off
  - 9.0V < VCC < 16.3V

- **Start-up**
  - PFC Gate ON
  - Inverter Gates OFF
  - 9.0V < VCC < 16.3V

- **Softstart**
  - Inverter Gates ON
  - 9.0V < VCC < 16.3V

- **Run**
  - 9.0V < VCC < 16.3V
  - Vsm < 0.75V

- **BM ENTRY**
  - t = 10ms

- **BM Sleep**
  - 0.25 < Vsm < 2.2V
  - All Gates OFF
  - Ibm = xxx µA

- **BM Pulse**
  - Vsm = 2.2V
  - Ibm = 0µA

- **BM EXIT 1 - 4**
  - VBUS < 12.5%
  - VBUS > 109%

- **Fault**
  - 16.3V < VCC < 9.0V
  - Gate Drives off
  - POWER Down
  - AUTO RESTART

- **Full Protection**
  - t > 50ms
  - Vio < 1.2V
  - Vcc < 115%
  - VLSCS > 0.8V
  - t > 620µs
  - OTP / CapLoad
  - t > 5.0µs
  - OVP
  - VLSCS > 1.6V
  - t > 1.0µs
  - Vcc < 9.0V

- **EXIT 1 bis EXIT 4**

- **VCC Clamp OFF**

- **VCC Clamp ON when VCC > 16.3V**

- **Exempt BO**

- **VCC Clamp ON when VCC > 16.3V**

- **VCC Clamp OFF**

- **Full Protection**
  - t > 500ms
  - Exempt BO
ICL5102 operation flow chart

Figure 30    ICL5102 operation flow chart
## Protection features

All ICL5102 protection features are summarized in the following fault matrix.

### Table 19  ICL5102 fault matrix

<table>
<thead>
<tr>
<th>Description of fault</th>
<th>Characteristics of fault</th>
<th>Operating mode</th>
<th>Consequence</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Detection is active</td>
<td>Reaction</td>
</tr>
<tr>
<td></td>
<td>Definition of fault</td>
<td>Action</td>
<td>Minimum of</td>
</tr>
<tr>
<td>Supply voltage $V_{CC}$ less than 16.0 V before power-up</td>
<td>Below start-up threshold</td>
<td>W</td>
<td>1 ms</td>
</tr>
<tr>
<td>Supply voltage $V_{CC}$ less than 9.0 V after power-up</td>
<td>Below UVLO threshold</td>
<td>A</td>
<td>1 ms</td>
</tr>
<tr>
<td>Brown-out detection $V_{BO}$ less than 1.2 V</td>
<td>$BO$</td>
<td>A</td>
<td>50 ms</td>
</tr>
<tr>
<td>Brown-in control $V_{BO}$ less than 1.4 V</td>
<td>$BI$</td>
<td>W</td>
<td>1 ms</td>
</tr>
<tr>
<td>Over-temperature detection $V_{OTP1}$ less than 703 mV</td>
<td>$OTP$</td>
<td>W</td>
<td>620 µs</td>
</tr>
<tr>
<td>Over-temperature detection $V_{OTP2}$ less than 625 mV</td>
<td>$OTP$</td>
<td>A</td>
<td>620 µs</td>
</tr>
<tr>
<td>Bus voltage less than 12.5 percent of rated level</td>
<td>Open-loop detection</td>
<td>W</td>
<td>1 ms</td>
</tr>
<tr>
<td>Bus voltage less than 12.5 percent of rated level</td>
<td>Open-loop detection</td>
<td>W</td>
<td>1 ms</td>
</tr>
<tr>
<td>Bus voltage less than 75 percent of rated level</td>
<td>PFC under-voltage</td>
<td>W</td>
<td>1 ms</td>
</tr>
<tr>
<td>Bus voltage more than 105 percent of rated level</td>
<td>PFC over-voltage</td>
<td>W</td>
<td>5 µs</td>
</tr>
<tr>
<td>Bus voltage more than 109 percent of rated level</td>
<td>PFC over-voltage</td>
<td>W</td>
<td>5 µs</td>
</tr>
<tr>
<td>Bus voltage more than 115 percent of rated level</td>
<td>Inverter over-voltage</td>
<td>A</td>
<td>50 ms</td>
</tr>
</tbody>
</table>
## Protection features

<table>
<thead>
<tr>
<th>Description of fault</th>
<th>Characteristics of fault</th>
<th>Operating mode Detection is active</th>
<th>Consequence</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output over voltage $V_{OVP}$ more than 2.5 V</td>
<td>OVP</td>
<td>W 5 µs</td>
<td>X</td>
</tr>
<tr>
<td>Output over voltage $V_{OVP}$ more than 2.5 V</td>
<td>OVP</td>
<td>A 5 µs</td>
<td>X</td>
</tr>
<tr>
<td>Capacitive load operation below resonance</td>
<td>Capacitive load</td>
<td>A 620 µs</td>
<td>X</td>
</tr>
<tr>
<td>Capacitive load control</td>
<td>Capacitive load control</td>
<td>N Half-cycle</td>
<td>X</td>
</tr>
</tbody>
</table>

$N = $ handled during normal operation

$W = $ Wait while condition is present

$A = $ Auto-restart

### Definition of fault

| Voltage at PFCCS pin $V_{PFCCS}$ more than 1.0 V | PFC over-current control | N 200 ns | X | X | X | X | Stops on-time of PFC FET immediately |
| Voltage at LSCS pin $V_{LSCS}$ more than 0.8 V | Over-current control | N Half-cycle | X | X | X | Increases HB frequency |
| Voltage at LSCS pin $V_{LSCS}$ more than 0.8 V | Over-current shut-down | A 50 ms | X | X | Power-down Auto-restart |
| Voltage at LSCS pin $V_{LSCS}$ more than 1.6 V | Inverter over-current | A 500 ns | X | X | X | Power-down Auto-restart |

$N = $ handled during normal operation

$W = $ Wait while condition is present

$A = $ Auto-restart
Design guide for dual-stage PFC+LLC LED driver using ICL5102

Protection features

[1] ICL5102 datasheet
[3] ICL5102 LLC design tool
[4] Primary-side MOSFET selection for LLC topology, application note, Infineon Technologies
## Revision history

<table>
<thead>
<tr>
<th>Document version</th>
<th>Date of release</th>
<th>Description of changes</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.0</td>
<td>2019-02-26</td>
<td>First release</td>
</tr>
</tbody>
</table>
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