Infineon ISOFACE™ dual-channel digital isolators design guide

About this document

Scope and purpose

This document introduces Infineon's ISOFACE™ dual-channel digital isolators and gives design guidance for system engineers designing galvanical isolation in high-voltage (HV) applications.

Intended audience

This document is intended for design engineers who want to design with Infineon's digital isolators for isolation purposes in HV applications.

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1 Introduction to Infineon's ISOFACE™ digital isolators

Galvanic isolation provides level-shift functions, improves electrical noise immunity and ensures safety in HV applications. To meet the continually growing requirements for isolation in industrial applications, Infineon Technologies is introducing the first generation of ISOFACE™ digital isolators, providing high robustness while ensuring accurate timing performance and low power consumption.

1.1 Isolation technology

This first digital isolator family uses Infineon's patented coreless transformer (CT) technology to isolate the signals crossing different voltage domains. It is a magnetically coupled isolated technology, which uses semiconductor manufacturing processes to integrate an on-chip transformer consisting of metal spirals separated by a silicon dioxide (SiO_2) insulation barrier, as shown in **Figure 1**. The on-chip coreless transformers are used to transmit signals between the input and output chips. In addition, functions such as glitch filter, communication modulation, watchdog and undervoltage lockout (UVLO) are integrated to ensure robust and fail-safe data transmission even in critical industrial environments where high voltages and noises are present.

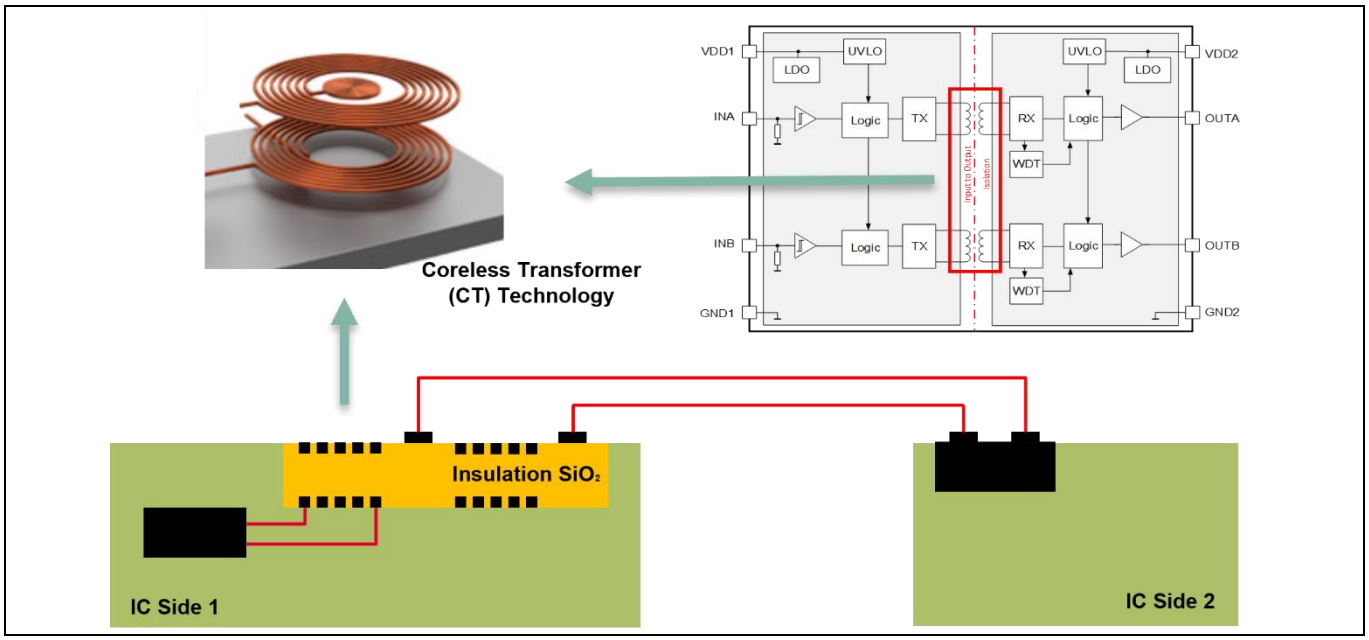

Figure 1 Cross-section of Infineon's CT, used in the ISOFACE™ digital isolator 2DIBx4xxF products

1.2 Product features

Infineon's ISOFACE™ digital isolators are designed to meet challenging requirements in industrial applications and have the following features:

- High common-mode transient immunity of more than 100 kV/µs
- TTL or CMOS input thresholds for dual-channel digital isolators
- High or low fail-safe default output options available
- Wide operating supply voltage from 2.7 to 6.5 V (absolute maximum 7.5 V)
- Accurate timing performance with 26 ns typical propagation delay and -5/+6 ns spread
- Low power consumption with maximum 3.3 mA at 3.3 V and 1 Mbps

1.3 Product variants overview

Product variants with different channel configurations, fail-safe default output states, and variable or fixed input thresholds are available, as listed in **Table 1**.

Table 1 Product variants of Infineon ISOFACE™ dual-channel digital isolator family

Part number	Channel configuration	Default output state	Input thresholds	Isolation rating	Package
2DIB0400F	2 forward 0 reverse (2+0)	Low	Variable (CMOS)	V_{ISO} = 3000 V_{RMS} (UL1577 Ed. 5)	PG-DSO-8 5 x 4 mm
2DIB0401F		High			
2DIB1400F	1 forward 1 reverse (1+1)	Low			
2DIB1401F		High			
2DIB0410F	2 forward 0 reverse (2+0)	Low	Fixed (TTL)		
2DIB0411F		High			
2DIB1410F	1 forward 1 reverse (1+1)	Low			
2DIB1411F		High			

The suitable target applications are:

- Low-voltage (LV) DC-DC brick in telecom and server power supply systems
- High-side floating driver gate control for GaN with integrated power stage (GaN-IPS)
- Isolated UART/CAN communication

2 Selection guide for ISOFACE™ digital isolators

Finding the right device from the ISOFACE™ dual-channel digital isolator family is not difficult, as they have certain common features but in different input threshold and default output states to meet requirements across various industrial applications. However, there are some important considerations when selecting the right digital isolator, depending on the application requirements.

- **Data rate**

The ISOFACE™ dual-channel digital isolator family provides a single data rate of maximum 40 Mbps, which is suitable for isolating gate drive signals in switched mode power supply (SMPS) applications and for isolating low/medium-speed communication interfaces. **Table 2** summarizes the applications that are suitable for the given data rate.

Table 2 Suitable applications for ISOFACE™ digital isolators with maximum 40 Mbps data rate

ISOFACE™ digital isolator	Part number	Maximum data rate	SMPS applications	Isolated communication interfaces
Dual-channel digital isolator	2DIBx4xxF	40 Mbps	Up to 20 MHz switching frequency	Isolated UART, CAN communication

- **Isolation specification requirements**

Isolation withstand voltage, together with package requirements such as creepage, clearance, comparative tracking index (CTI) and pollution degree, are the parameters mainly used to select the right digital isolator for the application.

For instance, Infineon's ISOFACE™ 2DIBx4xxF digital isolators have minimum 4 mm creepage and clearance, and a CTI of more than 400 V can withstand 3000 V_{RMS} isolation voltage (V_{ISO}) according to UL 1577. They are suitable for applications that require either functional or basic isolation. **Table 3** gives an overview of the isolation specifications of ISOFACE™ dual-channel digital isolators.

Table 3 Isolation specifications of ISOFACE™ digital isolators

ISOFACE™ digital isolator	Part number	Minimum creepage and clearance	Suitable isolation type	Maximum isolation voltage V_{ISO} (UL 1577)	Maximum working voltage (V_{IOWM})	Maximum surge isolation voltage (V_{IOSM})
Dual-channel digital isolator	2DIBx4xxF	4 mm	Functional or basic isolation	3000 V_{RMS}	558 V_{RMS} [1]	6 kV_{pk}

- **Channel configuration**

Determining channel configuration means choosing the number of channels and their direction. For instance, a 2+0 (two forward and zero reverse) dual-channel digital isolator is suitable for isolating gate drive signals (e.g., low- and high-side switches) in power converter topologies like half-bridge or full-bridge. On the other hand, a

[1] Basic isolation, pollution degree 2, material group II

1+1 (one forward and one reverse) dual-channel digital isolator is ideal for isolating the Tx and Rx signal paths in communication interfaces such as UART and CAN. **Table 4** summarizes the different possible channel configurations of the ISOFACE™ dual-channel digital isolators and their corresponding applications.

Table 4 Channel configurations and applications of ISOFACE™ digital isolators

ISOFACE™ digital isolator	Isolation requirement	Part number	Channel configuration	Suitable applications
Dual-channel digital isolator	Basic or functional isolation with isolation voltage (V_{ISO}) up to 3000 V_{RMS}	2DIB04xxF	2 forward 0 reverse (2+0)	SMPS applications with half- and full-bridge topologies
		2DIB14xxF	1 forward 1 reverse (1+1)	Isolated UART and CAN communication interfaces, level-shift for high side floating drive of GaN-IPS

- **Input threshold**

ISOFACE™ dual-channel digital isolators provide variants with either CMOS or TTL input logic thresholds. A TTL input threshold is independent of supply voltage and fixed at the level of 0.8 V (for low) and 2 V (for high). This is an advantage for SMPS applications where the switching noise can be coupled into the power supply of digital isolators: the input threshold will not change as a result of the switching noise. The CMOS input threshold is variable and related to supply voltage, which could provide more noise margin for isolated communications interfaces which have less noise on the power supply line.

Table 5 Preferred input threshold of ISOFACE™ digital isolators for different applications

Application	Default input threshold	Part number
Isolating gate drive signals in SMPS applications	TTL	2DIBx41xF
Isolating communication interfaces such as CAN, UART	CMOS	2DIBx40xF

- **Fail-safe default output state**

Fail-safe default output state indicates the output condition when the input channel of a digital isolator is unpowered or the input pins are open. This is an important criterion for selecting the right digital isolator depending on the application. Typically, default low output state is preferred when the digital isolators are used to isolate the gate driving signals, for example in SMPS applications. The output of digital isolators stays safely off whenever any error happens on the intput side. On the other hand, for isolating communication interfaces, it is preferred to have a default high output, because most communication buses are defined as high logic level when the bus is in idle state. **Table 6** summarizes the preferred default output states for different applications.

Table 6 Preferred default output state of ISOFACE™ digital isolators for different applications

Application	Default output state	Part number
Isolating gate drive signals in SMPS applications	Low	2DIBx4x0F
Isolating communication interfaces such as CAN, UART, SPI, RS 485	High	2DIBx4x1F

- **Common mode transient immunity (CMTI)**

CMTI is defined as the ability of a digital isolator to withstand fast changes in the potential difference between its grounds. A high CMTI value, typically specified in kV/µs, indicates a robust isolation technology and fail-free data transmission even under the critical condition of fast transients at high switching frequencies.

ISOFACE™ dual-channel digital isolators provide the benchmark highest CMTI of 100 kV/µs minimum currently on the market, and are the best choices for high power density designs using SiC/GaN that can have high dv/dt (more than 100 kV/µs) and motor control applications that have high common-mode noise.

Figure 2 gives an overview of how to select the right device from the ISOFACE™ digital isolator family according to key parameters and application requirements.

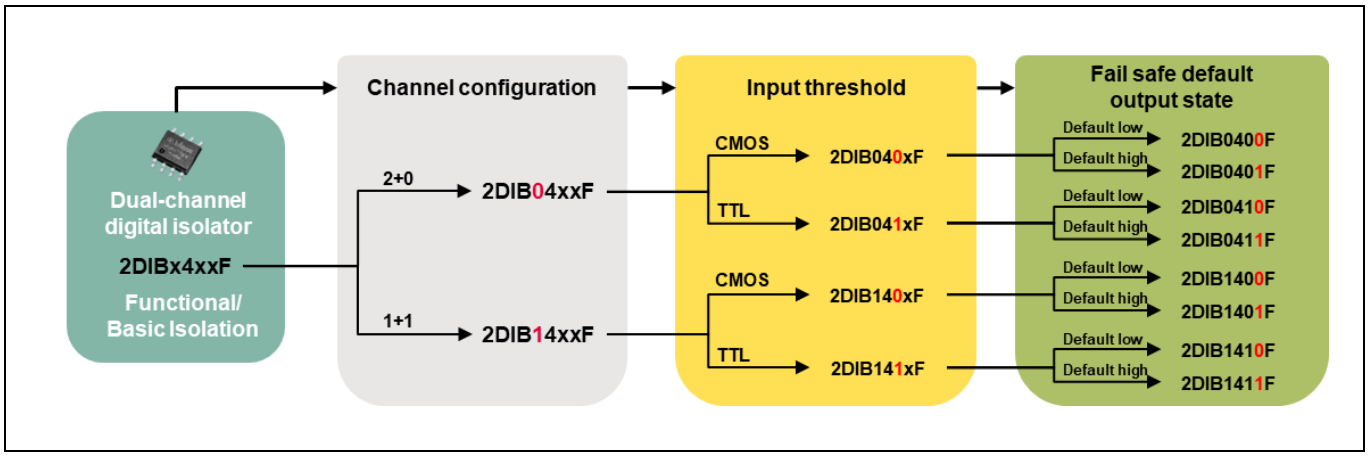

Figure 2 Selection guide for ISOFACE™ digital isolator

3 PCB design guidelines

3.1 PCB material

As Infineon's dual- and quad-channel digital isolators have a maximum data rate of 40 Mbps, commonly used FR-4 material is suitable for the PCB. Its characteristics of slight moisture absorption, reliable insulation, and considerable mechanical strength make it preferred over other alternatives.

3.2 Board layer stack

To achieve a low EMI performance on a system using digital isolators with high data rate up to 40 Mbps, it is highly recommended to design the system application board with a four-layer PCB design, described as follows:

- Layer 1: high-speed layer
  This layer is intended for high-speed signal traces, for example signal inputs and signal outputs.
- Layer 2: ground layer
  One ground layer is placed in between to provide the shielding effect.
- Layer 3: power layer
  This layer is intended for all power supply traces for the digital isolator.
- Layer 4: low-speed or ground layer
  If there are no low-speed signal traces available, this layer can be designed as a ground layer for better shielding.

The layer stacking is shown in **Figure 3**.

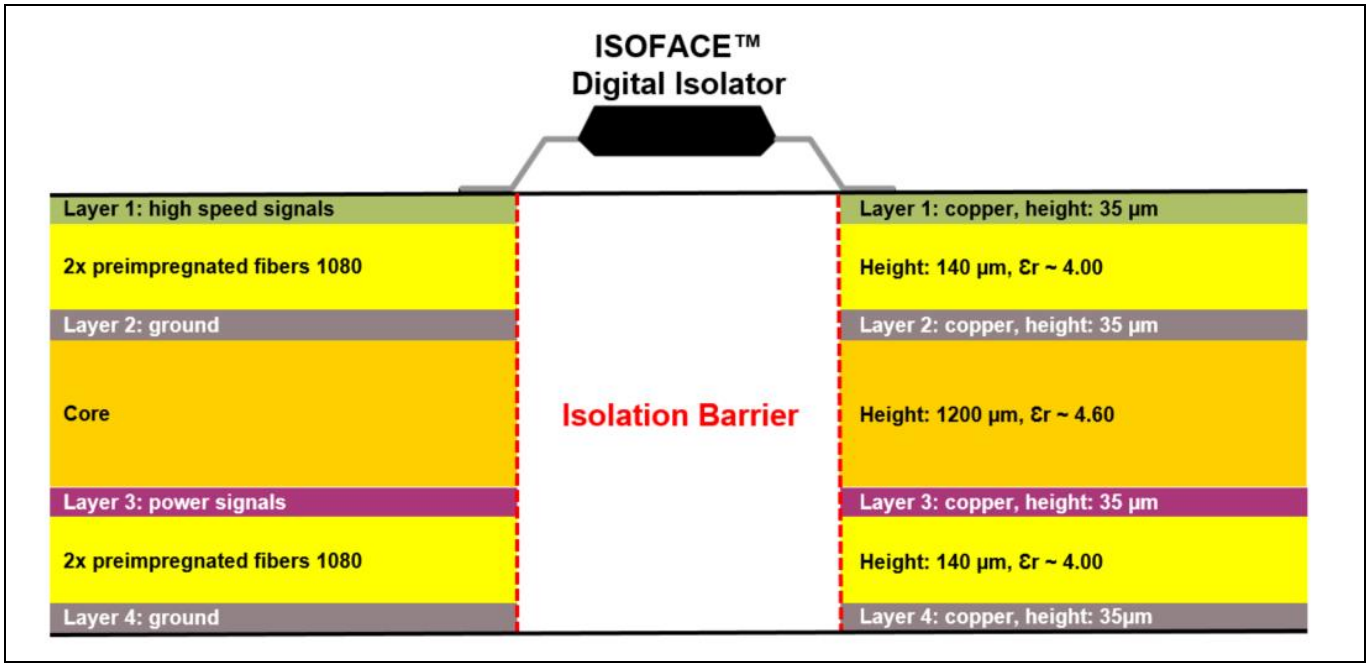

Figure 3 Layer stacking of the system design using digital isolators

3.3 Layout considerations

To design ISOFACE™ digital isolators in HV applications with a high data rate, there are some important layout considerations to ensure safe, fail-free data transmission. As **Figure 4** shows, using the example of ISOFACE™ 2DIB1400F, a digital isolator needs to be connected to high traces, power supplies and silent grounds.

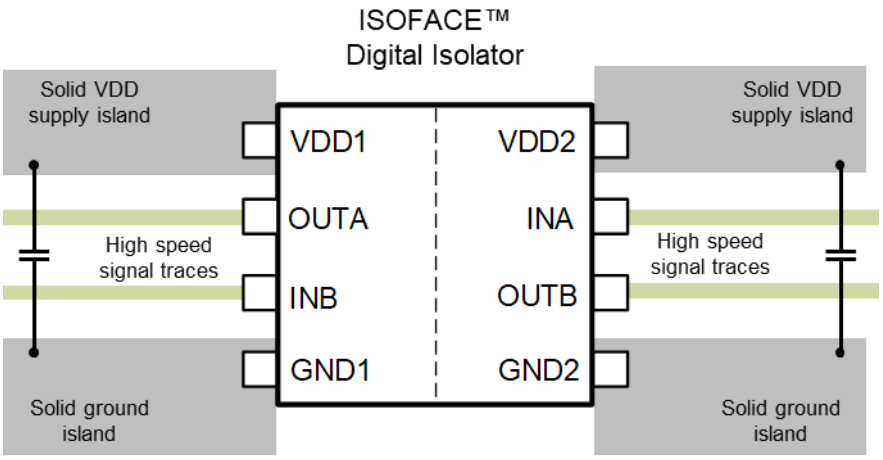

Figure 4 Layout considerations for designs with ISOFACE™ dual-channel digital isolators

There are some rules to observe, as summarized below:

- Place solid power supply islands directly at the power supply VDD pins to reduce inductance caused by traces, as currents with high peak flow into the VDD pins especially at high data rates.
- Place high-frequency bypass capacitors as close as possible to the VDD and GND pins. It is highly recommended to use two bypass capacitors of 100 nF and 1 µF on both sides at high data rates for smooth output signals.
- Place solid ground islands directly at the ground pins to help dissipate heat through the PCB.
- Route the high-speed signals on the top layer and avoid using vias to reduce parasitics, which could create noises and influence the data transmission.
- Route the low-speed signals on the bottom layer, as they can tolerate more parasitics.

4 Typical applications for ISOFACE™ digital isolators

ISOFACE™ digital isolators provide both functional and safety isolation for HV applciations. Together with non-isolated gate drivers, they are preferred in SMPS applications with high flexibility and integrated communication, especially with GaN-IPS. Together with transceivers or stand-alone, they are suitable for isolated communication interfaces.

4.1 Applications using dual-channel digital isolators

ISOFACE™ dual-channel digital isolators feature a wide supply range, TTL/CMOS input threshold and high CMTI to enable robust data transmission with high noise immunity in both SMPS applications and isolated communication interfaces.

- **Isolated LV DC-DC brick**

LV DC-DC bricks are widely used in **telecom** and **server SMPS** to achieve a stable 12 V DC output. In order to fulfill the growing demand for higher power density, enhanced safety requirements and communication capability, isolated DC-DC bricks above 800 W are predominantly designed with full-bridge to full-bridge (FB-FB) topology, which is controlled by a digital controller placed on the secondary side of the main power transformer. To ensure input-to-output safety isolation, a digital isolator with basic isolation is often utilized for transferring the PWM gate control signals over the isolation barrier.

As an example, **Figure 5** illustrates Infineon's solution for an isolated 1 kW DC-DC brick, which employs the **XDP™ XDPP1100 digital power controller** on the secondary side to control the primary-side full-bridge topology. The PWM signals are transmitted over the isolation barrier through ISOFACE™ dual-channel digital isolator 2DIB0410F.

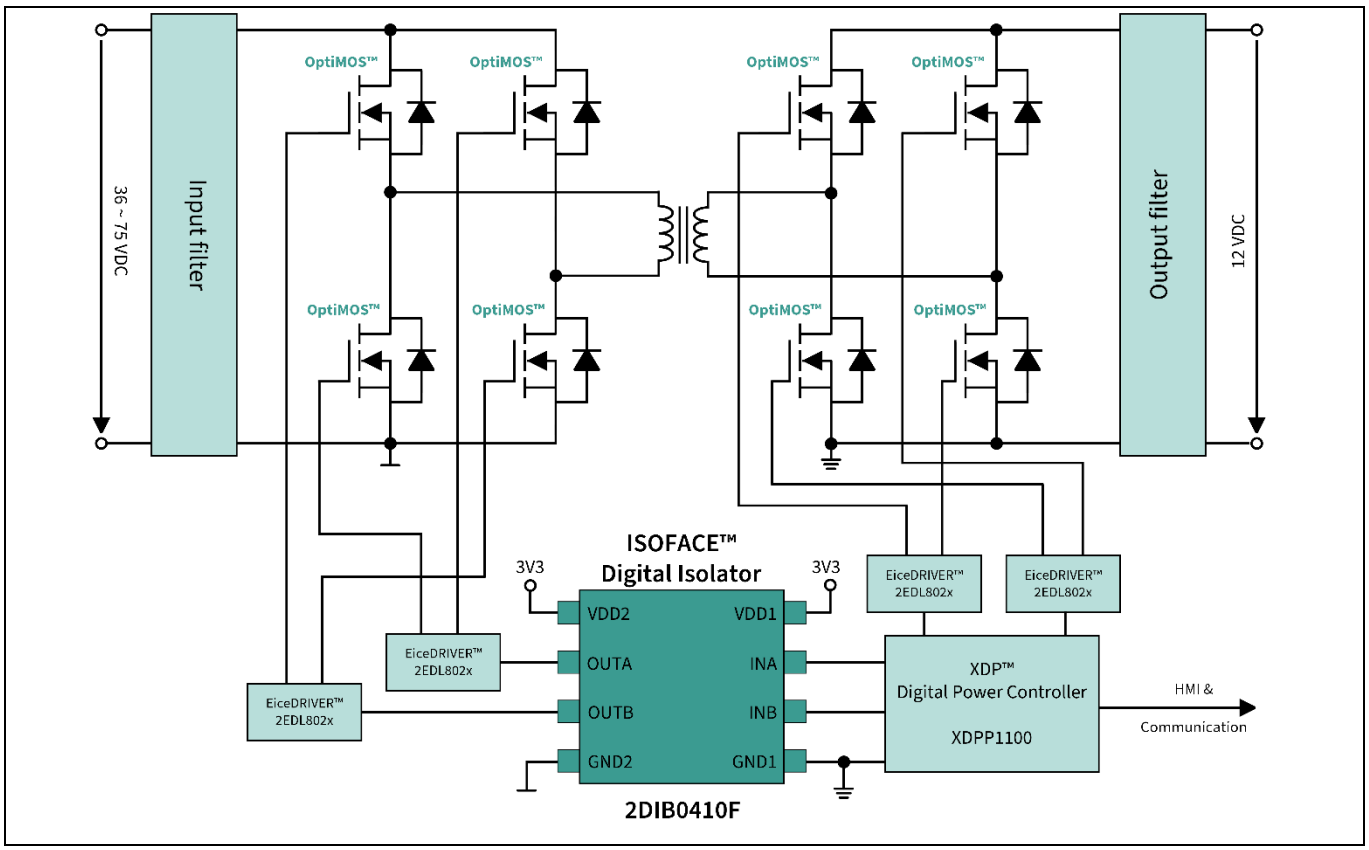

Figure 5 Isolated LV DC-DC brick using ISOFACE™ 2DIB0410F

Both sides of the converter use level-shift **EiceDRIVER™ 2EDL802x gate driver ICs**. The two channels of the digital isolator transfer the complementary PWM signals, which control the two **OptiMOS™ power MOSFETs** on different arms of the full-bridge diagonally. Furthermore, the ISOFACE™ 2DIB0410F provides a fixed TTL input threshold that is immune to noise on the V_{DD} power supply line in SMPS applications. The default low output state ensures a safe turn-off of all MOSFETs in case the input-side supply of the digital isolator is below the UVLO.

- **Isolated CAN and UART communication**

Controller area network (CAN) and universal asynchronous receiver/transmitter (UART) communication have been widely used in industrial and automotive applications. They have the common advantage that only a single pair of cables (two communication lines) is needed at the physical layer for data transmission. When it comes to ensuring safety or preventing noise interference in an isolated CAN or UART interface, the ISOFACE™ dual-channel digital isolator 2DIB1401F stands out as a top choice for providing galvanic isolation. This reliable isolator offers high CMTI and very low pulse-width distortion (PWD), which are crucial features for achieving reliable communication. Additionally, the isolator's default high output state ensures that the communication line (typically in a logic high during the idle state) will remain unblocked even in the event of a failure, preventing potential power supply loss on the input side.

Together with Infineon's **CAN transceiver TLE9251**, an example of an isolated CAN interface is illustrated in **Figure 6**. ISOFACE™ 2DIB1401F is placed between the controller and the transceiver to provide galvanic isolation.

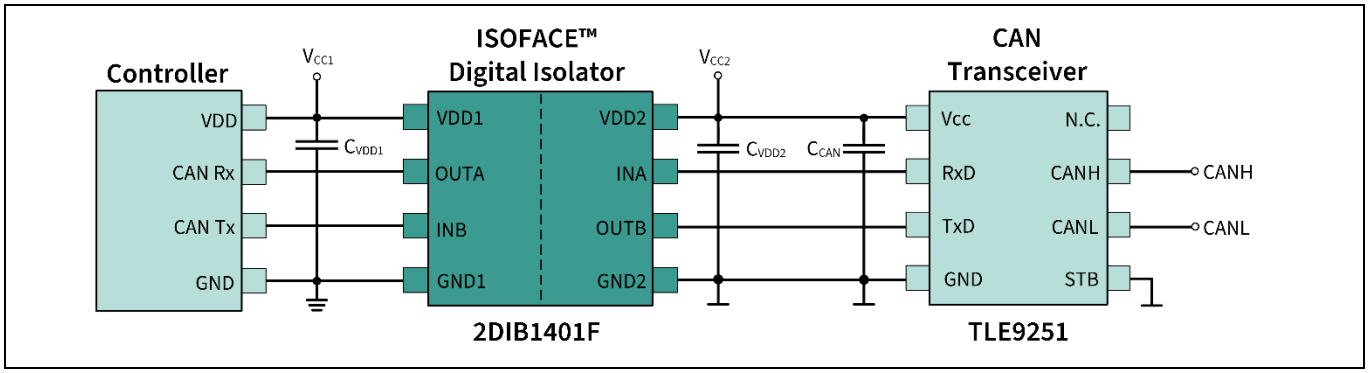

Figure 6 Isolated CAN communication using ISOFACE™ 2DIB1411F

- **Functional isolation in high-side floating drive for GaN-IPS**

The importance of 650 V **gallium nitride (GaN)-HEMTs** in SMPS designs has been increasing lately, owing to their ability to operate at far higher switching frequencies while significantly minimizing energy loss. Also, GaN-IPSs that combine a GaN switch with an integrated gate driver within a single package are becoming the preferred option to achieve designs with extreme power density, fewer components, reduced component count and minimum parasitics.

To ensure proper functioning of the high-side GaN-IPS, a digital isolator is necessary to perform a level-shift function for the gate driver, because the gate driver refers to the switching node. Due to the GaN-HEMT's ability to generate fast dv/dt commutations of up to 100 V/ns, high common-mode transients can occur, necessitating a robust solution. The ISOFACE™ digital isolators are suitable in this case as they can provide a minimum CMTI of 100 V/ns and ensure reliable transfer of PWM signals.

Figure 7 shows an example using ISOFACE™ dual-channel digital isolator 2DIB1410F for a high-side floating drive. One forward data channel is used to transfer the gate signal, while the reverse channel communicates the fault feedback signal to the controller.

Using another ISOFACE™ 2DIB1410F for the low-side GaN-IPS is optional. However, it is highly recommended to equalize the propagation delays between the high-side and low-side signal paths and to provide isolation for the different grounds of the GaN-IPS (power ground) and the controller (digital ground).

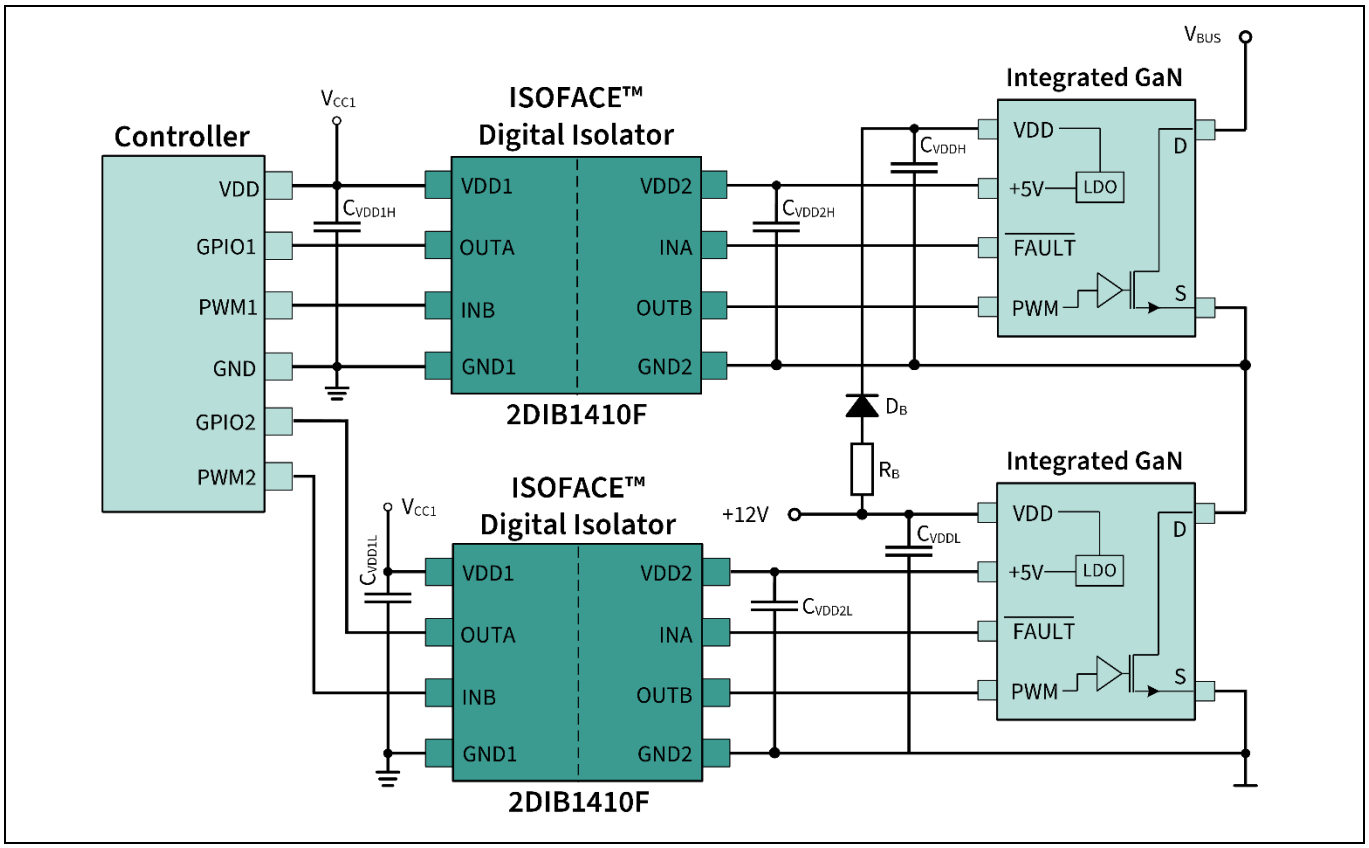

Figure 7 Functional isolation in GaN-IPS half-bridge provided by ISOFACE™ 2DIB1410F

Revision history

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V 1.0	2023-05-16	Initial release

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