5th Generation Fixed-Frequency Design Guide

Design Guide - ICE5xSAG and ICE5xRxxxxAG

About this document

Scope and purpose

This document is a design guide for a fixed-frequency Flyback converter using Infineon’s newest fifth-generation fixed-frequency PWM controller, ICE5xSAG, and CoolSET™, ICE5xRxxxxAG, which offer high-efficiency, low-standby power with selectable entry and exit standby power options, wider $V_{cc}$ operating range with fast start-up, robust line protection with input Line Over Voltage Protection (LOVP), and various protection modes for a highly reliable system.

Intended audience

This document is intended for power-supply design/application engineers, students, etc. who wish to design power supplies with Infineon’s newest fifth-generation fixed-frequency PWM controller, ICE5xSAG, and CoolSET™, ICE5xRxxxxAG.

Table of contents

About this document ........................................................................................................................................... 1
Table of contents .................................................................................................................................................. 1
1 Abstract ......................................................................................................................................................... 3
2 Description ..................................................................................................................................................... 4
  2.1 List of features .............................................................................................................................................. 4
  2.2 Pin configuration and functionality ........................................................................................................... 4
3 Overview of fixed-frequency Flyback converter .......................................................................................... 6
4 Functional description and component design ............................................................................................ 8
  4.1 $V_{cc}$ pre-charging and typical $V_{cc}$ voltage during start-up ..................................................................... 8
  4.1.1 $V_{cc}$ capacitor ......................................................................................................................................... 9
  4.2 Soft-start ........................................................................................................................................................ 9
  4.3 Normal operation ......................................................................................................................................... 10
  4.3.1 PWM operation and peak current mode control .................................................................................... 10
  4.3.1.1 Switch-on determination .................................................................................................................. 10
  4.3.1.2 Switch-off determination .................................................................................................................. 10
  4.3.2 Current sensing ...................................................................................................................................... 11
  4.3.3 Frequency reduction ............................................................................................................................. 12
  4.3.4 Slope compensation ............................................................................................................................... 12
  4.3.5 Oscillator and frequency jittering ......................................................................................................... 13
  4.3.6 Modulated gate drive ............................................................................................................................ 14
  4.4 Peak Current Limitation (PCL) .................................................................................................................. 14
  4.4.1 Propagation delay compensation ......................................................................................................... 15
  4.5 ABM with selectable power level .............................................................................................................. 16
    4.5.1 Entering ABM operation ..................................................................................................................... 16
    4.5.2 During ABM operation ....................................................................................................................... 16
    4.5.3 Leaving ABM operation ...................................................................................................................... 17
    4.5.4 ABM configuration ............................................................................................................................ 18

Please read the Important Notice and Warnings at the end of this document

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5th Generation Fixed-Frequency Design Guide
Design Guide - ICE5xSAG and ICE5xRxxxxAG

Abstract

4.6 Non-isolated/isolated configuration ................................................................. 19
4.6.1 Non-isolated FB ......................................................................................... 19
4.6.2 Isolated FB ............................................................................................... 20
4.7 Protection functions ..................................................................................... 21
4.7.1 LOVP ........................................................................................................ 21
4.7.2 VCC OV/UV ............................................................................................ 22
4.7.3 Over-load/open-loop ................................................................................ 22
4.7.4 Over-temperature .................................................................................... 22
4.7.5 CS short-to-GND ..................................................................................... 22
4.7.6 VCC short-to-GND .................................................................................. 22
4.7.7 Protection modes ..................................................................................... 23

5 Typical application circuit .................................................................................. 25

6 PCB layout recommendation ............................................................................. 27

7 Output power of fifth-generation fixed-frequency ICs ........................................... 28

8 Fifth-generation fixed-frequency FLYCAL design example ............................... 32
8.1 Pre-calculation .............................................................................................. 32
8.2 Input diode bridge (BR1) .............................................................................. 33
8.3 Input capacitor (C1) ..................................................................................... 33
8.4 Transformer design (T1) .............................................................................. 35
8.5 Post calculation ............................................................................................ 37
8.6 Transformer winding design .......................................................................... 38
8.6.1 Primary winding ...................................................................................... 38
8.6.2 Secondary 1 winding (Vout1) ................................................................... 39
8.6.3 Secondary 2 winding (Vout2) ................................................................... 40
8.7 Clamping network ......................................................................................... 41
8.8 CS resistor .................................................................................................... 42
8.9 Output rectifier ............................................................................................. 42
8.9.1 Output 1 .................................................................................................. 42
8.9.2 Output 2 .................................................................................................. 43
8.10 VCC diode and capacitor ............................................................................ 44
8.11 Calculation of losses .................................................................................. 45
8.12 CoolSET™/MOSFET temperature ............................................................... 46
8.13 LOVP ........................................................................................................... 46
8.14 Output regulation (non-isolated) ................................................................. 47

9 References ....................................................................................................... 48

Revision history ................................................................................................... 49
Abstract

1 Abstract

This design guide for a fixed-frequency Flyback converter using Infineon’s newest fifth-generation fixed-frequency PWM controller, ICE5xSAG, and CoolSET™, ICE5xRxxxxAG.

The IC is optimized for off-line SMPS applications including home appliances/white goods, TVs, PCs, servers, Blu-ray players, set-top boxes and notebook adapters. The frequency reduction with soft gate-driving and frequency-jitter operation offers lower EMI and better efficiency between light and medium loads. The selectable entry/exit standby power Active Burst Mode (ABM) enables flexibility and low power consumption in standby mode with small and controllable output voltage ripple. The product has a wide operating range (10~25.5 V) of IC power supply and lower power consumption. The numerous protection functions with input LOVP give full protection to the power supply system in failure situations. All of these features make the ICE5xSAG/ICE5xRxxxxAG an outstanding PWM controller/CoolSET™ for fixed-frequency Flyback converters.
2 Description

2.1 List of features

- Integrated 700 V/800 V avalanche rugged CoolMOS™
- Enhanced ABM with selectable entry and exit standby power
- Digital frequency reduction for better overall system efficiency
- Fast start-up, achieved with cascode configuration
- Discontinuous Conduction Mode (DCM) and Continuous Conduction Mode (CCM) operation with slope compensation
- Frequency jitter and soft gate-driving for low EMI
- Built-in digital soft-start
- Cycle-to-cycle Peak Current Limitation (PCL)
- Integrated error amplifier to support direct feedback (FB) in a non-isolated Flyback converter
- Comprehensive protection with input LOVP, VCC OV, VCC Under Voltage (UV), over-load/open-loop, over-temperature and Current Sense (CS) short-to-GND
- All protections are in auto-restart mode
- Limited charging current for VCC Short-to-GND
- Pb-free lead plating, halogen-free mold compound, RoHS compliant

2.2 Pin configuration and functionality

The pin configuration is shown in Figure 1 and the functions are described in Table 1.
## Pin Definitions and Functions

<table>
<thead>
<tr>
<th>Pin</th>
<th>Symbol</th>
<th>Function</th>
</tr>
</thead>
</table>
| 1   | VIN    | Input LOVP
The VIN pin is connected to the bus via a resistor divider (see Figure 2) to sense the line voltage. Internally, it is connected to the LOV comparator, which will stop the switching when a LOVP condition occurs. To disable LOVP, connect this pin to GND. |
| 2   | VERR   | Error amplifier
The VERR pin is internally connected to the transconductance error amplifier for non-isolated Flyback applications. Connect this pin to GND for isolated Flyback applications. |
| 3   | FB     | FB and ABM entry/exit control
The FB pin combines the functions of FB control, selectable burst entry/exit control and over-load/open-loop protection. |
| 4   | CS     | CS
The CS pin is connected to the shunt resistor for the primary current sensing externally and to the PWM signal generator block for switch-off determination (together with the FB voltage) internally. CS short-to-GND protection is also sensed via this pin. |
| 5   | SOURCE | Source
The SOURCE pin is connected to the source of the external power MOSFET (see Figure 2), which is in series with the internal low-side MOSFET and internal $V_{CC}$ diode D. |
| 6, 7, 8 | DRAIN | Drain (drain of integrated CoolMOS™)
The DRAIN pin is connected to the drain of the integrated CoolMOS™. |
| 9   | NC     | No connection |
| 10  | GATE   | Gate driver output
The GATE pin is connected to the gate of the power MOSFET, and a pull-up resistor is connected from the bus voltage to turn on the power MOSFET for charging up the $V_{CC}$ capacitor during start-up. |
| 11  | $V_{CC}$ | $V_{CC}$ (positive voltage supply)
The $V_{CC}$ pin is the positive voltage supply to the IC. The operating range is between $V_{CC, OFF}$ and $V_{CC, OVP}$. |
| 12  | GND    | Ground
The GND pin is the common ground of the controller. |
3 Overview of fixed-frequency Flyback converter

Figure 2 and Figure 3 show the typical application of ICE5xSAG and ICE5xRxxxxAG in an isolated fixed-frequency Flyback converter using TL431 and an optocoupler.

Figure 4 and Figure 5 show the typical application of ICE5xSAG and ICE5xRxxxxAG in a non-isolated fixed-frequency Flyback converter using an integrated error amplifier.

![Figure 2](image1.png)

**Figure 2** Typical application of the PWM controller in an isolated fixed-frequency Flyback converter using TL431 and an optocoupler

![Figure 3](image2.png)

**Figure 3** Typical application of the CoolSET™ in an isolated fixed-frequency Flyback converter using TL431 and an optocoupler
Overview of fixed-frequency Flyback converter

Figure 4  Typical application of the PWM controller in a non-isolated Flyback converter using an integrated error amplifier

Figure 5  Typical application of the CoolSET™ in a non-isolated Flyback converter using an integrated error amplifier
4 Functional description and component design

4.1 \( V_{CC} \) pre-charging and typical \( V_{CC} \) voltage during start-up

When AC-line input voltage is applied, a rectified voltage appears across the capacitor \( C_{bus} \) (see Figure 2). The pull-up resistor \( R_{\text{StartUp}} \) provides a current to charge the \( C_{\text{iss}} \) (input capacitance) of the power MOSFET, generating one voltage level. If the voltage across \( C_{\text{iss}} \) is sufficiently high, the power MOSFET will turn on and the \( V_{CC} \) capacitor will be charged through primary inductance of transformer \( L_p \), the power MOSFET and the internal diode with two steps of constant current source \( I_{VCC, \text{Charge1}} \) and \( I_{VCC, \text{Charge3}} \).

A very small constant current source (\( I_{VCC, \text{Charge1}} \)) charges the \( V_{CC} \) capacitor until \( V_{CC} \) reaches \( V_{CC, \text{SCP}} \) to protect the controller from a \( V_{CC} \) pin short-to-GND during start-up. After this, the second step constant current source (\( I_{VCC, \text{Charge3}} \)) is provided to further charge the \( V_{CC} \) capacitor, until \( V_{CC} \) exceeds the turn-on threshold \( V_{CC, \text{ON}} \). As shown in Phase I in Figure 6, the \( V_{CC} \) voltage increases almost linearly, with two steps.

**Note:** The recommended typical value for \( R_{\text{StartUp}} \) is 50 M\( \Omega \) (20 M\( \Omega \)~100 M\( \Omega \)). \( R_{\text{StartUp}} \) value is directly proportional to \( t_{\text{StartUp}} \) and inversely proportional to no-load standby power.

![Figure 6 \( V_{CC} \) voltage and current at start-up](image)

The time taken for the \( V_{CC} \) pre-charging can then be approximated as:

\[
 t_{\text{StartUp}} = t_A + t_B = \frac{V_{CC, \text{SCP}} \cdot G_{VCC}}{I_{VCC, \text{Charge1}}} + \left( \frac{V_{CC, \text{ON}} - V_{CC, \text{SCP}}}{I_{VCC, \text{Charge3}}} \right) \cdot G_{VCC} \tag{Eq 201}
\]

\( I_{VCC, \text{Charge2/3}} \) is charging current from the controller to the \( V_{CC} \) capacitor during start-up.
Functional description and component design

where $V_{VCC,SCP}$ : VCC short-circuit protection voltage
$C_{VCC}$ : VCC capacitor
$V_{VCC,ON}$ : VCC turn-on threshold voltage
$I_{VCC,charge1}$ : VCC charge current 1
$I_{VCC,charge3}$ : VCC charge current 3

When the VCC voltage exceeds the $V_{VCC,ON}$ at time $t_1$, the IC begins to operate with a soft-start. Due to power consumption of the IC and the fact that there is still no energy from the auxiliary winding to charge the VCC capacitor before the output voltage is built up, the VCC voltage drops (Phase II). Once the output voltage rises close to regulation, the auxiliary winding starts to charge the VCC capacitor from the time $t_2$ onward, delivering the power to the IC. The VCC will then reach a constant value depending on output load.

### 4.1.1 VCC capacitor

Since there is a VCC UV protection, the VCC capacitor should be selected to be large enough to ensure that enough energy is stored in the VCC capacitor so that the VCC voltage will not drop below the VCC UV protection threshold $V_{VCC,OFF}$ before the auxiliary power kicks in. Therefore, the minimum capacitance should fulfill the following requirement:

$$C_{VCC} > \frac{I_{VCC,charge3} \times t_{ss}}{V_{VCC,ON} - V_{VCC,OFF}} \quad (Eq \ 202)$$

where $C_{VCC}$ : VCC capacitor
$I_{VCC,charge3}$ : VCC charge current 3
$t_{ss}$ : soft-start time

During ABM condition where the auxiliary winding cannot provide enough power to supply the IC because of the burst switching, the VCC voltage may drop below the $V_{VCC,OFF}$. Therefore the capacitance needs to be increased, as the calculation above may not be enough.

### 4.2 Soft-start

After the supply voltage of the IC exceeds 16 V, which corresponds to $t_1$ of Figure 6, the IC starts switching with a soft-start. The soft-start implemented is a digital time-based function. The preset soft-start time is $t_{ss}$ (12 ms) with four steps (see Figure 7). If not limited by other functions, the peak voltage on the CS pin will increase incrementally from 0.3 V to $V_{CS,N}$ (0.8 V). The normal FB loop will take over the control when the output voltage reaches its regulated value.
4.3 Normal operation

During normal operation the PWM controller consists of a digital signal processing circuit, including regulation control, and an analog circuit, including a current measurement unit and a comparator. Details of normal operation are illustrated in the following paragraphs.

4.3.1 PWM operation and peak current mode control

4.3.1.1 Switch-on determination

The power MOSFET turn-on is synchronized with the internal oscillator, with a switching frequency $f_{sw}$ that corresponds to the voltage level $V_{FB}$ (see Figure 10).

4.3.1.2 Switch-off determination

In peak current mode control, the PWM comparator monitors voltage $V_1$ (see Figure 8), which is the representation of the instantaneous current of the power MOSFET. When $V_1$ exceeds $V_{fb}$, the PWM comparator sends a signal to switch off the gate of the power MOSFET. Therefore, the peak current of the power MOSFET is controlled by the FB voltage $V_{FB}$ (see Error! Reference source not found.).
At switch-on transient of the power MOSFET, a voltage spike across \( R_{CS} \) can cause \( V_1 \) to increase and exceed \( V_{FB} \). To avoid a false switch-off, the IC has a blanking time \( t_{CS,\text{LEB}} \) before detecting the voltage across \( R_{CS} \) to mask the voltage spike. Therefore, the minimum turn-on time of the power MOSFET is \( t_{CS,\text{LEB}} \).

If the voltage level at \( V_1 \) takes a long time to exceed \( V_{FB} \), the IC will implement a maximum duty cycle control to force the power MOSFET to switch off when \( D_{MAX} = 0.75 \).

---

**Figure 9** PWM

### 4.3.2 Current sensing

The power MOSFET current generates a voltage \( V_{CS} \) across the CS resistor \( R_{CS} \) connected between the CS pin and the GND pin. \( V_{CS} \) is amplified with gain \( G_{PWM} \), then added with an offset \( V_{PWM} \) to become \( V_1 \), as described below.

\[
V_{CS} = I_D \times R_{CS} \quad \text{(Eq 203)}
\]

\[
V_1 = V_{CS} \times G_{PWM} + V_{PWM} \quad \text{(Eq 204)}
\]

where

- \( V_{CS} \): CS pin voltage
- \( I_D \): power MOSFET current
- \( R_{CS} \): resistance of the CS resistor
- \( V_1 \): voltage level compared to \( V_{FB} \) as described in section 4.3.1.2
- \( G_{PWM} \): PWM-OP gain
- \( V_{PWM} \): offset for voltage ramp
4.3.3 Frequency reduction

Frequency reduction is implemented to achieve better efficiency at light load. At light load, the reduced switching frequency $f_{\text{SW}}$ improves efficiency by reducing the switching losses.

When load decreases, $V_{\text{FB}}$ decreases as well. $f_{\text{SW}}$ is dependent on the $V_{\text{FB}}$ as shown in Figure 10. Therefore, $f_{\text{SW}}$ decreases as the load decreases.

Typically, $f_{\text{SW}}$ at high load is 100 kHz/125 kHz and starts to decrease at $V_{\text{FB}} = 1.7$ V. There is no further frequency reduction once it reaches the $f_{\text{OSC},\text{MIN}}$ even the load is further reduced.

![Frequency reduction curve](image)

**Figure 10** Frequency reduction curve

4.3.4 Slope compensation

In CCM operation, a duty cycle greater than 50 percent may generate a sub-harmonic oscillation. A small perturbation on the transformer flux $\varphi$ can result in loop instability where the system cannot auto-correct itself, as can be seen in the figure below right, where $\Delta \varphi_2$ is greater than $\Delta \varphi_1$. $\Delta \varphi_2$ should be less than $\Delta \varphi_1$ for a system to be stable (figure below left). DCM operation is more stable, as the transformer flux always goes to zero.

![Slope compensation](image)
ICE5xSAG/ICE5xRxxxxAG can operate in CCM. To avoid the sub-harmonic oscillation, slope compensation is added to $V_{CS}$ when the gate of the power MOSFET is turned on for more than 40 percent of the switching cycle period. The relationship between $V_{FB}$ and the $V_{CS}$ for CCM operation is described in the equation below:

$$V_{FB} = V_{CS} \cdot G_{PWM} + V_{PWM} + M_{COMP} \cdot (T_{ON} - 40\% \cdot T_{PERIOD})$$  \hspace{1cm} (Eq 205)

where $T_{ON}$ : gate turn-on time of the power MOSFET

$M_{COMP}$ : slope compensation rate

$T_{PERIOD}$ : switching cycle period

As a result of slope compensation, $\Delta \varphi_2$ is reduced to smaller than $\Delta \varphi_1$, and therefore the system is able to stabilize itself as shown in the figure below.

The slope compensation circuit is disabled and no slope compensation is added to the $V_{CS}$ pin during ABM to save on power consumption.

### 4.3.5 Oscillator and frequency jittering

The oscillator generates a frequency of 100 kHz/125 kHz with frequency jittering of ±4 percent at a jittering period of $T_{JITTER}$ (4 ms). The frequency jittering helps to reduce conducted EMI.

A capacitor, current source and current sink which determine the frequency are integrated. The charging and discharging current of the implemented oscillator capacitor are internally trimmed in order to achieve a highly accurate switching frequency.

Once the soft-start period is over and when the IC goes into normal operating mode, the frequency jittering is enabled. There is also frequency jittering during frequency reduction.
4.3.6 Modulated gate drive

The drive stage is optimized for EMI consideration. The switch-on speed is slowed down before it reaches the power MOSFET turn-on threshold. There is a slope control on the rising edge at the output of the driver (see Figure 13). In this way the leading switch spike during turn-on is minimized.

The gate drive is 10 V (V_{GATE, HIGH}), which is good enough for most of the available power MOSFETs. For a 1 nF load capacitance, the typical values of rise time and fall time are 117 ns and 27 ns respectively.

A gate resistor can be used to adjust the switch-on speed of the MOSFET. To speed up the switch-off, the gate resistor can be anti-parallelled with an ultrafast diode. To avoid the gate-drive oscillation on the power MOSFET, it is recommended to minimize the PCB loop. These suggestions are not applicable to CoolSET™, as the power MOSFET is already integrated with the controller and adjusted for optimized operation.

![Figure 13 Gate – rising waveform](image-url)

Attention: Do not add a gate discharge resistor on the gate of the power MOSFET or the GATE pin in ICE5xSAG/ICE5xRxxxxAG applications. The discharge resistor together with the R_{StartUp} forms a voltage divider. With the high ratio of the resistance of R_{StartUp} with discharge resistor, the gate voltage of the power MOSFET may not be enough turn it on and charge the V_C to exceed V_{CC, ON}. Similarly, connecting a voltage probe on the GATE pin even with CoolSET™ may result in a non-start-up or a longer start-up time, depending on the probe resistance.

4.4 Peak Current Limitation (PCL)

There is a cycle-by-cycle Peak Current Limitation (PCL) realized by the current limit comparator to provide primary Over Current Protection (OCP). The primary current generates a voltage V_{CS} across the CS resistor R_{CS} connected between the CS pin and the GND pin. If the voltage V_{CS} exceeds an internal voltage limit V_{CS,N}, the comparator immediately turns off the gate drive.

The primary peak current I_{PEAK_PRI} can be calculated as below:

\[ I_{PEAK_PRI} = \frac{V_{CS,N}}{R_{CS}} \]  \hspace{1cm} (Eq 206)

where
- \( I_{PEAK_PRI} \) : maximum peak current in the primary
- \( V_{CS,N} \) : threshold voltage for the PCL
- \( R_{CS} \) : resistance of the CS resistor

To avoid mis-triggering caused by MOSFET switch-on transient voltage spikes, a Leading Edge Blanking (LEB) time (t_{CS_LEB}) is integrated into the current sensing path.
Functional description and component design

Note: In case of high switch-on noise at the CS pin, the IC may switch off immediately after the LEB time, especially at light-load high-line conditions. To avoid this, a noise-filtering ceramic capacitor (e.g. 100 pF–100 nF) can be added across the CS pin and the GND pin.

4.4.1 Propagation delay compensation

In case of OC detection, there is always a propagation delay from sensing the $V_{CS}$ to switching off the power MOSFET. An overshoot on the peak current $I_{peak}$ caused by the delay depends on the ratio of $dI/dt$ of the primary current (see Figure 14).

![Figure 14 Current limiting](image)

The overshoot of Signal2 is larger than Signal1 due to the steeper rising waveform. This change in the slope depends on the AC input voltage. Propagation delay compensation is integrated to reduce the overshoot due to $dI/dt$ of the rising primary current. Thus the propagation delay time between exceeding the CS threshold $V_{CS,N}$ and the switching off of the power MOSFET is compensated over a wide bus voltage range. Current limiting becomes more accurate, which will result in a minimum difference of over-load protection triggering power between low and high AC-line input voltage.

Under CCM operation, the same $V_{CS}$ does not result in the same power. In order to achieve a close over-load triggering level for CCM, ICE5xSAG/ICE5xRxxxxAG has implemented a two-curve compensation, as shown in Figure 15. One of the curves is used for $T_{ON}$ greater than 0.40 duty cycle and the other is for $T_{ON}$ lower than 0.40 duty cycle.

![Figure 15 Dynamic voltage threshold $V_{CS,N}$](image)
Similarly, the same concept of propagation delay compensation is also implemented in ABM at a reduced level. With this implementation, the entry and exit burst mode power can remain close between low and high AC-line input voltage.

4.5 ABM with selectable power level

At light load, the IC enters ABM operation to minimize power consumption. Details of ABM operation are explained in the following paragraphs.

4.5.1 Entering ABM operation

The system will enter ABM operation when two conditions are met:

- the FB voltage is lower than the threshold of $V_{FB,EBLP}/V_{FB,EBHP}$ depending on burst configuration option set-up;
- and a certain blanking time $t_{FB,BEB}$.

Once both of these conditions are fulfilled, the ABM flip-flop is set and the controller enters ABM operation. This dual-condition determination for entering ABM operation prevents mis-triggering of ABM, so that the controller enters ABM operation only when the output power is really low.

The threshold power to enter burst mode can be determined using the equation below.

$$P_{enter, burst} = \frac{1}{2} \cdot L_p \cdot f_{OSC,MIN} \cdot \left(\frac{V_{FB,EBXP} - V_{PWM}}{R_{CS} \cdot G_{PWM}}\right)^2$$

(Eq 207)

where $L_p$ : primary inductance
$f_{OSC,MIN}$ : minimum switching frequency
$V_{FB,EBP}$ : $V_{FB}$ entering ABM

The burst power as a ratio to the maximum input power $P_{IN,Max}$ can be expressed in the equation below.

$$\frac{P_{enter, burst}}{P_{IN,Max}} = f_{OSC,MIN} \cdot \left(\frac{V_{FB,EBXP} - V_{PWM}}{V_{CS,N} \cdot G_{PWM}}\right)^2$$

(Eq 208)

4.5.2 During ABM operation

After entering ABM, the PWM section will be inactive, making the $V_{OUT}$ start to decrease. As the $V_{OUT}$ decreases, $V_{FB}$ rises. Once $V_{FB}$ exceeds $V_{FB,BOH}$, the internal circuit is again activated by the internal bias to start the switching.

If the PWM is still operating and the output load is still low, $V_{OUT}$ increases and the $V_{FB}$ signal starts to decrease. When $V_{FB}$ reaches the low threshold $V_{FB,BOH}$, the internal bias is reset again and the PWM section is disabled, with no switching until $V_{FB}$ increases and once again exceeds the $V_{FB,BOH}$ threshold.

In ABM, $V_{FB}$ is like a sawtooth waveform swinging between $V_{FB,BOH}$ and $V_{FB,BOH}$, as shown in Figure 16.

During ABM, the switching frequency $f_{OSC,ABM}$ is 83 kHz for the 100 kHz version and 103 kHz for the 125 kHz version of the IC. The peak current $I_{PEAK,ABM}$ of the power MOSFET is defined by:

$$I_{PEAK,ABM} = \frac{V_{CS,BXP}}{R_{CS}}$$

(Eq 209)

where $V_{CS,BXP}$ is the PCL in ABM.
4.5.3 Leaving ABM operation

The FB voltage immediately increases if there is a sudden increase in the output load. When $V_{FB}$ exceeds $V_{FB, LB}$, it will leave ABM and the PCL threshold voltage will return back to $V_{CS, N}$ immediately.

The power on leaving ABM can be determined using the equation below.

$$P_{\text{leave burst}} = \frac{1}{2} \cdot L_p \cdot f_{OSC, ABM} \cdot \left( \frac{V_{CS, BP}}{R_{CS}} \right)^2$$

(Eq 2.10)

where $f_{OSC, ABM}$ : ABM switching frequency

$V_{CS, BP}$ : PCL in ABM

Therefore, the ratio of the power on leaving ABM to maximum input power can be determined using the equation below.

$$\frac{P_{\text{leave burst}}}{P_{IN, Max}} = \frac{f_{OSC, ABM}}{f_{OSC}} \cdot \left( \frac{V_{CS, BP}}{V_{CS, N}} \right)^2$$

(Eq 2.11)
4.5.4 ABM configuration

The burst mode entry level can be selected by changing the resistance $R_{\text{Sel}}$ at the FB pin. There are three configuration options depending on $R_{\text{Sel}}$, which corresponds to the options of no ABM (Option 1), low range of ABM power (Option 2) and high range of ABM power (Option 3). The table below shows the control logic for the entry and exit levels with the FB voltage.
Table 2  ABM configuration option set-up

<table>
<thead>
<tr>
<th>Option</th>
<th>( R_{\text{Sel}} )</th>
<th>( V_{\text{FB}} )</th>
<th>( V_{\text{CS,BxP}} )</th>
<th>Entry level</th>
<th>Exit level</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>( V_{\text{FB,EbXP}} )</td>
<td>( V_{\text{FB,lb}} )</td>
</tr>
<tr>
<td>1</td>
<td>&lt; 470 k( \Omega )</td>
<td>( V_{\text{FB}} &lt; V_{\text{FB,P_Bias1}} )</td>
<td>–</td>
<td>–</td>
<td>No ABM</td>
</tr>
<tr>
<td>2</td>
<td>720~790 k( \Omega )</td>
<td>( V_{\text{FB,P_Bias1}} &lt; V_{\text{FB}} &lt; V_{\text{FB,P_Bias2}} )</td>
<td>0.22 V</td>
<td>0.93 V</td>
<td>–3 %</td>
</tr>
<tr>
<td>3 (default)</td>
<td>&gt; 1210 k( \Omega )</td>
<td>( V_{\text{FB}} &gt; V_{\text{FB,P_Bias2}} )</td>
<td>0.27 V</td>
<td>1.03 V</td>
<td>~4.5 %</td>
</tr>
</tbody>
</table>

\( P_{\text{IN,Max}} \) is the input power before the over-load protection is triggered.

During start-up of the IC, the controller pressets the ABM selection to Option 3, the FB resistor (\( R_{\text{fb}} \)) is turned off by internal switch S2 (see Figure 17) and a current source \( I_{\text{sel}} \) is turned on instead. From \( V_{\text{CC}} = 4.44 \) V to the \( V_{\text{CC}} \) on-threshold, the FB pin will start to charge resistor \( R_{\text{Sel}} \) with current \( I_{\text{sel}} \) to a certain voltage level. When \( V_{\text{CC}} \) reaches the \( V_{\text{CC}} \) on-threshold, the FB voltage is sensed. The burst mode option is then chosen according to the FB voltage level. After finishing the selection, any change on the FB level will not change the burst mode option, and the current source \( (I_{\text{sel}}) \) is turned off while the FB resistor \( (R_{\text{fb}}) \) is connected back to the circuit.

Figure 17  ABM detect and adjust

4.6  Non-isolated/isolated configuration

ICE5xSAG/ICE5xRxxxxAG has a VERR pin, which is connected to the input of an integrated error amplifier to support non-isolated Flyback application (see Figure 4 and Figure 5). When the \( V_{\text{CC}} \) is charging and before reaching the \( V_{\text{CC}} \) on-threshold, a current source \( I_{\text{ERR_P_Bias}} \) from the VERR pin together with \( R_{\text{F1}} \) and \( R_{\text{F2}} \) will generate a voltage across it. If the VERR voltage is more than \( V_{\text{ERR_P_Bias}} \) (0.2 V), non-isolated configuration is selected; otherwise, isolated configuration is selected. In isolated configuration, the error amplifier output is disconnected from the FB pin.

Connect the VERR pin to GND if an error amplifier is not used or if isolated configuration is selected.

4.6.1  Non-isolated FB

In case of non-isolated configuration (refer to Figure 4 and Figure 5), the voltage divider \( R_{\text{f1}} \) and \( R_{\text{f2}} \) is used to sense the output voltage and compared with the internal reference voltage \( V_{\text{ERR_REF}} \). The difference between the sensed voltage and the reference voltage is converted as an output current by the error amplifier. The output
current will charge/discharge the resistor and capacitor network connected at the FB pin for the loop compensation.

To properly detect a non-isolated configuration, the minimum resistance for the parallel combination of resistors $R_{F1}$ and $R_{F2}$ is calculated below:

$$R_{F1//F2} \geq \frac{V_{ERR.P.BIAS_{max}}}{I_{ERR.P.BIAS_{min}}} = \frac{0.24V}{9.5\mu A} = 25.3 \, k\Omega \quad (Eq \ 212)$$

where $R_{F1//F2}$ : parallel combination of $R_{F1}$ and $R_{F2}$

$V_{ERR.P.BIAS_{max}}$ : maximum voltage for error amplifier mode

$I_{ERR.P.BIAS_{min}}$ : minimum bias current for error amplifier mode

The output voltage $V_{P1}$ (see Figure 4) is set by $R_{F1}$ and $R_{F2}$ using the equation below:

$$R_{F2} = R_{F1} \cdot \left( \frac{V_{P1}}{V_{ERR.REF}} - 1 \right) \quad (Eq \ 213)$$

where $R_{F1}$ and $R_{F2}$ : voltage divider resistors

$V_{P1}$ : output voltage

$V_{ERR.REF}$ : error amplifier reference voltage

### 4.6.2 Isolated FB

In isolated configuration, the output is usually sensed by a TL431, and the output is fed to the FB pin by the optocoupler (see Figure 18). Inside the IC, the FB pin is connected to a $V_{ref}$ 3.3 V reference voltage through an internal pull-up resistor $R_{FB}$. Outside the IC, this pin is connected to the collector of the optocoupler. Normally, a ceramic capacitor $C_{FB}$, e.g. 1 nF, can be placed between this pin and GND to filter out noise.

![FB circuit for isolated configuration](image)

The output voltage $V_{O1}$ (see Figure 18) is set by $R_{OVS1}$ and $R_{OVS2}$ using the equation below:

$$R_{OVS1} = R_{OVS2} \left( \frac{V_{O1}}{V_{REF.TL}} - 1 \right) \quad (Eq \ 214)$$
Functional description and component design

where $R_{OVS_1}$ and $R_{OVS_2}$ : voltage divider resistors

$V_{O1}$ : output voltage

$V_{REF_TL}$ : TL431 reference voltage

4.7 Protection functions

The ICE5xSAG/ICE5xRxxxxAG provides numerous protection functions that considerably improve the power supply system robustness, safety and reliability. The following table summarizes these protection functions and the corresponding protection mode, whether non-switch auto-restart, auto-restart or odd-skip auto-restart. Refer to Figure 19, Figure 20 and Figure 21 for the waveform illustration of the protection modes.

<table>
<thead>
<tr>
<th>Protection functions</th>
<th>Normal mode</th>
<th>Burst mode</th>
<th>Protection mode</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Burst ON</td>
<td>Burst OFF</td>
</tr>
<tr>
<td>LOVP</td>
<td>√</td>
<td>√</td>
<td>√</td>
</tr>
<tr>
<td>$V_{CC} OV$</td>
<td>√</td>
<td>√</td>
<td>NA</td>
</tr>
<tr>
<td>$V_{CC} UV$</td>
<td>√</td>
<td>√</td>
<td>√</td>
</tr>
<tr>
<td>Over-load/open-loop</td>
<td>√</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>Over-temperature</td>
<td>√</td>
<td>√</td>
<td>√</td>
</tr>
<tr>
<td>CS short-to-GND</td>
<td>√</td>
<td>√</td>
<td>NA</td>
</tr>
<tr>
<td>$V_{CC}$ short to GND short-to-GND</td>
<td>√</td>
<td>√</td>
<td>√</td>
</tr>
</tbody>
</table>

4.7.1 LOVP

The input LOVP is detected by sensing the bus capacitor voltage through the VIN pin via voltage divider resistors $R_1$ and $R_2$ (Figure 2). Once the $V_{VIN}$ voltage is higher than the LOV threshold ($V_{VIN,LOVP}$), the controller enters protection mode until $V_{VIN}$ is lower than $V_{VIN,LOVP}$. This protection can be disabled by connecting the VIN pin to GND.

During LOVP, there is no MOSFET switching and $V_{VIN}$ is always monitored in every restart cycle. The sensing resistors (see Figure 2, Figure 3, Figure 4 and Figure 5) $R_{i1}$ and $R_{i2}$ can be calculated as in the equation below.

$$R_{i2} = \frac{R_{i1} \times V_{VIN,LOVP}}{(V_{LINE,OVP,AC} \times \sqrt{2}) - V_{VIN,LOVP}} \quad (Eq \ 215)$$

where

$R_{i1}$ : high-side line input sensing resistor (typ. 9 MΩ)

$R_{i2}$ : low-side line input sensing resistor

$V_{VIN,LOVP}$ : LOV threshold (typ. 2.85 V)

$V_{LINE,OVP,AC}$ : user-defined LOV ($V_{AC}$) for the system

1 Not applicable
4.7.2 VCC OV/UV

During operation, the VCC voltage is continuously monitored. If VCC is either below \( V_{CC_{OFF}} \) for 50 µs (\( t_{VCC_{OFF,B}} \)) or above \( V_{CC_{OVP}} \) for 55 µs (\( t_{VCC_{OVP,B}} \)), the power MOSFET is kept switched off. After the VCC voltage falls below the threshold \( V_{CC_{OFF}} \), the new start-up sequence is activated. The VCC capacitor is then charged up. Once the voltage exceeds the threshold \( V_{CC_{ON}} \), the IC begins to operate with a new soft-start.

4.7.3 Over-load/open-loop

In case of open control-loop or output over-load, the FB voltage will be pulled up. When \( V_{FB} \) exceeds \( V_{FB_{OLP}} \) after a blanking time of \( t_{FB_{OLP,B}} \), the IC enters odd-skip auto-restart mode. The blanking time enables the converter to provide peak power in case the increase in \( V_{FB} \) is due to a sudden load increase.

4.7.4 Over-temperature

If the junction temperature of the controller exceeds \( T_{J_{ON,OTP}} \), the IC enters Over Temperature Protection (OTP) in auto-restart mode. The IC is also implemented with a 40°C hysteresis. That means the IC can only be recovered from OTP when the controller junction temperature drops 40°C lower than the OTP trigger point.

4.7.5 CS short-to-GND

If the voltage at the CS pin is lower than the preset threshold \( V_{CS_{STG}} \) with a certain blanking time \( t_{CS_{STG,B}} \) for three consecutive pulses during the on-time of the power switch, the IC enters CS short-to-GND protection.

When CS pin is shorted to GND, the Drain peak current \( I_D \) will depend on bus voltage and transformer primary inductance. IC may be damaged if the Drain peak current exceeds the maximum Pulse drain current limit \( I_{D_{Pulse}} \) for CoolSET™ or maximum Single pulse source current at SOURCE pin \( I_{S_{pulse}} \) for standalone under the Absolute Maximum Ratings in datasheet before the CS short-to-GND protection is triggered.

4.7.6 VCC short-to-GND

To limit the power dissipation of the start-up circuit at VCC short-to-GND, the VCC charging current is limited to a minimum level of \( I_{VCC_{Charge1}} \). With such low current, the power loss of the IC is limited to prevent over-heating.
4.7.7 Protection modes

All the protections are in auto-restart mode with a new soft-start sequence. The three auto-restart modes are illustrated in the following figures.

Figure 19  Non-switch auto-restart mode

Figure 20  Auto-restart mode
Functional description and component design

Figure 21  Odd-skip auto-restart
5 Typical application circuit

A 60 W single-output demo board with ICE5GSAG and 14.5 W demo board with ICE5AR4770AG are shown below.

Figure 22  Schematic of DEMO_5GSAG_60W1
Figure 23  Schematic of DEMO_5AR4770AG_14W1
6 PCB layout recommendation

In an SMPS, the PCB layout is crucial to a successful design. Below are some recommendations (see Figure 22).

1. Minimize the loop with pulse share current or voltage; examples are the loop formed by the bus voltage source, primary winding, main power switch (Q1 in the controller or power switch CoolMOS™ inside the CoolSET™) and CS resistor or the loop consisting of the secondary winding, output diode and output capacitor, or the loop of the Vcc power supply.

2. Star the ground at the bulk capacitor C1: all primary grounds should be connected to the ground of the bulk capacitor C1 separately at one point. This can reduce the switching noise entering the sensitive pins of the CoolSET™ device. The primary star ground can be split into four groups as follows:
   i. Combine signal (all small-signal grounds connecting to the controller/CoolSET™ GND pin such as the filter capacitor ground C4, C5, C11 and optocoupler ground) and power ground (CS resistor R10A and R10B).
   ii. Vcc ground includes the Vcc capacitor C3 ground and the auxiliary winding ground, pin 2 of the power transformer.
   iii. EMI return ground includes the Y capacitor CY1.
   iv. DC ground from the bridge rectifier BR1.

3. Place the filter capacitor close to the controller ground: filter capacitors C4, C5 and C11 should be placed as close to the controller ground and the controller pin as possible so as to reduce the switching noise coupled into the controller.

4. HV traces clearance: HV traces should maintain sufficient spacing to the nearby traces. Otherwise, arcing could occur.
   i. 400 V traces (positive rail of bulk capacitor C1) to nearby traces: > 2.0 mm
   ii. 700/800 V traces (drain pin of power switch (Q1 in the controller and DRAIN pin of CoolSET™ IC1 [see Figure 23]) to nearby traces: > 3 mm

5. Recommended minimum of 232 mm² copper area at the DRAIN pin to add to the PCB for better thermal performance of the CoolSET™.
7 Output power of fifth-generation fixed-frequency ICs

Table 4 Output power of fifth-generation fixed-frequency controller

<table>
<thead>
<tr>
<th>Type</th>
<th>Package</th>
<th>Marking</th>
<th>( F_{sw} )</th>
<th>( V_{DS} )</th>
<th>( R_{DSon} )</th>
<th>( 220 , \text{V AC \pm 20%} ) at DCM (^2)</th>
<th>( 85–300 , \text{V AC} ) at DCM (^2)</th>
<th>( 85–300 , \text{V AC} ) at CCM (^2)</th>
</tr>
</thead>
<tbody>
<tr>
<td>ICE5ASAG</td>
<td>PG-DSO-8</td>
<td>SASAG</td>
<td>100 kHz</td>
<td>108 W</td>
<td>60 W</td>
<td>66 W</td>
<td></td>
<td></td>
</tr>
<tr>
<td>ICE5GSAG</td>
<td>PG-DSO-8</td>
<td>S5SAG</td>
<td>125 kHz</td>
<td>108 W</td>
<td>60 W</td>
<td>66 W</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Table 5 Output power of fifth-generation fixed-frequency CoolSET™

<table>
<thead>
<tr>
<th>Type</th>
<th>Package</th>
<th>Marking</th>
<th>( V_{DS} )</th>
<th>( F_{sw} )</th>
<th>( R_{DSon} )</th>
<th>( 220 , \text{V AC \pm 20%} ) at DCM (^2)</th>
<th>( 85–300 , \text{V AC} ) at DCM (^2)</th>
<th>( 85–300 , \text{V AC} ) at CCM (^2)</th>
</tr>
</thead>
<tbody>
<tr>
<td>ICE5AR4770AG</td>
<td>PG-DSO-12</td>
<td>SAR4770AG</td>
<td>700 V</td>
<td>100 kHz</td>
<td>4.73 Ω</td>
<td>27 W</td>
<td>15 W</td>
<td>16 W</td>
</tr>
<tr>
<td>ICE5GR4780AG</td>
<td>PG-DSO-12</td>
<td>SGR4780AG</td>
<td>800 V</td>
<td>125 kHz</td>
<td>4.13 Ω</td>
<td>27.5 W</td>
<td>15 W</td>
<td>16 W</td>
</tr>
<tr>
<td>ICE5GR2280AG</td>
<td>PG-DSO-12</td>
<td>SGR2280AG</td>
<td>800 V</td>
<td>125 kHz</td>
<td>2.13 Ω</td>
<td>41 W</td>
<td>23 W</td>
<td>24 W</td>
</tr>
<tr>
<td>ICE5GR1680AG</td>
<td>PG-DSO-12</td>
<td>SGR1680AG</td>
<td>800 V</td>
<td>125 kHz</td>
<td>1.53 Ω</td>
<td>48 W</td>
<td>27 W</td>
<td>28 W</td>
</tr>
<tr>
<td>ICE5AR0680AG</td>
<td>PG-DSO-12</td>
<td>SAR0680AG</td>
<td>800 V</td>
<td>100 kHz</td>
<td>0.71 Ω</td>
<td>68 W</td>
<td>40 W</td>
<td>42 W</td>
</tr>
</tbody>
</table>

The calculated output power curves showing typical output power against ambient temperature are shown below. The curves are derived based on an open-frame design at \( T_a = 50°C \), \( T_J = 125°C \) (integrated HV MOSFET for CoolSET™), using the minimum pin copper area in a 2 oz copper single-sided PCB and steady-state operation only (no design margins for abnormal operation modes are included). The output power figure is for selection purposes only. The actual power can vary depending on the specific design.

---

1 Calculated maximum output power rating in an open-frame design at \( T_a = 50°C \), \( T_J = 125°C \) using minimum pin copper area in a 2 oz copper single-sided PCB. The output power figure is for selection purposes only. The actual power can vary depending on the particular design. Please contact a technical expert from Infineon for more information.

2 Typ. at \( T_J = 25°C \) (inclusive of low-side MOSFET)
Output power of fifth-generation fixed-frequency ICs

Figure 24  Output power curve of ICE5xSAG

Figure 25  Output power curve of ICE5AR4770AG
Figure 26  Output power curve of ICE5GR4780AG

Figure 27  Output power curve of ICE5GR2280AG
Output power of fifth-generation fixed-frequency ICs

**Figure 28**  Output power curve of ICE5GR1680AG

**Figure 29**  Output power curve of ICE5AR0680AG
Fifth-generation fixed-frequency FLYCAL design example

A design example of a 14.5 W 15 V 5 V fixed-frequency non-isolated DCM Flyback converter with ICE5AR4770AG is shown below.

Define input parameters:

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Minimum AC input voltage:</td>
<td>( V_{\text{ACMin}} ) 85 V AC</td>
</tr>
<tr>
<td>Maximum AC input voltage:</td>
<td>( V_{\text{ACMax}} ) 330 V AC</td>
</tr>
<tr>
<td>Line frequency:</td>
<td>( f_{\text{AC}} ) 60 Hz</td>
</tr>
<tr>
<td>Bulk capacitor DC ripple voltage:</td>
<td>( V_{\text{DCRipple}} ) 27 V</td>
</tr>
<tr>
<td>Output voltage 1:</td>
<td>( V_{\text{Out1}} ) 15 V</td>
</tr>
<tr>
<td>Output current 1:</td>
<td>( I_{\text{Out1}} ) 0.83 A</td>
</tr>
<tr>
<td>Forward voltage of output diode 2:</td>
<td>( V_{\text{FOut1}} ) 0.6 V</td>
</tr>
<tr>
<td>Output ripple voltage 1:</td>
<td>( V_{\text{OutRipple1}} ) 0.2 V</td>
</tr>
<tr>
<td>Output voltage 2:</td>
<td>( V_{\text{Out2}} ) 5 V</td>
</tr>
<tr>
<td>Output current 2:</td>
<td>( I_{\text{Out2}} ) 0.4 A</td>
</tr>
<tr>
<td>Forward voltage of output diode 2:</td>
<td>( V_{\text{FOut2}} ) 0.2 V</td>
</tr>
<tr>
<td>Output ripple voltage 2:</td>
<td>( V_{\text{OutRipple2}} ) 0.2 V</td>
</tr>
<tr>
<td>Maximum output power:</td>
<td>( P_{\text{OutMax}} ) 17 W</td>
</tr>
<tr>
<td>Minimum output power:</td>
<td>( P_{\text{OutMin}} ) 1 W</td>
</tr>
<tr>
<td>Efficiency at ( V_{\text{ACMin}} ) and ( P_{\text{OutMax}} ):</td>
<td>( \eta ) 83 %</td>
</tr>
<tr>
<td>Reflection voltage:</td>
<td>( V_{\text{RSET}} ) 97.5 V</td>
</tr>
<tr>
<td>( V_{\text{CC}} ) voltage:</td>
<td>( V_{\text{VCC}} ) 14 V</td>
</tr>
<tr>
<td>Forward voltage of ( V_{\text{CC}} ) diode (D2):</td>
<td>( V_{\text{FVCC}} ) 0.6 V</td>
</tr>
<tr>
<td>Fifth-generation FF CoolSET™:</td>
<td>CoolSET™ ICE5AR4770AG</td>
</tr>
<tr>
<td>Switching frequency:</td>
<td>( f_{s} ) 100 kHz</td>
</tr>
<tr>
<td>Breakdown voltage:</td>
<td>( V_{\text{DSMax}} ) 700 V</td>
</tr>
<tr>
<td>Drain-to-source capacitance of MOSFET (including ( C_{\text{oer}} ) of MOSFET):</td>
<td>( C_{\text{DS}} ) 7 pF</td>
</tr>
<tr>
<td>Effective output capacitance of MOSFET:</td>
<td>( C_{\text{oer}} ) 3.4 pF</td>
</tr>
<tr>
<td>Start-up resistor ( R_{\text{StartUp}} ) (R2A, R2B, R2C):</td>
<td>( R_{\text{StartUp}} ) 45 MΩ</td>
</tr>
<tr>
<td>Maximum ambient temperature:</td>
<td>( T_{a} ) 50 °C</td>
</tr>
</tbody>
</table>

8.1 Pre-calculation

Output power of output 1:

\[ P_{\text{Out1}} = V_{\text{Out1}} \cdot I_{\text{Out1}} \quad \text{(Eq 001)} \]

\[ P_{\text{Out1}} = 15V \cdot 0.83A = 12.45W \]

Output power of output 2:

\[ P_{\text{Out2}} = V_{\text{Out2}} \cdot I_{\text{Out2}} \quad \text{(Eq 002)} \]

\[ P_{\text{Out2}} = 5V \cdot 0.4A = 2W \]

Nominal output power:

\[ P_{\text{OutNom}} = P_{\text{Out1}} + P_{\text{Out2}} \quad \text{(Eq 003)} \]

\[ P_{\text{OutNom}} = 12.45W + 2W = 14.45W \]
Output power 1 load weight:

\[ K_{L1} = \frac{P_{Out1}}{P_{OutNom}} \]  \hspace{1cm} (Eq 004)  \hspace{1cm} K_{L1} = \frac{12.45W}{14.45W} = 0.86

Output power 2 load weight:

\[ K_{L2} = \frac{P_{Out2}}{P_{OutNom}} \]  \hspace{1cm} (Eq 005)  \hspace{1cm} K_{L1} = \frac{2W}{14.45W} = 0.14

Maximum input power:

\[ P_{InMax} = \frac{P_{OutMax}}{\eta} \]  \hspace{1cm} (Eq 006)  \hspace{1cm} P_{InMax} = \frac{17W}{0.83} = 20.48W

### 8.2 Input diode bridge (BR1)

Input RMS current:

\[ I_{ACRMS} = \frac{P_{InMax}}{V_{ACMin} \cdot \cos\varphi} \]  \hspace{1cm} (Eq 007)  \hspace{1cm} I_{ACRMS} = \frac{20.48W}{85V \cdot 0.6} = 0.402A

Maximum DC input voltage:

\[ V_{DC_{max}PK} = V_{ACMax} \cdot \sqrt{2} \]  \hspace{1cm} (Eq 008)  \hspace{1cm} V_{DC_{max}PK} = 330V \cdot \sqrt{2} = 466.7V

### 8.3 Input capacitor (C1)

Peak voltage at minimum AC input:

\[ V_{DC_{min}PK} = V_{AC_{min}} \cdot \sqrt{2} \]  \hspace{1cm} (Eq 009)  \hspace{1cm} V_{DC_{min}PK} = 85V \cdot \sqrt{2} = 120.2V

Minimum DC input voltage-based ripple voltage setting:

\[ V_{DC_{min}Set} = V_{DC_{min}PK} - V_{DC_{Ripple}} \]  \hspace{1cm} (Eq 010)  \hspace{1cm} V_{DC_{min}Set} = 120.2V - 27V = 93.2V

Discharging time at each half-line cycle:

\[ T_D = \frac{1}{4 \cdot f_{AC}} \cdot \left( \frac{\sin^{-1} \frac{V_{DC_{min}Set}}{V_{DC_{min}PK}}}{90} \right) \]  \hspace{1cm} (Eq 011)  \hspace{1cm} T_D = \frac{1}{4 \cdot 60Hz} \cdot \left( \frac{\sin^{-1} \frac{93.2V}{120.2V}}{90} \right) = 6.52ms

Required energy at discharging time of input capacitor:

\[ W_{INV} = P_{InMax} \cdot T_D \]  \hspace{1cm} (Eq 012)  \hspace{1cm} W_{INV} = 20.48W \cdot 6.52ms = 0.13W \cdot s

Calculated input capacitor:

\[ C_{INCal} = \frac{2 \cdot W_{INV}}{V_{DC_{min}PK}^2 - V_{DC_{max}Set}^2} \]  \hspace{1cm} (Eq 013)  \hspace{1cm} C_{INCal} = \frac{2 \cdot 0.13W \cdot s}{(120.2V)^2 - (93.2V)^2} = 46.35\mu F
Alternatively, a rule of thumb for estimating the input capacitor may be applied based on maximum input power, as shown below:

<table>
<thead>
<tr>
<th>Input voltage</th>
<th>Factor</th>
</tr>
</thead>
<tbody>
<tr>
<td>115 V AC</td>
<td>2 µF/W</td>
</tr>
<tr>
<td>230 V AC</td>
<td>1 µF/W</td>
</tr>
<tr>
<td>85–265 V AC</td>
<td>2–3 µF/W</td>
</tr>
</tbody>
</table>

Applying the rule of thumb using the 2 µF/W factor:

\[
C_{\text{IN Est.}} = P_{\text{IN Max}} \cdot \text{factor} \tag{Eq 014}
\]

Choose a capacitance greater than or equal to calculated (Eq 013) or estimated (Eq 014) value, whichever is greater. The voltage rating should be greater than or equal to the maximum DC input voltage.

Input capacitor \(C_{\text{IN}}\) | 47 µF/500 V

Recalculation after input capacitor selection:

\[
V_{\text{DC Min}} = \sqrt{\frac{V_{\text{DC Min PK}}^2 - 2 \cdot W_{\text{IN}}}{C_{\text{IN}}}} \tag{Eq 015}
\]

\[
V_{\text{DC Min}} = \sqrt{(120.2V)^2 - \frac{2 \cdot 0.13W \cdot s}{47 \mu F}} = 93.63V
\]

Note: Special requirements for hold-up time, including cycle skip/drop-out, or other factors which affect the resulting minimum DC input voltage and capacitor discharging time is not considered above.
8.4 Transformer design (T1)

Figure 30 Typical waveforms of DCM operation

Maximum duty cycle:

\[ D_{\text{Max}} = \frac{V_{\text{RSET}}}{V_{\text{RSET}} + V_{\text{DCMin}}} \]  
(Eq 016)  
\[ D_{\text{Max}} = \frac{97.5V}{97.5V + 93.63V} = 0.51 \]

Primary inductance:

\[ L_p = \frac{(V_{\text{DCMin}} \times D_{\text{Max}})^2}{2 \times P_{\text{InMax}} \times f_s \times K_{RF}} \]  
(Eq 017)  
\[ L_p = \frac{(93.63V \times 0.51)^2}{2 \times 20.48W \times 100kHz \times 1} = 556.7 \mu H \]

Primary average current during turn-on:

\[ I_{AV} = \frac{P_{\text{InMax}}}{V_{\text{DCMin}} \times D_{\text{Max}}} \]  
(Eq 018)  
\[ I_{AV} = \frac{20.48W}{93.63V \times 0.51} = 0.43A \]
Primary peak-to-peak current:
\[
\Delta I = \frac{V_{DC\min} \times D_{\text{Max}}}{L_p \times f_s}
\]  
(Eq 019)  
\[
\Delta I = \frac{93.63\, \text{V} \times 0.51}{556.7\, \mu\text{H} \times 100\, \text{kHz}} = 0.86\, \text{A}
\]

Primary peak current:
\[
I_{P\text{Max}} = I_{AV} + \frac{\Delta I}{2}
\]  
(Eq 020)  
\[
I_{P\text{Max}} = 0.43\, \text{A} + \frac{0.86\, \text{A}}{2} = 0.86\, \text{A}
\]

Primary valley current:
\[
I_{\text{Valley}} = I_{P\text{Max}} - \Delta I
\]  
(Eq 021)  
\[
I_{\text{Valley}} = 0.86\, \text{A} - 0.86\, \text{A} = 0\, \text{A}
\]

Primary RMS current:
\[
I_{P\text{RMS}} = \sqrt{\left[3 \times (I_{AV})^2 + \left(\frac{\Delta I}{2}\right)^2\right] \times D_{\text{Max}} / 3}
\]  
(Eq 022)  
\[
I_{P\text{RMS}} = \sqrt{\left[3 \times (0.43)^2 + \left(\frac{0.86\, \text{A}}{2}\right)^2\right] \times \frac{0.51}{3}} = 0.35\, \text{A}
\]

Choose core type and bobbin from magnetics suppliers that can support the required power. Maximum flux density, typically from 200 mT to 400 mT, depends on the type of ferrite material. Below is the selected transformer material:

- Core type: E 20/10/6
- Core material: N87
- Maximum flux density \(B_s\): 390 mT at 100°C
- Cross-sectional area \(A_c\): 32 mm²
- Bobbin width \(BW\): 11 mm
- Winding cross-section \(A_N\): 34 mm²
- Winding perimeter \(l_N\): 41.2 mm

Set maximum flux density \(B_{\text{MAX}}\) to 200 mT

Calculate minimum primary number of turns:
\[
N_{P\text{Cal}} \geq \frac{I_{P\text{Max}} \cdot L_p}{B_{\text{MAX}} \cdot A_c}
\]  
(Eq 023)  
\[
N_{P\text{Cal}} \geq \frac{0.86\, \text{A} \times 556.7\, \mu\text{H}}{200\, \text{mT} \times 32\, \text{mm}^2} = 74.6\, \text{Turns}
\]

Primary number of turns \(N_p\):
78 turns

Calculate secondary number of turns for \(V_{\text{Out1}}\):
\[
N_{S1\text{Cal}} = \frac{N_p \cdot \left(V_{\text{Out1}} + V_{F\text{Out1}}\right)}{V_R}
\]  
(Eq 024)  
\[
N_{S1\text{Cal}} = \frac{78\, \text{Turns} \times (15\, \text{V} + 0.6\, \text{V})}{97.5\, \text{V}} = 12.48\, \text{Turns}
\]

Secondary 1 number of turns \(N_{S1}\):
12 turns

Calculate secondary number of turns for \(V_{\text{Out2}}\):
\[
N_{S2\text{Cal}} = \frac{N_p \cdot \left(V_{\text{Out2}} + V_{F\text{Out2}}\right)}{V_R}
\]  
(Eq 025)  
\[
N_{S2\text{Cal}} = \frac{78\, \text{Turns} \times (5\, \text{V} + 0.2\, \text{V})}{97.5\, \text{V}} = 4.16\, \text{Turns}
\]

Secondary 2 number of turns \(N_{S2}\):
4 turns
Calculate number of turns for $V_{cc}$:

$$N_{VccCal} = \frac{N_p \cdot (V_{Vcc} + V_{FVcc})}{V_R} \quad \text{(Eq 026)}$$

Auxiliary number of turns $N_{Vcc}$:

$$N_{Vcc} = 11 \text{ turns}$$

Auxiliary supply voltage:

$$V_{VccCal} = (V_{Out1} + V_{FOut1}) \cdot N_p / N_{S1} - V_{FVcc} \quad \text{(Eq 027)}$$

$$V_{VccCal} = \frac{(15V + 0.6V) \cdot 11/12 - 0.6V}{97.5V} = 13.7V$$

8.5 Post calculation

Primary to secondary 1 turns ratio:

$$N_{PS1} = N_p / N_{S1} \quad \text{(Eq 028)}$$

$$N_{PS1} = 78\text{ turns}/12\text{ turns} = 6.5$$

Primary to secondary 2 turns ratio:

$$N_{PS2} = N_p / N_{S2} \quad \text{(Eq 029)}$$

$$N_{PS2} = 78\text{ turns}/4\text{ turns} = 19.5$$

Post-calculated reflected voltage:

$$V_{RPost} = (V_{Out1} + V_{FOut1}) \cdot N_p / N_{S1} \quad \text{(Eq 030)}$$

$$V_{RPost} = (15V + 0.6V) \cdot 78/12 = 101.4V$$

Post-calculated maximum duty cycle:

$$D_{MaxPost} = \frac{V_{RPost}}{V_{RPost} + V_{DCMin}} \quad \text{(Eq 031)}$$

$$D_{MaxPost} = \frac{101.4V}{101.4V + 93.63V} = 0.52$$

Duty cycle prime:

$$D'_{Max} = \frac{L_p \cdot f_s \cdot (I_{PMax} - I_{Valley})}{V_{RPost}} \quad \text{(Eq 032)}$$

$$D'_{Max} = \frac{556.7 \mu H \cdot 100kHz \cdot (0.86A - 0A)}{101.4V} = 0.47$$

Actual flux density:

$$B_{MaxAct} = \frac{L_p \cdot I_{PMax}}{N_p \cdot A_e} \quad \text{(Eq 033)}$$

$$B_{MaxAct} = \frac{556.7 \mu H \cdot 0.86A}{78 \cdot 32mm^2} = 191mT$$

Maximum DC input voltage for CCM operation:

$$V_{DC_{max\ CCM}} = \left(\frac{1}{\sqrt{2} \cdot P_{InMax} \cdot L_p \cdot f_s} - \frac{1}{V_{RPost}}\right)^{-1} \quad \text{(Eq 034)}$$

$$V_{DC_{max\ CCM}} = \left(\frac{1}{\sqrt{2} \cdot 20.48W \cdot 557 \mu H \cdot 100kHz} - \frac{1}{101.4V}\right)^{-1} = 90.3V$$
8.6 Transformer winding design

Transformer design plays a big role in efficiency. Interlacing primary and output windings can reduce leakage inductance, and this is one way to improve efficiency. It is also critical for safety concerns, especially in isolated applications. Therefore, creepage and clearance should also be given serious consideration.

Standard safety margins between primary and secondary winding:

\[ M = 4 \text{ mm for European safety standard} \]
\[ M = 3.2 \text{ mm for UL1950} \]
\[ M = 0 \text{ mm for triple-insulated wire on either primary or secondary winding} \]

Standard safety margin \( M \) | Copper space factor \( f_{Cu} \) | 0 mm | 0.4 (0.2–0.4)

Effective bobbin width:

\[ BW_E = BW - (2 \times M) \quad \text{(Eq 035)} \]
\[ BW_E = 11\text{mm} - (2 \times 0) = 11\text{mm} \]

Effective winding cross-section:

\[ A_{Ne} = \frac{A_N \times BW_e}{BW} \quad \text{(Eq 036)} \]
\[ A_{Ne} = \frac{34\text{mm}^2 \times 1\text{mm}}{11\text{mm}} = 34\text{mm}^2 \]

The effective winding cross-section must be divided between the primary and secondary windings. The design example is divided as follows:

<table>
<thead>
<tr>
<th>Winding</th>
<th>Factor</th>
</tr>
</thead>
<tbody>
<tr>
<td>Primary winding ((AF_{NP}))</td>
<td>50 %</td>
</tr>
<tr>
<td>Secondary winding 1 ((AF_{NS1}))</td>
<td>30 %</td>
</tr>
<tr>
<td>Secondary winding 2 ((AF_{NS2}))</td>
<td>15 %</td>
</tr>
<tr>
<td>Auxiliary winding ((AF_{NVcc}))</td>
<td>5 %</td>
</tr>
</tbody>
</table>

8.6.1 Primary winding

Calculate copper wire cross-sectional area:

\[ A_{PCal} = \frac{AF_{NP} \times f_{Cu} \times A_{Ne}}{N_P} \quad \text{(Eq 037)} \]
\[ A_{PCal} = \frac{0.5 \times 0.4 \times 34\text{mm}^2}{78} = 0.087\text{mm}^2 \]

Calculate maximum wire size:

\[ AWG_{PCal} = 9.97 \cdot \left(1.8277 - 2 \cdot \log\left(2 \cdot \frac{A_{PCal}}{\pi}\right)\right) \quad \text{(Eq 038)} \]
\[ AWG_{PCal} = 9.97 \cdot \left(1.8277 - 2 \cdot \log\left(2 \cdot \sqrt{\frac{0.087}{\pi}}\right)\right) = 28 \]

Selected wire size \( AWG_{P} \) | 30
Number of parallel wires \( n_{P} \) | 1

Copper wire diameter:

\[ d_{P} = 10 \left(\frac{1.8277}{2} \cdot \frac{AWG_{P}}{29.97}\right) \quad \text{(Eq 039)} \]
\[ d_{P} = 10 \left(\frac{1.8277}{2} \cdot \frac{30}{29.97}\right) = 0.26\text{mm} \]
Copper wire cross-sectional area:

\[ A_p = \frac{\pi}{4} \cdot d_p^2 \cdot n_p \]  \hspace{1cm} (Eq 040) \hspace{1cm} A_p = \frac{\pi}{4} \cdot (0.26\text{mm})^2 \cdot 1 = 0.0517\text{mm}^2

Wire current density:

\[ S_p = \frac{I_{PRMS}}{A_p} \]  \hspace{1cm} (Eq 041) \hspace{1cm} S_p = \frac{0.35\text{A}}{0.052\text{mm}^2} = 6.8\text{A/mm}^2

**Note:** Recommended wire current density is less than 8 A/mm².

Number of turns per layer using INS = 0.01 mm:

\[ NL_p = \frac{BW_E}{n_p \cdot (d_p + 2 \cdot \text{INS})} \]  \hspace{1cm} (Eq 042) \hspace{1cm} NL_p = \frac{1\text{mm}}{1 \cdot (0.26\text{mm} + 2 \cdot 0.01\text{mm})} = 39\text{Turns/layer}

**Note:** Insulation thickness (INS) for single-, double- and triple-insulated wire is 0.01, 0.02 and 0.04 mm respectively. Ask the magnetics supplier for the actual insulation thickness.

Number of layers:

\[ Ln_p = N_p / NL_p \]  \hspace{1cm} (Eq 043) \hspace{1cm} Ln_p = 78\text{Turns} / (39\text{Turns/layer}) = 2\text{layers}

### 8.6.2 Secondary 1 winding (V\text{Out1})

Calculate copper wire cross-sectional area:

\[ A_{NSiCal} = \frac{AF_{NSi} \times f_{Cu} \times A_{Ne}}{N_s1} \]  \hspace{1cm} (Eq 044) \hspace{1cm} A_{NSiCal} = \frac{0.30 \times 0.4 \times 34\text{mm}^2}{12} = 0.34\text{mm}^2

Calculate maximum wire size:

\[ AWG_{NSiCal} = 9.97 \left( 1.8277 - \left( 2 \cdot \log \left( 2 \cdot \sqrt[4]{\frac{A_{NSiCal}}{\pi}} \right) \right) \right) \]  \hspace{1cm} (Eq 045) \hspace{1cm} AWG_{NSiCal} = 9.97 \left( 1.8277 - \left( 2 \cdot \log \left( 2 \cdot \sqrt[4]{\frac{0.34\text{mm}^2}{\pi}} \right) \right) \right) = 22

Selected wire size  
AWGₜ₂  26  
Number of parallel wires  
nₜ₂  2  

Copper wire diameter:

\[ d_{s1} = 10 \left( \frac{1.8277}{2} \right) \left( \frac{\text{AWG}_{s1}}{2.997} \right) \]  \hspace{1cm} (Eq 046) \hspace{1cm} d_{s1} = 10 \left( \frac{1.8277}{2} \right) \left( \frac{26}{2.997} \right) = 0.407\text{mm}

Copper wire cross-sectional area:

\[ A_{s1} = \frac{\pi}{4} \cdot d_{s1}^2 \cdot n_{s1} \]  \hspace{1cm} (Eq 047) \hspace{1cm} A_{s1} = \frac{\pi}{4} \cdot (0.407 \text{mm})^2 \cdot 2 = 0.261\text{mm}^2
5th Generation Fixed-Frequency Design Guide
Design Guide - ICE5xSAG and ICE5xRxxxxAG

Fifth-generation fixed-frequency FLYCAL design example

Peak current:
\[ I_{S1\text{Max}} = I_{P\text{Max}} \cdot K_{L1} \cdot N_{PS1} \]  \hspace{1cm} (Eq 048) \hspace{1cm} I_{S1\text{Max}} = 0.86A \cdot 0.86 \cdot 6.5 = 4.8A

RMS current:
\[ I_{S1\text{RMS}} = I_{PRMS} \cdot K_{L1} \cdot \sqrt{\frac{1-D_{\text{MaxPost}}}{D_{\text{MaxPost}}} \cdot N_{PS1}} \]  \hspace{1cm} (Eq 049) \hspace{1cm} I_{S1\text{RMS}} = 0.35A \cdot 0.86 \cdot \sqrt{\frac{1-0.52}{0.52} \cdot 6.5} = 1.9A

Wire current density:
\[ S_{s1} = \frac{I_{S1\text{RMS}}}{A_{s1}} \]  \hspace{1cm} (Eq 050) \hspace{1cm} S_{s1} = \frac{1.9A}{0.261mm^2} = 7.3A/mm^2

Number of turns per layer using INS = 0.01 mm (non-isolated design does not need triple-insulated wire):
\[ NL_{s1} = \left\lfloor \frac{BW_{E}}{nw_{s1} \cdot (d_{s1} + 2 \cdot INS_{s1})} \right\rfloor \]  \hspace{1cm} (Eq 051) \hspace{1cm} NL_{s1} = \left\lfloor \frac{11mm}{2 \cdot (0.407mm + 2 \cdot 0.01mm)} \right\rfloor = 12\text{Turns/layer}

Number of layers of secondary 1 winding:
\[ Ln_{s1} = \left\lfloor \frac{N_{s1}}{NL_{s1}} \right\rfloor \]  \hspace{1cm} (Eq 052) \hspace{1cm} Ln_{s1} = \left\lfloor \frac{12\text{Turns}/(12\text{Turns/layer})}{1\text{layers}} \right\rfloor = 1\text{layers}

8.6.3 Secondary 2 winding (V_{Out2})

Calculate copper wire cross-sectional area:
\[ A_{NS2\text{Cal}} = \frac{AF_{NS2} \times f_{Cu} \times A_{Ne}}{N_{s2}} \]  \hspace{1cm} (Eq 053) \hspace{1cm} A_{NS2\text{Cal}} = \frac{0.15 \times 0.4 \times 34mm^2}{4} = 0.51mm^2

Calculate maximum wire size:
\[ AWG_{NS2\text{Cal}} = 9.97 \left(1.8277 - 2 \cdot \log \left(2 \cdot \frac{\sqrt{A_{NS2\text{Cal}}}}{\pi} \right)\right) \]  \hspace{1cm} (Eq 054) \hspace{1cm} AWG_{NS2\text{Cal}} = 9.97 \left(1.8277 - 2 \cdot \log \left(2 \cdot \frac{0.34}{\pi} \right)\right) = 20

Selected wire size
\[ AWG_{s2} = 26 \]
Number of parallel wires
\[ n_{s2} = 1 \]
Copper wire diameter:
\[ d_{s2} = 10^{\frac{1.8277 \cdot AWG_{s2}}{2 \cdot 2.997}} \]  \hspace{1cm} (Eq 055) \hspace{1cm} d_{s2} = 10^{\frac{1.8277 \cdot 26}{2 \cdot 2.997}} = 0.407mm

Copper wire area:
\[ A_{s2} = \frac{\pi}{4} \cdot d_{s2}^2 \cdot n_{s2} \]  \hspace{1cm} (Eq 056) \hspace{1cm} A_{s2} = \frac{\pi}{4} \cdot (0.407)^2 \cdot 1 = 0.13mm^2

Peak current:
\[ I_{S2\text{Max}} = I_{P\text{Max}} \cdot K_{L2} \cdot N_{PS2} \]  \hspace{1cm} (Eq 057) \hspace{1cm} I_{S2\text{Max}} = 0.86A \cdot 0.14 \cdot 19.5 = 2.3A
RMS current:

\[ I_{S2, RMS} = I_{PRMS} \cdot K_{L2} \cdot \sqrt{1 - \frac{D_{MaxPost}}{D_{MaxPost}}} \cdot N_{PS2} \]  (Eq 058)

| \[ I_{S2, RMS} = 0.35A \cdot 0.14 \cdot \sqrt{1 - \frac{0.52}{0.52}} \cdot 19.5 = 0.9A \]  

Wire current density:

\[ S_{S2} = \frac{I_{S2, RMS}}{A_{S2}} \]  (Eq 059)

| \[ S_{S2} = \frac{0.9A}{0.130mm^2} = 7A/mm^2 \]  

Number of turns per layer using INS = 0.01 mm (non-isolated design does not need triple-insulated wire):

\[ NL_{S2} = \left| \frac{BW_E}{nW_{S2} \cdot (d_{S2} + 2 \cdot INS_{S2})} \right| \]  (Eq 060)

| \[ NL_{S2} = \left| \frac{11mm}{1\cdot(0.407mm + 2\cdot0.01mm)} \right| = 25 \text{Turns/layer} \]  

Number of layers:

\[ Ln_{S2} = \left\lfloor \frac{N_{S2}}{NL_{S2}} \right\rfloor \]  (Eq 061)

| \[ Ln_{S2} = \left\lfloor \frac{4 \text{Turns}}{25 \text{Turns/layer}} \right\rfloor = 1 \text{layer} \]  

### 8.7 Clamping network

For calculating the clamping network, it is necessary to know the leakage inductance \( L_{LK} \). The most common approach is to have the \( L_{LK} \) value given in a percentage of the \( L_p \). If it is known that the transformer construction is consistent, the \( L_{LK} \) can be measured by shorting the secondary windings (assuming the availability of a good LCR meter).

Leakage inductance:

Leakage inductance percentage

\[ L_{LK} = L_{LK\%} \cdot L_p \]  (Eq 062)

| \[ L_{LK} = 2.5\% \times 556.7\mu H = 13.9\mu H \]  

Clamping voltage:

\[ V_{Clamp} = V_{DSMax} - V_{DCMaxPk} - V_{RPost} \]  (Eq 063)

| \[ V_{Clamp} = 700V - 466.7V - 101.4V = 131.9V \]  

Calculate clamping capacitor:

\[ C_{ClampCal} = \frac{I_{PMax}^2 \cdot L_{LK}}{(V_{RPost} + V_{Clamp}) \cdot V_{Clamp}} \]  (Eq 064)

| \[ C_{ClampCal} = \frac{(0.86A)^2 \times 13.9\mu H}{(101.4V + 131.9V) \times 131.9V} = 334\mu F \]  

Clamping capacitor \( C_{Clamp} = 1 \text{nF} \)

Calculate clamping resistor:

\[ R_{ClampCal} = \frac{(V_{Clamp} + V_{RPost})^2 - V_{RPost}^2}{0.5 \cdot L_{LK} \cdot I_{PMax}^2 \cdot f_S} \]  (Eq 065)

| \[ R_{ClampCal} = \frac{(131.9V + 101.4V)^2 - (101.4V)^2}{0.5 \times 13.9\mu H \times (0.86A)^2 \times 100kHz} = 86k\Omega \]  

Clamping resistor \( R_{Clamp} = 68k\Omega \)
8.8 **CS resistor**

The CS resistor value defines the peak current of the power MOSFET. Therefore, the transformer should be designed not to saturate at this peak current value. Because the IC cycle-by-cycle PCL is defined by this resistor, it also defines the maximum output power that can be delivered.

CS resistor:

$$ R_{\text{Sense}} = \frac{V_{CS,N}}{I_{PMax}} $$  

(Eq 066)

\[ R_{\text{Sense}} = \frac{0.8V}{0.86A} = 0.93\Omega \]

8.9 **Output rectifier**

A low forward voltage and an ultrafast diode such as a Schottky diode are recommended for a highly efficient design. These diodes are subjected to large peak and RMS current stress. The minimum voltage rating (not including voltage spikes) and minimum current rating (not including peak power transients) are calculated below.

The output capacitor is necessary to minimize the output ripple. It also holds the necessary energy needed during high load jumps. Therefore, the output capacitor should have enough capacitance and low ESR. It should also meet the ripple current rating.

An LC filter can be added to further reduce the output ripple.

8.9.1 **Output 1**

Diode reverse voltage:

$$ V_{RDiode1} = V_{Out1} + \left( \frac{V_{DCMaxPK}}{N_{PS1}} \right) $$  

(Eq 067)

\[ V_{RDiode1} = 15V + \left( \frac{466.7V}{6.5} \right) = 86.8V \]

Diode RMS current

\[ I_{S1RMS} = 1.9A \]

Output capacitor ripple current:

\[ I_{Ripple1} = \sqrt{\left(I_{S1RMS}\right)^2 - \left(I_{Out1}\right)^2} \]  

(Eq 068)

\[ I_{Ripple1} = \sqrt{(1.9A)^2 - (0.83A)^2} = 1.71A \]

Calculated output capacitance:

\[ C_{Out1Cal} = \frac{I_{Out1} \cdot n_{CP1} \cdot \Delta V_{OUT1} \cdot f_s}{\Delta V_{OUT1} \cdot f_s} \]  

(Eq 069)

\[ C_{Out1Cal} = \frac{0.83A \cdot 20}{0.3V \cdot 100kHz} = 553\mu F \]

Output capacitor

\[ C_{Out1} = 680\mu F \]

ESR

\[ R_{ESR1} = 32\,m\Omega \]

Number of output capacitors in parallel

\[ n_{COut1} = 1 \]

Zero-frequency output capacitor:
5th Generation Fixed-Frequency Design Guide
Design Guide - ICE5xSAG and ICE5xRxxxxAG

Fifth-generation fixed-frequency FLYCAL design example

\[
f_{ZCOut1} = \frac{1}{2 \cdot \pi \cdot R_{ESR1} \cdot C_{Out1}} \quad \text{(Eq 070)}
\]

Ripple voltage of first stage:

\[
V_{Ripple1} = \frac{I_{SMax1} \cdot R_{ESR1}}{nC_{Out1}} \quad \text{(Eq 071)}
\]

Calculated LC filter capacitor:

Select LC filter inductor

\[
L_{Out1} = 2.2 \, \mu H \quad \text{(Eq 072)}
\]

\[
C_{LC1} = 680 \, \mu F
\]

LC filter frequency:

\[
f_{LC1} = \frac{1}{2 \cdot \pi \cdot \sqrt{C_{LC1} \cdot L_{Out1}}} \quad \text{(Eq 073)}
\]

Second stage ripple voltage:

\[
V_{outRipple1} = V_{Ripple1} \cdot \frac{1}{2 \cdot \pi \cdot f_s \cdot C_{LC1}} \quad \text{(Eq 074)}
\]

8.9.2 Output 2

Diode reverse voltage:

\[
V_{RDiode2} = V_{Out2} + \left( \frac{V_{DCMaxPk}}{N_{PS2}} \right) \quad \text{(Eq 075)}
\]

Diode RMS current

\[
I_{S2RMS} = 0.92 \, A
\]

Output capacitor ripple current for \( V_{Out2} \):

\[
I_{Ripple2} = \sqrt{(I_{S2RMS})^2 - (I_{Out2})^2} \quad \text{(Eq 076)}
\]

Calculated output capacitance:

\[
C_{Out2} = \frac{I_{Out2} \cdot n_{CP2}}{\Delta V_{OUT2} \cdot f_s} \quad \text{(Eq 077)}
\]

Output capacitor

\[
C_{Out2} = 680 \, \mu F
\]

ESR

\[
R_{ESR2} = 32 \, m\Omega
\]

Number of output capacitors in parallel

\[
n_{COut2} = 1
\]

Zero-frequency output capacitor:
5th Generation Fixed-Frequency Design Guide
Design Guide - ICE5xSAG and ICE5xRxxxxAG

Fifth-generation fixed-frequency FLYCAL design example

\[ f_{ZCO_{\text{Out2}}} = \frac{1}{2 \cdot \pi \cdot R_{ESR2} \cdot C_{\text{Out2}}} \quad \text{(Eq 078)} \]
\[ f_{ZCO_{\text{Out2}}} = \frac{1}{2 \cdot \pi \cdot 32 \text{m}\Omega \cdot 680 \mu\text{F}} = 7.3\text{kHz} \]

Ripple voltage of first stage:
\[ V_{\text{Ripple2}} = \frac{I_{S2\text{Max}} \cdot R_{ESR2}}{nC_{\text{Out2}}} \quad \text{(Eq 079)} \]
\[ V_{\text{Ripple2}} = \frac{2.31\text{A} \cdot 32\text{m}\Omega}{1} = 0.07\text{V} \]

Calculated LC filter capacitor:

Select LC filter inductor \[ L_{\text{Out2}} = 2.2\text{\mu}\text{H} \quad \text{(Eq 080)} \]

LC filter capacitor \[ C_{\text{LC2}} = 330\mu\text{F} \]

LC filter frequency:
\[ f_{\text{LC2}} = \frac{1}{2 \cdot \pi \cdot \sqrt{C_{\text{LC2}} \cdot L_{\text{OUT2}}}} \quad \text{(Eq 081)} \]
\[ f_{\text{LC1}} = \frac{1}{2 \cdot \pi \cdot \sqrt{330\mu\text{F} \cdot 2.2\text{\mu}\text{H}}} = 5.9\text{kHz} \]

Second stage ripple voltage:
\[ V_{2\text{nd\_Ripple2}} = V_{\text{Ripple2}} \cdot \left( \frac{1}{2 \cdot \pi \cdot f_{\text{LC2}} \cdot C_{\text{LC2}}} + \left( \frac{1}{2 \cdot \pi \cdot f_{\text{LC2}} \cdot L_{\text{OUT2}}} \right) \right) \quad \text{(Eq 082)} \]
\[ V_{2\text{nd\_Ripple2}} = 0.07\text{V} \cdot \left( \frac{1}{2 \cdot \pi \cdot 100\text{kHz} \cdot 330\mu\text{F}} + \left( \frac{1}{2 \cdot \pi \cdot 100\text{kHz} \cdot 2.2\text{\mu}\text{H}} \right) \right) = 0.26\mu\text{V} \]

8.10 \text{V}_{\text{CC}} \text{ diode and capacitor}

Auxiliary diode reverse voltage:
\[ V_{\text{RDiode}_{\text{VCC}}} = V_{\text{VccCal}} + \left( V_{\text{DCMaxPk}} \cdot \frac{N_{\text{VCC}}}{N_{p}} \right) \quad \text{(Eq 083)} \]
\[ V_{\text{RDiode}_{\text{VCC}}} = 13.7\text{V} + \left( 466.7 \times \frac{11}{78} \right) = 79.5\text{V} \]

Calculate minimum \text{V}_{\text{CC}} \text{ capacitor:}

Soft-start time from datasheet \[ t_{\text{SS}} = 12\text{ms} \]
\[ I_{\text{VCC\_Charge3}} = 3\text{mA} \]
\[ V_{\text{VCC\_ON}} = 16\text{V} \]
\[ V_{\text{VCC\_OFF}} = 10\text{V} \]

\[ C_{\text{VCC}} > \frac{I_{\text{VCC\_Charge3}} \cdot t_{\text{SS}}}{V_{\text{VCC\_ON}} - V_{\text{VCC\_OFF}}} \quad \text{(Eq 084)} \]
\[ C_{\text{VCCCal}} > \frac{3\text{mA} \cdot 12\text{ms}}{16\text{V} - 10\text{V}} = 6\mu\text{F} \]

Selected \text{V}_{\text{CC}} \text{ capacitor} \[ C_{\text{VCC}} = 22\mu\text{F} \]

Start-up time:

\[ V_{\text{CC\_short threshold from datasheet}} = V_{\text{VCC\_SCP}} = 1.1\text{V} \]
\[ I_{\text{VCC\_charge1 from datasheet}} = 0.2\text{mA} \]
8.11 Calculation of losses

Input diode bridge loss:

Diode bridge forward voltage

\[ V_{\text{FBR}} = 1 \text{V} \]

\[ P_{\text{DIN}} = I_{\text{ACRMS}} \cdot V_{\text{FBR}} \cdot 2 \]  \hspace{1cm} \text{(Eq 086)}

Transformer copper loss:

Copper resistivity at 100°C

\[ \rho_{100} = 0.0172 \Omega \cdot \text{mm}^2/\text{m} \]

\[ R_{\text{PCu}} = \frac{I_{N} \cdot N_{P} \cdot \rho_{100}}{A_{P}} \]  \hspace{1cm} \text{(Eq 087)}

\[ R_{\text{SICu}} = \frac{I_{N} \cdot N_{S1} \cdot \rho_{100}}{A_{S1}} \]  \hspace{1cm} \text{(Eq 088)}

\[ R_{\text{S2Cu}} = \frac{I_{N} \cdot N_{S2} \cdot \rho_{100}}{A_{S2}} \]  \hspace{1cm} \text{(Eq 089)}

\[ P_{\text{PCu}} = I_{\text{PRMS}} \cdot R_{\text{PCu}} \]  \hspace{1cm} \text{(Eq 090)}

\[ P_{\text{SICu}} = I_{\text{SIRMS}} \cdot R_{\text{SICu}} \]  \hspace{1cm} \text{(Eq 091)}

\[ P_{\text{S2Cu}} = I_{\text{S2RMS}} \cdot R_{\text{S2Cu}} \]  \hspace{1cm} \text{(Eq 092)}

\[ P_{\text{Cu}} = P_{\text{PCu}} \cdot P_{\text{SICu}} \cdot P_{\text{S2Cu}} \]  \hspace{1cm} \text{(Eq 093)}

Output rectifier diode loss:

\[ P_{\text{Diode1}} = I_{\text{S1RMS}} \cdot V_{\text{FOut1}} \]  \hspace{1cm} \text{(Eq 094)}

\[ P_{\text{Diode2}} = I_{\text{S2RMS}} \cdot V_{\text{FOut2}} \]  \hspace{1cm} \text{(Eq 095)}

RCD clapper loss:

\[ P_{\text{Clapper}} = \frac{1}{2} \cdot L_{LK} \cdot I_{\text{PRMS}}^2 \cdot t_{S} \cdot \frac{V_{\text{Clamp}} + V_{\text{RPost}}}{V_{\text{Clamp}}} \]

\[ P_{\text{Clapper}} = \frac{1}{2} \cdot 13.9 \mu \text{H} \cdot (0.86A)^2 \cdot 100\text{kHz} \cdot \frac{132V + 101.4V}{132V} = 0.91\text{W} \]  \hspace{1cm} \text{(Eq 096)}

CS resistor loss:

\[ P_{\text{CS}} = (I_{\text{PRMS}})^2 \cdot R_{\text{CS}} \]  \hspace{1cm} \text{(Eq 097)}

\[ P_{\text{CS}} = (0.35A)^2 \cdot 0.93\Omega = 0.12\text{W} \]
MOSFET loss:
\[ R_{DSON} = 8.73 \, \Omega \]
\[ C_{\text{ger}} = 3.4 \, \text{pF} \]

External drain-to-source capacitance
\[ P_{\text{condMaxAC}} = \frac{1}{2} \left( C_{\text{ger}} + C_{\text{DS}} \right) \left( V_{\text{DCMin}} - V_{\text{VRPost}} \right)^2 \cdot f_S \]  
\[ P_{\text{condMaxAC}} = I_{\text{PRMS}}^2 \cdot R_{DSON} \]  
\[ P_{\text{MOSMinAC}} = P_{\text{SONMinAC}} + P_{\text{condMinAC}} \]  
\[ P_{\text{MOSMaxAC}} = P_{\text{SONMaxAC}} + P_{\text{condMaxAC}} \]  
\[ P_{\text{MOSMaxAC}} = P_{\text{SONMaxAC}} + P_{\text{condMaxAC}} \]  
\[ P_{\text{MOSMaxAC}} = P_{\text{SONMaxAC}} + P_{\text{condMaxAC}} \]

Controller loss:

Controller current consumption
\[ I_{\text{VCC, normal}} = 0.9 \, \text{mA} \]  
\[ P_{\text{Ctrl}} = V_{\text{VCC, normal}} \cdot I_{\text{VCC, normal}} \]  
\[ P_{\text{Ctrl}} = 13.7V \cdot 0.9mA = 12.3mW \]

Total power loss:
\[ P_{\text{losses}} = P_{\text{DN}} + P_{\text{CS}} + P_{\text{Diode1}} + P_{\text{Diode2}} + P_{\text{Champer}} + P_{\text{CS}} + P_{\text{MOS}} + P_{\text{Ctrl}} \]  
\[ (\text{Eq 105}) \]
\[ P_{\text{losses}} = 0.8 + 0.27 + 1.14 + 0.18 + 0.91 + 0.12 + 1.1 + 0.01 = 4.53W \]

Efficiency after losses:
\[ \eta_{\text{Post}} = \frac{P_{\text{OutMax}}}{(P_{\text{OutMax}} + P_{\text{losses}})} \]  
\[ (\text{Eq 106}) \]
\[ \eta_{\text{Post}} = 17W / (17W + 4.53W) = 78.95\% \]

8.12 CoolSET™/MOSFET temperature

CoolSET™/MOSFET temperature:

Assumed junction-to-ambient thermal impedance (include copper pour)
\[ R_{\text{thJA, Ar}} = 65 \, \text{K/W} \]
\[ \Delta T = R_{\text{thJA, Ar}} \cdot P_{\text{MOS}} \]  
\[ (\text{Eq 107}) \]
\[ \Delta T = 65K \cdot 1.098W = 71.4^\circ K \]
\[ T_{\text{j, max}} = \Delta T + T_{\text{a, max}} \]  
\[ (\text{Eq 108}) \]
\[ T_{\text{j, max}} = 71.4 + 50 = 121.4^\circ C \]

8.13 LOVP

LOVP:

Selected AC input LOVP
\[ V_{\text{VOP, AC}} = 330 \, \text{V AC} \]

High-side DC input voltage divider resistor (R3A, R3B, R3C)
\[ R_3 = 9 \, \text{M} \Omega \]

Controller LOVP threshold
\[ V_{\text{VIN, LOVP}} = 2.85 \, \text{V} \]
### Fifth-generation fixed-frequency FLYCAL design example

\[
R_{12\text{cal}} = \frac{R_{11} \cdot V_{\text{VIN,LOVP}}}{\left( V_{\text{OVP,AC}} \cdot \sqrt{2} - V_{\text{VIN,LOVP}} \right)} \quad \text{(Eq 109)}
\]

Select low-side DC input voltage divider resistor

\[
V_{\text{OVP,ACPost}} = \frac{V_{\text{VIN,LOVP}}}{R_{12}} \cdot \frac{R_{11} + R_{12}}{\sqrt{2}} \quad \text{(Eq 110)}
\]

#### 8.14 Output regulation (non-isolated)

Setting resistor dividers for two non-isolated outputs:

- **Error amplifier reference voltage** \( V_{\text{ERR,REF}} \) 1.8 V
- **Weighted regulation factor of** \( V_{\text{Out}} \) \( W_1 \) 31 %
- **Select voltage divider RO1** \( R_{O1} \) 39 kΩ

\[
R_{O2\text{cal}} = \frac{V_{\text{Out1}} - V_{\text{ERR,REF}}}{W_1 \cdot V_{\text{ERR,REF}} / R_{O1}} \quad \text{(Eq 125)}
\]

Select voltage divider RO2 \( R_{O2} \) 910 kΩ

\[
R_{O3\text{cal}} = \frac{V_{\text{Out2}} - V_{\text{ERR,REF}}}{V_{\text{ERR,REF}} \cdot \frac{V_{\text{Out1}} - V_{\text{ERR,REF}}}{R_{O1} - R_{O2}}} \quad \text{(Eq 126)}
\]

Select voltage divider RO3 \( R_{O3} \) 100 kΩ
9 References

[1] ICE5xSAG datasheet, Infineon Technologies AG
[2] ICE5xRxxxxAG datasheet, Infineon Technologies AG
[3] AN_201702_PL83_005 60W 19V SMPS Demo Board with ICE5GSAG and IPA80R600P7
[4] ER_201708_PL83_016 14 W 15 V 5 V SMPS demo board with ICE5AR4770AG
## Revision history

<table>
<thead>
<tr>
<th>Document version</th>
<th>Date of release</th>
<th>Description of changes</th>
</tr>
</thead>
<tbody>
<tr>
<td>V 2.1</td>
<td>24 Jul 2019</td>
<td>Page 22, section 4.7.5</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Addition of statement when CS pin is shorted to GND</td>
</tr>
<tr>
<td>V 2.0</td>
<td>07 Dec 2017</td>
<td>First release</td>
</tr>
</tbody>
</table>
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