LLC design guide: 600 W converter

Simplified algorithm based on FHA and vector method

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About this document

Scope and purpose

This note will review the basics of the LLC multi-resonant converter, and describe a new vector method based on first harmonic approximation (FHA) that will provide a simple algorithm to design the resonant tank system for the LLC converter. LTspice® simulation is used to calculate actual values of the RMS current, and they are compared with FHA values. The design process is demonstrated on the **600 W LLC demo board**.

Intended audience

This document is intended for design engineers who wish to develop a deeper understanding of the operation of LLC converters and their design.

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1 Introduction

The multi-resonant LLC converter has several desirable features, such as high efficiency, low EMI and high-power density. However, the design of a resonant converter is a challenging task, and requires more effort for design optimization compared to PWM converters. Current state-of-the-art LLC design methods are based on calculus and graphs using a time-consuming iterative procedure. This document aims to simplify this task, and make it easier to optimally design the LLC converter. This paper provides an overview of LLC converter operation and a new design method based on vector analysis. This new method enables a simple algorithm to calculate key component values of the LLC converter based on given requirements.

1.1 Overview of the LLC resonant converter

Figure 1 shows a basic half-bridge LLC converter with a center-tap rectifier. In a simplistic discussion, the switching bridge generates a square waveform to excite the LLC resonant tank, which will output a resonant sinusoidal current that gets scaled and rectified by the transformer and rectifier circuit. The output capacitor filters the rectified AC current and delivers a DC voltage for the output.

This is a frequency-controlled topology. The frequency operating range is selected such that input impedance of the converter always stays inductive, and the current lags behind the voltage. This enables zero-voltage switching (ZVS) on the primary side and zero-current switching (ZCS) on the secondary side, which practically eliminates turn-on losses and minimizes turn-off losses. Using the LLC converter in the correct operating modes is key to realizing these benefits. As an example, be careful with buck mode. Buck operation mode when LLC operates above the resonant tank frequency reduces RMS current but will incur non-ZCS switching losses on the secondary side.

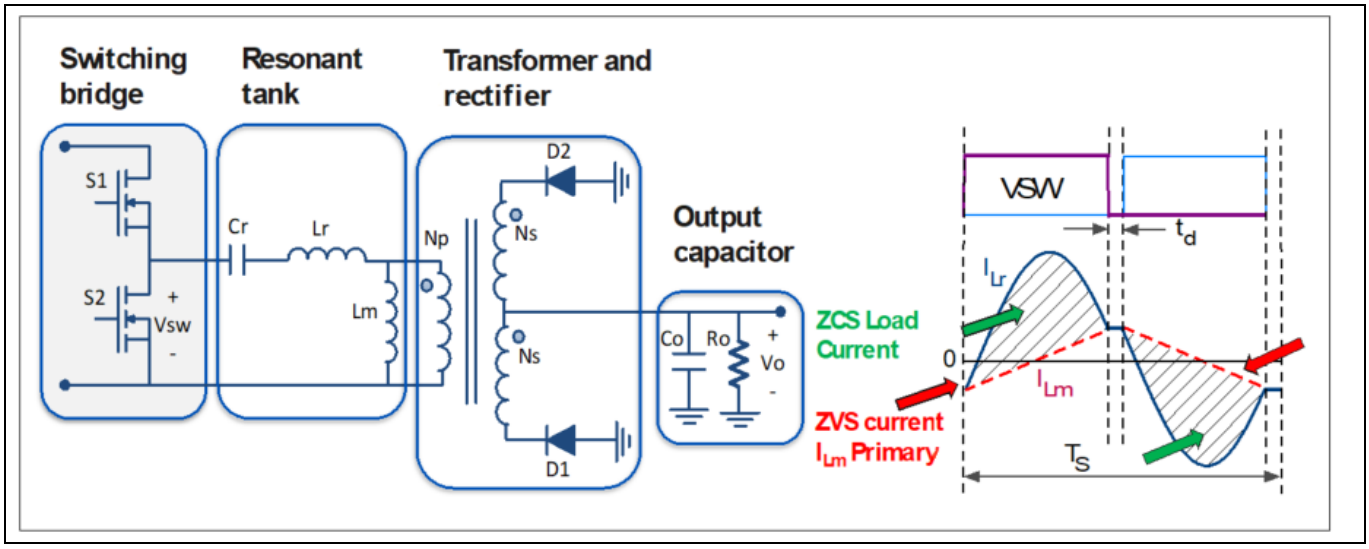

Figure 1 Principle schematic of a half-bridge LLC converter

1.2 First harmonic approximation

The LLC converter is a non-linear topology that combines a linear network (resonant tank and transformer) with active switches (MOSFETs) and passive switches (diodes). The non-linear nature of the switching topology prevents simple and effective methods of the linear AC circuit analysis from being directly applied in this case. Averaging methods common in PWM topologies are not directly applicable either, because operating switching frequency is very close to the resonant frequency. However, harmonic analysis shows that the first harmonic represents LLC current very well. This is used to simplify the topology schematic, generate a linear circuit schematic (FHA model) and enable the use of linear circuit analysis methods.

2 Design-oriented analysis

Design is the reverse of analysis: you start with the specification, which is the answer to analysis, and you have to work the analysis backward to find the starting point, which is the circuit configuration and the element values. The intentional form of all equations should follow the idea that is simple to move from analysis to design, and vice versa.

The objective here is power conversion from HV input to LV input using an LLC converter with a transformer. The key objectives are efficiency and density. **Figure 2** shows the process.

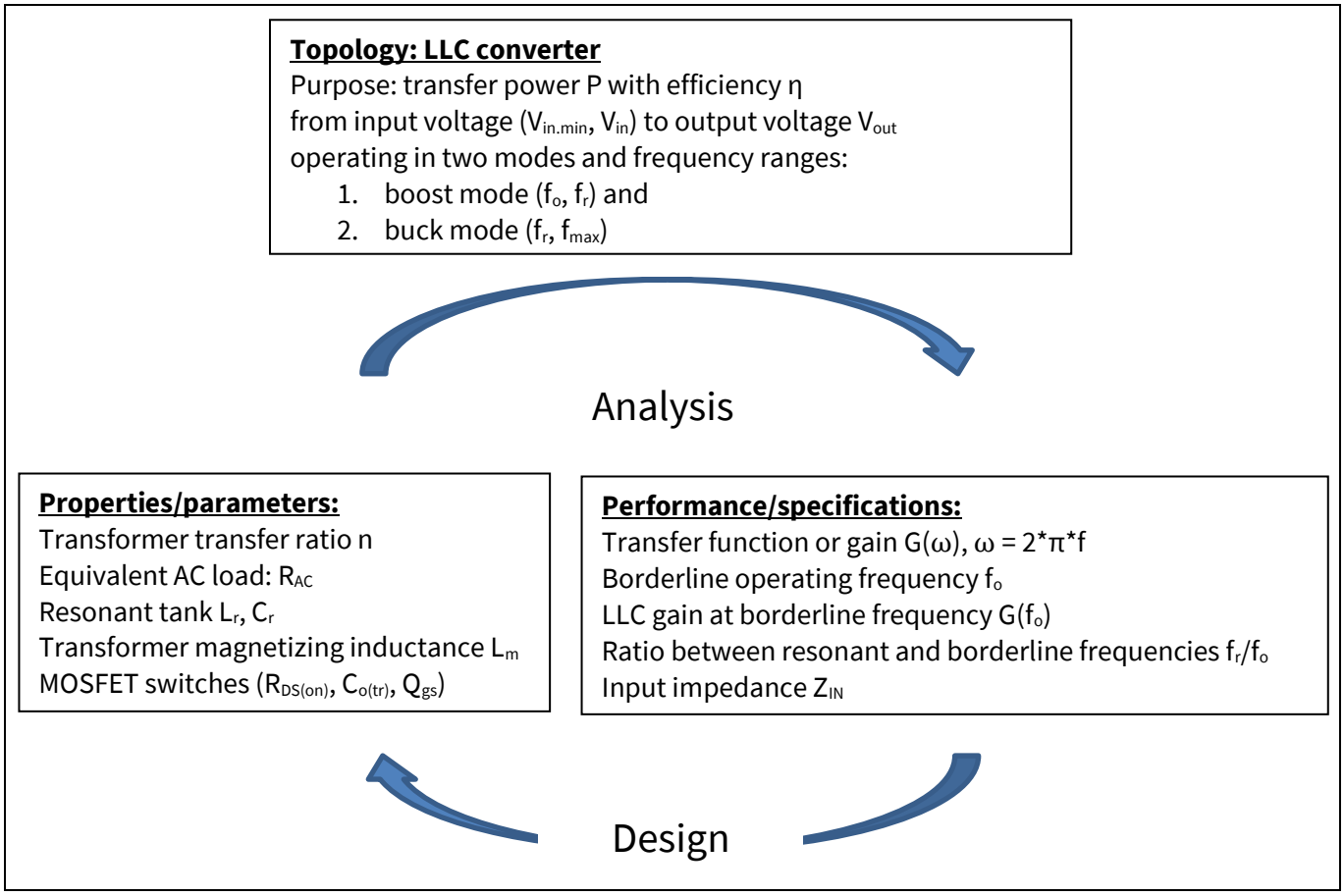

Figure 2 Design-oriented analysis

Let's start, and derive key equations that connect properties (parameters) with performance (specifications).

The LLC converter gain G(ω) has three components:

Gain = (switching bridge gain)*(transformer turns ratio ($n = N_s/N_p$) *(impedance ratio gain)

The switching bridge gain depends on the topology employed. The full-bridge topology has gain equal to one, while the half-bridge topology has a gain of half. Let's represent topology gain as "p".

$$p = 1 \ldots for\ full - bridge\ topology \quad (1)$$

$$p = ½ \ldots for\ half - bridge\ topology \quad (2)$$

The resonant tank gain is based on the load and resonant tank impedance ratio. Note that it behaves like a frequency-driven voltage divider G(ω) composed of resonant tank impedance and load impedance. See **Figure 3** and equation (3) below.

2.1 LLC as a frequency-controlled voltage divider

$$G(\omega) = \frac{V_o}{V_{in}} = \frac{Z_{lp}(\omega)}{Z_{lp}(\omega)+Z_r(\omega)} \quad (3)$$

Where:

- resonant tank impedance: $Z_r(\omega_o) = j * \omega_o * L_r + \frac{1}{j*\omega_o*C_r}$ (4)
- parallel load impedance: $Z_{lp}(\omega o) = \frac{R_{ac}*(j*\omega_o*L_m)}{R_{ac}+j*\omega_o*L_m}$ (5)
- series load impedance: $Z_{ls}(\omega o) = R_{ac} + j * \omega_o * L_m$ (6)

Also, we would use another form of this equation (3), called the inverse gain equation (7):

$$\frac{1}{G(\omega)} = 1 + \frac{Z_r(\omega)}{Z_{lp}(\omega)} \quad (7)$$

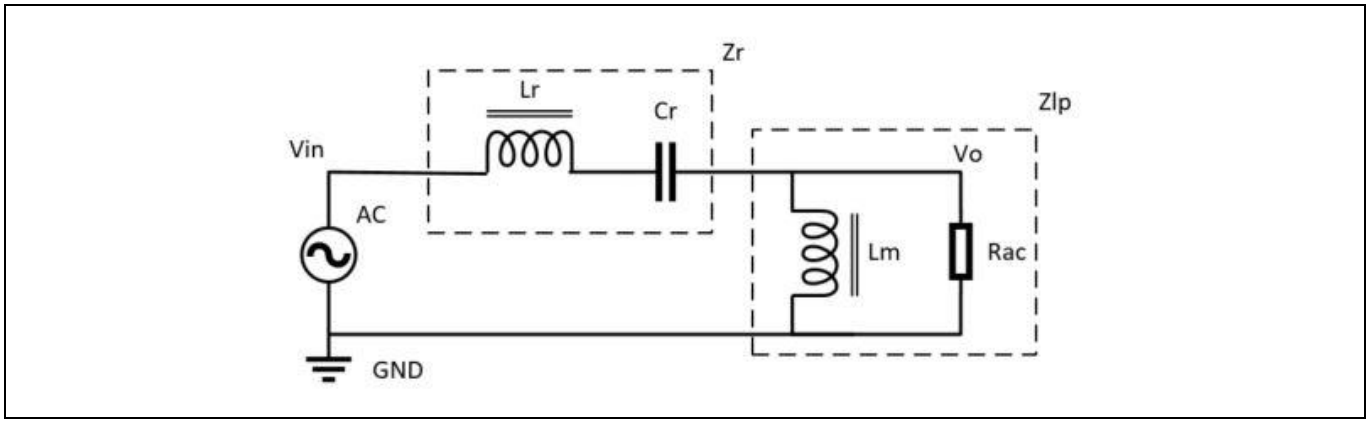

Figure 3 LLC converter as a voltage divider, with resonant tank and load impedances

When the frequency is changing, both impedances (Z_r and Z_{lp}) will change and the divider will change the effective ratio, providing a different gain. It is important to monitor the input impedance of the divider. The input impedance is equal to the sum of resonant impedance Z_r and load impedance Z_{lp}:

$$Z_{in}(\omega) = Z_{lp}(\omega) + Z_r(\omega) \quad (8)$$

The load impedance Z_{lp} always has an inductive character. Let's have a look at the resonant impedance Z_r (**Figure 3**). When the operating frequency is equal to the resonant frequency f_r, the reactive portion of the Z_r impedance is equal to zero, and the total impedance of Z_r is equal just to the parasitic resistance of L_r and has its minimal value. When the frequency is changing around the resonant frequency f_r, the resonant impedance Z_r is changing both its amplitude and character, from capacitive to inductive. When the operating frequency drops below the resonant frequency, the capacitive impedance becomes larger and larger, and at a certain point it prevails over the load impedance Z_{lp}, so the total impedance becomes capacitive. When:

1. **Operating frequency ω_{sw} (switching frequency) $\geq \omega_r$ (resonant tank frequency),**
   Z_r is inductive, $Z_{lp} + Z_r > Z_l$ gain is less than one (buck) and input impedance is inductive.
2. **Operating frequency ω_{sw} (switching frequency) $= \omega_r$ (resonant tank frequency),**
   Z_r = 0, $Z_{lp} + Z_r = Z_l$ gain is one and input impedance is inductive.
3. **Operating frequency ω_{sw} (switching frequency) $< \omega_r$ (resonant tank frequency),**
   Z_r is capacitive, $Z_{lp} + Z_r < Z_l$ and input impedance is still inductive, the gain is larger than one (boost).

Borderline case:

Input impedance $Z_i(\omega o)$ angle is equal to zero.

ω_{sw}(switching frequency) = ω_o (zero angle frequency).

If the operating frequency is less than ω_o, the input impedance has a capacitive character and the converter will operate in so-called capacitive mode. The primary-side MOSFET body diodes are hard commutated during MOSFET turn-on, and switching losses are becoming very high. We don't want the converter to operate in that mode. Note that the input impedance angle is a very important parameter to monitor.

2.2 Input impedance angle

Let's analyze the input impedance in detail:

$$Z_{in} = Z_{lp}(\omega) + Z_r(\omega) = Z_{lp}(\omega) * \frac{Z_{lp}(\omega)+Z_r(\omega)}{Z_{lp}(\omega)} \qquad (9)$$

$$Z_{in}(\omega) = \frac{Z_{lp}(\omega)}{G(\omega)} \qquad (10)$$

The borderline case is when the input impedance angle is equal to zero. If the frequency goes up, the angle becomes positive (or inductive); if the frequency goes down, the angle becomes negative (or capacitive). Let's say that the impedance angle is equal to zero, at minimum operating frequency $\boldsymbol{\omega_o}$:

$$Angle(Z_{in}(\boldsymbol{\omega_o})) = 0 \qquad (11)$$

This leads to the most important conclusion:

$$Angle\left(\frac{1}{G(\boldsymbol{\omega_o})}\right) = -Angle\left(Z_{lp}(\boldsymbol{\omega_o})\right) = Angle\left(Z_{ls}(\boldsymbol{\omega_o})\right) - \frac{\pi}{2} \qquad (12)$$

It means that vectors $\left(\frac{1}{G(\omega_o)}\right)$ and $Z_{ls}(\omega_o)$ are orthogonal at minimum operating frequency ω_o. Where Z_{lp} is a parallel combination of R_{AC} and $(j * \omega_o * L_m)$, while Z_{ls} is a serial combination of R_{AC} and $(j * \omega_o * L_m)$.

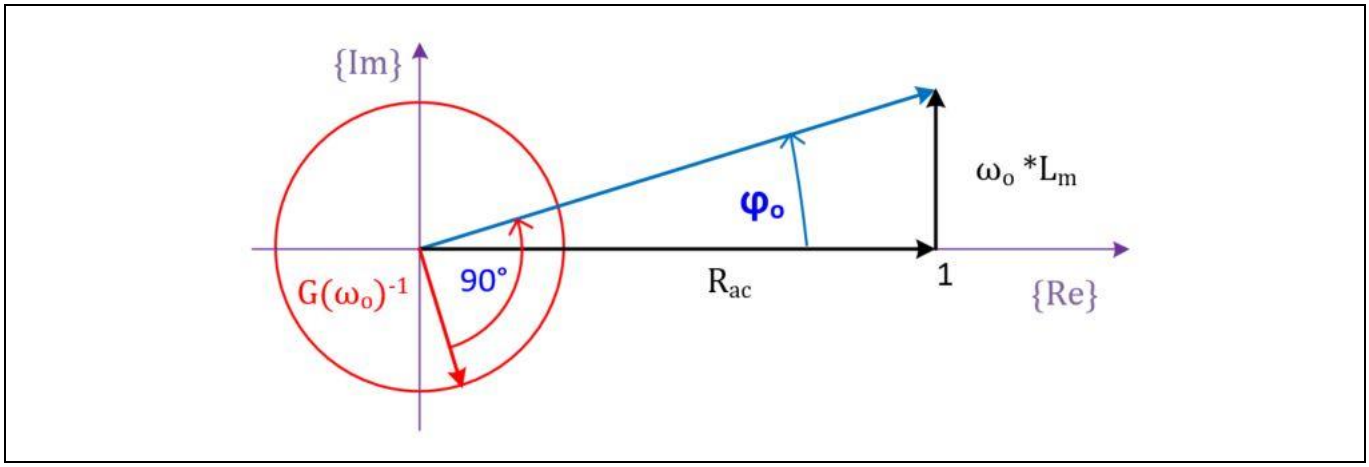

Figure 4 Vectors $\frac{1}{G(\boldsymbol{\omega_o})}$ and $Z_{ls}(\boldsymbol{\omega_o})$ are orthogonal at $\boldsymbol{\omega_o}$

Input impedance angle is a key element of the solution. It will help us to find a simple solution for the LLC maximum useful gain point that is borderline between the inductive and capacitive modes of operation. When operating frequency is reducing, LLC gain is increasing. The gain is useful until LLC stays in the inductive mode of operation, and when the impedance character changes from inductive to capacitive the LLC gain still can go up. That increment is not useful for us because current will advance the voltage, and when the LLC MOSFET switches the body diodes will operate in hard commutation, and switching losses will greatly increase. You can visualize the relation (12) in the form of the vector diagram in **Figure 4**.

2.3 LLC gain

Let's use the LLC inverse gain equation (7) for further analysis. The vector diagram of inverse gain $\left(\frac{1}{G(\omega_o)}\right)$ and the serial equivalent impedance $Z_{ls}(\omega_o)$ are given in **Figure 4**. The LLC gain equation is given in the inverse gain form (13):

$$\frac{1}{G(\omega_o)} = 1 + \frac{Z_r(\omega_o)}{Z_{lp}(\omega_o)} \qquad (13)$$

This equation could be written in a different form (14), and it is used to draw a vector diagram in **Figure 5**:

$$\frac{1}{G(\omega_o)} = 1 + p * (Z_r) * (Z_{ls}) \text{ where p } = \frac{1}{\omega_o * R_{ac} * L_m} \qquad (14)$$

A key equation is derived (15) using the vector diagram (**Figure 5**). It connects LLC gain, magnetizing inductance L_m of the transformer and equivalent AC load R_{AC}, operating at a border frequency between inductive and capacitive modes.

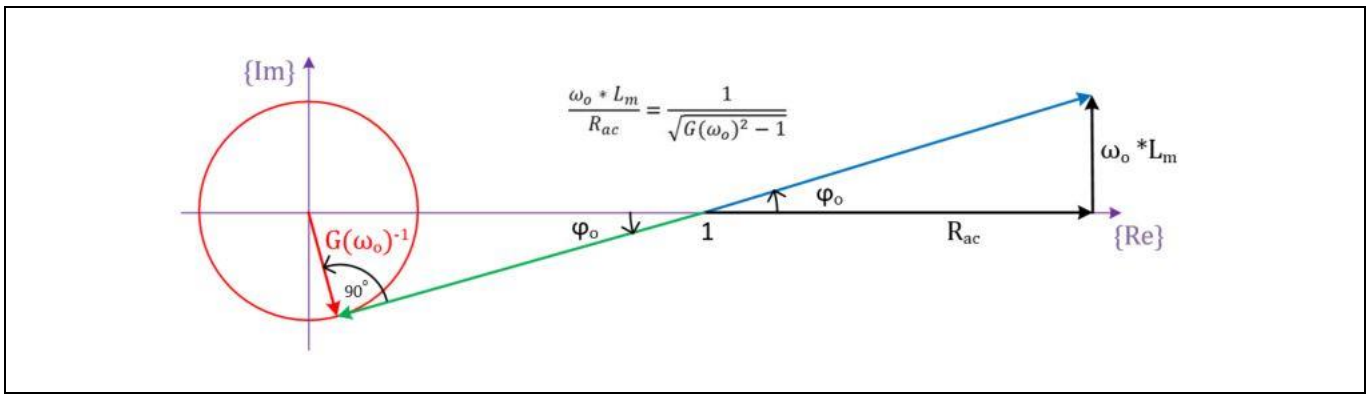

Figure 5 LLC converter inverse gain vector diagram

This shows a simple relation between LLC gain $G(\omega_o)$ and LLC parameters at the maximum useful gain operating point defined by the minimum operating frequency $\boldsymbol{\omega_o}$.

$$\frac{\boldsymbol{\omega_o * L_m}}{\boldsymbol{R_{ac}}} = \frac{\mathbf{1}}{\sqrt{\boldsymbol{G(\omega_o)^2 - 1}}} \qquad (15)$$

2.4 Component calculation

Using the vector diagram in **Figure 5** and equation (12), all components of the LLC converter could be calculated as a function of the maximum gain at border frequency $\boldsymbol{G(\omega_o)}$, equivalent AC load R_{AC}, border frequency ω_o and resonant tank frequency ω_r. See reference **[1]** for details.

$$L_m = \frac{1}{\sqrt{G(\omega_0)^2 - 1}} * \frac{R_{AC}}{\omega_o} \qquad (16)$$

$$L_r = L_m * \frac{1 - \frac{1}{G(\omega_0)^2}}{(\frac{\omega_r}{\omega_o})^2 - 1} \qquad (17)$$

$$C_r = \frac{1}{\omega_r{}^2 * L_r} \qquad (18)$$

The set of equations (14) to (17) connect performance and properties of the LLC in a way that makes it very easy to connect analysis and design and move in either direction (analysis <=> design).

3 Design steps

In previous calculations, the key performance parameters were LLC gain and equivalent AC load. They could be directly generated from the specification. The third parameter used was minimum operating frequency, and this had a voluntary value. How the selection of the minimum operating frequency impacts the size of the passive components of the LLC converter is explained in detail in references [1], [4]. Essentially, when minimum operating frequency ω_o is equal to the half of the resonant tank frequency, the resonant tank components are smallest. That value will be used in the design below.

3.1 Input design data

Table 1 gives an overview of the design parameters.

Table 1 Design parameters

Description	Minimum	Nominal	Maximum
Input voltage	350 V DC	380 V DC	410 V DC
Output voltage	11.9 V DC	12.0 V DC	12.1 V DC
Output power			600 W
Efficiency at 50% P_{max}	97.5%*		
Switching frequency	90 kHz	150 kHz	250 kHz
Dynamic output voltage regulation (0 to 90% load-step)			Max. overshoot = 0.1 V Max. undershoot = 0.3 V
V_{out_ripple}			150 mV_{pk-pk}

3.2 Design parameters

Below are the variables from Table 1:

Nominal input voltage	$V_{in.nom}$ = 380 V
Minimum input voltage	$V_{in.min}$ = 350 V
Nominal output voltage	$V_{o.nom}$ = 12 V
Nominal output power	P_o = 600 W
Minimum operating frequency (borderline)	f_o = 90 kHz
Resonant tank frequency	f_r = 160 kHz
Maximum operating frequency	f_{max} = 250 kHz
LLC efficiency	$\eta = 97.5\ percent$

Note that circular frequency $\omega = 2 * \pi * f$ might be used along with frequency f in the formulas below.

We will use design inputs to calculate design parameters such as:

i. Transformer transfer ratio **n**
ii. Equivalent AC load $\boldsymbol{R_{AC}}$
iii. Required LLC maximum gain $\boldsymbol{G(\omega_o)}$

The transformer transfer ratio is given as (19):

$$\boldsymbol{n} = p * round\left(\frac{V_{in.nom}}{V_{o.nom}}\right) = 16 \quad (19), \qquad where\ p = \frac{1}{2}\ for\ HB\ LLC$$

Maximum LLC gain at border operating frequency (minimum frequency) is given by (20):

$$\boldsymbol{G(\omega_o)} = \left(\frac{2*n*V_{o.nom}}{V_{o.nom}}\right) = 1.1 \qquad (20)$$

Equivalent AC load based on the first harmonic model (21):

$$\boldsymbol{R_{AC}} = \frac{8}{\pi^2}\frac{n^2*V_{o.nom}{}^2}{P_o} = 49.8\ \Omega \qquad (21)$$

3.3 Calculation of LLC parameters

Using formulas (14) to (16), it is easy to calculate LLC converter parameters as:

Transformer magnetizing inductance:

$$L_m = \frac{1}{\sqrt{G(\omega_0)^2 - 1}} * \frac{R_{AC}}{2*\pi*f_o} = 192\ \mu H \qquad (22)$$

Resonant tank inductance:

$$L_r = L_m * \frac{1-\frac{1}{G(\omega_0)^2}}{\left(\frac{\omega_r}{\omega_o}\right)^2 - 1} = 15.66\ \mu H \qquad (23)$$

Resonant tank capacitance:

$$C_r = \frac{1}{\omega_r{}^2 * L_r} = 63.2\ nF \qquad (24)$$

This is not a standard value capacitor, and we need to select a standard value or a combination of them.

Let's select:

$$C_{rn} = 66\ nF\ (2x33\ nF) \qquad (25)$$

Then we need to recalculate resonant tank inductance to keep the same resonant tank frequency:

$$L_{rn} = \frac{1}{\omega_r{}^2 * C_{rn}} = 15\ \mu H \qquad (26)$$

Also, we can round to $L_{mn} = 195\ \mu H$. This will slightly lower the magnetizing current, and slightly improve efficiency around the resonant tank frequency.

LLC parameters summary:

Transformer transfer ratio	$\boldsymbol{n} = 16$
Transformer magnetizing inductance	$L_m = 195\ \mu H$
Resonant tank inductance	$L_{rn} = 15\ \mu H$
Resonant tank capacitance	$C_{rn} = 66\ nF$

3.4 LLC transfer function

The useful operating range of the LLC is in the frequency range where input impedance has an inductive character, shown in **Figure 6**. The input impedance angle is positive. The current lags behind the voltage, and enables use of the input current to charge/discharge MOSFET parasitic capacitances during turn-off.

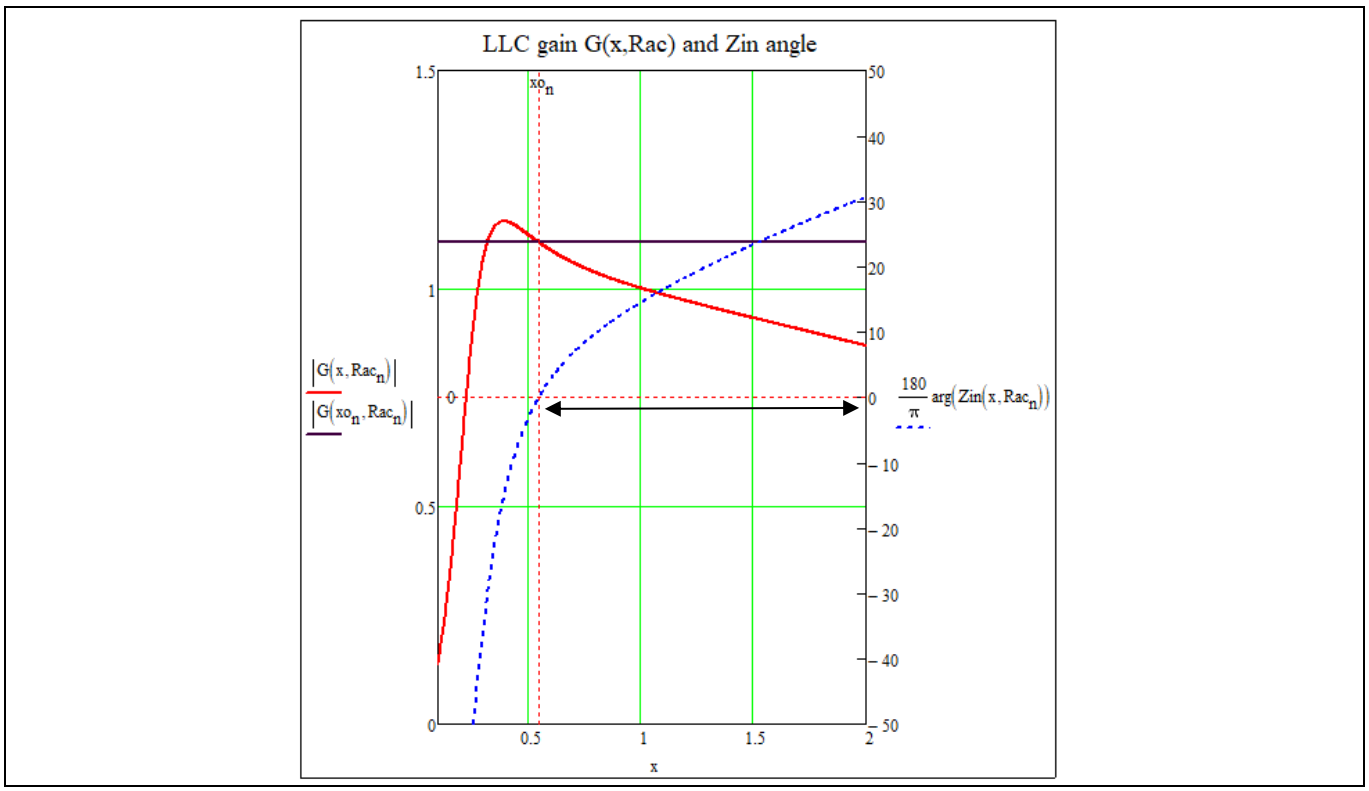

Figure 6 LLC useful operating range, marked with black arrow

Input voltage and input current are in phase at the boundary frequency (**Figure 7**). The question then naturally arises: How can ZVS exist in an LLC converter at boundary frequency, because the current is zero? This question cannot be answered in the FHA domain. A simulation of the LLC converter that includes more details that were disregarded during FHA approximation will provide the answer.

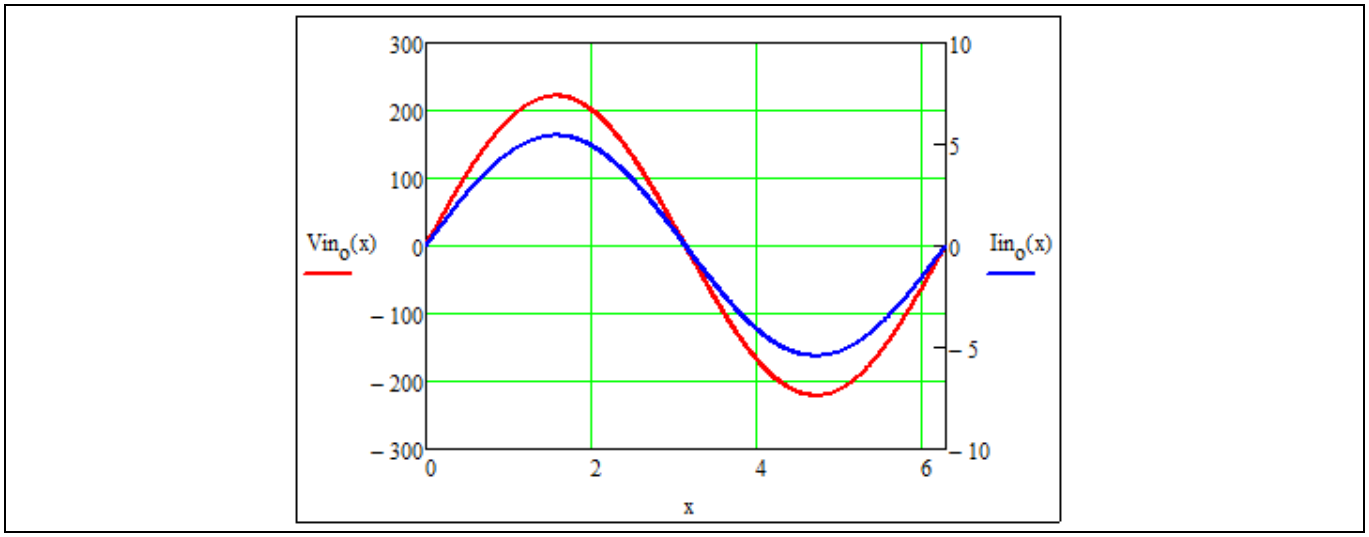

Figure 7 FHA: input voltage and input current at boundary frequency

4 Design verification using LTspice® simplified model

4.1 LTspice® simulation setup

Figure 8 shows a simplified HB LLC converter. The primary side of the LLC is modeled as a variable-frequency unipolar pulse with amplitude equal to the input voltage. The transformer has a unit transfer ratio to enable better convergence of the simulation and minimize the losses caused by the output diodes (D4, D5). Load is represented with the voltage source equal to the output voltage multiplied by the transformer ratio. The control loop is closed around the output power.

Input current information at the beginning of the switching cycle is very important, because it determines transition time from one switch to another. It is monitored using a sample-and-hold circuit, and measured at each positive edge of the input voltage. The output of the A1 sample-and-hold circuit is initial current (IO-current).

The sign of the input current is also monitored. When the sign is positive it means that LLC operates in the inductive mode; when the sign is negative, LLC operates in the capacitive mode. This is completed by the source B3.

Output power is also monitored using the sample-and-hold circuit. The intention is to minimize the size of the output filter and measure the power at the same point, and eliminate the impact of the ripple.

Operating frequency is calculated using bias current of the LTC6990. The output of the source B4 represents the operating frequency.

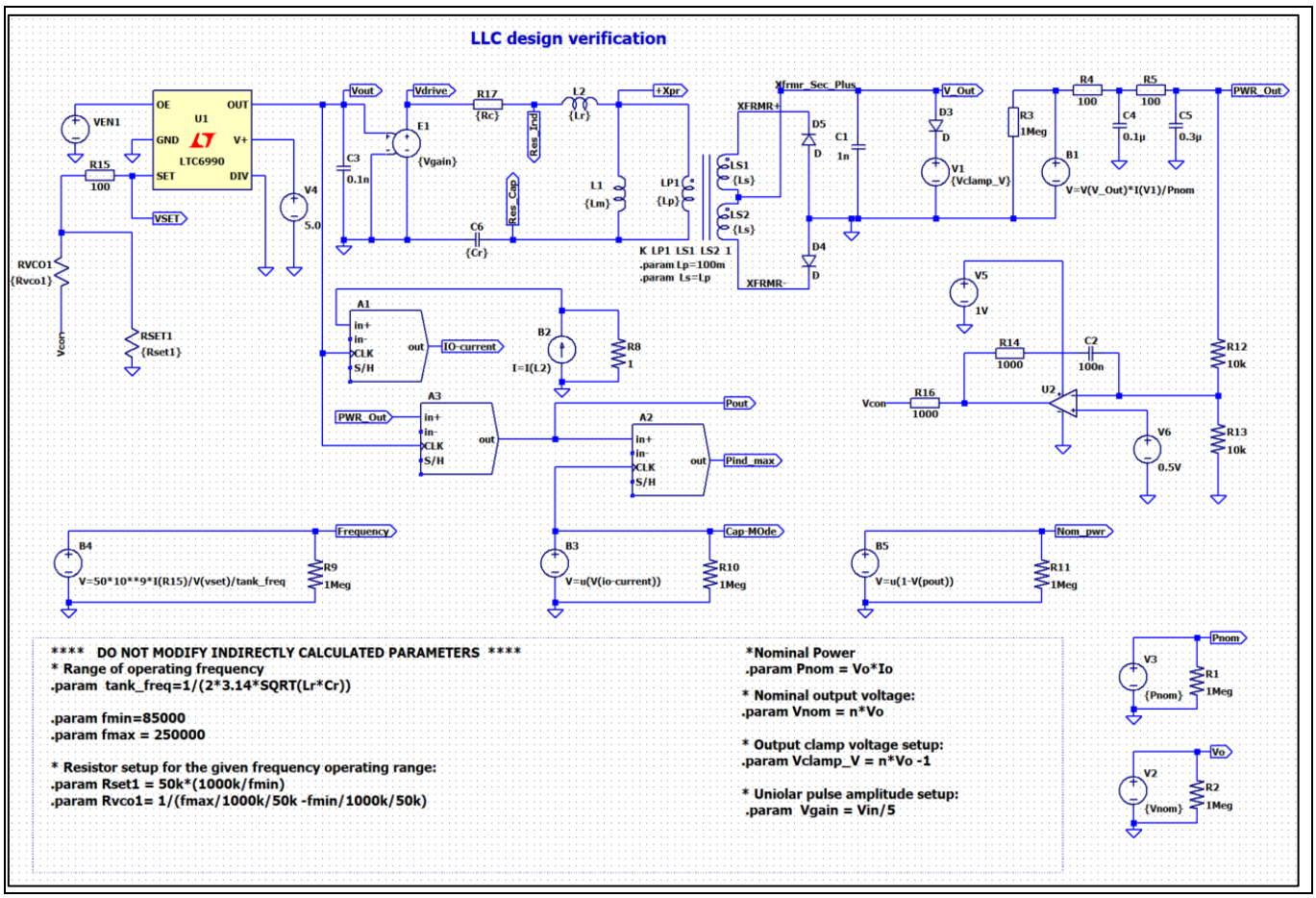

Figure 8 HB LLC simplified schematic

The script for variable setup simulation is self-explanatory. Voltage and current variables are taken from the specification, and LLC parameters are given by design output. Notice parameter R_c, which represents the $R_{DS(on)}$ of the MOSFET that would be selected in the design process.

```
* USER SUPPLIED TEST PARAMETERS - UPDATE HERE FOR YOUR VERIFICATION TEST
*********************************************************************
***LLC converter operating range***
* Minimum Input voltage:
.param  Vin =384

* Nominal output voltage:
.param  Vo = 12
.param    Io =50


***Parameters from LLC Calculator***
.param  Cr=66n
.param  Lr=15u
.param  Lm=192u

* Transfromer transfer ratio:
.param n = 16

*Conduction losses evaluation
.param Rc = 0.23
```

Figure 9 LLC parameters setup

The transient process of the LLC will be simulated (**Figure 10**).

```
*Transient simulation setup:
.PARAM Ts=8m;
.tran 0 {Ts} 0
.options plotwinsize=0 ;.options numdgt=7; .options maxstep 20n
```

Figure 10 Transient simulation setup

The key variables of the LLC operation are measured using built-in functions of LTspice®. The script is given in **Figure 11**. The names of the variables are given too, to easily correlate with the simulation schematic. When the simulation is complete, the results are found in the error log (**Figure 11**).

```
io: v(io-current )=-1.65574 at 0.0072
fop: AVG(v(frequency))=0.922392 FROM 0.0072 TO 0.008
i_l2_rms: RMS(i(l2))=3.8049 FROM 0.0072 TO 0.008
i_l2_peak: MAX(i(l2))=5.58368 FROM 0.0072 TO 0.008
i_l1_rms: RMS(i(l1))=0.980266 FROM 0.0072 TO 0.008
i_l1_peak: MAX(i(l1))=1.66896 FROM 0.0072 TO 0.008
i_d3_rms: RMS(i(d3))=3.68105 FROM 0.0072 TO 0.008
i_d3_avg: AVG(i(d3))=3.21795 FROM 0.0072 TO 0.008
i_d4_rms: RMS(i(d4))=2.59872 FROM 0.0072 TO 0.008
i_d4_avg: AVG(i(d4))=1.60651 FROM 0.0072 TO 0.008
```

Figure 11 Results for optimum operating conditions $V_{in} = V_{in.nom}$

```
* Measurements results found in .LOG file
**************************************************
*Initial current at nominal power
.MEASURE TRAN Io FIND V(io-current ) AT 0.9*Ts

*operating freguency
.MEASURE fop AVG(V(frequency))  from 0.9*Ts to Ts

*Key RMS variables
*Primary side current
.MEASURE I_L2_RMS RMS(I(L2))  from 0.9*Ts to Ts
.MEASURE I_L2_peak MAX(I(L2))  from 0.9*Ts to Ts

*Magnetizing current
.MEASURE I_L1_RMS RMS(I(L1))  from 0.9*Ts to Ts
.MEASURE I_L1_peak MAX(I(L1))  from 0.9*Ts to Ts

*Secondary side current
.MEASURE I_D3_RMS RMS(I(D3))  from 0.9*Ts to Ts
.MEASURE I_D3_AVG AVG(I(D3))  from 0.9*Ts to Ts

*Resonant capacitor voltage
.MEASURE V_Res_Cap_RMS RMS(V(res_cap))  from 0.9*Ts to Ts
.MEASURE V_Res_Cap_peak MAX(V(res_cap))  from 0.9*Ts to Ts
```

Figure 12 Measurements of key operating variables

4.2 Nominal operating conditions V_{in} = 384 V

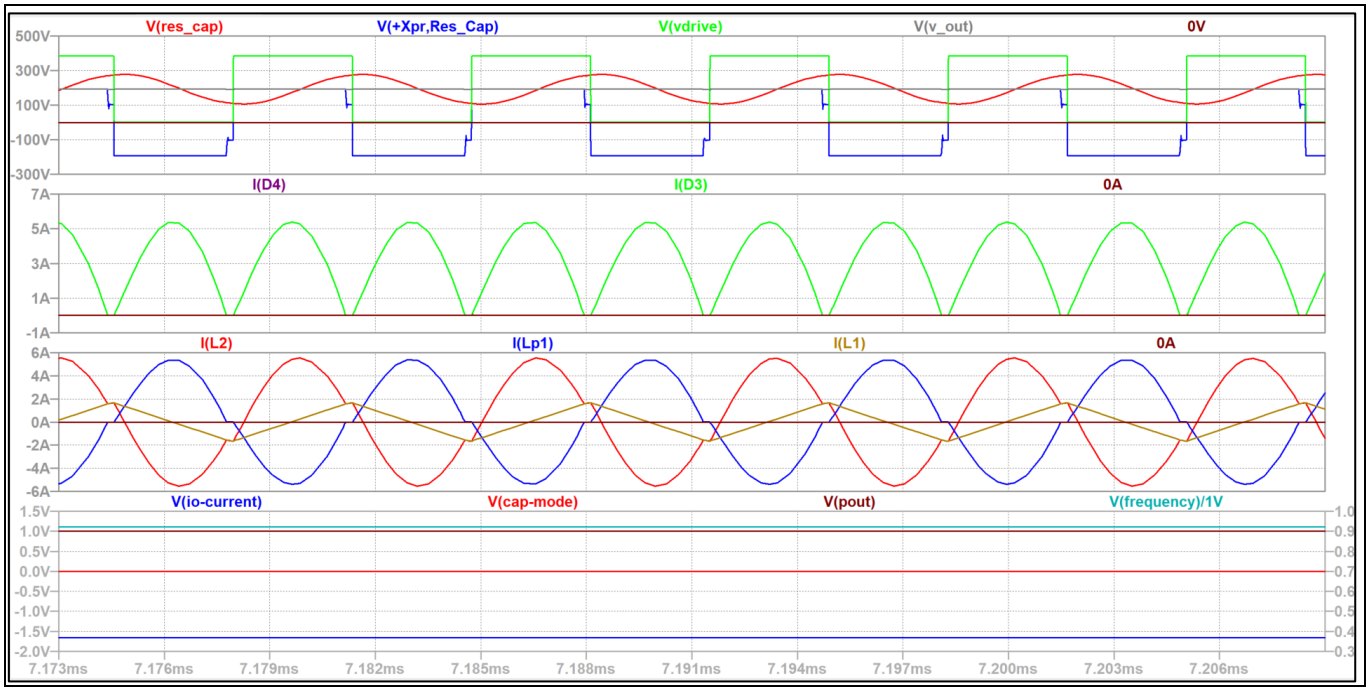

Figure 13 Key curves capture for optimum operating conditions V_{in} = V_{nom}

At nominal operating conditions V_{in} = 384 V, the LLC converter operates very close to the resonant tank frequency. The measurement summary is given in **Figure 11**:

Operating frequency is equal to f_{op} = 160 kHz * 0.922 = 147.5 kHz

Primary-side RMS current is equal to I_{RMSp} = 3.8 A

Secondary-side MOSFET RMS current is equal to the diode D4 current multiplied by n – I_{RMSs} = 2.6 * 16 = 41.6 A

4.3 Boundary operating conditions V_{in} = 350 V

At minimum input voltage V_{in} = 350 V, the LLC converter operates at the highest gain and highest RMS currents. The measurement summary is given in **Figure 14**, and waveforms are given in **Figure 15**:

Operating frequency is equal to f_{op} = 160 kHz * 0.652 = 104.3 kHz

Primary-side RMS current is equal to I_{RMSp} = 4.36 A

Secondary-side MOSFET RMS current is equal to I_{RMSs} = 3.07 * 16 = 49.1 A

To answer the question about initial current from **Figure 7**, note that initial current at minimum input voltage is different from zero (I_o = -1.88 A), and it is even higher than at nominal input voltage where (I_o = -1.65 A). This means that FHA fails to predict I_o, and this opens up a new area for optimizing LLC design.

```
io: v(io-current )=-1.88119 at 0.0072
fop: AVG(v(frequency))=0.652066 FROM 0.0072 TO 0.008
i_l2_rms: RMS(i(l2))=4.36045 FROM 0.0072 TO 0.008
i_l2_peak: MAX(i(l2))=7.42768 FROM 0.0072 TO 0.008
i_l1_rms: RMS(i(l1))=1.24199 FROM 0.0072 TO 0.008
i_l1_peak: MAX(i(l1))=1.90305 FROM 0.0072 TO 0.008
i_d3_rms: RMS(i(d3))=4.34262 FROM 0.0072 TO 0.008
i_d3_avg: AVG(i(d3))=3.22401 FROM 0.0072 TO 0.008
i_d4_rms: RMS(i(d4))=3.07386 FROM 0.0072 TO 0.008
i_d4_avg: AVG(i(d4))=1.61778 FROM 0.0072 TO 0.008
```

Figure 14 Results for boundary operating conditions V_{in} = $V_{in.min}$

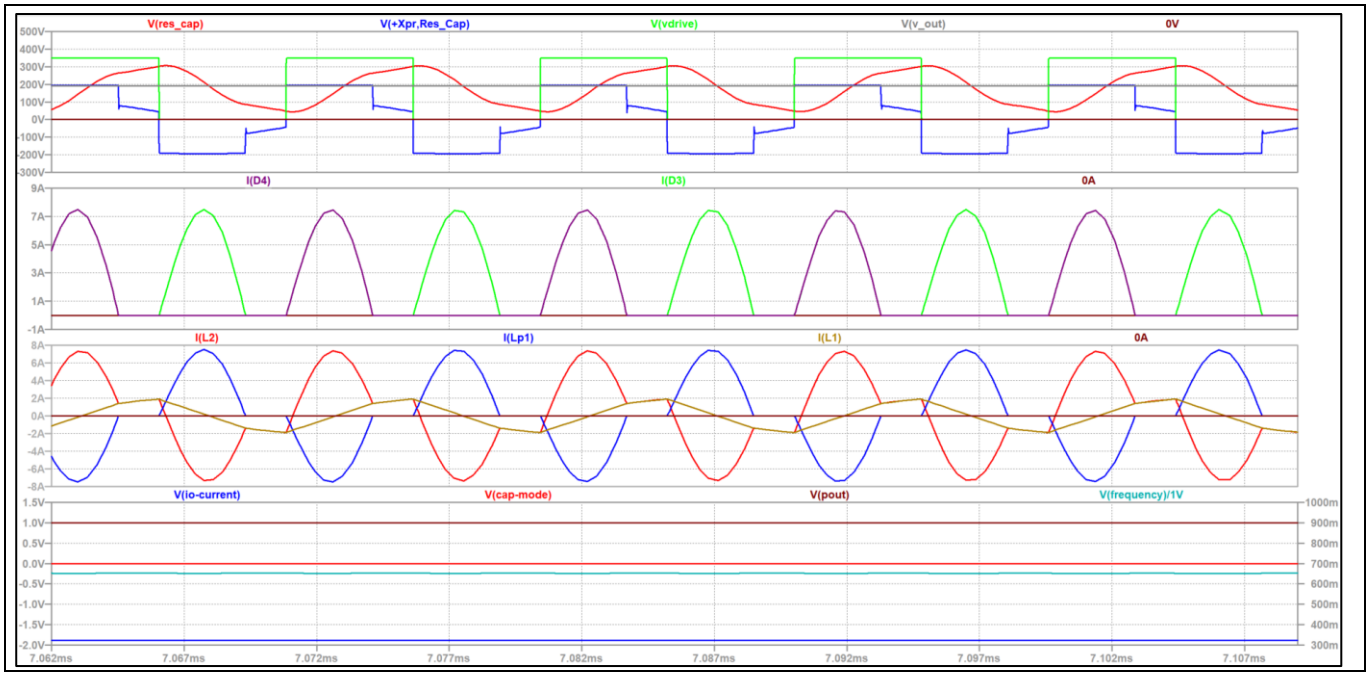

Figure 15 Key curves capture at boundary operating conditions V_{in} = $V_{in.min}$

4.4 LLC model comparison: FHA versus LTspice® simulation

FHA describes the behavior of the LLC very well around resonant tank frequency. The gain of LLC is close to one. Due to the LLC operation that requires higher gain, larger than one, operating frequency moves below resonant tank frequency. FHA becomes less accurate and the discrepancy between FHA and real LLC becomes more apparent. On the other hand, LTspice® simulation represents real LLC much better. LLC half-bridge is replaced by unipolar pulse. The only discrepancy is LLC switching losses, because they are not taken into account with this model. **Figure 16** shows that real LLC gain is higher than the FHA model predicts. Yellow points on **Figure 16** identify operating conditions when the FHA model changes from inductive to capacitive mode.

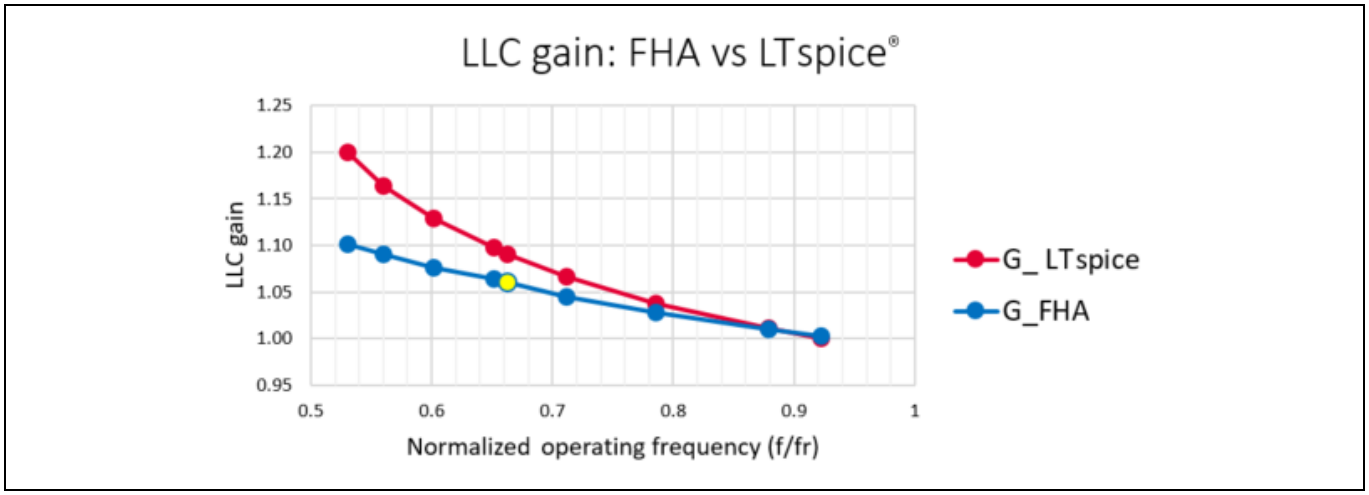

Figure 16 LLC gain: model comparison

Changing mode means that the initial current changes sign from negative to positive. Yellow points on **Figure 17** identify that condition. A more accurate LLC converter model, such as LTspice® simulation, shows that the current stays negative when the FHA model reaches crossover point.

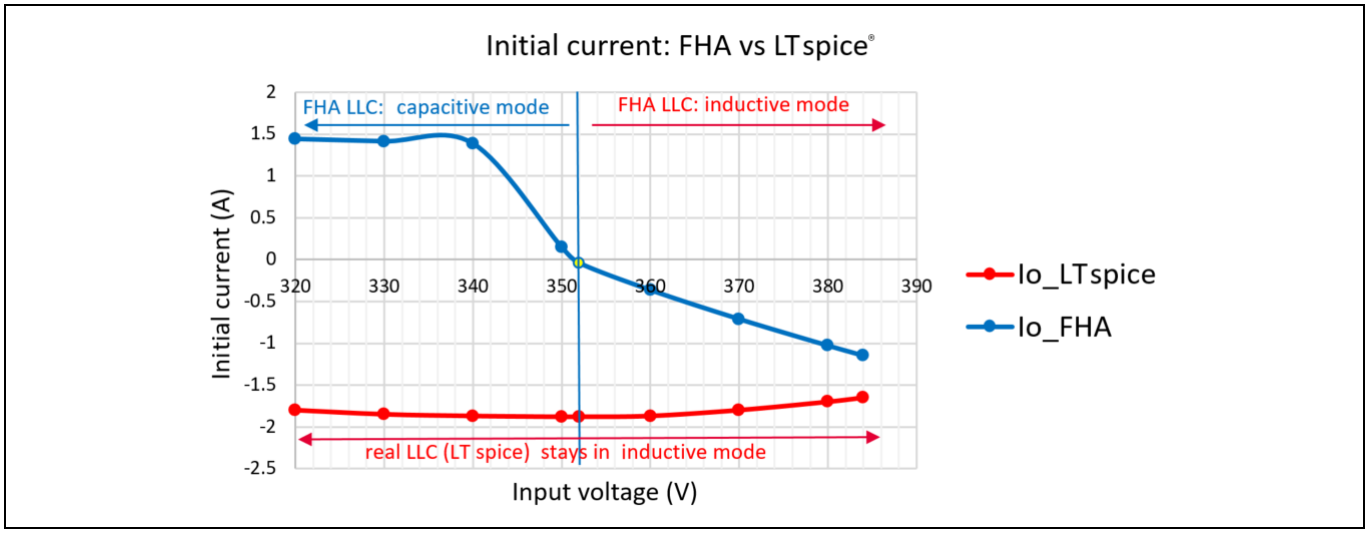

Figure 17 LLC initial current: model comparison

The results in **Figures 16** and **17** show that using FHA for LLC design provides a good margin. LLC can deliver much more power and still stay in the inductive mode, and/or transfer power from the much lower input voltage. This opens up new possibilities to optimize LLC design, such as designing a FHA LLC converter for lower power, and/or increasing transformer magnetizing inductance, and/or changing ratio between minimum operating frequency and resonant tank frequency. See references **[3]**, **[4]**.

5 MOSFET selection

LLC will operate close to the resonant tank frequency at nominal operating conditions. The operating frequency of the LLC converter is $f_{sw} \leq f_r$. Conduction losses dominate on the LLC switches because ZVS turn-on condition switching losses are much smaller than conduction losses. Conduction losses will be used as a criteria to select the MOSFET $R_{DS(on)}$. On the other side, the MOSFET will bring parasitic output capacitance $C_{o(tr)}$ that needs to be charged/discharged during each switching cycle, lowering the interval when power is transferred to the secondary side.

The algorithm to calculate RMS current values is based on the FHA. The results will be compared with the simulation results generated above.

5.1 Primary-side MOSFET $R_{DS(on)}$ selection

Conduction losses are equal to the product of the MOSFET resistance when $R_{DS(on)}$ and RMS current pass through it:

$$P_c = R_{dson} * {I_{rms}}^2 \qquad (27)$$

RMS currents on the primary and secondary side are calculated using the FHA approximation. RMS current on the primary side has two components: transformer magnetizing current and reflected secondary current. Magnetizing current is given as:

$$i_m = I_{pk} * (4 * t * f_{sw} - 1)\ when\ 0 \leq t \leq T_{sw}/2$$

Where:

$$I_{pk} = \frac{n * V_{o.nom}}{4 * L_m * f_{sw}} \qquad (28)$$

Reflected secondary-side current is half sinewave:

$$i_{Rp} = \frac{\pi}{2} I_o * \sin(2 * \pi * f_r * t)\ when\ 0 \leq t \leq T_{sw}/2$$

Where:

$$I_o = \frac{Po}{n * V_{o.nom}} \qquad (29)$$

Then primary-side RMS current is given as:

$$I_{pr.rms} = \sqrt{(\frac{\pi}{2*\sqrt{2}} I_o)^2 + \frac{{I_{pk}}^2}{3}} = 3.61\ A \qquad (30)$$

MOSFET selection criteria are based on conduction losses. The $R_{DS(on)}$ is selected in the way that total conduction losses are smaller than a certain percentage of the total power. Having in mind high demand for efficiency (η = 97.5 percent), we have assigned 20 percent of the total LLC losses to the primary-side MOSFET conduction, which translates to:

$$R_{dson.T} * {I_{rms}}^2 = k_R * P_o \qquad (31)$$

k_R – conduction losses coefficient, typical value $k_R = 0.005$ or 0.5 percent

$R_{DS(on)}$ of the MOSFET is changing with temperature. $R_{DS(on).T}$ represents resistance at a certain junction temperature:

$$R_{DS(on).T} = R_{DS(on)} * k_T \qquad (32)$$

$R_{DS(on)}$ – MOSFET on-resistance at $T_j = 25°C$

We will use $k_T = 1.3$ for CoolMOS™ junction temperature $T_j = 75°C$

MOSFET $R_{DS(on)}$ selection based on criteria that conduction losses are less than 0.5 percent of output power gives:

$$R_{DS(on)} = \frac{k_R * P_o}{k_T * {I_{pr.rms}}^2} = 177\text{m}\Omega \qquad (33)$$

Let's select IPP60R180P7. It has $R_{DS(on)}$ = 180 mΩ, and $C_{o(tr)}$ = 381 pF.

5.2 Primary-side MOSFET: impact of $C_{o(tr)}$

LLC operates in a certain frequency range that can be characterized by three typical frequencies:

1. Minimum operating frequency (boundary frequency) related to the maximum LLC gain,
2. Resonant tank operating frequency – related to the optimum operating point, and
3. Maximum operating frequency – related to the burst mode of operation.

When LLC operates at maximum frequency the magnetizing current is at a minimum and it takes the longest time to commutate current from one side switch to the other side switch. This commutation time should not take more than 10 percent of the switching cycle. That impact could be quantified using this equation, which connects the dead time and switching cycle:

$$T_d = k_d * T_{sw} \qquad (34)$$

Maximum frequency is selected in the way that $k_d \leq 7.5\ percent$. The maximum frequency, where dead time takes the k_d portion of the switching cycle, is given as:

$$f_{max} = \sqrt{\frac{k_d}{16 * L_m * C_o(tr)}} = 251kHz \qquad (35)$$

This is very close to the specified maximum operating frequency of 250 kHz.

5.3 Secondary-side MOSFET: $R_{DS(on)}$ selection

Selection of the SR MOSFETs depends on required peak efficiency. The objective is to achieve peak efficiency at 50 percent load. It is demonstrated in **Figure 18**, below. **BSC010N04LS** is selected, which is the best-in-class SuperSO8 MOSFET from Infineon's latest OptiMOS™ 40 V family. A quick evaluation, below, shows that the best option consisted of paralleling two such MOSFETs per synchronous rectification (SR) branch.

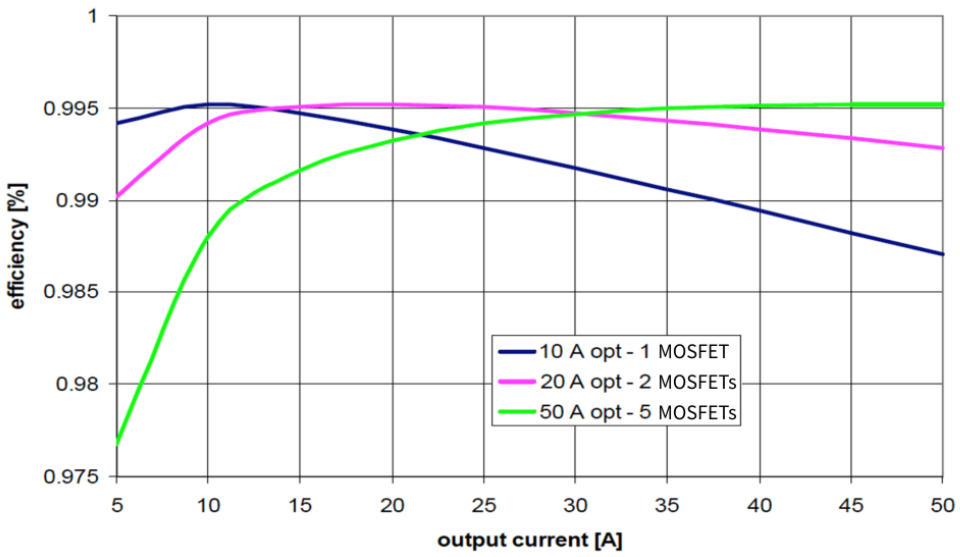

Figure 18 Impact of the total SR MOSFET $R_{DS(on)}$ on efficiency profile

There are two dominant loss mechanisms for SR MOSFETs – the conduction and gate driving losses. The best solution is a balance between these two loss mechanisms. High $R_{DS(on)}$ will take advantage of the light load, because it will minimize gate driving losses. On the other hand, low $R_{DS(on)}$ will take advantage of the full load by reducing conduction losses.

We shall use the FHA waveforms that will lead to the following formulas to compute the total conduction losses (P_{cond}) generated by the SR MOSFETs:

$$P_{cond} = 2 \times I_{RMS}^2 \times \frac{R_{DS(on).T}}{N} \quad (36)$$

Where:

$$I_{RMS} = I_{OUT} \times \frac{\pi}{4} = 39.3A \quad (37)$$

$$R_{DS(on).T} = R_{DS(on)} * k_T \quad (38)$$

N is the number of paralleled FETs per SR branch.

Factor 2 highlights that we have two SR branches in our center-tap configuration.

$R_{DS(on)}$ is the MOSFET on-resistance at $T_j = 25°C$.

$k_T = 1.25$ for OptiMOS™ junction temperature $T_j = 75°C$.

Gate drive switching losses are given as:

$$P_{gate} = 2 \times N \times Q_{g(sync)} \times U_g \times f_{sw} \quad (39)$$

P_{gate} is dependent on the gate charge $Q_{g(sync)}$, the gate driving voltage U_g and the switching frequency f_{sw}. The factors 2 and N were already defined for P_{cond}.

In SR, because no plateau exists on the gate waveform, using $Q_{g(sync)}$ instead of the more familiar total gate charge Q_g provides a more accurate representation of the gate driving losses.

For a 600 W demo board, U_g = 12 V, whereas f_{sw} = 150 kHz if the input voltage is 380 V. Moreover, with a driving voltage of 12 V, $Q_{g(sync)}$ = 102 nC for BSC010N04LS. In addition to that, as a first approximation, we have neglected the variation of f_{sw} and $R_{DS(on)}$ with the load.

The table below shows that two MOSFETs in parallel will give the lowest overall losses at 50 percent load. The gate losses dominate, and adding more MOSFETs just brings more overall losses.

Table 2 Total losses table

At 50% P_{max}	Conduction losses P_{cond}	Gate driving losses P_{gate}	P_{cond} + P_{gate}
1 x BSC010N04LS per SR branch	771 mW	367 mW	1138 mW
2 x BSC010N04LS per SR branch	386 mW	734 mW	1120 mW
3 x BSC010N04LS per SR branch	257 mW	1102 mW	1359 mW

5.4 FHA calculation vs. LTspice® simulation

Comparing RMS current calculation using FHA approximation and LTspice® simulation shows that the difference is on the primary side (3.6 A/3.8 A = 0.947) and secondary side (39.3/41.6 = 0.944) in the range of 5 percent. This difference will bring the error in the prediction of conduction losses to about 10 percent. It means that for quick calculations, FHA approximation could be used, but for more accurate prediction of the conduction losses simulation is necessary.

6 Summary

This application note has used simple algorithms for LLC design. It is based on the FHA model. The novel vector method provided simple formulas to calculate LLC parameters. The essence of the vector method is to use the input impedance angle between voltage and current on the primary side of the LLC converter as a key variable to distinguish operating modes of the LLC and determine the boundary condition between inductive and capacitive modes of operation. The major benefit of this method is simplicity and clarity.

The vector method is based on the FHA and AC circuit analysis. The critical transfer point between inductive and capacitive modes is identified as a simple vector criterion, where the inverse transfer function vector and the vector of serial combinations of load components are orthogonal. A simple set of equations followed this conclusion.

The calculation procedure becomes straightforward. Key formulas are derived by using simple trigonometry. The minimum operating frequency (ω_o) is such that it gives a minimum size for the resonant tank. A simple design procedure follows through calculations of LLC parameters.

FHA was also used to calculate RMS currents based on sine waveforms. The FHA RMS calculations are compared with simulation results. The error is in the range of 10 percent, and justifies use of the FHA method for quick calculations.

MOSFET selection is based on budgeted losses to achieve required efficiency. The primary-side MOSFET is selected based on conduction losses being around 0.5 percent of nominal output power, while selection of the SR MOSFETs was based on the criteria to achieve maximum efficiency at 50 percent of load.

The design algorithm has the following steps:

1. Provide basic specification for the LLC converter:
    a. Input voltage range
    b. Output voltage
    c. Output power
    d. Efficiency
    e. Frequency operating range
2. Select LLC topology option:
    a. Full-bridge or half-bridge
3. Calculate performance parameters of the LLC:
    a. Transformer transfer ratio $\boldsymbol{n}$ – equation (19)
    b. LLC gain $\boldsymbol{G(\omega_o)}$ – equation (20)
    c. Equivalent AC load $\boldsymbol{R_{AC}}$ – equation (21)
4. Calculate property parameters of LLC:
    a. Magnetizing inductance $\boldsymbol{L_m}$ – equation (22)
    b. Resonant tank inductance $\boldsymbol{L_r}$ – equation (23)
    c. Resonant tank capacitance $\boldsymbol{C_r}$ – equation (24)
        i. Close the loop to select standard value capacitor – equations (25) and (26)
5. Calculate RMS current variables on primary (equation (30)) and secondary side (equation (37)).
6. Select primary-side MOSFETs based on loss budget – equation (33).
7. Select secondary-side MOSFETs based on minimum losses at 50 percent load (total losses in **Table 2**).
8. Verify design using LTspice® simulation.

Summary

Design and optimization are based on the FHA approximation. The LLC optimization could be done using different criteria. More optimization options for the LLC design are covered in reference [3].

7 References

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