Fifth-generation QR design guide

Design guide - ICE5QSxG and ICE5QRxxxxxx

About this document

Scope and purpose

This document is a design guide for a QR Flyback converter using Infineon's latest fifth-generation QR controllers, ICE5QSxG and CoolSET™ ICE5QRxxxxxx, which offer high-efficiency, low-standby power with selectable entry and exit standby power options, wide V_{CC} operating range with fast start-up, robust line protection with input Over Voltage Protection (OVP), brown-out and various protection modes for a highly reliable system.

Intended audience

This document is intended for power-supply design/application engineers, students, etc. who wish to design power supplies with fifth-generation QR controllers, ICE5QSxG and CoolSET™ ICE5QRxxxxxx.

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Abstract

1 Abstract

This is a design guide for a QR Flyback converter using ICE5QSxG/ICE5QRxxxxxx, the fifth-generation QR PWM controller/CoolSET™ developed by Infineon.

The IC is optimized for off-line SMPS applications such as home appliances/white goods, TVs, PCs, servers, Blu-ray players, set-top boxes and notebook adapters. The improved digital frequency reduction with proprietary QR operation offers lower EMI and higher efficiency for a wide AC range by reducing the switching frequency difference between low-line and high-line. The enhanced Active Burst Mode (ABM) power enables flexibility not only in standby power operation range selection but also QR switching, even in burst mode. The product has a wide operating range (10 V~25.5 V) of IC power supply and lower power consumption. The numerous protection functions including robust line protection with input OVP and brown-out give full protection to the power-supply system in failure situations. All of these make the ICE5QSxG an outstanding controller on the market for QR Flyback converters.

2 Description

2.1 List of features

- Integrated 700 V/800 V avalanche rugged CoolMOS™[1]
- New QR operation and propriety implementation for low EMI
- Enhanced ABM with selectable entry and exit standby power
- ABM to reach the lowest standby power < 100 mW
- Fast start-up achieved with cascade configuration
- Digital frequency reduction for better overall system efficiency
- Built-in digital soft-start
- Cycle-by-cycle Peak Current Limitation (PCL)
- Maximum on-/off-time limitation to avoid audible noise during start-up and power-down
- Robust line protection with input OVP and brown-out
- Auto-restart mode protection for V_{CC} Over Voltage (OV), V_{CC} Under Voltage (UV), over-load/open-loop, output OV, over-temperature
- Limited charging current for V_{CC} short-to-GND
- Pb-free lead plating, halogen-free mold compound, RoHS compliant

2.2 Pin layout

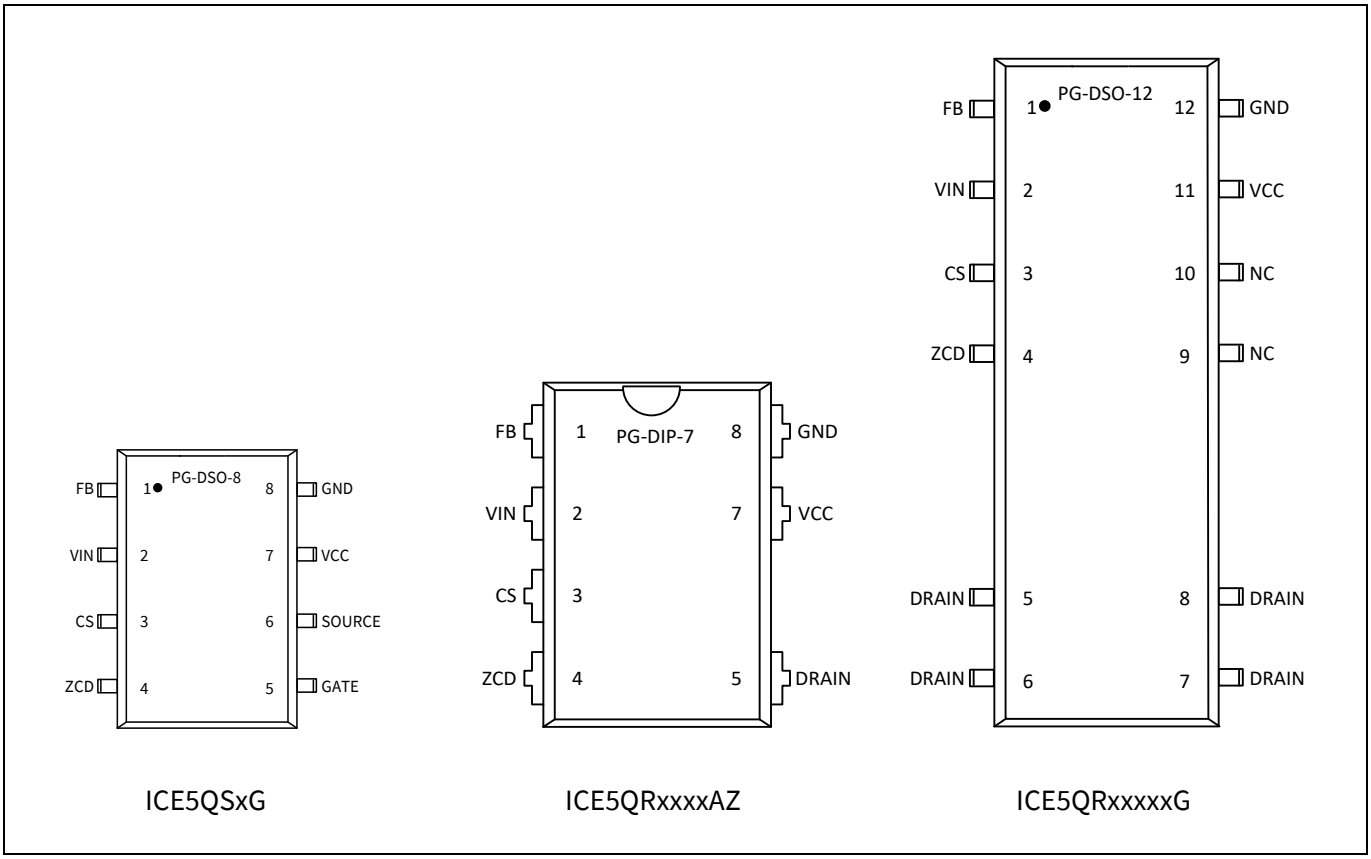

Figure 1 Pin configuration

[1] CoolSET™ only

2.2.1 Feedback and burst entry/exit control

The feedback (FB) pin combines the functions of FB loop control, selectable burst entry/exit control and over-load/open-loop protection.

2.2.2 V_{IN} (input line OVP and brown-out)

The V_{IN} pin is connected to the bus via a resistor divider (see Figure 2) to sense the line voltage. This pin combines the functions of input-line OVP, brown-out and minimum Zero Crossing (ZC) count setting for low-line and high-line.

2.2.3 Current Sense (CS)

The CS pin is connected to the shunt resistor for the primary current sensing externally and to the PWM signal generator block for switch-off determination (together with the FB voltage) internally.

2.2.4 Zero Crossing Detection (ZCD)

The ZCD pin combines the functions of start-up, ZCD and output OVP. During start-up, it is used to provide a voltage level to the gate of the power-switch CoolMOS™ to charge the V_{CC} capacitor.

2.2.5 Gate (gate drive output, controller only)

The gate pin is the output of the internal driver stage, which has a rise time of 117 ns and a fall time of 27 ns when driving a 1 nF capacitive load.

2.2.6 Source (source, controller only)

The source pin is connected to the source of the external power switch Q1 (see Figure 2), which is in series connection with the internal low-side MOSFET and internal V_{CC} diode D.

2.2.7 Drain (drain, CoolSET™ only)

The drain pin is connected to the drain of the integrated 700 V/800 V CoolMOS™.

2.2.8 V_{CC} (positive voltage supply)

The V_{CC} pin is the positive voltage supply to the IC. The operating range is 10 V~25.5 V.

2.2.9 GND (ground)

The GND pin is the common ground of the controller/CoolSET™.

3 Overview of the QR Flyback converter

Figure 2 and Figure 3 show a typical application of ICE5QSxG and ICE5QRxxxxxx in a QR Flyback converter. In this converter, the mains input voltage is rectified by the diode bridge and then smoothed by the capacitor C_{bus} where the bus voltage V_{bus} is available. The transformer has one primary winding W_p, one or more secondary windings W_{s1} and W_{s2} and one auxiliary winding W_a. When QR control is used for the Flyback converter, the typical waveforms are shown in Figure 4. The voltage from the auxiliary winding provides information about demagnetization of the power transformer and the output voltage.

As shown in Figure 4, after switch-on of the power switch the voltage across the shunt resistor R_{CS} shows a spike caused by the discharging of the drain-source capacitor. After the spike, the voltage V_{CS} shows information about the real current through the main inductance of the transformer L_p. Once the measured current signal V_{CS} exceeds the maximum value determined by the FB voltage V_{FB}, the power switch is turned off. During this on-time, a negative voltage proportional to the input bus voltage is generated across the auxiliary winding.

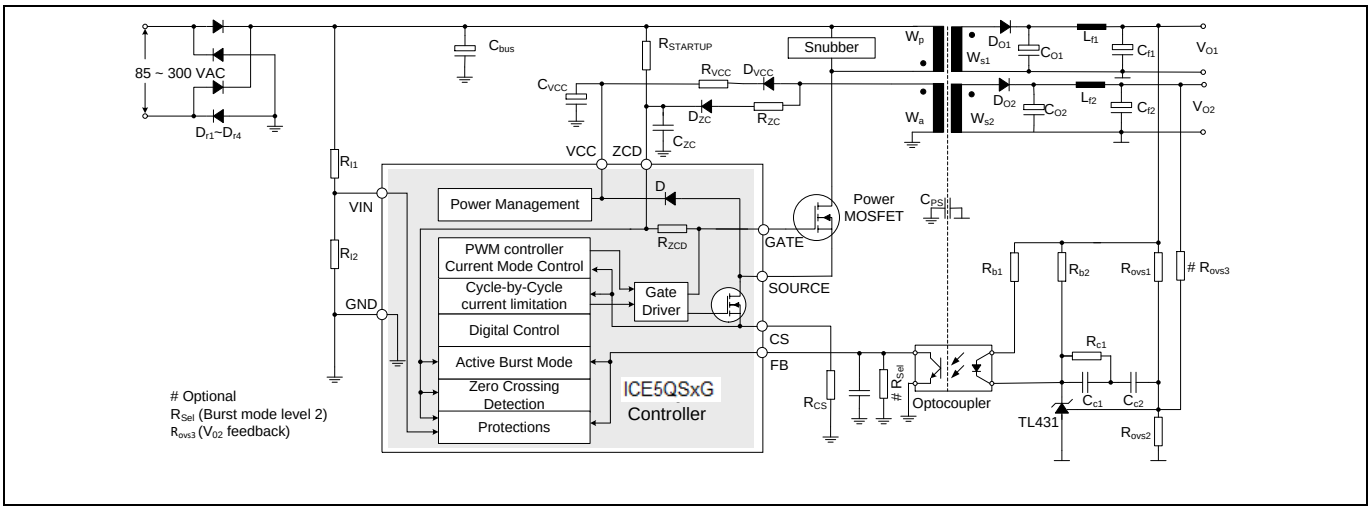

Figure 2 Typical application of controller

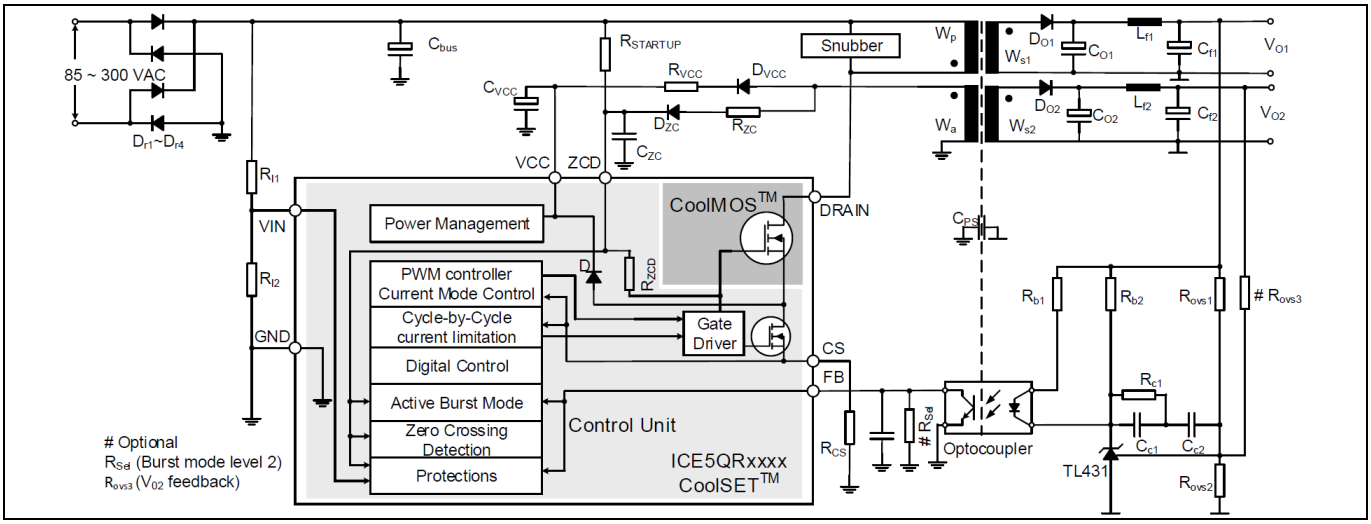

Figure 3 Typical application of CoolSET™

The drain-source voltage of the power switch V_{DS} will rise very fast after the MOSFET is turned off. This is caused by the energy stored in the leakage inductance of the transformer. A snubber circuit, RCD in most cases, can be used to limit the maximum drain-source voltage. After oscillation 1, the drain-source voltage goes to its steady value. Here, the voltage v_R is the reflected value of the secondary voltage at the primary side of the transformer, and is calculated as:

$$V_R = \frac{(V_{out} + V_{FOut}) \times N_P}{N_S} \quad \textbf{(Eq. 23)}^1$$

where, V_R : reflected voltage

V_{out} : output voltage

V_{FOut} : forward voltage of the secondary diode

N_P : number of primary turns of the transformer

N_S : number of secondary turns of the transformer

After oscillation 1 is damped, the drain-source voltage of the power switch shows a constant value of $V_{bus} + V_R$ until the transformer is fully demagnetized. This duration builds up the first portion of the off-time t_{off1}.

After the secondary-side current falls to zero, the drain-source voltage of the power switch shows another oscillation (oscillation 2 in Figure 4; this is also mentioned as the main oscillation in this document). This oscillation happens in the circuit consisting of the equivalent main inductance of the transformer L_p and the capacitor across the drain-source (or drain-GND) terminal C_{DS}, which includes $C_{o(er)}$ of the MOSFET. The frequency of this oscillation is calculated as:

$$f_{OSC2} = \frac{1}{2\pi \times \sqrt{L_P \times C_{DS}}} \quad \textbf{(Eq. 109)}$$

where, f_{OSC2} : oscillation 2 in Figure 4

L_P : primary main inductance of the transformer

C_{DS} : capacitance across drain-to-source/GND of the power switch

The amplitude of this oscillation begins with a value of v_R and decreases exponentially with the elapsing time, which is determined by the losses factor of the resonant circuit. The first minimum of the drain voltage appears at half of the oscillation period after the time t_4 and can be approximated as:

$$V_{DS\_Min} = V_{bus} - V_R \quad \textbf{(Eq. 110)}$$

In the QR control, the power switch is switched on at the minimum of the drain-source voltage. From this kind of operation, the switching-on losses are minimized, and switching noise due to dV_{DS}/dt is reduced compared to a normal hard-switching Flyback converter.

[1] Equation is used in Section 8 (fifth-generation QR FLYCAL design example)

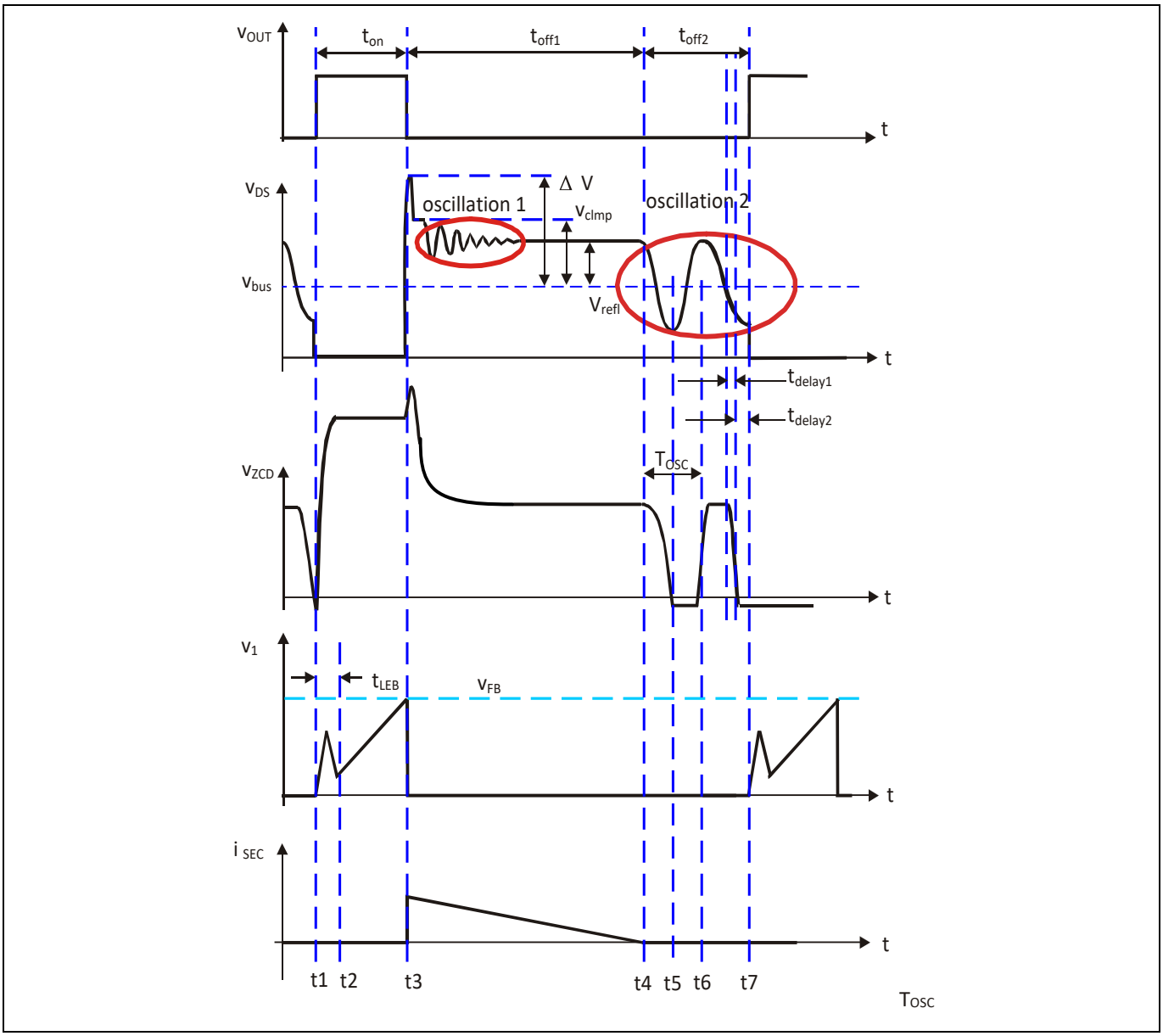

Figure 4 Typical waveforms of the fifth-generation QR Flyback converter

4 Functional description and component design

4.1 V_{CC} pre-charging and typical V_{CC} voltage during start-up

When AC-line input voltage is applied as shown in Figure 2 and Figure 3, a rectified voltage appears across the capacitor $C_{bus.}$ The pull-up resistor $R_{START-UP}$ provides a current to charge the C_{iss} (input capacitance) of the power switch and gradually generate one voltage level. If the voltage over C_{iss} is high enough, power switch-on and the V_{CC} capacitor will be charged through primary inductance of transformer L_P, the power switch and the internal diode with two steps of constant current source $I_{VCC\_Charge1}$[1] and $I_{VCC\_Charge3}$[1].

A very small constant current source ($I_{VCC\_Charge1}$) is charged to the V_{CC} capacitor until V_{CC} reaches V_{CC_SCP} to protect the controller from V_{CC} pin short-to-GND during start-up. After this, the second step of constant current source ($I_{VCC\_Charge3}$) is provided to charge the V_{CC} capacitor further, until the V_{CC} voltage exceeds the turn-on threshold V_{VCC_ON}. As shown in the time phase I in Figure 5, the V_{CC} voltage increases almost linearly, in two steps.

Note: Recommended typical value for $R_{START-UP}$ is 50 MΩ (20 MΩ~100 MΩ), and the $R_{START-UP}$ value is directly proportional to $t_{Start-up}$ and inversely proportional to no-load standby power.

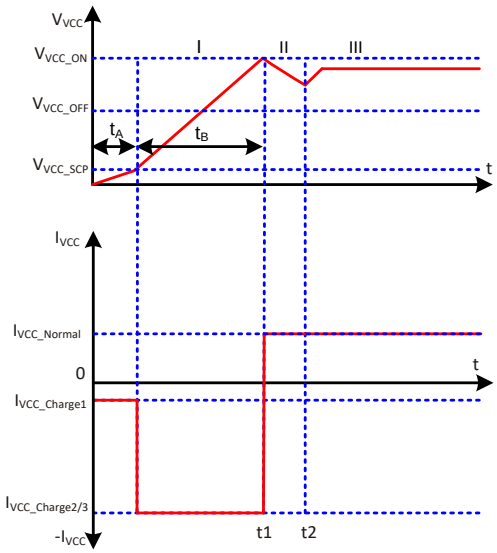

Figure 5 V_{CC} voltage and current at start-up

The time taken for V_{CC} pre-charging can then be approximately calculated as:

$$t_{\mathrm{StartUp}} = t_{\mathrm{A}} + t_{\mathrm{B}} = \frac{V_{VCC\_SCP} \cdot C_{VCC}}{I_{VCC\_Charge1}} + \frac{(V_{VCC\_ON} - V_{VCC\_SCP}) \cdot C_{VCC}}{I_{VCC\_Charge3}} \qquad \textbf{(Eq. 56B)}^{2}$$

where, V_{VCC_SCP} : V_{CC} short-circuit protection voltage

C_{VCC} : V_{CC} capacitor

V_{VCC_ON} : V_{CC} turn-on threshold voltage

$I_{VCC\_Charge1}$: V_{CC} charge current 1

$I_{VCC\_Charge3}$: V_{CC} charge current 3

[1] $I_{VCC\_Charge1/2/3}$ is charging current from the controller to the V_{CC} capacitor during start-up

[2] Equation is used in Section 8 (fifth-generation QR FLYCAL design example)

When the V_{CC} voltage exceeds the V_{CC} turn-on threshold V_{VCC_ON} at time t_1, the IC begins to operate with a soft-start. Due to the power consumption of the IC and the fact that there is still no energy from the auxiliary winding to charge the V_{CC} capacitor before the output voltage is built up, the V_{CC} voltage drops (phase II). Once the output voltage is high enough, the V_{CC} capacitor receives the energy from the auxiliary winding from the time t_2 onward and delivering the I_{VCC_Normal}[1] to the controller. The V_{CC} will then reach a constant value depending on the output load.

4.1.1 V_{CC} capacitor

Since there is a V_{CC} Under Voltage Protection (UVP), the capacitance of the V_{CC} capacitor should be selected to be high enough to ensure that enough energy is stored in the V_{CC} capacitor so that the V_{CC} voltage will never touch the V_{CC} UVP threshold V_{VCC_OFF} before the output voltage is built up. Therefore, the minimum capacitance should fulfill the following requirement:

$$C_{VCC} > \frac{I_{VCC\_Charge3} \times t_{ss}}{V_{VCC\_ON} - V_{VCC\_OFF}} \quad \textbf{(Eq. 56A)}^2$$

where, $I_{VCC\_Charge3}$: V_{CC} charge current 3

t_{ss} : soft-start time

4.2 Soft-start

After the supply voltage of IC is higher than 16 V, which corresponds to t_1 of Figure 5, the IC will start with a soft-start. The soft-start function is digitally built into the IC. During soft-start, the peak current of the power switch is controlled by an internal voltage reference instead of the voltage on the FB pin. The maximum voltage on the CS pin for peak current control is increased step by step, as shown in Figure 6. The maximum duration of soft-start is 12 ms, with 3 ms for each step. During soft-start, the over-load protection function is disabled.

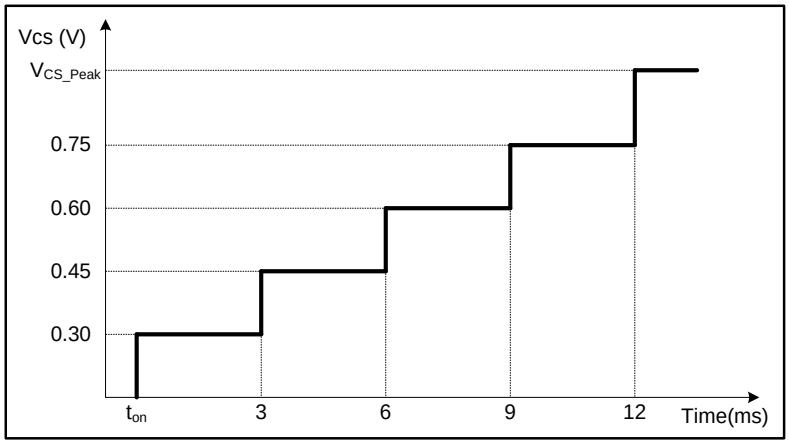

Figure 6 Maximum CS voltage during soft-start

4.3 Normal operation

During normal operation, the IC consists of a digital signal-processing circuit including an up/down counter, a ZC counter and a comparator, and an analog circuit including a current measurement unit and a comparator. The switch-on and switch-off time points are determined by the digital circuit and the analog circuit,

[1] I_{VCC_Normal} is supply current from the V_{CC} capacitor or auxiliary winding to the controller during normal operation

[2] Equation is used in Section 8 (fifth-generation QR FLYCAL design example)

respectively. As input information for the switch-on determination, the ZC input signal and the value of the up/down counter are needed, while the FB signal V_{FB} and the current sensing signal V_{CS} are necessary for the switch-off determination. Details about the full operation of the controller in normal operation are given in the following paragraphs.

4.3.1 Digital frequency reduction

As mentioned above, the digital signal processing circuit consists of an up/down counter, a ZC counter and a comparator. These three parts are the key to implementing digital frequency reduction with decreasing load. In addition, a ringing suppression time controller is implemented to avoid mis-triggering by the HF oscillation, when the output voltage is very low under conditions such as the soft-start period or output short-circuit. Functionality of these parts is described as in the following paragraphs.

4.3.1.1 Minimum ZC count determination

To reduce the switching frequency difference between low-line and high-line, minimum ZC count determination is implemented. The minimum ZC count is set to 1 if V_{IN} is less than V_{IN_REF}, which represents low-line. For high-line, the minimum ZC count is set to 3 after V_{IN} is higher than V_{IN_REF}. There is also a hysteresis V_{IN_REF} with a certain blanking time t_{VIN_REF} for stable AC-line selection between low-line and high-line.

4.3.1.2 Up/down counter

The up/down counter stores the number of the ZC which determines valley numbers to switch on the main MOSFET after demagnetization of the transformer. This value is fixed according to the FB voltage V_{FB}, which contains information about the output power. Indeed, in a typical peak current mode control, a high output power results in a high FB voltage, and a low output power leads to a low FB voltage. Hence, according to V_{FB}, the value in the up/down counter is changed to vary the power MOSFET off-time according to the output power. The variation of the up/down counter value according to the FB voltage is explained below.

The FB voltage V_{FB} is internally compared with three threshold voltages V_{FB_LHC}, V_{FB_HLC} and V_{FB_R} at each clock period of 48 ms. The up/down counter then counts upward, remains unchanged or counts downward, as shown in Table 1.

Table 1 Operation of up/down counter

V_{FB}	Up/down counter action
Always lower than V_{FB_LHC}	Count upward until n = 8/10[1]
Once higher than V_{F_LHC}, but always lower than $V_{FB,HLC}$	Stop counting, no value changing
Once higher than V_{FB_HLC}, but always lower than V_{FB_R}	Count downward until n = 1/3[2]
Once higher than V_{FB_R}	Set up/down counter to n = 1/3[2]

The number of ZC is limited and therefore, the counter varies from 1 to 8 (for low-line) or 3 to 10 (for high-line), and any attempt beyond this range is ignored. When V_{FB} exceeds V_{FB_R} voltage, the up/down counter is reset to 1 (low-line) and 3 (high-line) in order to allow the system to react rapidly to a sudden load increase. The up/down counter value is also reset to 1 (low-line) and 3 (high-line) at the start-up time, to ensure an efficient maximum load start-up. Figure 7 shows some examples of how the up/down counter is changed over time according to the FB voltage.

The use of two different thresholds V_{FB_LHC} and V_{FB_HLC} to count upward or downward is to prevent frequency jittering when the FB voltage is close to the threshold point.

[1] n = 8 (for low-line) and n = 10 (for high-line)

[2] n = 1 (for low-line) and n = 3 (for high-line)

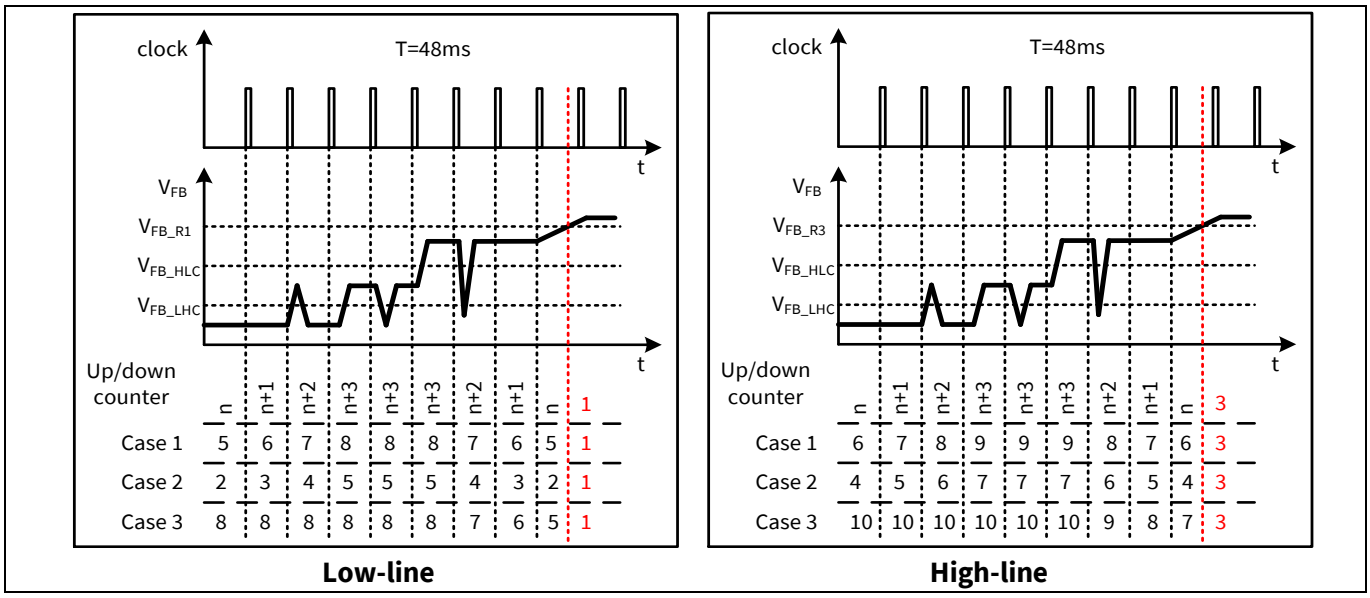

Figure 7 Up/down counter operation

4.3.1.3 Switch-on determination

After the gate drive goes to low, it cannot be changed to high during the ring suppression time.

After the ring suppression time, the gate drive can be turned on when the ZC counter value is equal to the up/down counter value.

However, it is also possible that the oscillation between the primary inductor and the drain-source capacitor damps very fast and the IC cannot detect ZC events. In this case, a maximum off-time is implemented. After the gate drive has remained off for the period of T_{OffMax}, the gate drive will be turned on again regardless of the ZC counter values and V_{ZCD}. This function can effectively prevent the switching frequency from going lower than 20 kHz. Otherwise it will cause audible noise.

4.3.2 Switch-off determination

In the converter system, the primary current is sensed by an external shunt resistor, which is connected between the source terminal of the internal low-side MOSFET and the common GND. The sensed voltage across the shunt resistor V_{CS} is applied to an internal current measurement unit, and its output voltage V_1 is compared with the FB voltage V_{FB}. Once the voltage V_1 exceeds the voltage V_{FB}, the output flip-flop is reset. As a result, the main power switch is switched off. The relationship between the V_1 and the V_{CS} is described by:

$$V_1 = G_{PWM} \cdot V_{CS} + V_{PWM} \quad \textbf{(Eq. 111A)}$$

where, V_1 : output voltage of comparator

G_{PWM} : PWM output gain

V_{CS} : voltage across the CS resistor

V_{PWM} : offset for voltage ramp

To avoid mis-triggering caused by the voltage spike across the shunt resistor at the turn-on of the main power switch, a Leading Edge Blanking (LEB) time, t_{LEB}, is applied to the output of the comparator. In other words, once the gate drive is turned on, the minimum on-time of the gate drive is the LEB time.

In addition, there is a maximum on-time t_{OnMax} limitation implemented in the IC. Once the gate drive has been in a high state longer than the maximum on-time, it will be turned off to prevent the switching frequency from going too low because of long on-time.

4.4 ABM with selectable power level

At light-load condition, the IC enters ABM operation to minimize power consumption. Details about ABM operation are explained in the following paragraphs.

The burst mode entry level can be selected by changing the different resistor R_{Sel} at the FB pin. There are two levels to be selected with different resistors, which are targeted for the lower range of ABM power (Level 1) and the higher range of ABM power (Level 2). The following table shows the control logic for the entry and exit level with the FB voltage.

Table 2 Two levels: entry and exit ABM power

Level	R_{Sel}	V_{FB}	V_{CS}	Entry level	Exit level
				V_{FB_EBLX}	V_{FB_LB}
1	Open	$V_{FB} > V_{REF\_B}$	V_{CS_BL1} = 0.31 V	0.90 V	2.75 V
2	580 kΩ~670 kΩ	$V_{FB} < V_{REF\_B}$	V_{CS_BL2} = 0.35 V	1.05 V	2.75 V

During IC start-up, the Ref_{GOOD} signal is logic low when V_{CC} < 4 V. The low Ref_{GOOD} signal will reset the burst mode level detection latch. When the burst mode level detection latch is low and the IC is off, the FB resistor is isolated from the FB pin and a current source I_{sel} is turned on instead.

From V_{CC} = 4 V to V_{CC} on-threshold, the FB pin will start to charge to a voltage level associated with the R_{Sel} resistor. When V_{CC} reaches the V_{CC} on-threshold, the FB voltage is sensed. The burst mode thresholds are then chosen according to the FB voltage level. The burst mode level detection latch is then set to high. Once the detection latch is set to high, any change in the FB level will not change the threshold selection. The current source I_{sel} is turned off 2 µs after V_{CC} reaches the V_{CC} on-threshold and the R_{FB} resistor is re-connected to FB pin (see Figure 8).

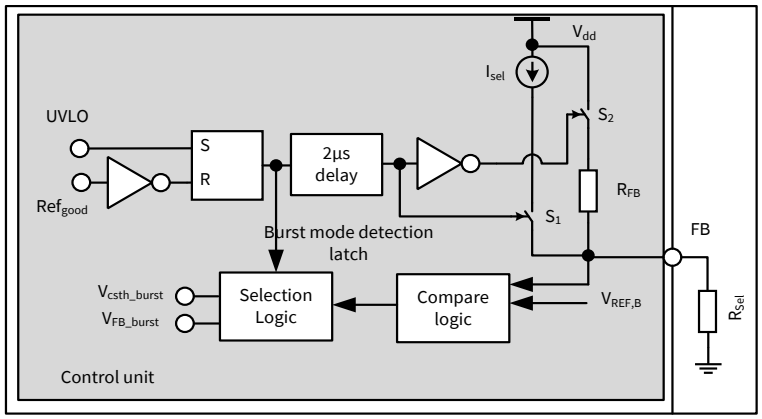

Figure 8 Burst mode detect and adjust

4.4.1 Entering ABM operation

In order to enter ABM operation, three conditions must apply:

- the FB voltage must be lower than the threshold of V_{FB_EBLX}
- the up/down counter must be 8 for low-line and 10 for high-line, and
- the above two conditions must remain after a certain blanking time t_{FB_BEB} (20 ms).

Once all of these conditions are fulfilled, the ABM flip-flop is set and the IC enters ABM operation. This multi-condition determination for entering ABM operation prevents mis-triggering of ABM, so that the controller enters ABM operation only when the output power is really low during the preset blanking time.

4.4.2 During ABM operation

After entering the ABM the FB voltage rises as V_O starts to decrease due to the inactive PWM section. One comparator observes the FB signal if the voltage level V_{FB_BOn} is exceeded. In that case the internal circuit is powered up to restart with switching.

Turn-on of the power switch is triggered by the ZC counter with a fixed value of 8 ZC for low-line and 10 ZC for high-line. Turn-off results if the voltage across the shunt resistor at the CS pin hits the threshold V_{CS_BL1}/ V_{CS_BL2}.

If the output load is still low, the FB signal decreases as the PWM section is operating. When the FB signal reaches the low threshold V_{FB_BOff}, the internal circuit is reset again and the PWM section is disabled until next time the V_{FB} signal increases beyond the V_{FB_BOn} threshold. In ABM, the FB signal is changing like a sawtooth between V_{FB_BOff} and V_{FB_BOn} (see Figure 9).

4.4.3 Leaving ABM operation

The FB voltage immediately increases if there is a high load jump. This is observed by a comparator with a threshold of V_{FB_LB}. As the current limit is V_{CS_BLX} (31% or 35%) during ABM, a certain load is needed so that FB voltage can exceed V_{FB_LB}. After leaving ABM, normal peak current control through V_{FB} is re-activated. In addition, the up/down counter will be set to 1 (low-line) or 3 (high-line) immediately after leaving ABM. This is helpful to minimize the output voltage undershoot.

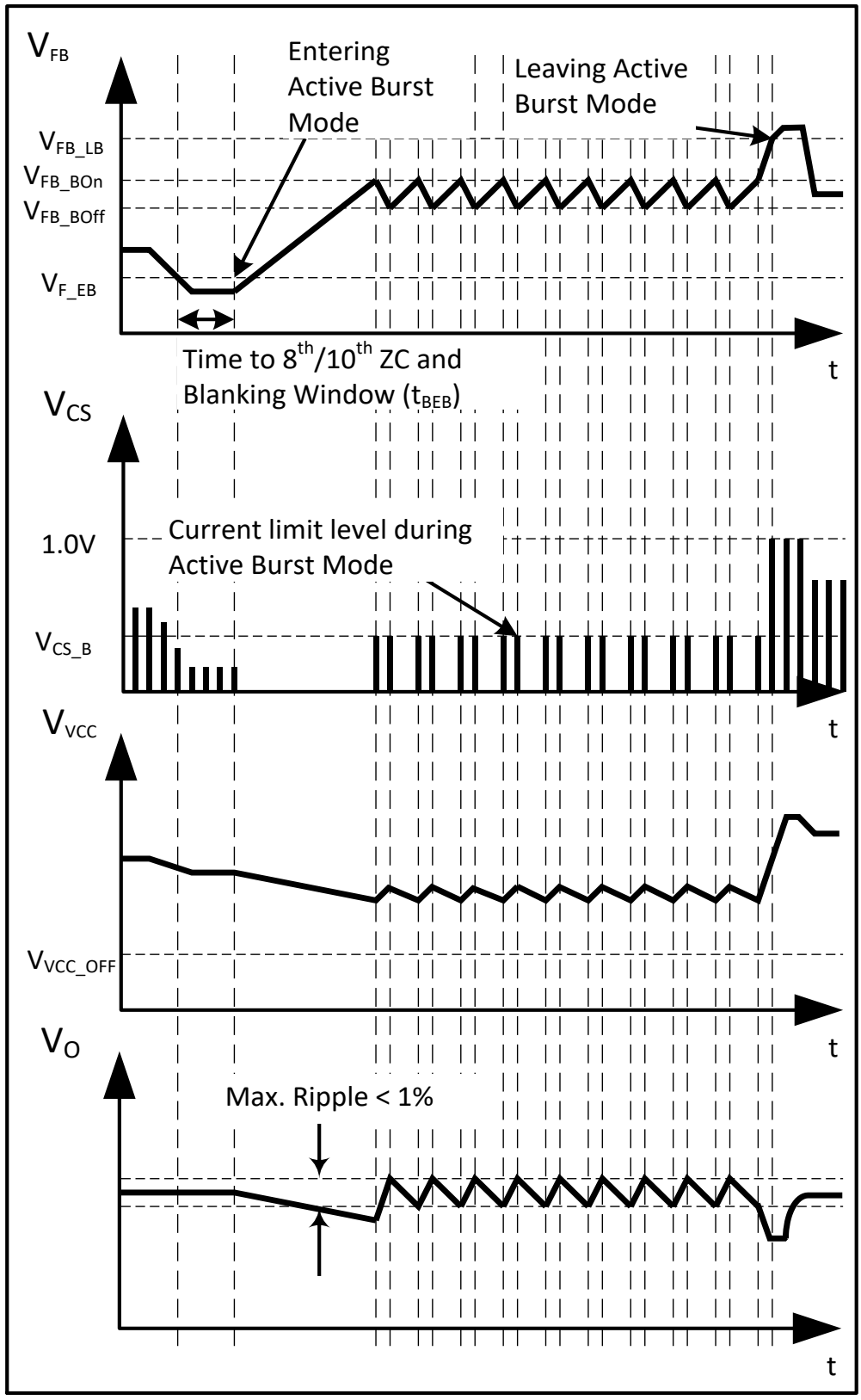

Figure 9 Signals in ABM

4.5 Current Sense

The PWM comparator inside the IC has two inputs: one from the CS pin and the other from the FB voltage. Before being sent to the PWM comparator, there is an offset and operational gain on the CS voltage. In normal operation, the relationship between FB voltage and maximum CS voltage is determined by Eq. 10.

$$V_{FB} = G_{PWM} \cdot V_{CS} + V_{PWM} \quad \textbf{(Eq. 111B)}$$

where, V_{FB} : FB voltage
V_{CS} : voltage across the CS resistor
G_{PWM} : PWM output gain
V_{PWM} : offset for voltage ramp

The absolute maximum CS voltage V_{CS} is 1 V. Therefore, the CS resistor can be chosen according to the maximum required peak current in the transformer, as shown in equation 11.

$$R_{Sense} = \frac{V_{CS\_N}}{I_{PMax}} \quad \textbf{(Eq. 21)}^{1}$$

where, R_{Sense} : CS resistor
V_{CS_N} : PCL in normal operation (1 V)
I_{PMax} : peak current of primary inductance

In addition, an LEB is already built inside the CS pin. The typical value of LEB time is 220 ns, which can be thought of as a minimum on-time.

Note: In case of higher switch-on noise at the CS pin, the IC may switch off immediately after LEB time especially at light-load high-line conditions. To avoid this, noise-filtering ceramic capacitor C112 (e.g., 100 pF~100 nF, see Figure 12) can be added.

4.6 FB

Inside the IC, the FB pin is connected to the V_{REF} 3.3 V voltage source through a pull-up resistor R_{FB}. Outside the IC, this pin is connected to the collector of the optocoupler. Normally, a ceramic capacitor C_{FB}, 1 nF for example, can be put between this pin and GND to smooth the signal.

FB voltage will be used for two functions:

- It determines the maximum CS voltage, equivalent to the transformer peak current.
- It determines the ZC counter value according to load conditions.

Regulation loop with dual FB calculation is explained in Section 8.13. Voltage divider resistors of TL431 single FB loop can be calculated as shown below.

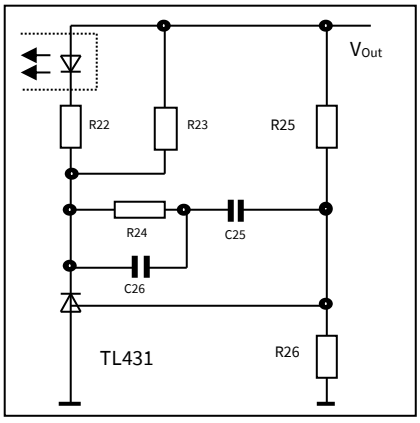

Figure 10 Regulation loop with dual FB

[1] Equation is used in Section 8 (fifth-generation QR FLYCAL design example)

$$R_{25} = R_{26} \cdot \left(\frac{V_{Out}}{V_{REF\_TL}} - 1 \right) \quad \textbf{(Eq. 81)}$$

[1]

where, V_{Out} : output voltage
V_{REF_TL} : TL431 reference voltage

4.7 Zero Crossing Detection

The circuit components connected to the ZCD pin include resistors R_{ZC} and R_{ZCD} and capacitor C_{ZC}. The values of three components shall be chosen so that the three functions combined to this pin will perform as designed. At first, the ratio between R_{ZC} and R_{ZCD} is chosen to set the trigger level of output OVP. Assuming the protection level of output voltage is V_{Out_OVP}, the turns of the auxiliary winding is N_A and the turns of the secondary output winding is N_S, the ratio is calculated as:

$$\frac{R_{ZCD}}{R_{ZC}+R_{ZCD}} < \frac{V_{ZCD\_OVP\_Min} \times N_S}{V_{Out\_OVP} \times N_A} \quad \textbf{(Eq. 113)}$$

where, R_{ZCD} : internal resistor at the ZCD pin
R_{ZC} : external resistor at the ZCD pin
$R_{ZCD\_OVP\_Min}$: minimum voltage of output OV threshold
N_S : number of secondary turns of the transformer
N_A : number of auxiliary turns of the transformer
V_{Out_OVP} : user-defined output OV threshold

Secondly, as shown in Figure 4, there are two delay times for detection of the ZC and turn-on of the power switch. The delay time t_{delay1} is the delay from the drain-source voltage across the bus voltage to the ZCD voltage and falls below $V_{ZCD\_CT\_Typ}$ (100 mV). This delay time can be adjusted by changing C_{ZC}. The second one, t_{delay2}, is the delay time from the ZC voltage and falls below 100 mV until the MOSFET is turned on. This second delay time is determined by the internal circuit and cannot be changed. Therefore, the capacitance C_{ZC} is chosen to adjust the delay time t_{delay1} and the power switch is turned on at the valley point of the drain-source voltage. This is normally done through experimentation.

In addition, as shown in Figure 4, an overshoot is possible on ZCD voltages when the power switch is turned off. This is because oscillation 1 on drain voltage, shown in Figure 4, may be coupled to the auxiliary winding. Therefore, the capacitance C_{ZC} and the ratio can be adjusted to obtain the trade-off between the output OVP accuracy and the valley switching performance.

If, however, the amplitude of the ring at the ZCD pin is too small and the ZC cannot be detected, it is advisable to increase the drain-source capacitor C_{DS} of the power switch. But this capacitor would incur switching loss, so it is suggested that the value be as small as possible – less than 100 pF.

Furthermore, to avoid mis-triggering of ZCD detection just after the power switch is turned off, a ring suppression time is provided. The ring suppression time is 2.5 µs typically, if V_{ZCD} is higher than 0.45 V, and it is 25 µs typically if V_{ZCD} is lower than 0.45 V. During the ring suppression time, the IC cannot be turned on again. Therefore, the ring suppression time can also be thought of as a minimum off time.

4.8 Gate drive (ICE5QSxG only)

Inside the gate pin, a totem-drive circuit is integrated. The gate-drive voltage is 10 V, which is enough for most of the available MOSFETs. In case of a 1nF load capacitance, the typical values of rise time and fall time are 117 ns and 27 ns respectively. In practice, a gate resistor can be used to adjust the turn-on speed of the MOSFET. In addition, to accelerate the turn-off speed, the gate resistor can be anti-paralleled with an ultra-fast diode like

[1] Equation is used in Section 8 (5th Generation QR FLYCAL design example)

1N4148. To avoid oscillation during turn-off of the MOSFET, it is suggested that the loop area of the driver, through the gate resistor and the MOSFET gate, to source and back to IC GND, should be as small as possible.

Note: The gate-to-source discharge resistor of the power switch Q1 (see Figure 2) is not allowed to add in ICE5QSxG as the gate pin is connected to the ZCD pin internally via R_{ZCD}. With a gate-to-source discharge resistor, the IC cannot start up at all because Q1 GATE is shorted to SOURCE and V_{GS} (the gate threshold voltage of Q1) cannot rise up during first start-up.

4.9 Line over-voltage, brown-out and line selection

The input-line OV and brown-out protections are detected by sensing the voltage level at the V_{IN} pin through the resistor divider from the bulk capacitor. Once the voltage level at the V_{IN} pin goes above 2.9 V, the IC stops switching and enters line OVP mode. When the V_{IN} pin voltage goes lower than 2.9 V and the V_{CC} hits 16 V, the line OVP mode is released.

If the V_{IN} pin voltage is lower than 0.4 V, the IC stops switching and enters brown-out mode, and it only releases brown-out mode when the V_{IN} pin voltage goes higher than 0.66 V. Note that there is no power switch (see Figure 2/Figure 3) switching but it always detects the V_{IN} level in every restart cycle during line OVP or brown-out mode. The input-line sensing resistors (see Figure 2/Figure 3) R_{l1} and R_{l2} can be calculated as below.

Choose R_{l1} = 9 MΩ.

Case 1: Line OVP is the first priority,

$$R_{l2} = \frac{R_{l1} \times V_{VIN\_LOVP}}{(V_{Line\_OVP\_AC} \times \sqrt{2}) - V_{VIN\_OVP}} \quad \textbf{(Eq. 105A)}^{1}$$

where, R_{l1} : high-side line input sensing resistor (typ. 9 MΩ)
R_{l2} : low-side line input sensing resistor
V_{VIN_LOVP} : line OV threshold (typ. 2.9 V)
$V_{LINE\_OVP\_AC}$: user-defined line OV (V AC) for the system

$$V_{BrownIn\_AC} = \frac{\left(V_{VIN\_BI} \times \frac{R_{l1} + R_{l2}}{R_{l2}}\right) + V_{DC\ Ripple}}{\sqrt{2}} \quad \textbf{(Eq. 106)}^{1}$$

where, V_{VIN_BI} : brown-in threshold voltage (typ. 0.66 V)
V_{DC_Ripple} : bus capacitor DC ripple voltage which depends on AC-line frequency and load (0~30 V)
$V_{BrownIn\_AC}$: brown-in voltage for the system (V AC)

$$V_{BrownOut\_AC} = \frac{\left(V_{VIN\_BO} \times \frac{R_{l1} + R_{l2}}{R_{l2}}\right) + V_{DC\_Ripple}}{\sqrt{2}} \quad \textbf{(Eq. 107)}^{2}$$

where, V_{VIN_BO} : brown-out threshold voltage (typ. 0.4 V)
$V_{Brown\text{-}out\_AC}$: brown-out voltage for the system (V AC)

$$V_{LineSelection\_AC} = \frac{\left(V_{VIN\_REF} \times \frac{R_{l1} + R_{l2}}{R_{l2}}\right) + V_{DC\_Ripple}}{\sqrt{2}} \quad \textbf{(Eq. 108)}^{1}$$

where, V_{VIN_REF} : V_{IN} voltage threshold for line selection (typ. 1.52 V)
$V_{Brown\text{-}out\_AC}$: brown-out voltage for the system (V AC)

Case 2: Brown-out is the first priority,

[1] Equation is used in Section 8 (fifth-generation QR FLYCAL design example)

[2] Equation is used in Section 8 (fifth-generation QR FLYCAL design example)

$$R_{l2} = \frac{V_{VIN\_BI} \times R_{l1}}{(V_{LineBI\_AC} \times \sqrt{2}) - V_{VIN\_BI}}$$ **(Eq. 105B)**[1]

where, V_{VIN_BI} : brown-in threshold voltage (typ. 0.66 V)

V_{LineBI_AC} : user-defined brown-in voltage (V AC) for the system

$$V_{BrownOut\_AC} = \frac{\left(V_{VIN\_BO} \times \frac{R_{l1} + R_{l2}}{R_{l2}}\right) + V_{DC\_Ripple}}{\sqrt{2}}$$ **(Eq. 107)**[1]

$$V_{LineOVP\_AC} = \frac{\frac{R_{l1} \times V_{VIN\_LOVP}}{R_{l2}} + V_{VIN\_LOVP}}{\sqrt{2}}$$ **(Eq. 114)**[1]

where, V_{VIN_LOVP} : line OV threshold (typ. 2.9 V)

$V_{LineOVP\_AC}$: line OV (V AC) for the system

4.10 Protection features

Protection is one of the major factors in determining whether the system is safe and robust. Therefore sufficient protection is necessary. ICE5QSxG and ICE5QRxxxxxx provide comprehensive protection to ensure the system is operating safely. These protections include line OV, brown-out, V_{CC} OV and UV, over-load, output OV, over-temperature (controller junction) and V_{CC} short-to-GND. When those faults are found, the system will enter protection mode until the fault is removed, when the system resumes normal operation. A list of protections and failure conditions are shown in the table below.

Table 3 Protection functions of ICE5QSxG and ICE5QRxxxxxx

Protection function	Failure condition	Protection mode
Line OV	V_{VIN} > 2.9 V	Non-switch auto restart
Brown-out	V_{VIN} < 0.4 V	Non-switch auto restart
V_{CC} OV	V_{VCC} > 25.5 V	Odd-skip auto restart
V_{CC} UV	V_{VCC} < 10 V	Auto restart
Over-load	V_{FB} > 2.75 V and lasts for 30 ms	Odd-skip auto restart
Output OV	V_{ZCD} > 2 V and lasts for 10 consecutive pulses	Odd-skip auto restart
Over-temperature (junction temperature of controller chip only)	T_J > 140°C with 40°C hysteresis to reset	Non-switch auto restart
V_{CC} short-to-GND (V_{VCC} = 0 V, $R_{StartUp}$= 50 MΩ, V_{DRAIN} = 90 V)	V_{VCC} < 1.1 V, $I_{VCC\_Charge1}$ ≈ -0.2 A	Cannot start up

4.11 Others

For a QR Flyback converter, it is possible that the operation frequency will go too low, which normally results in audible noise. To prevent this in the IC, a maximum on-time and off-time are provided.

The maximum on-time is typically 35 µs. If the gate is maintained on for 35 µs, the IC will turn off the gate regardless of the CS voltage.

When the power switch is off and the IC cannot detect enough ZC to turn on, the IC will wait until the maximum off-time, typically 42.5 µs, is reached, then only turn on the power switch. Please note that even a non-zero ZCD pin voltage cannot prevent the IC from turning on the power switch. Therefore, during soft-start, Continuous Conduction Mode (CCM) operation of the converter is expected.

For the transformer design, minimum switching frequency (at minimum line with maximum load) should be greater than or equal to 40 kHz. The maximum switching frequency should not be higher than 200 kHz in any line and load condition, due to LEB time and minimum ringing suppression time.

5 Typical application circuit

A 60 W demo board with ICE5QSBG and 16 W demo board with ICE5QR4780AZ are shown below.

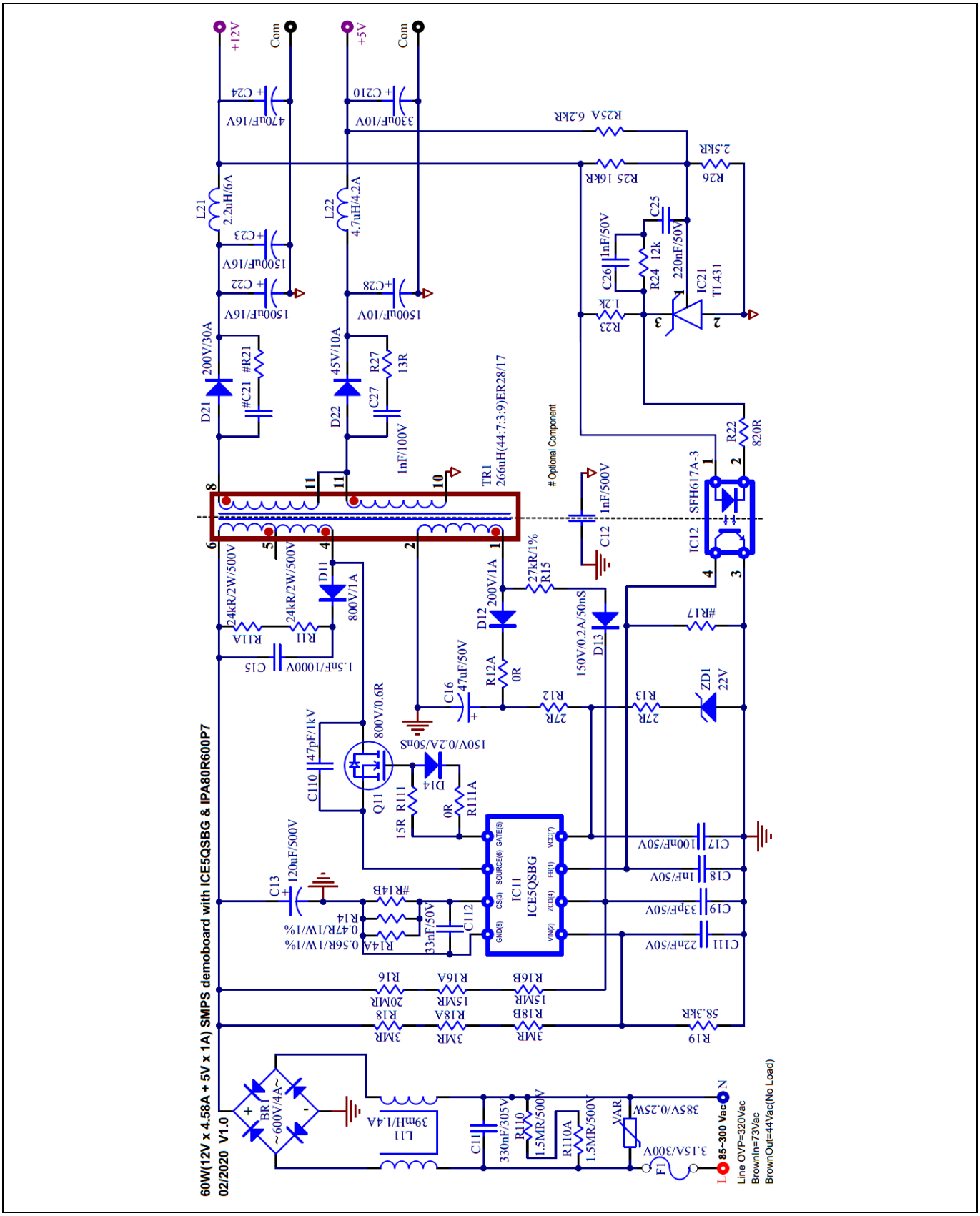

Figure 11 Schematic of DEMO_5QSBG_60W1

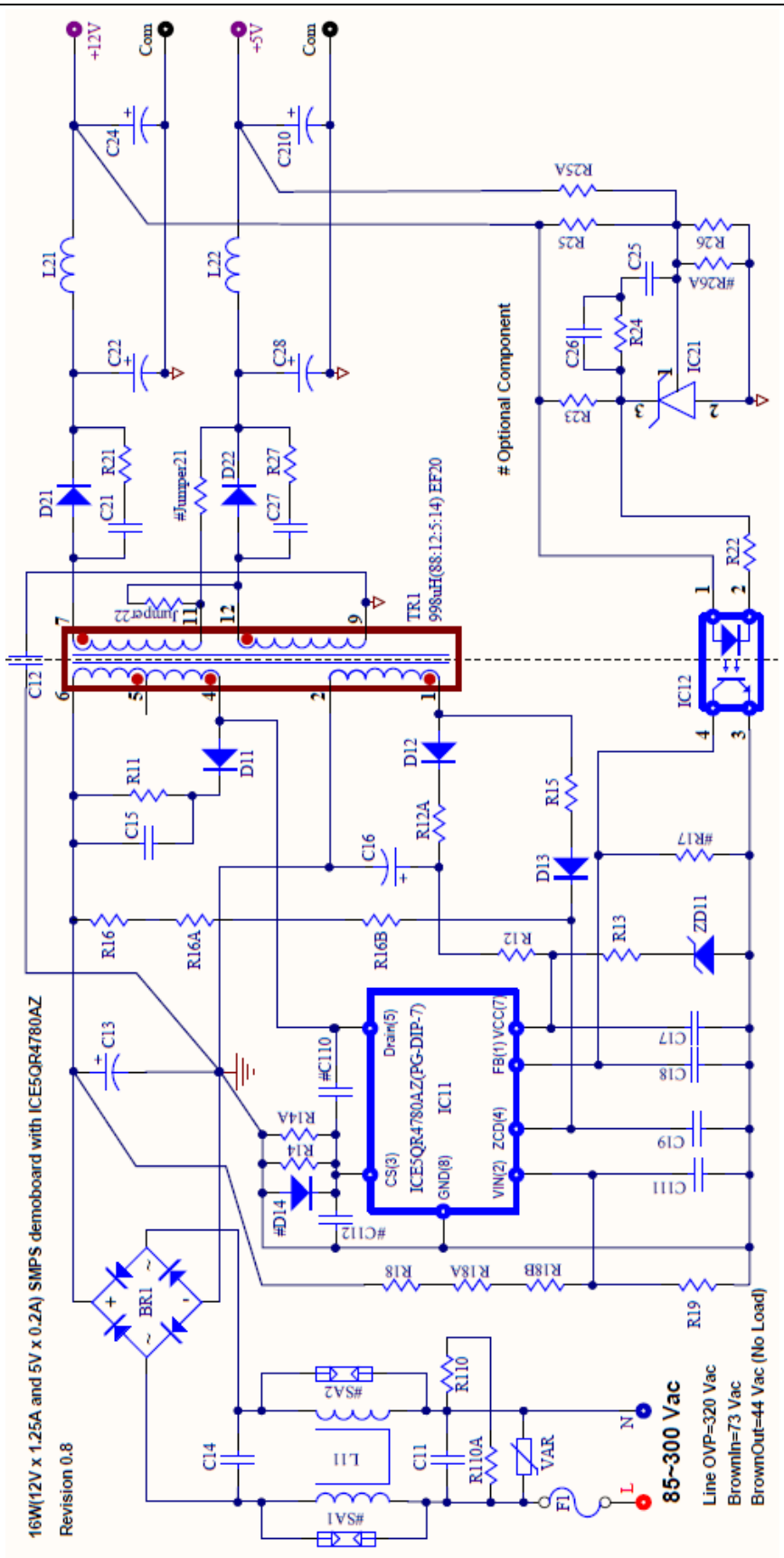

Figure 12 Schematic of DEMO_5QR4780AZ_16W1

6 PCB layout recommendation

In a power-supply system, PCB layout is key to a successful design. Following are some suggestions for this (see Figure 11 and Figure 12).

1. Minimize the loop with pulse-share current or voltage; examples are the loop formed by the bus voltage source, primary winding, main power switch (Q11 (see Figure 11) in the controller and CoolSET™ power switch CoolMOS™ inside the IC) and current sensing resistor or the loop consisting of secondary winding, output diode and output capacitor, or the loop of the V_{CC} power supply.
2. Star GND at bulk capacitor C13: all primary GNDs should be connected to the GND of bulk capacitor C13 separately in one point. This can reduce the switching noise going into the sensitive pins of the CoolSET™ device effectively. The primary star GND can be split into four groups as follows:
    i. Combine signal (all small-signal GNDs connecting to the CoolSET™ GND pin such as filter capacitor GND C17, C18, C19, C111, C112 and optocoupler GND) and power GND (CS resistor R14 and R14A).
    ii. V_{CC} GND includes the V_{CC} capacitor GND C16 and the auxiliary winding GND, pin 2 of the power transformer.
    iii. EMI return GND includes Y capacitor C12.
    iv. DC GND from bridge rectifier BR1.
3. Filter capacitor close to the controller GND: filter capacitors, C17, C18, C19, C111 and C112 should be placed as close to the controller GND and the controller pin as possible to reduce the switching noise coupled into the controller.
4. HV traces clearance: HV traces should maintain enough spacing from the nearby traces. Otherwise, arcing could occur.
    i. 400 V traces (positive rail of bulk capacitor C13) to nearby trace: > 2.0 mm.
    ii. 700 V/800 V traces (drain pin of power switch Q11 (see Figure 11) in controller and drain pin of CoolSET™ IC11 (see Figure 12)) to nearby trace: > 3 mm.
5. Recommended minimum 232 mm^2 copper area (2 oz thickness) at the drain pin to add on the PCB for better thermal performance for the CoolSET™.

7 Output power of fifth-generation QR ICs

Table 4 Output power of fifth-generation QR controller

Type	Package	Marking	220V AC ±20%[1]	85–300 V AC[1]
ICE5QSxG	PG-DSO-8	5QSAG	109 W	60 W
ICE5QSBG	PG-DSO-8	5QSBG	109 W	60 W

Table 5 Output power of fifth-generation QR CoolSET™

Type	Package	Marking	V_{DS}	R_{DSon}[2]	220V AC ±20%[3]	85–300 V AC[3]
ICE5QR4770AZ	PG-DIP-7	5QR4770AZ	700 V	4.73 Ω	27 W	15 W
ICE5QR4780AZ	PG-DIP-7	5QR4780AZ	800 V	4.13 Ω	28 W	15 W
ICE5QR2270AZ	PG-DIP-7	5QR2270AZ	700 V	2.13 Ω	41 W	22 W
ICE5QR2280AZ	PG-DIP-7	5QR2280AZ	800 V	2.13 Ω	41 W	22 W
ICE5QR1070AZ	PG-DIP-7	5QR1070AZ	700 V	1.15 Ω	58 W	32 W
ICE5QR0680AZ	PG-DIP-7	5QR0680AZ	800 V	0.71 Ω	74 W	41 W
ICE5QR4770AG	PG-DSO-12	5QR4770AG	700 V	4.73 Ω	27 W	15 W
ICE5QR1680AG	PG-DSO-12	5QR1680AG	800 V	1.53 Ω	50 W	27 W
ICE5QR0680AG	PG-DSO-12	5QR0680AG	800 V	0.71 Ω	77 W	42 W
ICE5QR0680BG	PG-DSO-12	5QR0680BG	800 V	0.71 Ω	77 W	42 W
ICE5QR1680BG	PG-DSO-12	5QR1680BG	800 V	1.53 Ω	50 W	27 W
ICE5QR2280BG	PG-DSO-12	5QR2280BG	800 V	2.13 Ω	42 W	23 W
ICE5QR4780BG	PG-DSO-12	5QR4780BG	800 V	4.13 Ω	28 W	15 W

The calculated output power curves giving the typical output power vs ambient temperature are shown below. The curves are based on a typical discontinuous mode Flyback in an open-frame design at T_a = 50°C, T_J = 125°C (integrated HV MOSFET), using minimum drain pin copper area in a 2 oz copper single-sided PCB and steady-state operation only (no design margins for abnormal operation modes are included). The output power figure is for selection purpose only. The actual power can vary depending on particular designs.

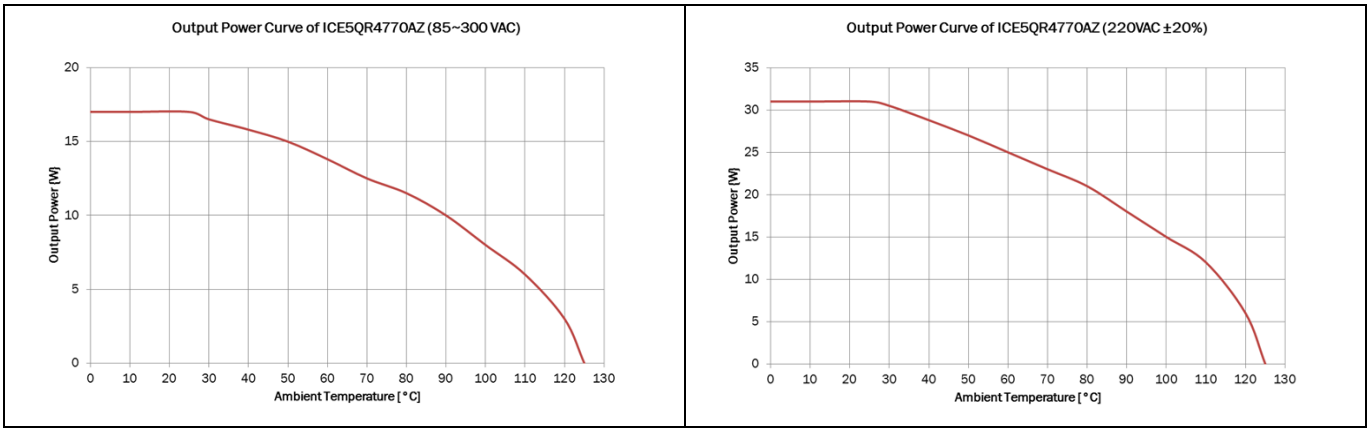

Figure 13 Output power curve of ICE5QR4770AZ

[1] Calculated maximum output power rating in an open-frame design at T_a = 50°C, T_J = 125°C. The output power figure is for reference purposes only. The actual power can vary depending on particular designs. Please contact a technical expert from Infineon for more information.

[2] Typ. at T_J = 25°C (inclusive of low-side MOSFET)

[3] Calculated maximum output power rating in an open-frame design at T_a = 50°C, T_J = 125°C (integrated HV MOSFET) and using minimum drain pin copper area in a 2 oz copper single-sided PCB. The output power figure is for selection purposes only. The actual power can vary depending on particular designs. Please contact a technical expert from Infineon for more information.

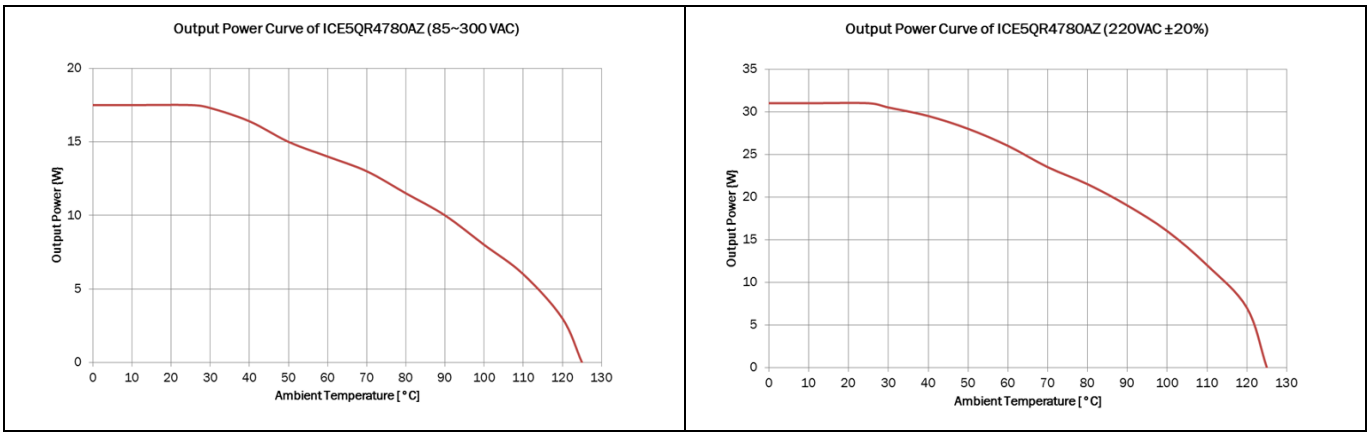

Figure 14 Output power curve of ICE5QR4780AZ

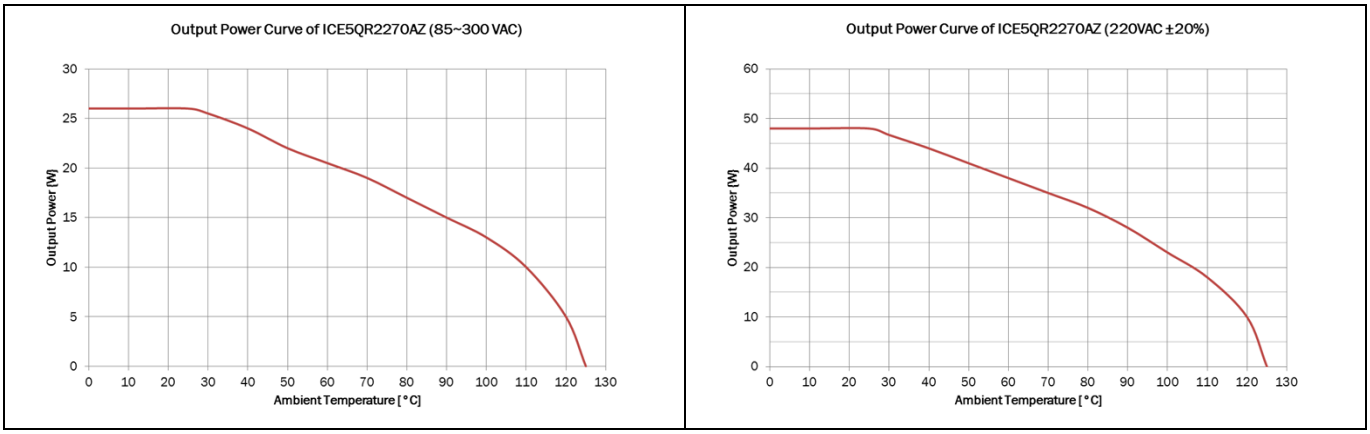

Figure 15 Output power curve of ICE5QR2270AZ

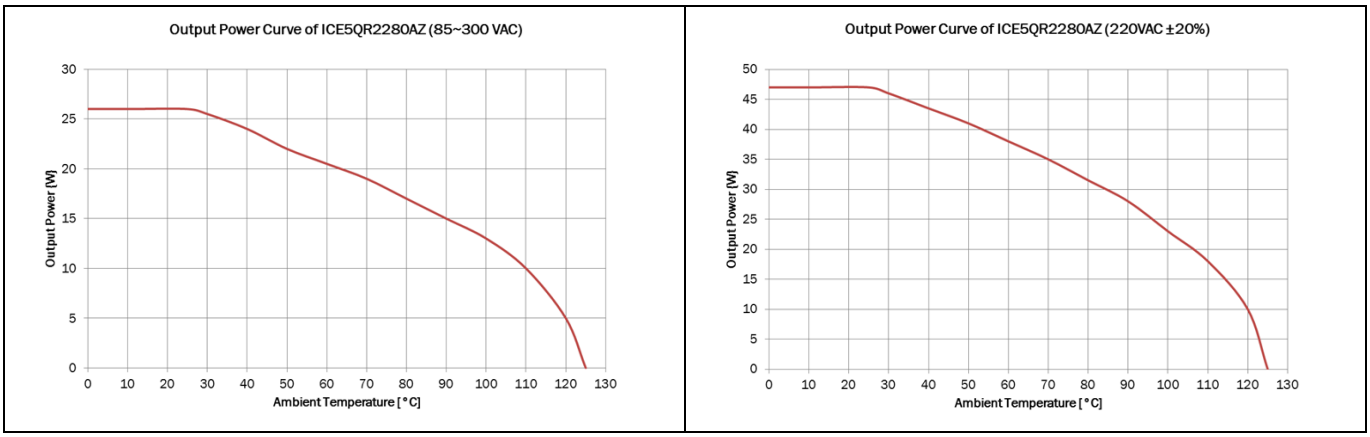

Figure 16 Output power curve of ICE5QR2280AZ

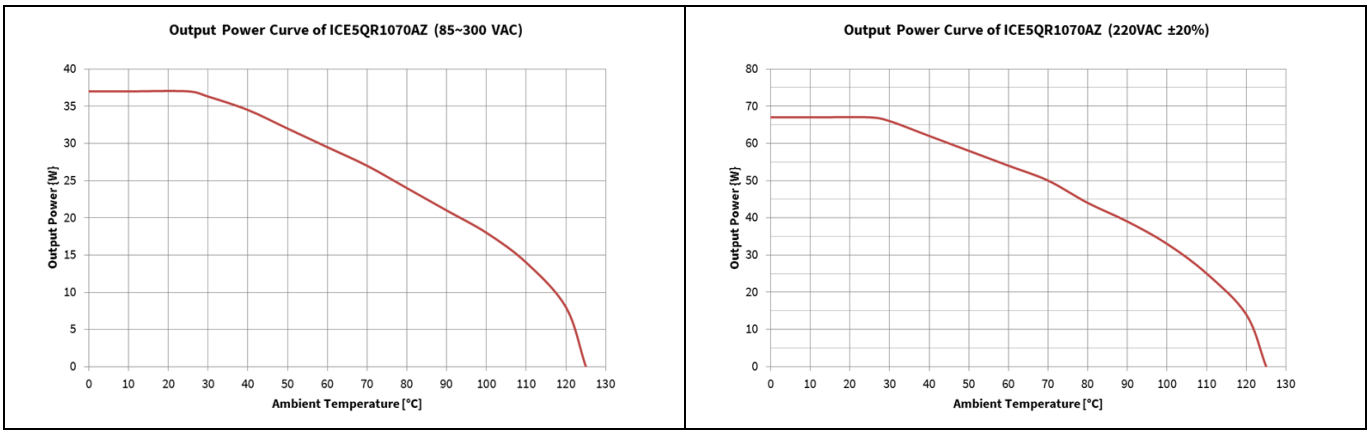

Figure 17 Output power curve of ICE5QR1070AZ

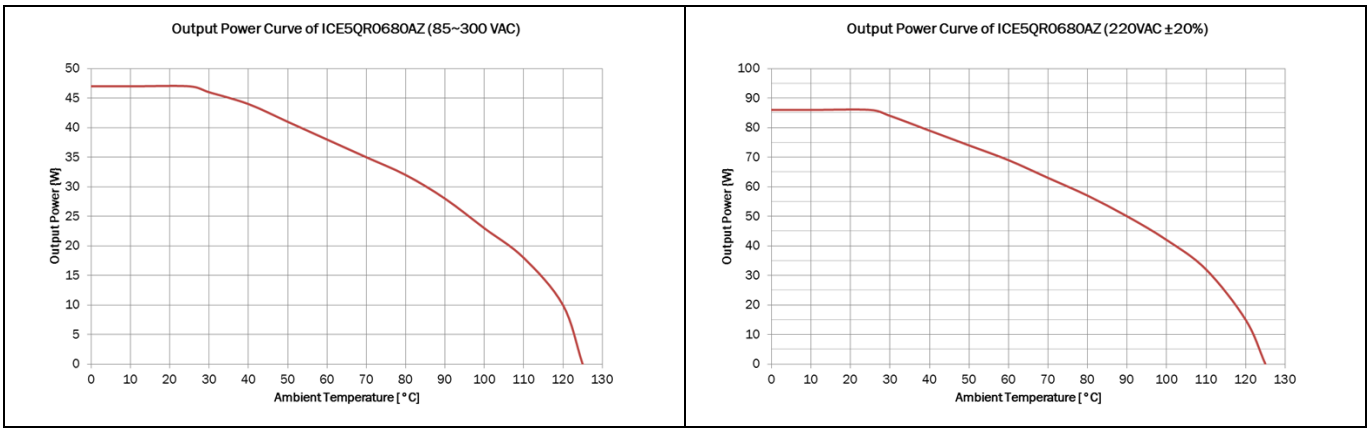

Figure 18 Output power curve of ICE5QR0680AZ

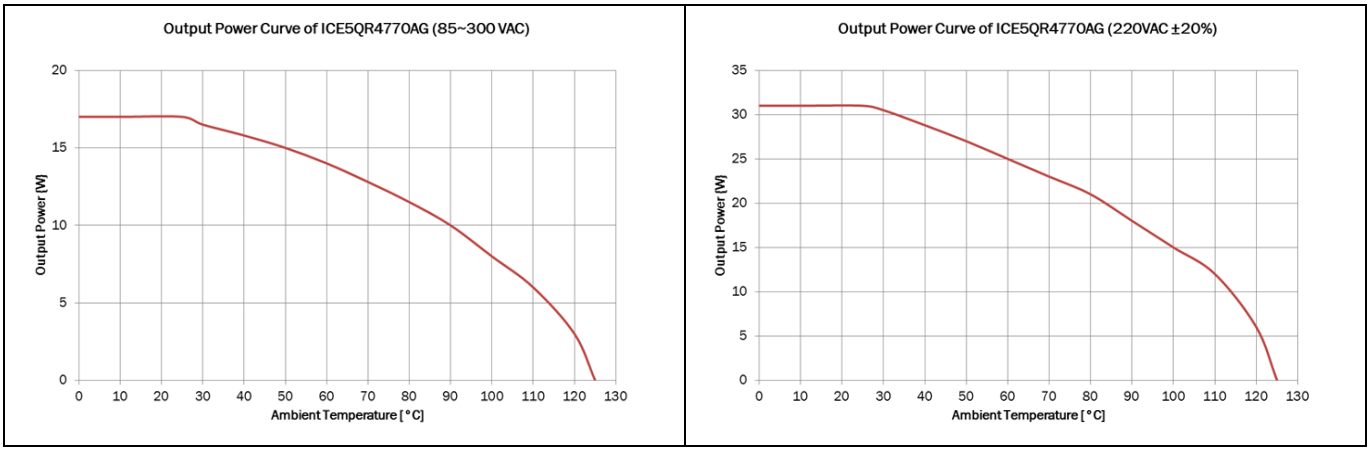

Figure 19 Output power curve of ICE5QR4770AG

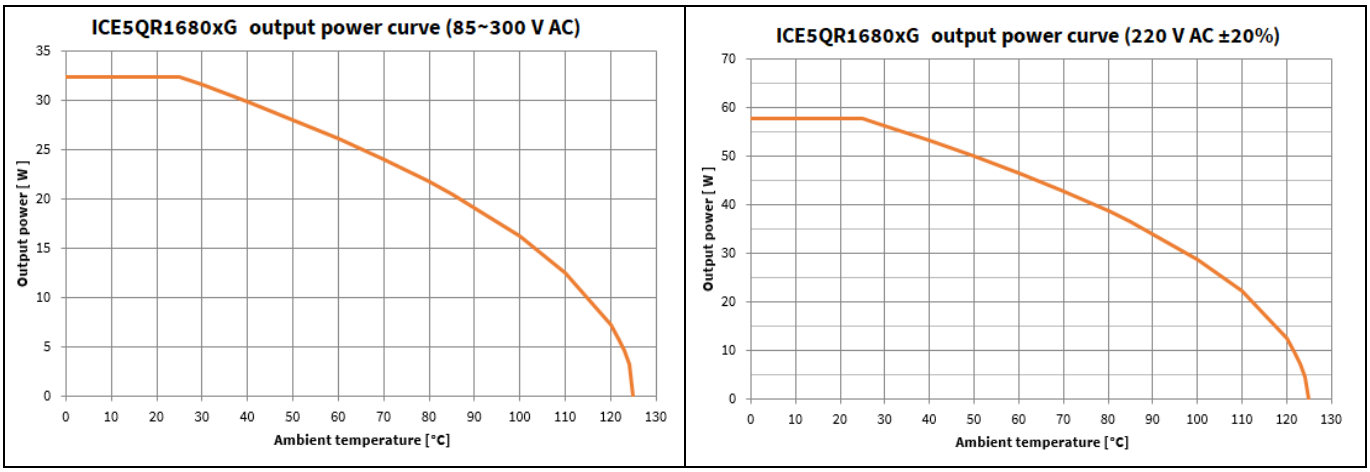

Figure 20 Output power curve of ICE5QR1680xG

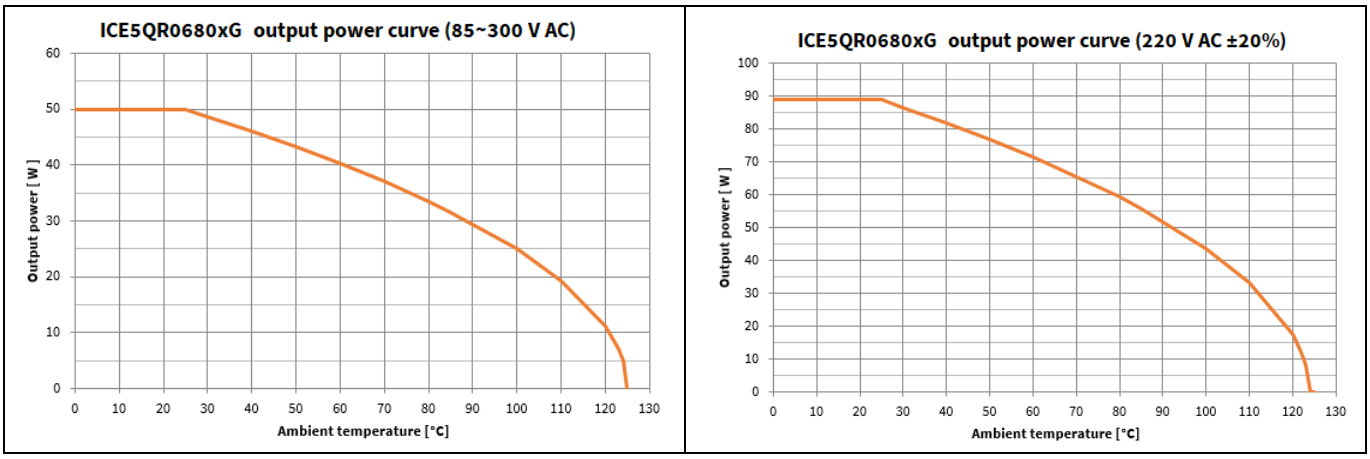

Figure 21 Output power curve of ICE5QR0680xG

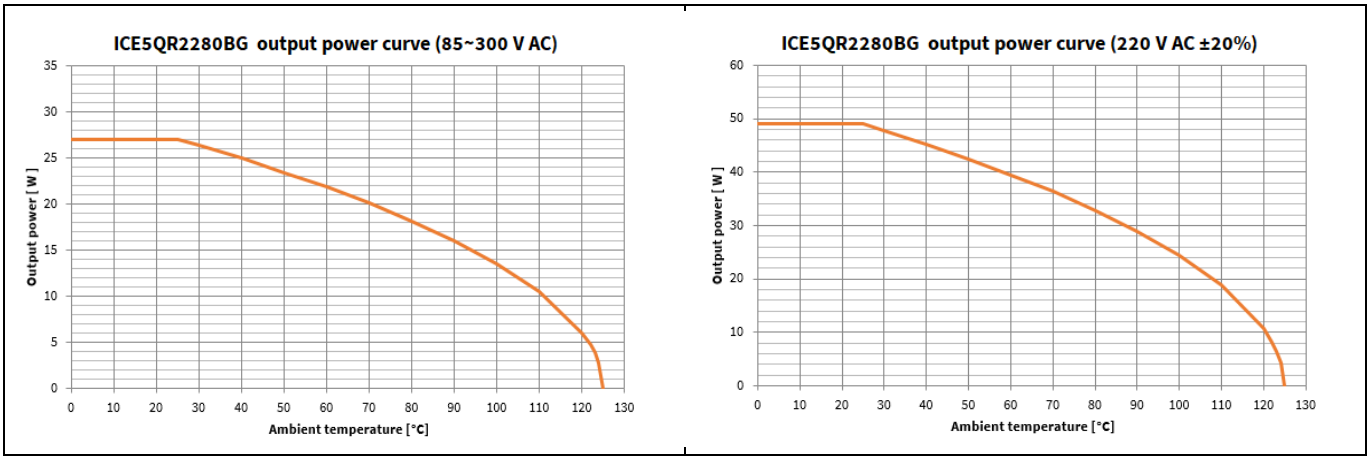

Figure 22 Output power curve of ICE5QR2280BG

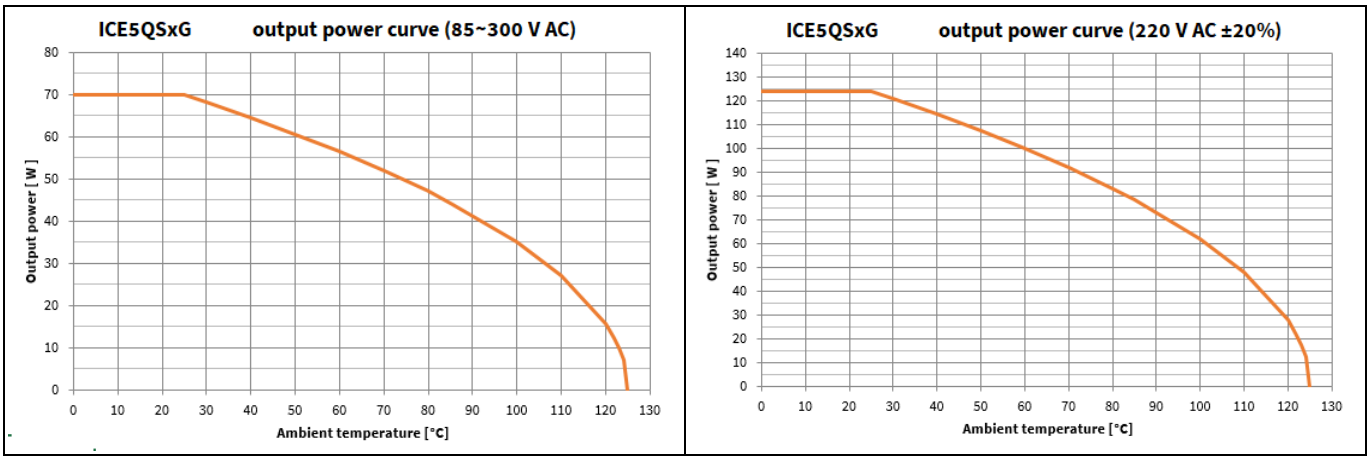

Figure 23 Output power curve of ICE5QSxG

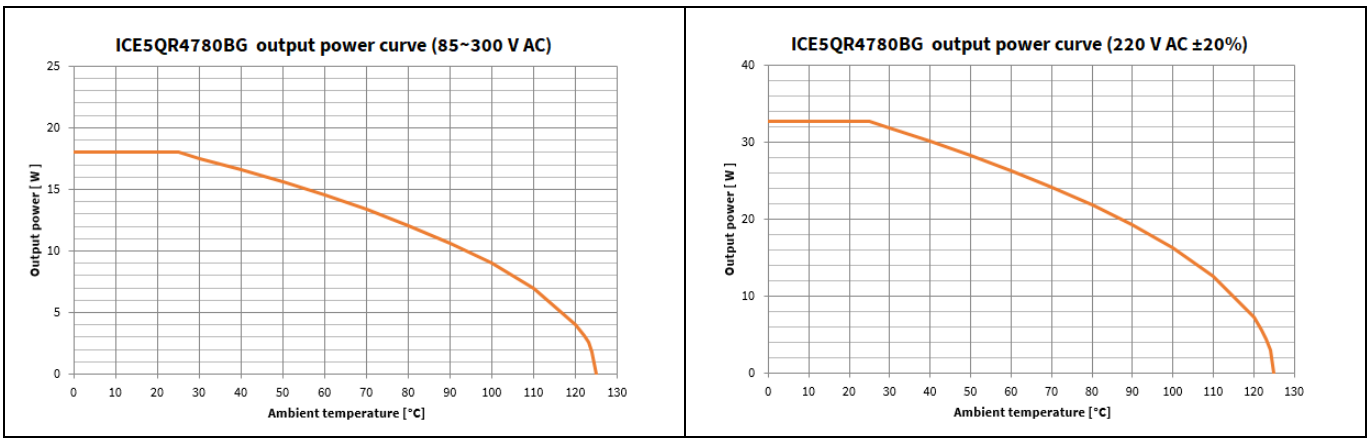

Figure 24 Output power curve of ICE5QR4780BG

8 Fifth-generation QR FLYCAL design example

A 16 W dual-output (12 V and 5 V) QR Flyback converter with ICE5QR4780AZ design example is as shown below.

Procedure		Example
Define input parameters:		
Minimum AC input voltage:	$V_{AC\ Min}$	85 V
Maximum AC input voltage:	$V_{AC\ Max}$	320 V
Line frequency:	f_{AC}	60 Hz
Bulk capacitor (C13) DC ripple voltage:	$V_{DC\ Ripple}$	24.5 V
Output voltage 1:	V_{Out1}	12 V
Forward voltage of output diode 1:	$V_{FDiode1}$	0.3 V
Output current 1:	I_{Out1}	1.25 A
Output voltage 2:	V_{Out2}	5 V
Forward voltage of output diode 2:	$V_{FDiode2}$	0.3 V
Output current 2:	I_{Out2}	0.2 A
Maximum output power:	$P_{Out\ Max}$	16 W
Minimum output power:	$P_{Out\ Min}$	3.2 W
Efficiency:	η	85 %
Reflection voltage:	V_R	90 V
V_{CC} voltage:	V_{Vcc}	14 V
Forward voltage of V_{CC} diode (D12):	$V_{FDiodeVcc}$	0.6 V
Fifth-generation QR CoolSET™:	CoolSET™	ICE5QR4780AZ
Switching frequency at $V_{AC\ Min}$ and $P_{Out\ Max}$:	f_s	55 kHz
Targeted max. drain-source voltage:	$V_{DS\ Max}$	600 V
Drain-to-source capacitance of MOSFET (including $C_{o(er)}$ of MOSFET):	C_{DS}	7 pF
Maximum ambient temperature:	T_a	50°C

8.1 Input diode bridge (BR1)

There is no special requirement imposed on the input rectifier and storage capacitor in the Flyback converter. The components will be chosen to meet the power rating and hold-up requirements.

Max. input power:

$$P_{InMax} = \frac{P_{OutMax}}{\eta} \quad \textbf{(Eq. 1)} \qquad P_{InMax} = \frac{16W}{0.85} = 18.82W$$

Power factor	cosφ	0.6

Input RMS current:

$$I_{ACRMS} = \frac{P_{InMax}}{V_{ACMin} \cdot \cos\varphi} \quad \textbf{(Eq. 2)} \qquad I_{ACRMS} = \frac{18.82W}{85V \cdot 0.6} = 0.369A$$

Max. DC input voltage:

$$V_{DC\,max\,PK} = V_{ACMax} \cdot \sqrt{2} \quad \textbf{(Eq. 3)} \qquad V_{DCMaxPk} = 320V \cdot \sqrt{2} = 452.55V$$

8.2 Input capacitor (C13)

Min. peak input voltage at no-load condition:

$$V_{DCMinPk} = V_{ACMin} \cdot \sqrt{2} \quad \textbf{(Eq. 4)} \qquad V_{DCMinPk} = 85V \cdot \sqrt{2} = 120.2V$$

$$V_{DCMin} = V_{DCMinPk} - V_{DCRipple} \quad \textbf{(Eq. 5)} \qquad V_{DCMin} = 120.2V - 24.5V = 95.69V$$

Discharging time at each half-line cycle:

$$T_D = \frac{1}{4 \cdot f_{AC}} \cdot \left(1 + \frac{\sin^{-1} \frac{V_{DCMin}}{V_{DCMinPk}}}{90} \right) \quad \textbf{(Eq. 6)} \qquad T_D = \frac{1}{4 \cdot 60Hz} \cdot \left(1 + \frac{\sin^{-1} \frac{95.69V}{120.2V}}{90} \right) = 6.61ms$$

Required energy at discharging time of input capacitor:

$$W_{IN} = P_{INMax} \cdot T_D \quad \textbf{(Eq. 7)} \qquad W_{IN} = 18.82W \cdot 6.61ms = 0.12W \cdot s$$

Input capacitor (cal.):

$$C_{IN} = \frac{2 \cdot W_{IN}}{V_{DCMinPk}^2 - V_{DCMin}^2} \quad \textbf{(Eq. 8)} \qquad C_{IN} = \frac{2 \cdot 0.12W \cdot s}{(120.2V)^2 - (95.69V)^2} = 47.04\mu F$$

Alternatively, a rule of thumb for choosing the input capacitor may be applied:

Input voltage	Factor
115 V	2 µF/W
230 V	1 µF/W
85 V–265 V	2–3 µF/W

$$C_{IN} = P_{INMax} \cdot factor \quad \textbf{(Eq. 9)} \qquad C_{IN} = 18.82 \cdot 2.5\mu = 47.05\mu F$$

Select an input capacitor from the Epcos Databook of **Aluminum Electrolytic Capacitors**
The following types are preferred:
For 85°C applications:
Series B43303: 2000 hrs lifetime
B43501: 10000 hrs lifetime
For 105°C applications:
Series **B43504:** **2000 hrs lifetime**
B43505: 5000 hrs lifetime

Choose the rated voltage greater than or equal to the calculated $V_{DCMaxPk}$ — Since $V_{DCMaxPk}$ = 452.55 V, choose 500 V

Choose the capacitance greater than or equal to the calculated C_{IN} from Eq. 8 — Since C_{IN} = 47 µF, choose 47 µF

Input capacitor (C13):	C_{IN}	47 µF

Recalculation after input capacitor chosen:

8.2.1.1.1 $V_{DCMin} = \sqrt{V_{DCMinPk}^2 - \frac{2 \cdot W_{IN}}{C_{IN}}}$ **(Eq. 10)**

$$V_{DCMin} = \sqrt{(120.2)^2 - \frac{2 \cdot 0.12}{47\mu}} = 95.69V$$

Note that special requirements for hold-up time, including cycle skip/drop-out, or other factors which affect the resulting minimum DC input voltage and capacitor time, should be considered at this point as well.

8.3 Transformer design (TR1)

Max. duty cycle:

$$D_{Max} = \frac{V_R}{V_R + V_{DCMin}} \quad \textbf{(Eq. 11)}$$

$$D_{Max} = \frac{90}{90 + 95.69} = 0.48$$

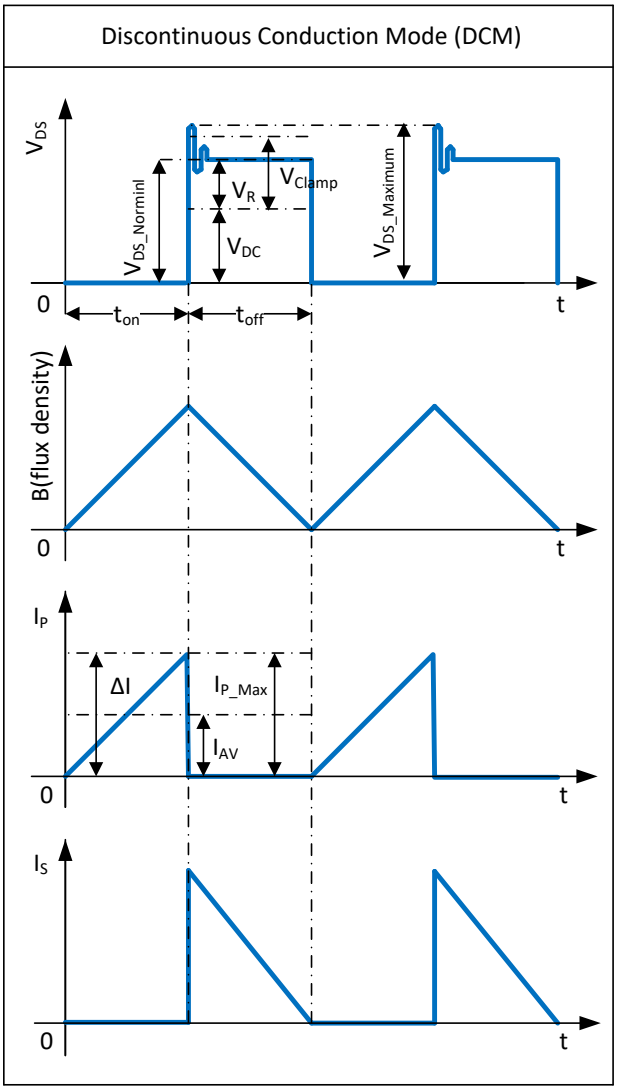

Figure 25 Typical waveforms of DCM operation

$$L_P = \frac{1}{\left[\frac{1}{V_{DC\,Min}} \times \sqrt{2 \times f_s \times P_{In\,Max}} \times \left(\frac{V_{DC\,Min}}{V_R} + 1\right) + \left(\pi \times f_s \times \sqrt{C_{DS}}\right)\right]^2}$$ **(Eq. 12)**

$$L_P = \frac{1}{\left[\frac{1}{95.69} \times \sqrt{2 \times 55 \times 18.82} \times \left(\frac{95.69}{90} + 1\right) + \left(\pi \times 55 \times \sqrt{7p}\right)\right]^2} = 1mH$$

$$I_{AV} = \frac{P_{InMax}}{V_{DCMin} \times D_{Max}}$$ **(Eq. 13)**

$$I_{AV} = \frac{18.82}{95.69 \times 0.48} = 0.41A$$

$$\Delta I = \frac{V_{DCMin} \times D_{Max}}{L_P \times f_s}$$ **(Eq. 14)**

$$\Delta I = \frac{95.69 \times 0.48}{1 \times 10^{-3} \times 55 \times 10^{3}} = 0.82A$$

Maximum current of primary inductance:

$$I_{PMax} = I_{AV} + \frac{\Delta I}{2}$$ **(Eq. 15)**

$$I_{PMax} = 0.41 + \frac{0.84}{2} = 0.82A$$

$$I_{Valley} = I_{PMax} - \Delta I$$ **(Eq. 16)**

$$I_{Valley} = 0.82 - 0.82 = 0A$$

RMS current of primary inductance :

$$I_{PRMS} = \sqrt{[3 \times (I_{AV})^2 + (\frac{\Delta I}{2})^2] \times \frac{D\max}{3}}$$ **(Eq. 17)**

$$I_{PRMS} = \sqrt{[3 \times (0.41)^2 + (\frac{0.82}{2})^2] \times \frac{0.48}{3}} = 0.33A$$

Select core type and data from **Epcos "Ferrite Magnetic Design Tool" or "Datasheet"**.
Fix max. flux density:
Typically, B_{Max} ≈ 0.2 T–0.4 T for ferrite cross depending on core material.
We choose **300 mT** for Material **N87**.

Select core: **E 20/10/6**
Material = N87
B_S = 390 mT @ 100°C
A_e = 32 mm²
BW = 11 mm
A_N = 34 mm²
l_N = 41.2 mm

Maximum flux density	B_{Max}	300 mT

Number of primary inductance (cal.):

$$N_P \geq \frac{I_{PMax} \cdot L_p}{B_{Max} \cdot A_e}$$ **(Eq. 18)**

$$N_P \geq \frac{0.82 \times 1 \times 10^{-3}}{0.3 \times 32 \times 10^{-6}} = 86.57Turns$$

Number of primary turns:	N_P	88 turns

Number of secondary 1 turns (cal.):

$$N_{S1} = \frac{N_P \cdot (V_{OUT1} + V_{FDidoe1})}{V_R}$$ **(Eq. 19)**

$$N_{S1\_cal} = \frac{88 \times (12 + 0.3)}{90} = 12.03Turns$$

Number of secondary turns:	N_{S1}	12 turns

Number of secondary 2 turns (cal.):

$$N_{S2} = \frac{N_P \cdot (V_{OUT2} + V_{FDiode2})}{V_R}$$ **(Eq. 19a)**

$$N_{S2\_cal} = \frac{88 \times (5 + 0.3)}{90} = 5.18Turns$$

Number of secondary turns:	N_{S2}	5 turns

Number of V_{CC} turns (cal.):

$$N_{Vcc} = \frac{N_P \cdot (V_{Vcc} + V_{FDiodeVcc})}{V_R} \quad \textbf{(Eq. 20)} \qquad N_{Aux\_cal} = \frac{88 \times (14 + 0.6)}{90} = 14.27 Turns$$

Number of V_{CC} turns:	N_{Vcc}	14 turns

8.4 Sense resistor (R14)

The sense resistance can be used to individually define the max. peak current and thus the max. power transmitted.

Caution:
When calculating the max. peak current, short-term peaks in output power must also be taken into consideration.

Sense resistor (R14):

$$R_{Sense} = \frac{V_{csth}}{I_{PMax}} \quad \textbf{(Eq. 21)} \qquad R_{Sense} = \frac{1}{0.82} = 1.21\Omega$$

Power rating of sense resistor:

$$P_{SR} = I_{PRMS}^2 \times R_{Sense} \quad \textbf{(Eq. 22)} \qquad P_{SR} = (0.33)^2 \times 1.21 = 0.13W$$

Verification of reflection voltage, duty cycle and maximum flux density:

Reflected voltage:

$$V_R = \frac{(V_{OUT1} + V_{FDiode1}) \cdot N_P}{N_{S1}} \quad \textbf{(Eq. 23)} \qquad V_R = \frac{(12 + 0.3) \cdot 88}{12} = 90.20V$$

Max. turn-on duty cycle:

$$D_{\max} = \frac{L_P \cdot (I_{PMax} - I_{Valley}) \cdot f_S}{V_{DC\,\min}} \quad \textbf{(Eq. 24)} \qquad D_{\max} = \frac{1 \times 10^{-3} \times (0.82A - 0A) \times 55 \times 10^3}{95.69} = 0.48$$

Max. turn-off duty cycle:

$$D'_{\max} = \frac{L_P \cdot (I_{PMax} - I_{Valley}) \cdot f_S}{V_R} \quad \textbf{(Eq. 25)} \qquad D'_{\max} = \frac{1 \times 10^{-3} \times (0.82A - 0A) \times 55 \times 10^3}{90.2} = 0.51$$

Max. flux density:

$$B_{\max} = \frac{L_P \cdot I_{PMax}}{N_P \cdot A_e} \quad \textbf{(Eq. 26)} \qquad B_{\max} = \frac{1 \times 10^{-3} \times 0.82}{88 \times 32 \times 10^{-6}} = 295mT$$

Maximum secondary 1 current and load factor:

$$K_{L(n)} = \frac{P_{O(n)}}{P_O} \quad \textbf{(Eq. 27)} \qquad K_{L(1)} = \frac{15}{16} = 0.94$$

$$I_{SMax} = K_{L(n)} \times I_{PMax} \times \frac{N_P}{N_S} \quad \textbf{(Eq. 28)} \qquad I_{SMax1} = 0.94 \times 0.82 \times \frac{88}{12} = 5.66A$$

$$I_{SRMS} = I_{PRMS} \times \sqrt{\frac{1 - D_{Max}}{D_{Max}}} \times \frac{V_R}{V_{Out} + V_{FOut}} \quad \textbf{(Eq. 29)} \qquad I_{SRMS1} = 0.33 \times \sqrt{\frac{1 - 0.48}{0.48}} \times \frac{90.2}{12 + 0.3} = 2.33A$$

Secondary RMS 1 current:

$$I_{SMax} = K_{L(n)} \times I_{PMax} \times \frac{N_P}{N_S}$$ **(Eq. 28)**

$$I_{SMax1} = 0.94 \times 0.82 \times \frac{88}{12} = 5.66A$$

Maximum secondary 2 current and load factor:

$$K_{L(n)} = \frac{P_{O(n)}}{P_O}$$ **(Eq. 27)**

$$K_{L(2)} = \frac{1}{16} = 0.06$$

$$I_{SMax} = K_{L(n)} \times I_{PMax} \times \frac{N_P}{N_S}$$ **(Eq. 28)**

$$I_{SMax2} = 0.06 \times 0.82 \times \frac{88}{5} = 0.91A$$

Secondary RMS 2 current:

$$I_{SRMS} = I_{PRMS} \times \sqrt{\frac{1-D_{Max}}{D_{Max}}} \times \frac{V_R}{V_{Out} + V_{FOut}}$$ **(Eq. 29)**

$$I_{SRMS2} = 0.33 \times \sqrt{\frac{1-0.48}{0.48}} \times \frac{90.2}{5+0.3} = 0.36A$$

8.5 Winding design

Safety standard margin:
M = 4 mm for European safety standard
M = 3.2 mm for UL1950
M = 0 for triple-insulated wire

Safety standard margin:	M	0 mm
Copper space factor:	f_{Cu}	0.3 (range 0.2–0.4)

Effective bobbin width:

$$BW_E = BW - (2 \times M)$$ **(Eq. 30)**

$$BW_e = 11 - 0 = 11mm$$

Effective winding cross-section:

$$A_{Ne} = \frac{A_N \times BW_e}{BW}$$ **(Eq. 31)**

$$A_{Ne} = \frac{34 \times 11}{11} = 34mm^2$$

The winding cross-section A_N has to be subdivided according to the number of windings:

Primary winding	0.5
Secondary winding	0.45
Auxiliary winding	0.05

Wire copper area for primary winding:

$$A_P = \frac{0.5 \times f_{Cu} \times A_{Ne}}{N_P}$$ **(Eq. 32)**

$$A_P = \frac{0.5 \times 0.3 \times 34}{88} = 0.06mm^2$$

Wire copper area for secondary winding:

$$A_S = \frac{0.45 \cdot f_{Cu} \cdot A_{Ne}}{N_S}$$ **(Eq. 33)**

$$A_S = \frac{0.45 \cdot 0.3 \cdot 34mm^2}{12} = 0.38mm^2$$

Wire copper area for auxiliary winding:

$$A_{Vcc} = \frac{0.05 \cdot f_{Cu} \cdot A_{Ne}}{N_{Aux}}$$ **(Eq. 34)**

$$A_{Vcc} = \frac{0.05 \cdot 0.3 \cdot 34mm^2}{14} = 0.03mm^2$$

Wire size can be calculated in AWG units:

$$AWG = 9.97 \cdot (1.8277 - (2 \cdot \log(d)))$$ **(Eq. 35)**

Wire diameter from copper area:

$$d = 2 \cdot \sqrt{\frac{A}{\pi}} \qquad \textbf{(Eq. 36)}$$

Wire diameter from AWG units:

$$d = 10^{\left(\frac{1.8277}{2} - \frac{AWG}{2 \cdot 9.97}\right)} \qquad \textbf{(Eq. 37)}$$

Wire size in AWG units, using a combination of Eq. 35 and Eq. 36:

$$AWG_{Pc} = 9.97 \cdot \left(1.8277 - \left(2 \cdot \log\left(2 \cdot \sqrt{\frac{A_P}{\pi}}\right)\right)\right)$$

$$AWG_{Pc} = 9.97 \cdot \left(1.8277 - \left(2 \cdot \log\left(2 \cdot \sqrt{\frac{0.06mm^2}{\pi}}\right)\right)\right)$$

$AWG_{Pc} = 30$

$$AWG_{Sc} = 9.97 \cdot \left(1.8277 - \left(2 \cdot \log\left(2 \cdot \sqrt{\frac{A_S}{\pi}}\right)\right)\right)$$

$$AWG_{Sc} = 9.97 \cdot \left(1.8277 - \left(2 \cdot \log\left(2 \cdot \sqrt{\frac{0.38mm^2}{\pi}}\right)\right)\right)$$

$AWG_{Sc} = 21$

$$AWG_{Vccc} = 9.97 \cdot \left(1.8277 - \left(2 \cdot \log\left(2 \cdot \sqrt{\frac{A_{Aux}}{\pi}}\right)\right)\right)$$

$$AWG_{Vccc} = 9.97 \cdot \left(1.8277 - \left(2 \cdot \log\left(2 \cdot \sqrt{\frac{0.03mm^2}{\pi}}\right)\right)\right)$$

$AWG_{Vccc} = 32$

It is good practice to use smaller wires in parallel instead of using one big wire. However, the following conditions should be satisfied for choosing the wire size and number of parallel wires:

- $EffCuArea_X$ (Eq. 40) ≤ A_X (Eq. 34/35)
- S_X (Eq. 41) ≤ 8 A/mm²
- NP_X ≤ 10
- 0.18 mm ≤ wire diameter ≤ 0.6 mm

Note: X = P/primary or S/secondary winding

Wire size in AWG unit for primary:	AWG_P	30
Num. of parallel wires for primary:	NP_P	1
Insulation thickness of primary wire:	INS_P	0.02 mm
Wire size in AWG units for secondary:	AWG_S	21
Num. of parallel wires for secondary:	NP_S	1
Insulation thickness of secondary wire:	INS_S	0.1 mm

Typically, the auxiliary winding consists of only one wire and its size is insignificant due to low current.

Recalculate wire diameter using Eq. 37:

$$d_P = 10^{\left(\frac{1.8277}{2} - \frac{AWG_P}{2 \cdot 9.97}\right)}$$

$$d_P = 10^{\left(\frac{1.8277}{2} - \frac{30}{2 \cdot 9.97}\right)} = 0.25mm$$

$$d_S = 10^{\left(\frac{1.8277}{2} - \frac{AWG_S}{2 \cdot 9.97}\right)}$$

$$d_S = 10^{\left(\frac{1.8277}{2} - \frac{21}{2 \cdot 9.97}\right)} = 0.72mm$$

Eff. copper area:

$$EffCuArea = \left(\frac{d}{2}\right)^2 \cdot \pi \cdot NP \quad \textbf{(Eq. 38)}$$

$$EffCuArea_P = \left(\frac{d_P}{2}\right)^2 \cdot \pi \cdot NP_P \qquad EffCuArea_P = \left(\frac{0.25}{2}\right)^2 \cdot \pi \cdot 88 = 0.05mm^2$$

$$EffCuArea_S = \left(\frac{d_S}{2}\right)^2 \cdot \pi \cdot NP_S \qquad EffCuArea_S = \left(\frac{0.72mm}{2}\right)^2 \cdot \pi \cdot 12 = 0.41mm^2$$

Current density:

$$S = \frac{I_{RMS}}{EffCuArea} \quad \textbf{(Eq. 39)}$$

$$S_P = \frac{I_{PRMS}}{EffCuArea_P} \qquad S_P = \frac{0.33}{0.05} = 6.35\frac{A}{mm^2}$$

$$S_S = \frac{I_{SRMS}}{EffCuArea_S} \qquad S_S = \frac{2.49}{0.41} = 6.01\frac{A}{mm^2}$$

Wire outer diameter including insulation:

$$Od = d + (2 \cdot INS) \quad \textbf{(Eq. 40)}$$

$$Od_P = d_P + (2 \cdot INS_P) \qquad Od_P = 0.25 + (2 \times 0.02) = 0.29mm$$

$$Od_S = d_S + (2 \cdot INS_S) \qquad Ods = 0.72 + (2 \times 0.1) = 0.92mm$$

Max. number of turns per layer:

$$NL = \left\lfloor \frac{BW_e}{Od \cdot NP} \right\rfloor \quad \textbf{(Eq. 41)}$$

$$NL_P = \left\lfloor \frac{BW_e}{Od_P \cdot NP_P} \right\rfloor \qquad NL_P = \left\lfloor \frac{11}{0.29 \times 1} \right\rfloor = 37Turns/Layer$$

$$NL_S = \left\lfloor \frac{BW_e}{Od_S \cdot NP_S} \right\rfloor \qquad NLs = \left\lfloor \frac{11}{0.92 \times 1} \right\rfloor = 12Turns/Layer$$

Min. number of layers:

$$Ln = \left\lceil \frac{N}{NL} \right\rceil \quad \textbf{(Eq. 42)}$$

$$Ln_P = \left\lceil \frac{N_P}{NL_P} \right\rceil \qquad Ln_P = \left\lceil \frac{88}{37} \right\rceil = 3Layers$$

$$Ln_S = \left\lceil \frac{N_S}{NL_S} \right\rceil \qquad Lns = \left\lceil \frac{12}{12} \right\rceil = 1Layer$$

8.6 Reverse voltage of diode (D21, D22, D12)

The output rectifier diodes in Flyback converters are subjected to large peak and RMS current stress. The values depend on the load and operating mode. The voltage requirements depend on the output voltage and transformer winding ratio.

Max. reverse voltage for output diode 1:

$$V_{RDiode} = V_{OUT} + \left(V_{DCMaxPk} \cdot \frac{N_S}{N_P} \right) \quad \textbf{(Eq. 43A)} \qquad V_{RDiode1} = 12 + \left(452.54 \times \frac{12}{88} \right) = 73.71V$$

Max. reverse voltage for output diode 2:

$$V_{RDiode} = V_{OUT} + \left(V_{DCMaxPk} \cdot \frac{N_S}{N_P} \right) \quad \textbf{(Eq. 43A)} \qquad V_{RDiode2} = 12 + \left(452.54 \times \frac{5}{88} \right) = 30.71V$$

Max. reverse voltage for the V_{CC} diode:

$$V_{RDiode} = V_{Vcc} + \left(V_{DCMaxPk} \cdot \frac{N_{Vcc}}{N_P} \right) \quad \textbf{(Eq. 43B)} \qquad V_{RDiode} = 14 + \left(452.54 \times \frac{14}{88} \right) = 86.00V$$

8.7 Clamping network (R11, C15, D11)

Clamping voltage:

$$V_{Clamp} = V_{DSMax} - V_{DCMaxPk} - V_R \quad \textbf{(Eq. 44)} \qquad V_{Clamp} = 600 - 452.54 - 90.2 = 57.25V$$

To calculate the clamping network, it is necessary to know the leakage inductance. The most common approach is to have the leakage inductance value given as a percentage of the primary inductance.
If it is known that the transformer construction is very consistent, measuring the primary leakage inductance by shorting the secondary windings will give an exact number (assuming the availability of a good LCR analyzer).

Leakage inductance in % of L_P:	$L_{LK\%}$	1.06%

Leakage inductance:

$$L_{LK} = L_{LK\%} \cdot L_P \quad \textbf{(Eq. 45)} \qquad L_{LK} = 1.06\% \times 1 \times 10^{-3} = 10.7\mu H$$

Clamping capacitor :

$$C_{Clamp} = \frac{I_{PMax}^2 \cdot L_{LK}}{(V_R + V_{Clamp}) \cdot V_{Clamp}} \quad \textbf{(Eq. 46)} \qquad C_{Clamp} = \frac{(0.82)^2 \times 10.7 \times 10^{-6}}{(90.2 + 57.25) \times 57.25} = 0.9nF$$

Clamping capacitor:	C_{Clamp}	1 nF

Clamping resistor:

$$R_{Clamp} = \frac{(V_{Clamp} + V_R)^2 - V_R^2}{0.5 \cdot L_{LK} \cdot I_{PMax}^2 \cdot f_S} \quad \textbf{(Eq. 47)} \qquad R_{Clamp} = \frac{(57.25 + 90.2)^2 - (90.2)^2}{0.5 \times 10.7 \times 10^{-6} \times (0.82A)^2 \times 55 \times 10^3} = 68.2k\Omega$$

Clamping resistor:	R_{Clamp}	68 kΩ

8.8 Output capacitors

Output capacitors are highly stressed in Flyback converters. Normally, capacitors are chosen based on **three major parameters: capacitance, low ESR and ripple current rating.**
To calculate output capacitors, the max. voltage overshoot in case of switching off at max. load condition must be set.

8.8.1 Output capacitors 1 (C22, C23)

Max. voltage overshoot:	ΔV_{OUT1}	0.5 V

After switching off the load, the control loop needs about 10–20 internal clock periods to reduce the duty cycle.

Number of clock periods:	n_{CP}	20

Ripple current:

$$I_{Ripple1} = \sqrt{(I_{SRMS1})^2 - (I_{Out1})^2} \quad \textbf{(Eq. 49)}$$

$$I_{Ripple1} = \sqrt{(2.33)^2 - (1.25)^2} = 1.97A$$

Output capacitance (cal.):

$$C_{Out1} = \frac{I_{OUT1} \cdot n_{CP}}{\Delta V_{OUT1} \cdot f} \quad \textbf{(Eq. 50)}$$

$$C_{Out1} = \frac{1.25 \times 20}{0.5 \times 55 \times 10^3} = 909\mu F$$

The output capacitor can be selected, as the following conditions can be summarized as the following:
- Rated voltage of cap. ≥ (1.45 V_{Out})
- (I_{acR} nc) close to I_{Ripple}
- (C_{OUT} nc) close to C_{OUT_cal}
- nc ≤ 5

We chose Rubycon ZLH (low impedance)
1000 µF 16 V (R_{ESR1} = 0.028 Ω, I_{acR} = 1.76 A @ 100 kHz 105°C)

Output capacitor:	C_{Out1}	1000 µF
Number of parallel capacitors:	nc	1

8.8.2 Output capacitors 2 (C28, C29)

Max. voltage overshoot:	ΔV_{OUT2}	0.25 V

After switching off the load, the control loop needs about 10–20 internal clock periods to reduce the duty cycle.

Number of clock periods:	n_{CP}	20

Ripple current:

$$I_{Ripple2} = \sqrt{(I_{SRMS2})^2 - (I_{Out2})^2} \quad \textbf{(Eq. 49)}$$

$$I_{Ripple2} = \sqrt{(0.36)^2 - (0.2)^2} = 0.30A$$

Output capacitance (cal.):

$$C_{Out2} = \frac{I_{OUT2} \cdot n_{CP}}{\Delta V_{OUT2} \cdot f} \quad \textbf{(Eq. 50)}$$

$$C_{Out2} = \frac{0.2 \times 20}{0.25 \times 55 \times 10^3} = 291\mu F$$

The output capacitor can be selected, as the following conditions can be summarized as the following:
- Rated voltage of cap. ≥ (1.45 V_{Out})
- (I_{acR} nc) close to I_{Ripple}
- (C_{OUT} nc) close to C_{OUT_cal}
- nc ≤ 5

We choose Rubycon ZLH (low impedance) 330 µF 10 V (R_{ESR2} = 0.094 Ω, I_{acR} = 0.54 A @ 100 kHz 105°C)

Output capacitor:	C_{Out2}	330 µF
Number of parallel capacitors:	nc	1

8.9 Output filter

The output filter consists of one capacitor and one inductor in a L-C filter topology.
Zero frequency of output capacitors and associated ESR:

8.9.1 Output filter 1 (L21, C24)

$$f_{ZCOut1} = \frac{1}{2 \cdot \pi \cdot R_{ESR1} \cdot C_{Out1}} \quad \textbf{(Eq. 51)}$$

$$f_{ZCOut1} = \frac{1}{2 \times \pi \times 0.028 \times 1000 \times 10^{-6}} = 5.68kHz$$

This equation is based on the assumption that all output capacitors have the same capacitance and ESR.

Ripple voltage at first stage:

$$V_{Ripple1} = \frac{I_{SMax1} \cdot R_{ESR1}}{nc} \quad \textbf{(Eq. 52)}$$

$$V_{Ripple1} = \frac{5.66 \times 0.028}{1} = 0.16V$$

The inductance is required to compensate the zero frequency caused by output capacitors:

L-C filter inductance:	L_{OUT1}	2.2 µH

L-C capacitor (cal.):

$$C_{LC1} = \frac{(C_{Out1} \cdot R_{ESR1})^2}{L_{Out1}} \quad \textbf{(Eq. 53)}$$

$$C_{LC1} = \frac{(1000 \times 10^{-6} \times 0.028)^2}{2.2 \times 10^{-6}} = 356\mu F$$

L-C capacitor:	C_{LC1}	470 µF

Frequency of L-C filter:

$$f_{LC1} = \frac{1}{2 \cdot \pi \cdot \sqrt{C_{LC1} \cdot L_{OUT1}}} \quad \textbf{(Eq. 54)}$$

$$f_{LC1} = \frac{1}{2 \cdot \pi \cdot \sqrt{470 \times 10^{-6} \times 2.2 \times 10^{-6}}} = 4.95kHz$$

Ripple voltage at second stage:

$$V_{Ripple2} = V_{Ripple1} \cdot \frac{\frac{1}{2 \cdot \pi \cdot f \cdot C_{LC1}}}{\frac{1}{2 \cdot \pi \cdot f \cdot C_{LC1}} + (2 \cdot \pi \cdot f \cdot L_{OUT1})} \quad \textbf{(Eq. 55)}$$

$$V_{Ripple2} = 0.16 \times \frac{\frac{1}{2 \times \pi \times 55 \times 10^3 \times 470 \times 10^{-6}}}{\frac{1}{2 \times \pi \times 55 \times 10^3 \times 470 \times 10^{-6}} + (2 \times \pi \times 55 \times 10^3 \times 2.2 \times 10^{-6})} = 1.27mV$$

8.9.2 Output filter 2 (L22, C210)

$$f_{ZCOut2} = \frac{1}{2 \cdot \pi \cdot R_{ESR2} \cdot C_{Out2}} \quad \textbf{(Eq. 51)}$$

$$f_{ZCOut2} = \frac{1}{2 \times \pi \times 0.094 \times 330 \times 10^{-6}} = 5.13kHz$$

This equation is based on the assumption that all output capacitors have the same capacitance and ESR.

Ripple voltage at first stage:

$$V_{Ripple1} = \frac{I_{SMax2} \cdot R_{ESR2}}{nc} \quad \textbf{(Eq. 52)} \qquad V_{Ripple1} = \frac{0.91 \times 0.094}{1} = 0.09V$$

The inductance is required to compensate the zero frequency caused by output capacitors:

L-C filter inductance:	L_{OUT2}	4.7 µH

L-C capacitor (cal.):

$$C_{LC2} = \frac{(C_{Out2} \cdot R_{ESR2})^2}{L_{Out2}} \quad \textbf{(Eq. 53)} \qquad C_{LC1} = \frac{(330 \times 10^{-6} \times 0.094)^2}{4.7 \times 10^{-6}} = 205\mu F$$

L-C capacitor:	C_{LC2}	330 µF

Frequency of L-C filter:

$$f_{LC2} = \frac{1}{2 \cdot \pi \cdot \sqrt{C_{LC2} \cdot L_{OUT2}}} \quad \textbf{(Eq. 54)} \qquad f_{LC1} = \frac{1}{2 \cdot \pi \cdot \sqrt{330 \times 10^{-6} \times 4.7 \times 10^{-6}}} = 4.04kHz$$

Ripple voltage at second stage:

$$V_{Ripple2} = V_{Ripple1} \cdot \frac{\frac{1}{2 \cdot \pi \cdot f \cdot C_{LC2}}}{\frac{1}{2 \cdot \pi \cdot f \cdot C_{LC2}} + (2 \cdot \pi \cdot f \cdot L_{OUT2})} \quad \textbf{(Eq. 55)}$$

$$V_{Ripple2} = 0.09 \times \frac{\frac{1}{2 \times \pi \times 55 \times 10^3 \times 330 \times 10^{-6}}}{\frac{1}{2 \times \pi \times 55 \times 10^3 \times 330 \times 10^{-6}} + (2 \times \pi \times 55 \times 10^3 \times 4.7 \times 10^{-6})} = 0.46mV$$

8.10 V_{CC} capacitors (C16, C17)

The V_{CC} capacitor needs to ensure the power supply of the IC until the power can be provided by the V_{CC} winding. In addition, it is recommended to use a 100 nF ceramic capacitor very close between pins 7 and 8 in parallel to the V_{CC} capacitor. Alternatively, an HF-type electrolytic with low ESR and ESL may be used.

V_{CC} capacitor:

$I_{VCC\_Charge3}$ from datasheet:	$I_{VCC\_Charge3}$	3 mA
t_{SS} from datasheet:	t_{SS}	12 ms

$$C_{Vcc} > \frac{I_{VCC\_Charge3} \times t_{SS}}{V_{VCC\_ON} - V_{VCC\_OFF}} \quad \textbf{(Eq. 56A)} \qquad C_{Vcc} > \frac{3 \times 10^{-3} \times 12 \times 10^{-3}}{16 - 10} = 6\mu F$$

V_{CC} capacitor:	C_{Vcc}	22 µF

Start-up time:

V_{VCC_SCP} from datasheet:	V_{VCC_SCP}	1.1 V

$$t_{Start-up} = \frac{V_{VCC\_SCP} \cdot C_{VCC}}{I_{VCC\_Charge1}} + \frac{(V_{VCC\_ON} - V_{VCC\_SCP}) \cdot C_{VCC}}{I_{VCC\_Charge3}} \quad \textbf{(Eq. 56B)}$$

$$t_{Start-up} = \frac{1.1 \times 22 \times 10^{-6}}{0.2 \times 10^{-3}} + \frac{(16 - 1.1) \cdot 22 \times 10^{-6}}{3 \times 10^{-3}} = 238ms$$

8.11 Losses

Diode bridge forward voltage:	V_F	1 V

Input diode bridge loss:

$P_{DIN} = 2 \cdot I_{ACRMS} \cdot V_F$	**(Eq. 57)**	$P_{DIN} = 2 \times 0.36 \times 1 = 0.74W$
Copper resistivity @ 100°C:	ρ_{100}	0.0172 Ω · mm²/m
Copper resistance:		
$R_{Cu} = \frac{l_N \cdot N \cdot \rho_{100}}{EffCuArea}$	**(Eq. 58)**	
$R_{PCu} = \frac{l_N \cdot N_P \cdot \rho_{100}}{EffCuArea_P}$		$R_{PCu} = \frac{41.2mm \times 88 \times 0.0172 \frac{\Omega \cdot mm^2}{m}}{0.05mm^2} = 1205.44m\Omega$
$R_{SCu1} = \frac{l_N \cdot N_{S1} \cdot \rho_{100}}{EffCuArea_S}$		$R_{SCu1} = \frac{41.2mm \times 12 \times 0.0172 \frac{\Omega \cdot mm^2}{m}}{0.41mm^2} = 20.57m\Omega$
$R_{SCu2} = \frac{l_N \cdot N_{S2} \cdot \rho_{100}}{EffCuArea_S}$		$R_{SCu2} = \frac{41.2mm \times 5 \times 0.0172 \frac{\Omega \cdot mm^2}{m}}{0.41mm^2} = 8.57m\Omega$
Copper resistance loss on the primary side:		
$P_{PCu} = I_{PRMS}^2 \cdot R_{PCu}$	**(Eq. 59)**	$P_{PCu} = (0.33)^2 \times 1205.44 = 130.26mW$
Copper resistance loss on the secondary side:		
$P_{SCu1} = I_{SRMS1}^2 \cdot R_{SCu1}$	**(Eq. 60)**	$P_{SCu1} = (2.33)^2 \times 20.57 = 111.68mW$
$P_{SCu2} = I_{SRMS2}^2 \cdot R_{SCu2}$	**(Eq. 60)**	$P_{SCu2} = (0.36)^2 \times 8.57 = 1.11mW$
Total copper resistance loss:		
$P_{Cu} = P_{PCu} + P_{SCu1} + P_{SCu2}$	**(Eq. 61)**	$P_{Cu} = 130.26 + 111.68 + 1.11 = 243.10mW$
Output rectifier diode loss:		
$P_{DOut1} = I_{SRMS1} \cdot V_{FOut1}$	**(Eq. 62)**	$P_{DOut1} = 2.33 \times 0.3 = 0.70W$
$P_{DOut2} = I_{SRMS2} \cdot V_{FOut2}$	**(Eq. 62)**	$P_{DOut2} = 0.36 \times 0.3 = 0.11W$
Clamping network loss:		
$P_{Clamper} = \frac{1}{2} \cdot L_{LK} \cdot I_{PMax}^2 \cdot f_S \cdot \frac{V_{Clamp} + V_R}{V_{Clamp}}$	**(Eq. 63)**	$P_{Clamper} = \frac{1}{2} \times 10.7 \times 10^{-6} \times (0.82)^2 \times 55 \times 10^3 \times \frac{57.25 + 90.2}{57.25} = 0.51W$
Junction Temperature:	T_j	125°C
On-resistance at junction temperature:		
$R_{DSon@T_j} = R_{DSon@25°C} \cdot \left(1 + \frac{\alpha}{100}\right)^{(T_j - 25°C)}$	**(Eq. 64)**	$R_{DSon@T_j} = 4.03 \cdot \left(1 + \frac{0.8}{100}\right)^{(125-25)} = 8.59\Omega$
MOSFET losses in V_{ACmin} scenario:		
Switching loss in V_{ACmin} scenario:		
$P_{SON1} = \frac{1}{2} \cdot \left(C_{o(er)} + C_{DS}\right) \cdot (V_{DCMin} - V_R)^2 \cdot f_S$	**(Eq. 65)**	$P_{SON1} = \frac{1}{2} \times (3+4) \times 10^{-12} \times (95.69 - 90.2)^2 \times 55 \times 10^3 = 5.792\mu W$
Conduction loss in V_{ACmin} scenario:		
$P_{D1} = I_{PRMS}^2 \cdot R_{DSon@T_j}$	**(Eq. 66)**	$P_{D1} = (0.33)^2 \cdot 8.59 = 928.3mW$

Total MOSFET loss in V_{ACmin} scenario:

$$P_{MOSFET1} = P_{SON1} + P_{D1} \quad \textbf{(Eq. 67)} \qquad P_{MOSFET1} = 5.792\,\mu W + 928.3mW = 928.3mW$$

MOSFET losses in V_{ACmax} scenario:

Switching loss in V_{ACmax} scenario:

$$P_{SON2} = \tfrac{1}{2}\cdot\left(C_{o(er)} + C_{DS}\right)\cdot\left(V_{DCMaxPk} - V_R\right)^2 \cdot f_S \quad \textbf{(Eq. 68)} \qquad P_{SON1} = \tfrac{1}{2}\times(3+4)\times10^{-12}\times(424.26-90.2)^2\times72\times10^3 = 32.9mW$$

Conduction loss in V_{ACmax} scenario:

$$P_{D2} = \tfrac{1}{3}\cdot R_{DSon@T_j}\cdot I_{PMax}^2\cdot\left(\frac{L_P\cdot I_{PMax}\cdot f_S}{V_{DCMaxPk}}\right) \quad \textbf{(Eq. 69)} \qquad P_{D2} = \tfrac{1}{3}\times8.59\times(0.82)^2\times\left(\frac{1\times10^{-3}\times0.82\times72\times10^3}{424.26}\right) = 255.15mW$$

Total MOSFET loss in V_{ACmax} scenario:

$$P_{MOSFET2} = P_{SON2} + P_{D2} \quad \textbf{(Eq. 70)} \qquad P_{MOSFET2} = 32.86mW + 255.15mW = 288mW$$

MOSFET losses:

$$P_{MOSFET} = \max\left(P_{MOSFET1}, P_{MOSFET2}\right) \quad \textbf{(Eq. 71)} \qquad P_{MOSFET} = \max(928.3mW, 288mW) = 928.3mW$$

8.12 Heat dissipater

A CoolSET™ in a DSO/DIP package cannot use a heatsink, but the copper area is possible. However, in general CoolMOS™ can use a heatsink.

Thermal resistance:

In case NO heatsink (for CoolSET™)

Typical thermal resistance [K/W]:

R_{thJA} = 96 K/W (DIP-7)
R_{thJA} = 110 K/W (DSO-12)
R_{thJA} = 185 K/W (DSO-8)

$$R_{th} = R_{thJA} \quad \textbf{(Eq. 72)} \qquad R_{th} = 96K/W$$

WITH heatsink (for controller)

$$R_{th} = R_{thJC} + R_{thHT} + R_{thHS} \quad \textbf{(Eq. 73)}$$

where R_{thJC} : TR. junction-case — From CoolMOS™/power switch datasheet
R_{thHT} : TR. case-heatsink — Typ. 1 K/W
R_{thHS} : TR. heatsink-ambient — Depending on heatsink

Delta temperature from MOSFET losses:

$$\Delta T = P_{MOSFET}\cdot R_{th} \quad \textbf{(Eq. 74)} \qquad \Delta T = 928.3mW\cdot96K/W = 89.1K$$

Max. junction temperature:

$$T_{j\max} = T_a + \Delta T \quad \textbf{(Eq. 75)} \qquad T_{j\max} = 50°C + 89.1 = 139.1°C$$

Max. junction temperature must not exceed the limitation stated in the datasheet, typically 150°C.

Controller loss:

$$P_{Controller} = V_{Vcc}\cdot I_{VCC\_Normal} \quad \textbf{(Eq. 76)} \qquad P_{Controller} = 13.75\times0.9\times10^{-3} = 12.4mW$$

Total loss:

$$P_{Losses} = P_{DIN} + P_{Cu} + P_{DOut1} + P_{DOut2} + P_{Clamp} + P_{MOSFET} + P_{Controller} \quad \textbf{(Eq. 77)}$$

$$P_{Losses} = 0.74 + 0.24 + 0.70 + 0.11 + 0.51 + 0.9283 + 0.0124 = 3.13W$$

Efficiency consideration after losses:

$$\eta_L = \frac{P_{OutMax}}{P_{OutMax} + P_{Losses}} \quad \textbf{(Eq. 78)}$$

$$\eta_L = \frac{16}{16 + 3.13} = 83.62\%$$

Please note that the calculated efficiency above is based on the **worst-case scenario** where the highest loss is present.

8.13 Regulation loop

Reference: TL431
Optocoupler: SFH617-3

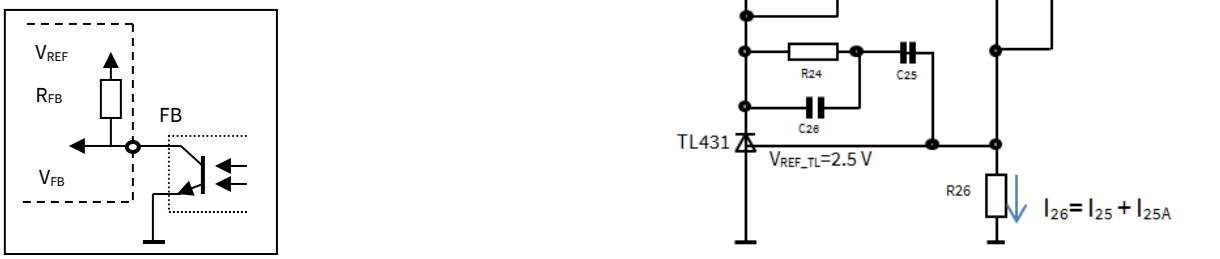

Figure 26 Regulation loop

TL431 reference voltage:	V_{REF_TL}	2.5 V
Min. current for TL431 diode:	I_{KAmin}	1 mA
Max. current of SFH617-3 diode:	I_{Fmax}	10 mA
Forward voltage of optocoupler diode:	V_{FOpto}	1.25 V
Optocoupler gain	G_C(150%)	1.5
CoolSET™ trimmed reference voltage:	V_{REF}	3.3 V
PWM-OP gain	G_{PWM}	2.05
CoolSET™	V_{FBmax}	2.75 V
Weighted factor of V_{Out1}	W_1	0.6
Weighted factor of V_{Out2}	W_2	0.4
Current for FB resistor R26	I_{R26}	1 mA
R_{FB} (FB pull-up resistor)	R_{FB}	15 kΩ

Primary side:

Max. FB current:

$$I_{FB\max} = \frac{V_{REF}}{R_{FB}} \quad \textbf{(Eq. 79)} \qquad I_{FB\max} = \frac{3.3}{15\times10^{3}} = 0.22mA$$

Min. FB current:

$$I_{FB\min} = \frac{V_{REF} - V_{FB\max}}{R_{FB}} \quad \textbf{(Eq. 80)} \qquad I_{FB\min} = \frac{3.3-2.75}{15\times10^{3}} = 0.036mA$$

Secondary side:

R26 value of voltage divider:

$$R_{26} = \left(\frac{V_{REF\_TL}}{I_{26}}\right) \quad \textbf{(Eq. 112)} \qquad R_{25} = \left(\frac{2.5}{1\times10^{3}}\right) = 2.5k\Omega$$

R26 value of voltage divider:	R26	2.5 kΩ

R25 value of voltage divider:

$$R_{25} = \left(\frac{V_{Out1} - V_{REF\_TL}}{W_1 \times I_{26}}\right) \quad \textbf{(Eq. 112A)} \qquad R_{25} = \left(\frac{12-2.5}{0.6\times1\times10^{3}}\right) = 15.83k\Omega$$

R25 value of voltage divider:	R25	16 kΩ

R25A value of voltage divider:

$$R_{25A} = \left(\frac{V_{Out2} - V_{REF\_TL}}{W_2 \times I_{26}}\right) \quad \textbf{(Eq. 112B)} \qquad R_{25A} = \left(\frac{5-2.5}{0.4\times1\times10^{3}}\right) = 6.25k\Omega$$

R25A value of voltage divider:	R25A	6.2 kΩ

R22 Value to supply opto. diode:

$$R22 \geq \frac{V_{Out1} - (V_{FOpto} + V_{REF\_TL})}{I_{F\max}} \quad \textbf{(Eq. 82)} \qquad R22 \geq \frac{12-(1.25+2.5)}{10\times10^{3}} = 825\Omega$$

R22 Value to supply opto. diode:	R22	820 Ω

R23 Value to supply TL431 diode:

$$R23 \leq \frac{V_{FOpto} + \left(R22 \cdot \frac{I_{FB\min}}{G_c}\right)}{I_{KA\min}} \quad \textbf{(Eq. 83)} \qquad R23 \leq \frac{1.25 + \left(820 \times \frac{0.036\times10^{-3}}{2}\right)}{1\times10^{-3}} = 1.27k\Omega$$

R_{23} Value to supply TL431 diode:	R23	1.2 kΩ

Output voltage from regulation loop:

$$V_{OUT1\_RL} = (R25 \times W_1 \times I_{26}) + V_{REF\_TL} \quad \textbf{(Eq. 112A)} \qquad V_{OUT\_RL} = \left(16\times10^{3} \times 0.6 \times 1 \times 10^{-3}\right) + 2.5 = 12.1V$$

$$V_{OUT2\_RL} = (R25A \times W_2 \times I_{26}) + V_{REF\_TL} \quad \textbf{(Eq. 112B)} \qquad V_{OUT\_RL} = \left(6.2\times10^{3} \times 0.4 \times 1 \times 10^{-3}\right) + 2.5 = 4.98V$$

Regulation loop elements:

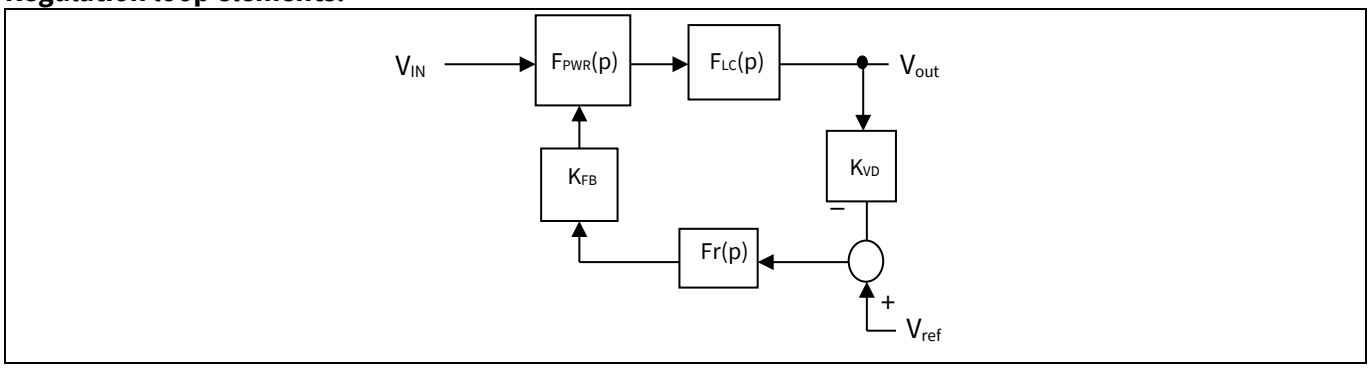

Figure 27 Block diagram of regulation loop

FB transfer characteristic:

$$K_{FB} = \frac{G_c \cdot R_{FB}}{R22} \quad \textbf{(Eq. 85)}$$

$$K_{FB} = \frac{1.5 \times 15 \times 10^3}{820} = 27.44$$

Gain of FB transfer characteristic:

$$G_{FB} = 20 \cdot \log(K_{FB}) \quad \textbf{(Eq. 86)}$$

$$G_{FB} = 20 \times \log 27.44 = 28.77dB$$

Voltage divider transfer characteristic:

$$K_{VD} = \frac{V_{REF\_TL}}{V_{OUT\_RL}} = \frac{R26}{R25 + R26} \quad \textbf{(Eq. 87)}$$

$$K_{VD} = \frac{2.5 \times 10^3}{16 \times 10^3 + 2.5 \times 10^3} = 0.14$$

Gain of voltage divider transfer characteristic:

$$G_{VD} = 20 \cdot \log(K_{VD}) \quad \textbf{(Eq. 88)}$$

$$G_{VD} = 20 \times \log(0.14) = -17.38dB$$

Zeros and poles of transfer characteristics:

Resistance at max. load pole:

$$R_{LH} = \frac{V_{OUT\_RL}^2}{P_{OutMax}} \quad \textbf{(Eq. 89)}$$

$$R_{LH} = \frac{12^2}{16} = 9\Omega$$

Resistance at min. load pole:

$$R_{LL} = \frac{V_{OUT\_RL}^2}{P_{OutMin}} \quad \textbf{(Eq. 90)}$$

$$R_{LL} = \frac{12^2}{3.2} = 45\Omega$$

Poles of power stage at max. load pole:

$$f_{OH} = \frac{1}{\pi \cdot R_{LH} \cdot (nc \cdot C_{OUT})} \quad \textbf{(Eq. 91)}$$

$$f_{OH} = \frac{1}{\pi \times 9 \times (1 \times 1000 \times 10^6)} = 35.37Hz$$

Poles of power stage at min. load pole:

$$f_{OL} = \frac{1}{\pi \cdot R_{LL} \cdot (nc \cdot C_{OUT})} \quad \textbf{(Eq. 92)}$$

$$f_{OL} = \frac{1}{\pi \times 45 \times (1 \times 1000 \times 10^6)} = 7.07Hz$$

In order to have sufficient phase margin at low-load conditions, we chose the zero frequency of the compensation network to come in the middle between the min. and max. load poles of the power stage.

Zero frequency of the compensation network:

$$f_{OM} = f_{OH} \cdot 10^{0.5 \cdot \log\left(\frac{f_{OL}}{f_{OH}}\right)}$$ **(Eq. 93)**

$$f_{OM} = 35.37 \times 10^{0.5 \times \log\left(\frac{7.07}{35.37}\right)} = 15.82Hz$$

With adjustment of the transfer characteristics of the regulator, we want to reach equal gain within the operating range and compensate the pole f_o of the power stage $F_{PWR}(\omega)$.
Because of the compensation of the output capacitor's zero (Eq. 53), we neglect it as well as the LC-filter pole (Eq. 56). Consequently, the transfer characteristic of the power stage is reduced to a single-pole response.
In order to calculate the gain of the open loop, we have to choose the crossover frequency.
We calculate the gain of the power stage with max. output power at the chosen crossover frequency.

Zero dB crossover frequency:	f_g	3 kHz

Transient impedance calculation:

Transient impedance defines the direct relationship between the level of the peak current and the FB pin voltage. It is required for the calculation of the power stage amplification.

Transient impedance:

$$Z_{PWM} = \frac{\Delta V_{FB}}{\Delta I_{PK}} = G_{PWM} \cdot \frac{R_{Sense}}{V_{csth}}$$ **(Eq. 94)**

$$Z_{PWM} = 2.05 \times \frac{1.214}{1} = 2.49\frac{V}{A}$$

Power stage at crossover frequency:

$$\left|F_{PWR}(f_g)\right| = \frac{1}{Z_{PWM}} \cdot \sqrt{\frac{R_{LH} \cdot L_p \cdot f \cdot \eta_P}{2}} \cdot \left(\frac{1}{\sqrt{1+\left(\frac{f_g}{f_{OH}}\right)^2}}\right)$$ **(Eq. 95)**

$$\left|F_{PWR}(f_g)\right| = \frac{1}{2.49} \times \sqrt{\frac{9 \times 1 \times 10^3 \times 55 \times 10^3 \times 0.85}{2}} \cdot \left(\frac{1}{\sqrt{1+\left(\frac{3 \times 10^3}{35.37}\right)^2}}\right) = 0.069$$

Gain of power stage at crossover frequency:

$$G_{PWR}(f_g) = 20 \cdot \log\left(\left|F_{PWR}(f_g)\right|\right)$$ **(Eq. 96)**

$$G_{PWR}(3kHz) = 20 \times \log(0.069) = -23.22dB$$

At the crossover frequency (f_g), we calculate the open-loop gain:

$$G_{OL}(\omega) = Gs(\omega) + Gr(\omega) = 0$$ **(Eq. 97)**

With the equations for the transfer characteristics, we calculate the gain of the regulation loop at f_g:

$$Gs(\omega) = G_{FB} + G_{PWR} + G_{VD}$$ **(Eq. 98)**

$$Gs(\omega) = 28.77 - 23.22 - 17.38 = -11.839dB$$

Separated components of the regulator:

$$Gr(\omega) = 0 - Gs(\omega)$$ **(Eq. 99)**

$$Gr(\omega) = 0 - (-11.839dB) = 11.839dB$$

R24 value of the compensation network:

$$R24 = 10^{\frac{Gr}{20}} \cdot \frac{R25 \cdot R26}{R25 + R26}$$ **(Eq. 100)**

$$R24 = 10^{\frac{11.83}{20}} \times \frac{2.5 \times 10^3 \times 16 \times 10^3}{2.5 \times 10^3 + 16 \times 10^3} = 8.45k\Omega$$

R24 value of the compensation network:	R24	12 kΩ

8.13.1.1.1 C26 value of the compensation network:

$$C26 = \frac{1}{2 \cdot \pi \cdot R24 \cdot f_g} \quad \textbf{(Eq. 101)} \qquad C26 = \frac{1}{2 \times \pi \times 12 \times 10^3 \times 3 \times 10^3} = 4.4nF$$

Using table E12, find the closest higher value:

C26 value of the compensation network:	C26	4.7 nF

C25 value of the compensation network:

$$C25 = \frac{1}{2 \cdot \pi \cdot R24 \cdot f_{OM}} - C26 \quad \textbf{(Eq. 102)} \qquad C25 = \frac{1}{2 \times \pi \times 12 \times 10^3 \times 15.82} - 4.7 \times 10^{-9} = 833nF$$

C25 value of the compensation network:	C25	820 nF

8.14 ZC and output OVP

R_{ZC}(R_{15}) value of ZC and output OVP:

User-defined V_{Out_OVP} value:	V_{Out_OVP}	16 V
R_{ZCD} value from datasheet:	R_{ZCD}	3 kΩ

$$R_{15} = R_{ZCD} \times \left[\left(\frac{N_{VCC}}{N_{S1}} \times \frac{V_{Out\_OVP} + V_{FOut}}{V_{ZCD\_OVP\_Min}} \right) - 1 \right] \quad \textbf{(Eq. 103)} \qquad R_{15} = 3 \times 10^3 \times \left[\left(\frac{14}{12} \times \frac{16 + 0.3}{1.9} \right) - 1 \right] = 27.03k\Omega$$

R_{15} value of ZC and output OVP:	R_{15}	27 kΩ

C_{19} value of ZC and output OVP:

Measured f_{osc2} (see Figure 4):	f_{osc2}	820 kHz
Delay time of controller:	t_{delay}	100 ns

$$C_{19} = \tan\left[2 \times \pi \times \left(\frac{1}{4} - t_{delay} \times f_{osc2} \right) \right] \times \frac{R_{15} + R_{ZCD}}{R_{15} \times R_{ZCD}} \times \frac{1}{2 \times \pi \times f_{osc2}} \quad \textbf{(Eq. 104)} \qquad C_{19} = \tan\left[2 \times \pi \times \left(\frac{1}{4} - 100 \times 10^{-9} \times 820 \times 10^3 \right) \right] \times \frac{27 \times 10^3 + 3 \times 10^3}{27 \times 10^3 \times 3 \times 10^3} \times \frac{1}{2 \times \pi \times 820 \times 10^3} = 127pF$$

C_{19} value of ZC and output OVP:	C_{19}	120 pF

8.15 Line OVP, brown-out and line selection

The voltage divider resistors R_{l1} (R_{18}+R_{18A}+R_{18B}) and R_{l2} (R_{19}) can be used to define the line OVP and brown-out of the system.

R_{19} value for line OVP and brown-out:

User-defined $V_{Line\_OVP\_AC}$ value:	$V_{Line\_OVP\_AC}$	320 V
V_{VIN_LOVP} value from datasheet:	V_{VIN_LOVP}	2.9 V
V_{VIN_LOVP} value from datasheet:	V_{VIN_BO}	0.4 V
V_{VIN_LOVP} value from datasheet:	V_{VIN_BI}	0.66 V
V_{VIN_REF} value from datasheet:	V_{VIN_REF}	1.52 V
Selected R_{l1} (R_{18}+R_{18A}+R_{18B}) value:	R_{l1}	9 MΩ

$$R_{19} > \frac{R_{l1} \times V_{VIN\_LOVP}}{(V_{Line\_OVP\_AC} \times \sqrt{2}) - V_{VIN\_LOVP}} \quad \textbf{(Eq. 105A)} \qquad R_{19} > \frac{9 \times 10^6 \times 2.9}{(320 \times \sqrt{2}) - 2.9} = 58.04k\Omega$$

R_{I2} (R_{19}) value for line OVP and brown-out: R_{19}	58.3 kΩ
$V_{BrownIn\_AC}$ value with the selected R_{19}: $V_{BrownIn\_AC} = \frac{\left(V_{VIN\_BI} \times \frac{R_{I1}+R_{I2}}{R_{I2}}\right) + V_{DC\ Ripple}}{\sqrt{2}}$ **(Eq. 106)**	$V_{BrownOut\_AC} = \frac{\left(0.66 \times \frac{9\times10^6 + 58.3\times10^3}{58.3\times10^3}\right)}{\sqrt{2}} = 73V$
$V_{Brown\text{-}out\_AC}$ value with the selected R_{19} and $V_{DC\ Ripple}$ (for full-load condition): $V_{BrownOut\_AC} = \frac{\left(V_{VIN\_BO} \times \frac{R_{I1}+R_{I2}}{R_{I2}}\right) + V_{DC\ Ripple}}{\sqrt{2}}$ **(Eq. 107)**	$V_{BrownOut\_AC} = \frac{\left(0.4 \times \frac{9\times10^6 + 58.3\times10^3}{58.3\times10^3}\right) + 24.5}{\sqrt{2}} = 61V$
$V_{Brown\text{-}out\_AC}$ value with the selected R_{19} and neglect $V_{DC\ Ripple}$ (for light-load condition):	$V_{BrownOut\_AC} = \frac{\left(0.4 \times \frac{9\times10^6 + 58.3\times10^3}{58.3\times10^3}\right)}{\sqrt{2}} = 44V$
$V_{LineSelection\_AC}$ value with the selected R_{19} and $V_{DC\ Ripple}$ (for full-load condition): $V_{LineSelection\_AC} = \frac{\left(V_{VIN\_REF} \times \frac{R_{I1}+R_{I2}}{R_{I2}}\right) + V_{DC\ Ripple}}{\sqrt{2}}$ **(Eq. 108)**	$V_{LineSelection\_AC} = \frac{\left(1.52 \times \frac{9\times10^6 + 58.3\times10^3}{58.3\times10^3}\right) + 24.5}{\sqrt{2}} = 184V$
$V_{LineSelection\_AC}$ value with the selected R_{19} and neglect $V_{DC\ Ripple}$ (for light-load condition):	$V_{LineSelection\_AC} = \frac{\left(1.52 \times \frac{9\times10^6 + 58.3\times10^3}{58.3\times10^3}\right)}{\sqrt{2}} = 167V$

9 References

[1] ICE5QSAG datasheet, Infineon Technologies AG

[2] ICE5QSBG datasheet, Infineon Technologies AG

[3] ICE5QRxxxxBG datasheet, Infineon Technologies AG

[4] ICE5QRxxxxAx datasheet, Infineon Technologies AG

[5] 60W 12V 5V SMPS demonstration board with ICE5QSBG and IPA80R600P7G

[6] AN-201609_PL83_025-16W 12V 5V SMPS Demo Board with ICE5QR4780AZ

[7] FlyCal_QR Q5 CoolSET_V1.0

Revision history

Document version	Date of release	Description of changes
V 1.3	2020 Mar 23	Page 19, section 4.10 Update protection Page 21, typical application circuit Update schematic Page 24, Output power of fifth-generation QR ICs Update models and output power curves Page 35, insulation thickness Update thickness and calculation Page 49, references Update links
V 1.2	2019 Jul 24	Page 19, section 4.10 Update protection
V 1.1	2017 Sep 18	Pages 25 and 27 Addition of ICE5QR1070AZ Page 29–48 Dual-output design example
V 1.0	2017 Mar 10	First release

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