Design Guide Line for PFC & LLC Converter using ICL5101

Design Guide

About this document

Scope and purpose

This document describes in details about how to design in the ICL5101 in a PFC and LLC application. It illustrates all necessary steps to get a design, related environment up and evaluate. It provides all information to become familiar with a comprehensive solution. As an example, the IFX ICL5101 evaluation board is build up to have a reverence to this design in guide line.

The ICL5101 is a mixed signal PFC + resonant controller for SMPS and LED (also dimmable) lighting applications using LLC topology for highest efficiency levels exceeding 94 %, including PFC for lowest THD < 5 % and high power factor correction figures > 95 % @ > 50 % load in a wide line input voltage range. The ICL5101 evaluation board is designed to show the performance and flexibility of the ICL5101. It supports an output power of 110 W, easily configurable by using only resistor settings without any user interface tool.

Intended audience

This document is intended for anyone who needs to design in the ICL5101 in a customized board, either for their own application tests or to use it as a reference for a new ICL5101-based development.

According to this guideline, an EXCEL based software tool is also available in version V1.1 in order to minimize the calculation efforts.

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1 Introduction

Two-stage converter “PFC+LLC” is, at the moment, the most popular topology for middle power range power supply which requires a good PF, THD and high efficiency – also for high ambient temperature applications.

Common uses are two separate ICs for PFC control and LLC control. Redundant peripheral supply and additional components may be required for redundant protection functions. Also, for improving the cooperation of two separate IC use is the synchronisation of different voltage levels or different timing meets the need of extended BOM cost.

Infineon smart “PFC+LLC” smart Combi controller ICL5101 combines PFC and LLC controller in one slim SO16 package. By using digital PFC controller and notch filter, a high PF and very low THD could be easily achieved with only 4 IC Pins and very few resistive peripheral components. The LLC stage also requires only a few simple resistors at periphery for normal operation and protection functions setting. The ideal cooperation of internal PFC and LLC blocks, the ICL5101 offers circuit designers the possibility of using a few simple components to achieve a good performance and reliable protection functions compared to the existing two IC solutions.

This Design Guide provides a guidance of how to design in a “PFC+LLC” converter using ICL5101 with an example of a wide input voltage range 110W/54V power supply by supporting an ambient temperature of T_{Amb} up to 100°C.

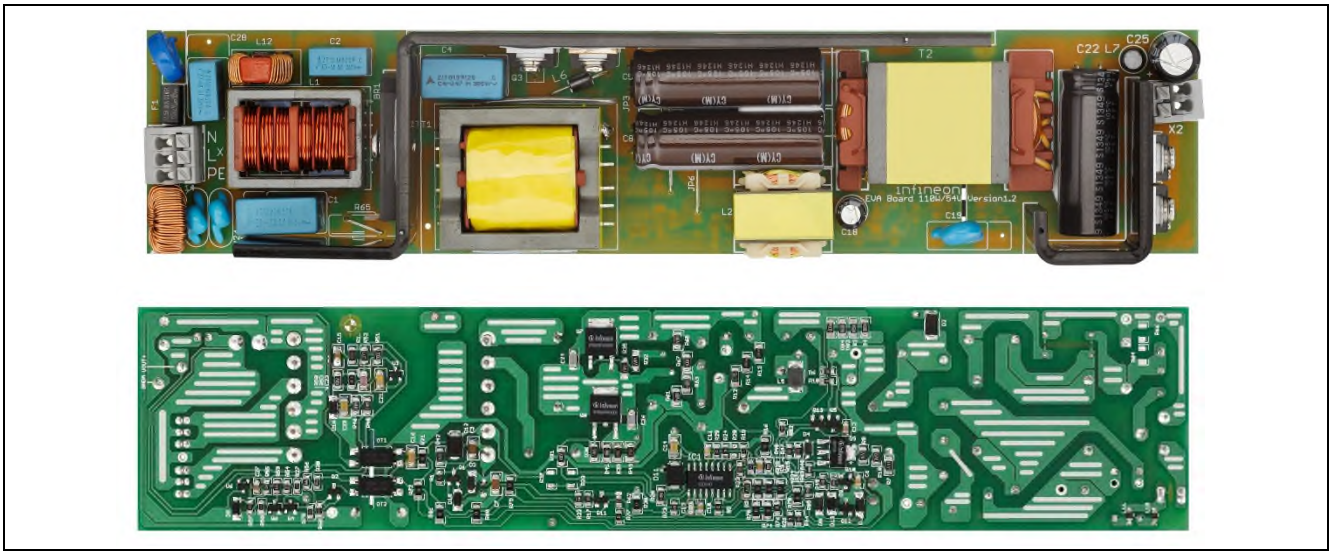

Figure 1 Demonstration Board of 110 W / 54 V Power Supply

2 ICL5101 Pin configuration

2.1 Package: PG-DSO-16

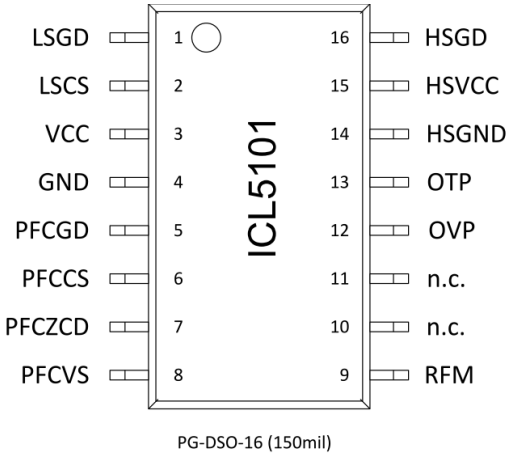

Figure 2 Package PG-DSO-16

2.2 Pin Configuration

Pin	Symbol	Function
1	LSGD	Low-side gate drive
2	LSCS	Low-side current sense signal
3	VCC	Chip Supply voltage
4	GND	IC GND
5	PFCGD	PFC gate drive
6	PFCCS	PFC current sense signal
7	PFCZCD	PFC zero current detection
8	PFCVS	PFC voltage sensing
9	RFM	Set RUN frequency
10	n.a.	NOT APPLICABLE: Leave PIN OPEN
11	n.a.	NOT APPLICABLE: SET to GND
12	OVP	Over voltage protection of secondary output
13	OTP	Over temperature protection
14	HSGND	High-side GND
15	HSVCC	High-side supply voltage
16	HSGD	High-side gate drive

Table 1 PIN Configuration

3 110W/54V Reference Design Brief Information

3.1 110W/54V reference design schematic

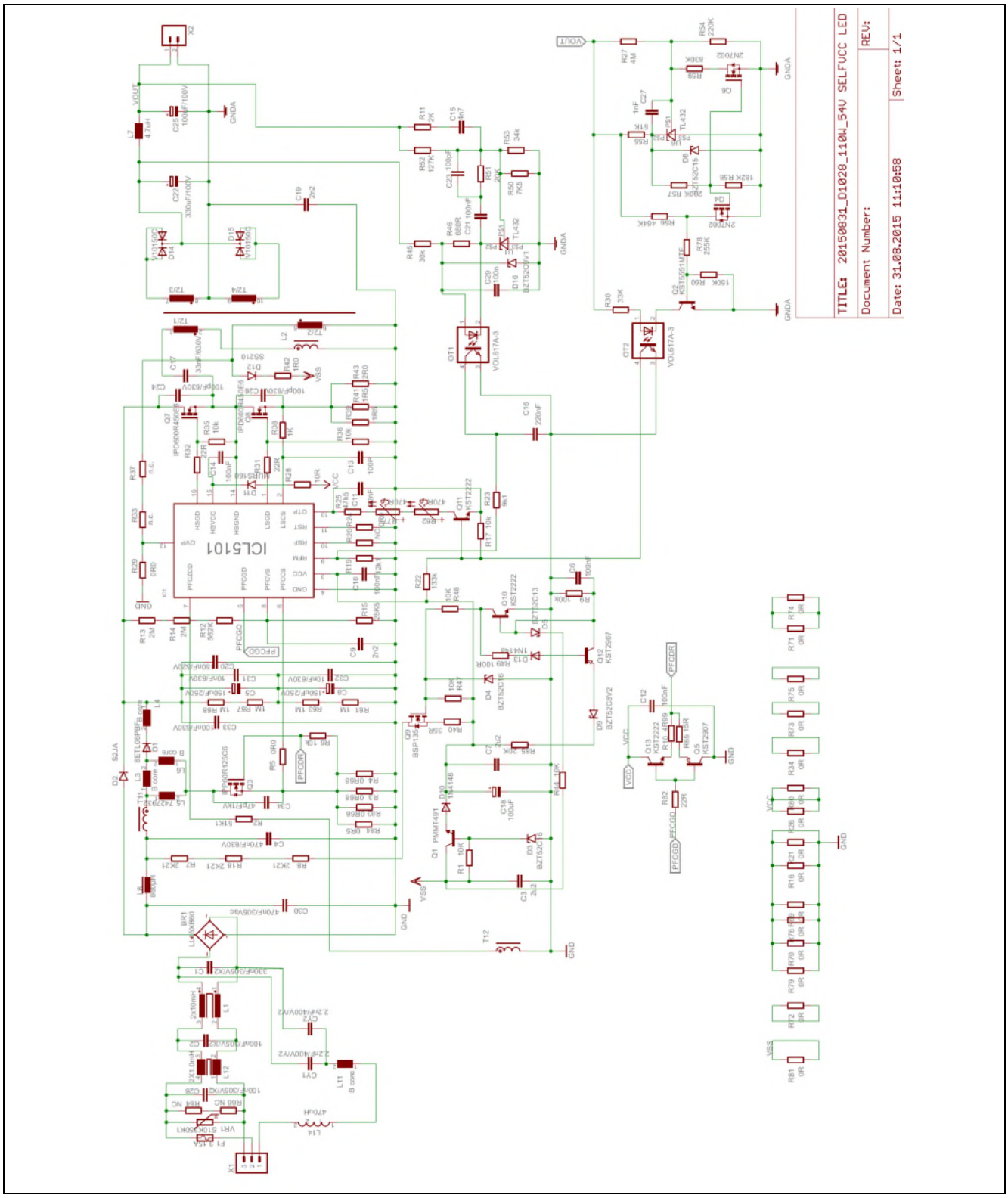

Figure 3 Reference design schematic

3.2 110W/54V Reference Design Brief Specification

Items	symbol	Min	Typ	Max	Units	Remark
AC Input Voltage	U_{in}	85	110 / 230	305	VAC	
DC Output Voltage	U_{out}		54		VDC	
DC Output Current	I_{out_nom}		2037		mA	
Max Output Current	I_{out_max}		2570		mA	
Resonant Frequency	f_r		55		kHz	
Line Input Frequency	f_{line}	47 / 57	50 / 60	53 / 63	Hz	Europe / USA
Power Factor	PF	96			%	@ 80% to 100% Load
T. Harmonic Dist.	THD			8	%	@Pout=25W to 110W
Efficiency	η		94		%	@Pout=110W, 230VAC input
Operation Ambient Temperature	T_a	-40	50	80	℃	
Maximum comp. case temperature	T_c			105	℃	
Life Time	t_{life}		50,000		hours	

Table 2 Design Specification

4 PFC Stage Design Guide

4.1 PFC Introduction

A Switch Mode Power Supply (“SMPS”) modulates the input voltage and current by switching on and off of the power switch and stores and transfers the electrical energy by magnetics and capacitors to achieve a voltage conversion and energy output. Nonlinear diodes are also necessary for SMPS. When connecting such a SMPS to AC Grid, it shifts the current phase from the phase of the line voltage and high current pulse generates high harmonic distortions to Grid. The phase shift caused unwanted reactive power increases the loading of the Grid and the high harmonic distortion could cause harmful effect to Grid or other electrical equipment connected to the Grid. This should be avoided. For such a purpose, Power Factor Correction (“PFC”) circuit is required. PFC modulates the input current of a SMPS to follow the waveform of the line voltage to minimize the reactive power and harmonic distortion to the Grid.

There are different kinds PFC circuit, boost, buck, buck-boost, flyback and etc. The most common and popular one is boost PFC. There are three different operation modes of boost PFC: CCM (Continuous Conduction Mode), CrCM (Critical Conduction Mode) and DCM (Discontinuous Conduction Mode). The PFC block of ICL5101 operates at CrCM Mode during normal operation and operates at DCM Mode at light load condition (approximately < 8% of nominal load). This helps reducing switching frequency of the PFC circuit at light load to ensure circuit stability and high efficiency. There is a hysteresis between CrCM and DCM Mode switching, which is shown in Figure **4**.

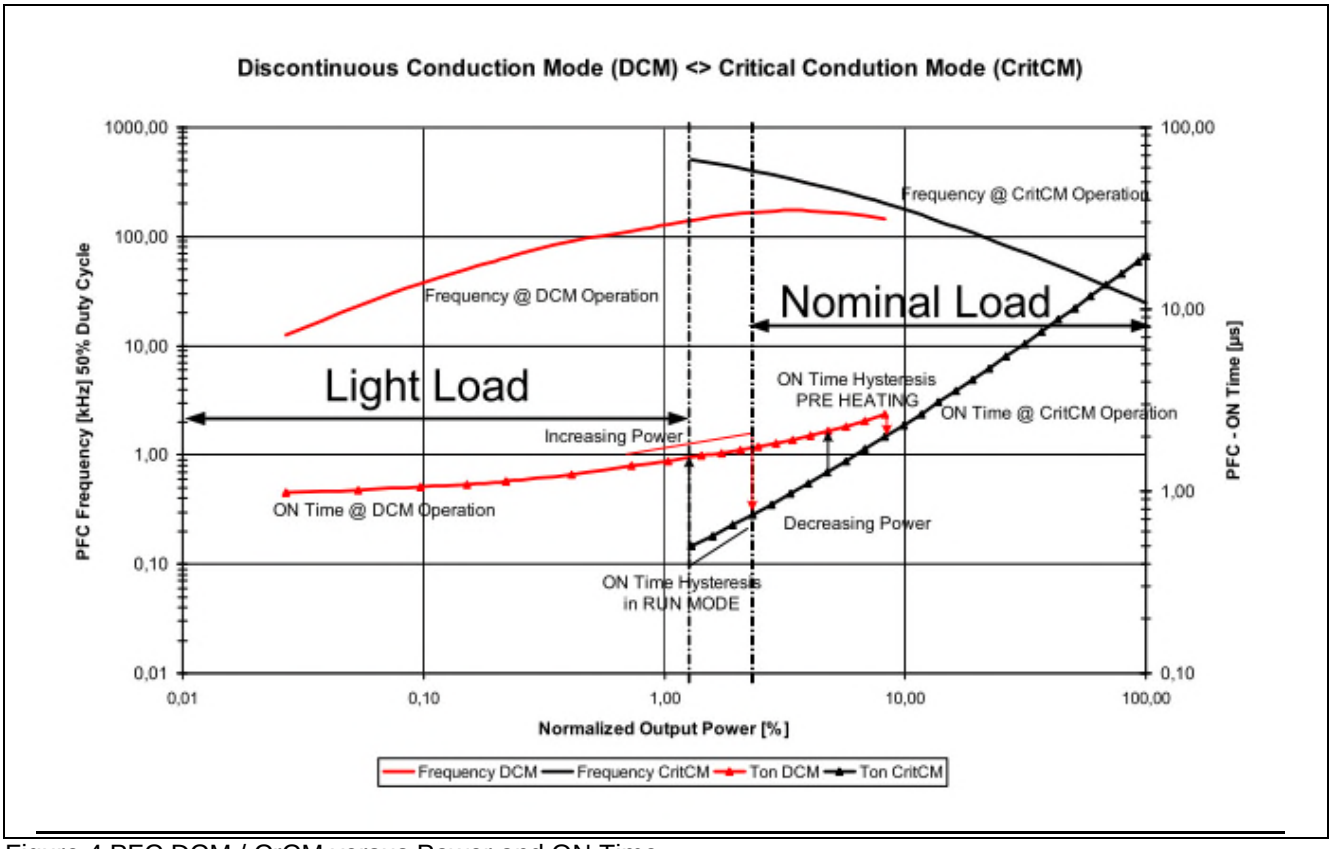

Figure 4 PFC DCM / CrCM versus Power and ON Time

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The On Time is regulated and set by IC internal digital regulator according to output power sensed via PFCVS pin and input voltage level sensed via PFCZCD pin. When output power decreases from nominal load to light load, the On Time decreases. If the On Time is shorter than approximate 500ns, PFC switches from CrCM Mode to DCM Mode. In the opposite direction, when On Time is longer than approximate 4us, PFC switches from DCM Mode to CrCM Mode.

To achieve CrCM Mode PFC, the most ICs sense the half sinusoidal waveform of the input voltage after bridge rectifier together with the feedback signal of the bus voltage to generate a reference voltage for peak current control, so that the peak current could follow the input voltage waveform and in parallel a stable bus voltage could be achieved. But the PFC block of ICL5101 has a constant “On Time” control, which makes the inductor peak current to follow the input voltage waveform automatically without sensing the input voltage waveform. This saves peripheral components. Following equations explain the principle.

Define $U(t)$ as input voltage after bridge rectifier and $\hat{U}$ as peak value of $U(t)$, we could have

$$U(t) = \hat{U}\left|\sin(wt)\right| \qquad \text{Equation 1}$$

Define L_{PFC} as PFC inductor, $i(t)$ as inductor current, $I(t)$ as inductor current peak envelope and t_{on} as MOSFET “On Time”, we could have

$$U(t) = L_{PFC} \bullet \frac{di(t)}{dt} = L_{PFC} \bullet \frac{I(t)}{t_{on}} \qquad \text{Equation 2}$$

Insert equation 1 into equation 2, we get:

$$I(t) = \frac{t_{on} \bullet \hat{U}}{L_{PFC}}\left|\sin(wt)\right| \qquad \text{Equation 3}$$

According to Equation 3, if t_{on} is set to constant under a pre-set AC input voltage, $I(t)$ follows input voltage waveform automatically.

Define $\hat{I}$ as peak value of $I(t)$, P_{in} as input power, we have

$$\hat{I} = \frac{P_{in} \bullet \sqrt{2}}{\hat{U}} \bullet \sqrt{2} \bullet 2 = \frac{4 \bullet P_{in}}{\hat{U}} = \frac{t_{on} \bullet \hat{U}}{L_{PFC}} \qquad \text{Equation 4}$$

$$t_{on} = \frac{4 \bullet P_{in} \bullet L_{PFC}}{\hat{U}^2} \qquad \text{Equation 5}$$

According to equation 5, t_{on} depends on P_{in} and $\hat{U}$. ICL5101 regulates t_{on} to different value under different power and input voltage conditions to achieve a gut PF and a stable bus voltage.

4.2 ICL5101 PFC Design Procedure

4.2.1 Calculation of the PFC Inductor

For PFC application, with consideration of efficiency and EMI, normally a low switching frequency is preferred. But in parallel to avoid audible noise the minimum frequency should be higher than 25 kHz.

Define $\hat{U}_{in}$ as peak value of input voltage, U_{bus} as PFC output voltage, f_{PFC} as PFC switching frequency, P_{PFC} as PFC output power and η as efficiency. Then we have following equation for PFC inductor:

$$L_{PFC} = \frac{\hat{U}_{in}^{2} * (U_{bus} - \hat{U}_{in}) * \eta}{4 * P_{PFC} * U_{bus} * f_{PFC}} \qquad \text{Equation 6}$$

Differentiation in three different PFC inductors L_{PFC} Values, after calculation choose the lowest PFC choke value:

- L_{PFC_Vinmin} @ V_{DCIN_min} see Equation 6.a
- L_{PFC_Vinmax} @ V_{DCIN_max} see Equation 6.b
- L_{PFC_tonmax} @ t_{ON_max} see Equation 8

$$L_{PFC\_Vin\min} = \frac{U_{DCIN\min}^{2} * (U_{bus} - U_{DCIN\min}) * \eta}{4 * P_{PFC} * U_{bus} * f_{PFC}} \quad \text{In respect to Equation 6} \qquad \text{Equation 6a}$$

$$L_{PFC\_Vin\max} = \frac{U_{DCIN\max}^{2} * (U_{bus} - U_{DCIN\max}) * \eta}{4 * P_{PFC} * U_{bus} * f_{PFC}} \quad \text{In respect to Equation 6} \qquad \text{Equation 6b}$$

Switching frequency equation could be converted from equation 6 as following:

$$f_{PFC} = \frac{\hat{U}_{in}^{2} * (U_{bus} - \hat{U}_{in}) * \eta}{4 * P_{PFC} * U_{bus} * L_{PFC}} \qquad \text{Equation 7}$$

Equation 7 is a cubic equation of $\hat{U}_{in}$. With fixed U_{bus}, η_{PFC}, P_{PFC} and L_{PFC}, the minimum switching frequency f_{PFC_min} could happen at peak value of maximum input voltage $\hat{U}_{in\_max}$ or at peak value of minimum input voltage $\hat{U}_{in\_min}$. To ensure f_{PFC_min} > 25 kHz, L_{PFC} should be smaller than the inductor value calculated with $\hat{U}_{in\_max}$ and $\hat{U}_{in\_min}$ when set f_{PFC} =25 kHz.

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Because ICL5101 has a limited maximum PFC Gate Signal On-Time t_{PFCON_max} = 24 µs (see datasheet ICL5101 chapter 3.4.4), it should also be considered that at $\hat{U}_{in\_min}$ within t_{PFCON_max} the maximum required inductor peak current could be achieved to ensure the full output power. Then we have following equation:

$$L_{PFC\_ton\max} = \frac{\hat{U}_{in\_\min}{}^2 * \eta * t_{PFCON\_max}}{4 * P_{PFC}} \qquad \text{Equation 8}$$

In the end the real L_{PFC} should be chosen to be smaller than the value which is calculated by equation 7 and 8. But it should also not be too small with consideration of EMI and t_{on} based PFC mode change which is introduced in chapter 4.1, especially for wide input voltage range design.

For 110W/54V reference design, according to chapter 3.2,
$\hat{U}_{in\_min} = 85V \bullet \sqrt{2} = 120.21V$ and $\hat{U}_{in\_max} = 305V \bullet \sqrt{2} = 431.34V$.

In this design we choose $U_{bus} = 450V > \hat{U}_{in\_max}$. As system efficiency requirement is 94% at full load and 230Vac input, we could have
$P_{in} = \frac{110W}{94\%} = 117.02W = \frac{P_{PFC}}{\eta_{PFC}}$, at 110W output power and 230Vac input voltage.
As P_{in} doesn't show large change under different input voltage, for estimation calculation for L_{PFC} we could use the above P_{in} for both $\hat{U}_{in\_min}$ and $\hat{U}_{in\_max}$ situation. Take $P_{in} = 117.02W$, $\hat{U}_{in\_min} = 120.21V$ and $\hat{U}_{in\_max} = 431.34V$ into equation 6 and to ensure minimum switching frequency to be larger than 25 kHz, f_{PFC} is set to 28 kHz, then we could have:

$$L_{PFC\_Vin\min} = \frac{120.2V^2 * (450V - 120.2V) * 0.94}{4 * 110W * 450V * 28kHz} = 808\mu H$$ Calculation via Equation 6a

L_{PFC} =808µH, at $\hat{U}_{in\_min} = 120.21V$;

$$L_{PFC\_Vin\max} = \frac{431.3V^2 * (450V - 431.3V) * 0.94}{4 * 110W * 450V * 28kHz} = 588.8\mu H$$ Calculation via Equation 6b

L_{PFC} =588.8µH, at $\hat{U}_{in\_max} = 431.34V$.

According to equation 8 and t_{PFCON_max} = 24µs, we could have

$$L_{PFC\_tPFCON\_max} = \frac{120.2V^2 * 0.94 * 24\mu s}{4 * 110W} = 740.9\mu H$$ Calculation via Equation 8

L_{PFC} =740.9µH, at $t_{PFCON\_max} = 24\mu s$ and $\hat{U}_{in\_min} = 120.21V$.

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So the practical L_{PFC} should be smaller than 588.8µH, for the reference design we choose L_{PFC} =580µH and a frequency of f_{PFC} @ nominal Line Input Voltage of 230V of 108kHz:

$$f_{PFC} = \frac{325V^2 * (450V - 325V) * 0.94}{4 * 110W * 450V * 580\mu H} = 108kHz$$ Calculated via Equation 7

Calculation of the maximum PFC peak current $\hat{I}_{PFC}$ at $\hat{U}_{in\_min}$:

Maximum Input Current I_{INmax}:

$$I_{IN\max} = \frac{P_{in}}{U_{in\_\min} * PowerFactor} = \frac{117W}{85V * 99\%} = 1.39A$$ Equation 9

Maximum PFC Peak Current $I_{PFCPeak}$:

$$\hat{I}_{PFCPeak} = I_{IN\max} * \sqrt{2} * 2 = 1.39A * \sqrt{2} * 2 = 3.9A$$ Equation 9a

With consideration of start-up condition and over power margin, the inductor saturation current I_{PFC_sat} should be at least

$$I_{PFC\_sat} > 1.1 \bullet \hat{I}_{PFC} = 1.1 * 3.9A = 4.29A$$ Equation 9b

Calculations of the number of turn of the PFC choke N_{PFC}:

We select an EFD30 core for the PFC choke; get values below of the data book of core.

K1 = 125
K2 = -0.712
Gap = 1.5mm

$$A_L = K1 * Gap^{K2} = 125 * 1.5mm^{-0.712} = 93,66nH$$ Equation 9c

$$N_{PFC} = \sqrt{\frac{L_{PFC}}{A_L}} = \sqrt{\frac{580\mu H}{93,66n}} = 78,69Turns$$ Equation 9d

N_{PFC} = 79 Turns

Cross checking of the calculated maximum saturation current from equation 9b with the maximum saturation current of the selected core:

Data book values of EFD30:
Maximum Flux Density: B_{max} = 340mT
Minimum Cross Section: A_{min} = 95mm²

$$I_{PFCChokeSat\max} = \frac{B_{\max} \bullet A_{\min}}{A_L \bullet N_{PFC}} = \frac{340mT \bullet 95mm^2}{93.66nH \bullet 79} = 4.37A$$ Equation 9e

$I_{PFC\_max} < I_{PFCChokeSatmax}$ → 4.29A < 4.37A → ok

PFC Stage Design Guide

The practical I_{PFC_sat} should be chosen also with consideration of efficiency, temperature rising, allowed or required over power limit and dimension.

CrCM PFC block of ICL5101 needs one auxiliary winding of PFC choke for Zero-Current-Detection. PFCZCD Pin senses the auxiliary winding voltage. When the PFCZCD Pin detects the voltage from above upper level (max. 1.5V) dropping to under lower level (min. 0.4V) the IC will initiate one turning on of PFC Gate. Normally the voltage dropping to under lower level is not critical, because when the energy in inductor reduces to zero the L and C swinging starts and the voltage on inductor will then change its polarity to negative automatically. The upper level of PFCZCD determines the turn ratio of the main inductor winding to auxiliary winding. We need to set an appropriate turn ratio to make sure that when MOSFET is turned off the voltage on PFCZCD Pin should be over 1.6V according to datasheet chapter 3.4.2. Define N_{PFC} as turns of PFC inductor main winding and N_{ZCD} as turns of auxiliary winding. We should ensure the turn ratio

$$n_{PFC} = \frac{N_{PFC}}{N_{ZCD}} < \frac{U_{bus} - \hat{U}_{in\_max}}{1.6V} = \frac{450V - 431{,}3}{1.6V} = 11.7 \qquad \text{Equation 10}$$

$$N_{ZCD} = \frac{N_{PFC}}{n_{PFC}} = \frac{79}{11.7} = 6.75 \qquad \text{Equation 10a}$$

N_{ZCD} = 7

So in 110W/54V reference design $\frac{N_{PFC}}{N_{ZCD}}$ should be smaller than 11.7. But to avoid high voltage on auxiliary winding, we could select the closest integer larger than $\frac{N_{PFC}}{11.7}$ as the turn number of the auxiliary winding.

4.2.2 Selection of the PZC Zero Crossing Detection (PFCZCD) Resistor

According to table 3.2 in datasheet of ICL5101, the current flowing through PFCZCD Pin is recommended to be in the range of -3mA < I_{PFCZCD} < 3mA. A resistor R_{ZCD} is required to limit the current flowing through PFCZCD Pin. Define U_{PFC_aux} as the voltage on PFC inductor auxiliary winding.

When PFC MOSFET is off, the maximum positive voltage on auxiliary winding is

$$U_{PFC\_aux+} = (U_{bus} - \hat{U}_{in\_\min}) \bullet \frac{N_{ZCD}}{N_{PFC}} = (450V - 120{,}2V) \bullet \frac{7}{79} = 29.22V \qquad \text{Equation 11}$$

When PFC MOSFET is on, the minimum negative voltage on auxiliary winding is:

$$U_{PFC\_aux-} = -\hat{U}_{in\_\max} \bullet \frac{N_{ZCD}}{N_{PFC}} = -431{,}2 \bullet \frac{7}{79} = -38.2V \qquad \text{Equation 12}$$

According to table 3.2 in datasheet of ICL5101, the minimum clamping of positive voltage on PFCZCD Pin is 4.1V and the maximum clamping of negative voltage on PFCZCD Pin is -1V. We should have the first criterion for R_{ZCD} selection:

$$R_{ZCD} \geq \frac{U_{PFC\_aux+} - 4.1V}{3mA} = \frac{29.2V - 4.1V}{3mA} = 8.4k\Omega \qquad \text{Equation 13}$$

$$R_{ZCD} \geq \left| \frac{-1V - U_{PFC\_aux-}}{-3mA} \right| = \left| \frac{-1V - (-38.2V)}{-3mA} \right| = 12.4k\Omega \qquad \text{Equation 14}$$

The PFCZCD Pin has a THD correction function, which extends the pulse width of PFC Gate signal according to detected I_{PFCZCD}. This could help to optimise the PFC input current waveform especially in the area near AC voltage zero crossing. Figure 5 shows the THD correction principle, which could also be found in chapter 2.3.5 in datasheet of ICL5101.

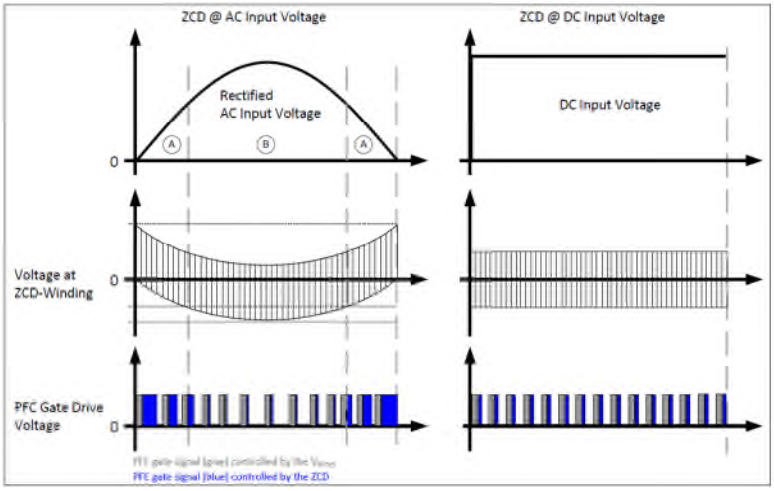

Figure 5 THD Improvement Automatic Pulse Width Extension

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So R_{ZCD} plays an important role for optimising the THD. The first value of R_{ZCD} can be calculated according to equation 15. A good practical value is given by a current < 1.5mA. For our example we use 800µA. In 110W/54V reference design, $\frac{N_{PFC}}{N_{ZCD}} = \frac{79}{7}$ and VBUS = 450V

$$R_{ZCD} = \frac{\frac{N_{ZCD}}{N_{PFC}} \bullet U_{bus}}{800\mu A} = \frac{\frac{7}{79} \bullet 450V}{800\mu A} = 49.8k\Omega$$ Equation 15

This is recommended by datasheet. The good practical R_{ZCD} value should be then fine-tuned in the application because there is a dependency on LPFC and the used PFC MOSFET.

Based on the calculation result of equation 13 and 14, we have RZCD resistance which should be above 12.4kΩ ($R_{ZCD} \geq 12.4k\Omega$). According to equation 15, the first value could be chosen as $R_{ZCD} = 49.8k\Omega$. After fine-tuning (adjustment of RZCD to the best THD results in vary the resistance up or down), THD is optimised when the zero crossing detection resistance is $R_{ZCD} = 51.1k\Omega$. Figure 6 shows the calculated components from chapter 4.2.1 and 4.2.2 in red.

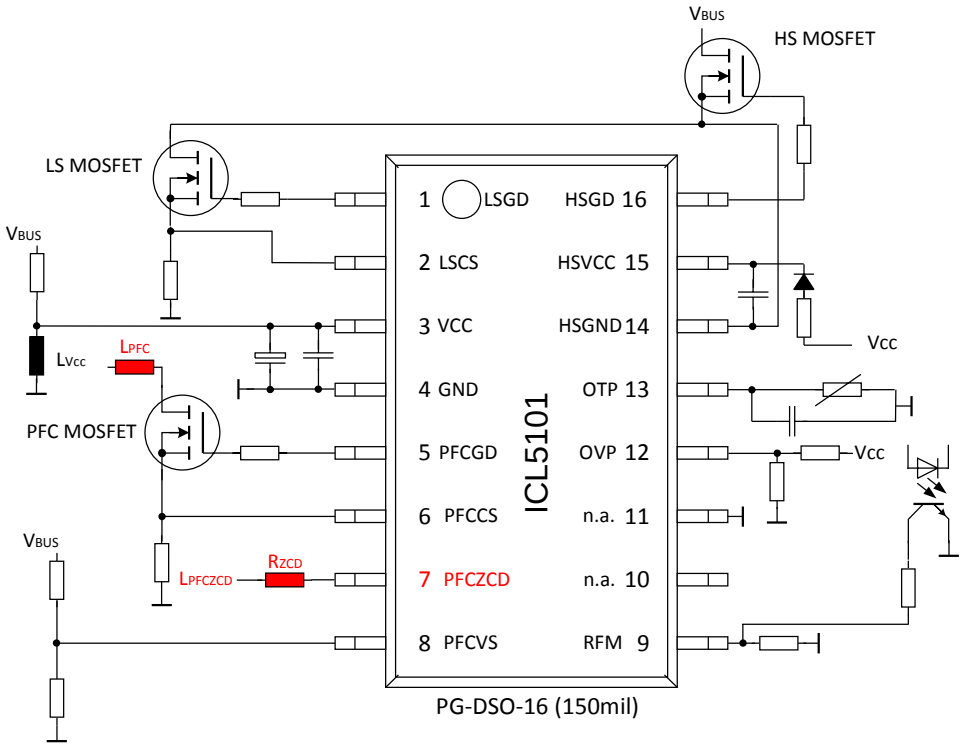

Figure 6 PIN Setup showing the calculated Components in red

4.2.3 Selection of the PFC Current Sense (PFCCS) Resistor

According to table 3.4.1 in datasheet the minimum value of turn-off threshold of PFCCS Pin is $V_{PFCCSOFF\_min} = 0.95V$. See datasheet chapter 3.4.1. The shunt resistor should be chosen to allow the maximum inductor peak current $\hat{I}_{PFC}$. We have following criterion:

$$R_{PFCCS} \leq \frac{V_{PFCCSOFF\_min}}{\hat{I}_{PFC}} \qquad \text{Equation 16}$$

But in the other side R_{PFCCS} should also not be too small, because it should limit the peak current to be smaller than the inductor saturation current:

$$R_{PFCCS} > \frac{V_{PFCCSOFF\_max}}{I_{PFC\_sat}} \qquad \text{Equation 17}$$

$V_{PFCCSOFF\_max} = 1.05V$ is the maximum value of the turn-off threshold of PFCCS Pin.

Selection of the practical value of R_{PFCCS} also depends on how large over power is allowed for the converter and whether the PF and THD should also be good during over power situation.

In 110W/54V reference design, we have defined inductor saturation current at $I_{PFC\_sat} = 6A$ and set the input current limitation for 130W. So

$$\hat{I}_{PFC} = \frac{4 * P_{PFC\_max}}{\hat{U}_{in\_min}} = \frac{4 * 130W}{85V_{ACIN} * \sqrt{2}} = 4.33A \qquad \text{Equation 17a}$$

According to Equation 16:

$R_{PFCCS} = \frac{V_{PFCCSOFF\_min}}{\hat{I}_{PFC}} = \frac{0.95V}{4.33A} = 0.22\Omega$. In practical we separate R_{PFCCS} to 4 parallel connected resistors for resistance value fine-tuning and also for thermal distribution. In the end we have

$R_3 = R_4 = 1\Omega$ and $R_{83} = R_{84} = 0.82\Omega$

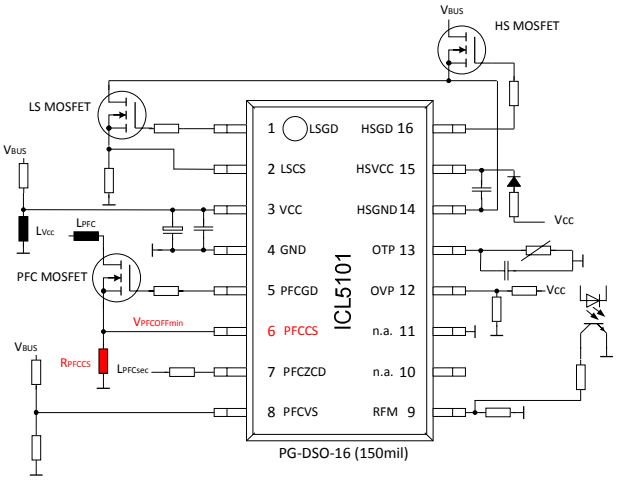

Figure 7 PIN Setup showing the calculated Components in red

4.2.4 Selection of PFC MOSFET

MOSFET selection is related to specified room temperature, DC-Link voltage, converter power, switching frequency, required efficiency, required limitation of component temperature rising, converter dimension and structure. In the end the practical MOSFET should be selected after testing and verification even at worst abnormal situation.

In PFC circuit with 450V DC-Link voltage and with surge protection diode from bridge rectifier to DC-Link capacitor (diode “D2” in 110W/54V reference design) normally 600V MOSFET is enough. To choose a suitable R_{DSon}, following brief theoretical calculation for MOSFET power loss could be taken as reference for the first selection. The practical R_{DSon} and package should be chosen according to above mentioned concrete criteria in the end.

Usually MOSFET loss includes conduction loss, switching on loss, switching off loss and Gate driving loss. Switching on loss in CrCM and DCM PFC is not necessary to calculate, because the current in PFC choke is zero at MOS switching on moment. But the loss of MOSFET output capacitor still needs to be considered.

The conduction loss and switching loss is hard to calculate, because in CrCM PFC the MOSFET switching frequency changes with the input voltage.

In order to approximately calculate the loss more easily, the input voltage of one double-line-frequency cycle can be segmented to several segments (e.g. in 110W/54V reference design, it is divided to 128 segments) and inside each segment the input voltage is approximated as constant, then also the switching frequency is constant. MOSFET power loss of each segment is calculated and will then be accumulated together for one cycle.

The segmented AC input voltage could be expressed as a function of time “t”, the segment number “i” and RMS value of “U_{in}”:

$$U_{in}(t, i, U_{in\_rms}) = \sqrt{2} \bullet U_{in\_rms} \bullet \sin\left\{2 \bullet \pi \bullet f_{line} \bullet \left[floor\left(\frac{t}{\frac{T_{line}}{2 \bullet i}} \right) \bullet \frac{T_{line}}{2 \bullet i} \right]\right\} \quad \text{Equation 18}$$

Note: “floor ()” is the round down equation to next possible integer.

“T_{line}” $= \frac{1}{f_{line}}$, is the line frequency cycle.

The PFC Inductor peak current envelope could be expressed as:

$$I_{peak}(t, i, U_{in\_rms}) = \frac{2 \bullet \sqrt{2} \bullet P_{PFC}}{\eta_{PFC} \bullet U_{in\_rms}} \bullet \sin\left\{2 \bullet \pi \bullet f_{line} \left[floor\left(\frac{t}{\frac{T_{line}}{2 \bullet i}} \right) \bullet \frac{T_{line}}{2 \bullet i} \right]\right\} \quad \text{Equation 19}$$

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The MOSFET on time could refer to equation 5. The off time till to inductor current dropping to zero could be expressed as:

$$t_{off}(t, i, U_{in\_rms}) = \frac{L_{PFC} \bullet I_{peak}(t, i, U_{in\_rms})}{U_{bus} - U_{in}(t, i, U_{in\_rms})}$$ Equation 20

The time from zero inductor current to MOSFET is turned on again could be expressed as:

$$t_{resonance} = \frac{1}{2} \bullet 2 \bullet \pi \bullet \sqrt{L_{PFC} \bullet C_{oss}}$$ Equation 21

Note: "C_{oss}" is the MOSFET output capacitance which could be read from datasheet.

The total switching cycle could be expressed as:

$$t_{sw}(t, i, U_{in\_rms}) = t_{on} + t_{off}(t, i, U_{in\_rms}) + t_{resonance}$$ Equation 22

To approximately calculate the MOSFET conduction loss during one double-line-frequency cycle, the time "t" in one cycle should be digitalized to $\frac{T_{line}}{2 \bullet i} \bullet n$ " . The conduction energy loss could then be expressed as:

$$E_{cycle\_con} = \sum_{n}^{i} \left\{ \left[\sqrt{\frac{t_{on}}{t_{sw}(\frac{T_{line}}{2 \bullet i} \bullet n, i, U_{in\_rms})}} \bullet \frac{I_{peak}(\frac{T_{line}}{2 \bullet i} \bullet n, i, U_{in\_rms})}{\sqrt{3}} \right]^2 \bullet R_{DSon} \right\} \bullet t_{sw}(\frac{T_{line}}{2 \bullet i} \bullet n, i, U_{in\_rms}) \bullet floor\left[\frac{\frac{T_{line}}{2 \bullet i}}{t_{sw}\left(\frac{T_{line}}{2 \bullet i} \bullet n, i, U_{in\_rms}\right)} \right]$$ Equation 23

The conduction power loss is then:

$$P_{loss\_MOS\_con} = E_{cycle\_con} \bullet 2 \bullet f_{line}$$ Equation 24

Note: The R_{DSon} value should be chosen based on the practical operation temperature. E.g. in 110W/54V reference design, a peak case temperature not over 105°C is required. The MOSFET junction temperature should be anyway lower than 150°C. Then we choose the R_{DSon} value based on 150°C junction temperature from the diagram from datasheet.

PFC Stage Design Guide

MOSFET switching energy loss could be approximately calculated as following:

$$E_{cycle\_sw} = \sum_{n}^{i} \left\{ \begin{array}{l} \frac{1}{2} \bullet I_{peak}(\frac{T_{line}}{2 \bullet i} \bullet n, i, U_{in\_rms}) \bullet U_{bus} \bullet t_{troff} \\ \bullet floor\left[\frac{\frac{T_{line}}{2 \bullet i}}{t_{sw}(\frac{T_{line}}{2 \bullet i} \bullet n, i, U_{in\_rms})} \right] \end{array} \right\} \quad \text{Equation 25}$$

The switching power loss is then:

$$P_{loss\_MOS\_sw} = E_{cycle\_sw} \bullet 2 \bullet f_{line} \quad \text{Equation 26}$$

Note: "t_{troff}" is the time period during turning off when MOSFET voltage and current changes. It could not be calculated exactly because the parasitic C_{GD} and C_{DS} capacitances change with the MOSFET V_{DS}. It can only be briefly approximately calculated according to Figure **8** as following:

$$t_{troff} = T_2 + T_3 \quad \text{Equation 27}$$

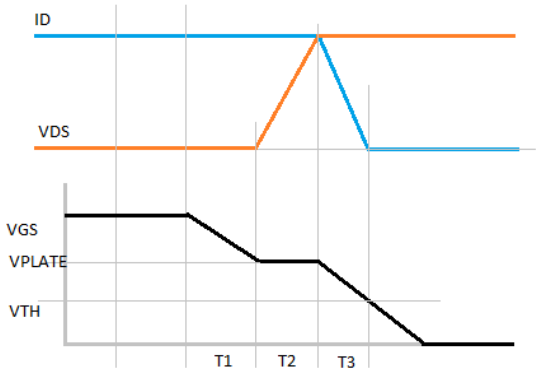

Figure 8 PFC MOSFET Turn OFF Procedure

$$T_2 = \frac{Q_{GD} * (R_{g\_off} + R_{g\_int})}{V_{g\_plate} - V_{off}} \quad \text{Equation 28}$$

$$T_3 = -(R_{g\_off} + R_{g\_int}) * C_{iss} * \ln(1 - \frac{V_{th}}{V_{g\_plate}}) \quad \text{Equation 29}$$

Note: "Q_{GD}" is the Gate-Drain charge of MOSFET at Drain Source voltage at 200V sees MOSFET DS

"V_{g_plate}" = VPlateau is the Gate plateau voltage see MOSFET DS

"R_{g_int}" is the internal gate resistance of MOSFET see MOSFET DS.

"R_{g_off}" is external set Gate resistance for turning off loop see MOSFET DS

"V_{off}" = VPFCGDASD turning off loop see DS of ICL5101 Chapter 3.4.5

"C_{iss}" is MOSFET input capacitance at 400V drain source voltage see MOSFET DS

"V_{th}" = VGS(th)typ is the MOSFET Gate threshold voltage see MOSFET DS

When $\left[2U_{in}(\frac{T_{line}}{2 \bullet i} \bullet n, i, U_{in\_rms}) - U_{bus}\right] > 0$, power loss of MOSFET output capacitor could be approximately calculated as following:

$$P_{loss\_MOS\_cos s} = \sum_{n}^{i} \left\{ \frac{Q_{oss} \bullet \left[2U_{in}(\frac{T_{line}}{2 \bullet i} \bullet n, i, U_{in\_rms}) - U_{bus}\right]}{2 \bullet floor\left[\frac{\frac{T_{line}}{2 \bullet i}}{t_{sw}(\frac{T_{line}}{2 \bullet i} \bullet n, i, U_{in\_rms})}\right]} \right\} \bullet 2 \bullet f_{line} \quad \text{Equation 30}$$

When $\left[2U_{in}(\frac{T_{line}}{2 \bullet i} \bullet n, i, U_{in\_rms}) - U_{bus}\right] \leq 0$, power loss of MOSFET output capacitor could be neglected because the "U_{ds}" of the MOSFET is zero at turning on moment for CrCM PFC.

Gate driving loss could be approximately presented as:

$$P_{loss\_MOS\_drive} = \sum_{n}^{i} \left\{ Q_g \bullet U_g \bullet floor\left[\frac{\frac{T_{line}}{2 \bullet i}}{t_{sw}(\frac{T_{line}}{2 \bullet i} \bullet n, i, U_{in\_rms})}\right] \right\} \bullet 2 \bullet f_{line} \quad \text{Equation 31}$$

Note: "Q_g" is Gate charge total.

"U_g" is Gate driver voltage.

With above theoretical calculation method an approximate power loss could be calculated for pre-selected MOSFET.

The absolute limit for MOSFET selection is that the junction temperature should be in the limit of $T_{j\max}$ at the situation of the case temperature stabilized at customer required case temperature T_c. Following equation could be applied for this limit:

$$T_{j\max} \geq T_c + R_{thjc} * \left(P_{loss\_MOS\_con} + P_{loss\_MOS\_SW} + P_{loss\_MOS\_Coss} + P_{loss\_MOS\_drive}\right) + Z_{thjc} * (P_{loss\_SW\_Tr\_\max}) \quad \text{Equation 32}$$

Note: "R_{thjc}" is the stable junction case thermal resistance of MOSFET.

"Z_{thjc}"is the transient junction case thermal impedance of MOSFET, which is related with pulse width and duty cycle, which could be checked in the "Max. Transient thermal impedance" diagram in MOSFET's datasheet.

"$P_{loss\_SW\_Tr\_\max}$" is the maximum transient switching off loss which happens at peak of $U_{in\_\min}$ (minimum AC input voltage):

$$P_{loss\_SW\_Tr\_max} = \frac{1}{2} \bullet \frac{2 \bullet \sqrt{2} \bullet P_{PFC}}{\eta_{PFC} \bullet U_{in\_min}} \bullet U_{bus} \qquad \text{Equation 33}$$

In 110W/54V reference design, with consideration of different criteria and requirements mentioned in begin of this chapter; we selected IPP60R125C6 after practical testing.

4.2.5 Selection of the PFC Gate Resistance (PFCGD)

The Gate Resistance should be selected with consideration of MOSFET power loss and EMI. A larger Gate Resistance slows down the turning on/off time, which leads to higher switching power loss, but it is good for EMI because of small dv/dt. Vice versa is good for switching power loss but bad for EMI.

The PFC Gate Driver of ICL5101 has a driver ability of 100mA sourcing and 500mA sinking. In order to maintain high switching frequency and low switching loss a big MOSFET is used. Therefore, a totem pole driver circuit is necessary, which consists of Q13 and Q5. For a freely setting of turning on/off time, the gate resistance is also separated to two paths with R10 and R65. The value of the gate resistances is adjusted to efficiency and EMI to $R_{PFCGD} = R_{82} = 22\Omega$.

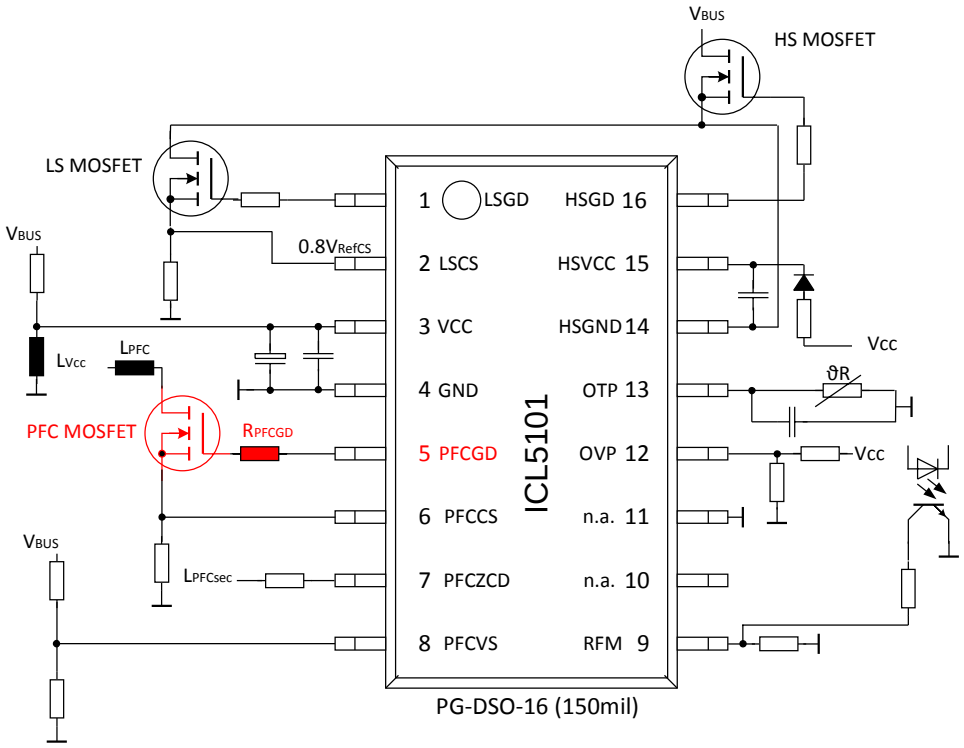

Figure 9 PIN Setup showing the calculated Components in red

4.2.6 Selection of the Bridge Rectifier

The selection of a bridge rectifier should be based on the practical requirement of input voltage range, surge current, efficiency and maximum allowed case temperature. Some main selection criteria are listed here.

1) Diode reverses breakdown voltage V_{BR_br}

The maximum reverse voltage V_{BR_br} should be larger than the maximum peak input voltage $\widehat{U}_{in\_max}$.

2) Average forward current

The bridge rectifier's average forward current limit at the required maximum case temperature should be larger than the maximum value of average input current $I_{in\_av\_max}$, which could be calculated according to following equation 34 and $\hat{I}_{in\_max} = 1.39A$ from equation 9:

$$I_{in\_av\_max} = \frac{2}{\pi} * \hat{I}_{in\_max} \qquad \text{Equation 34}$$

$$I_{in\_av\_max} = \frac{2}{\pi} * 1.39A = 0.89A$$

3) Peak surge forward current I_{FSM_BR}

The bridge rectifier's peak surge forward current I_{FSM_BR} should be able to cover the practical surge current requirement.

4) Forward voltage V_{F_BR}

To achieve a high efficiency, the rectifier forward voltage V_{F_BR} should be as small as possible at the nominal operating input current.

In 110W/54V reference design, a really low V_{F_BR} bridge rectifier LL15XB60 is chosen to meet the high efficiency and low temperature requirement.

4.2.7 Selection of the PFC Boost Diode

PFC boost diode is important for system efficiency. To select a PFC boost diode its forward voltage $V_{F\_PFC\_d}$, average rectified forward current $I_{F\_PFC\_d}$, peak repetitive forward current $I_{FM\_PFC\_d}$, reverse breakdown voltage $V_{br\_PFC\_d}$, reverse recovery time $t_{rr\_PFC\_d}$ are the first important parameter to be checked.

1) Reverse breakdown voltage $V_{br\_PFC\_d}$

The reverse breakdown voltage $V_{br\_PFC\_d}$ should be higher than U_{bus}. In our reference design for single phase input voltage and 450VDC bus voltage, $V_{br\_PFC\_d}$ = 600V is enough.

2) Peak repetitive forward current $I_{FM\_PFC\_d}$

The maximum peak repetitive forward current $I_{FM\_PFC\_d}$ should be larger than peak PFC inductor current $\widehat{I}_{PFC}$.

3) Average rectified forward current $I_{F\_PFC\_d}$

The limit of the average rectified forward current $I_{F\_PFC\_d}$ decrease with decreasing duty cycle and increasing diode case temperature. The detailed relation diagram between average forward current and duty cycle is normally not given in the datasheet. So for the selection of a diode for first trying, we could select a diode whose average rectified forward current at required case temperature is larger than the PFC output average current I_{PFC_out} at maximum system power.

$$I_{PFC\_out} = \frac{P_{sys\_\max}}{U_{bus}} = \frac{I_{out\_\max} * U_{OUT}}{U_{bus}} = \frac{2.57A * 54V}{450V} = 0.308A \qquad \text{Equation 35}$$

4) Forward voltage $V_{F\_PFC\_d}$

Forward voltage is directly related with system efficiency. It should be as small as possible. With the same current flowing through the diode, normally a diode with higher average rectified forward current limit has also lower forward voltage. Sometimes in purpose to achieve a high efficiency, this diode could be overdesigned from current ability point of view.

5) Reverse recovery time $t_{rr\_PFC\_d}$

For CrCM PFC and DCM PFC a normal fast recovery diode is enough. Reverse recovery time around 200ns is acceptable.

To meet the efficiency and temperature requirement, in reference design 8ETL06P from IR is chosen. It is 600V fast recovery diode with very low forward voltage.

4.2.8 Selection of PFC DC Link Capacitor (PFC BUS Capacitor)

Normally the bulk capacitor has to fulfil two requirements, bus voltage double line frequency ripple (The input and output high frequency ripple could be neglected here because for bulk capacitor the line frequency is not regulated and its ripple is much larger than the high frequency ripple.) and holdup time. In this reference design, the holdup time is not required.

The maximum double-line frequency ripple current is the PFC output current I_{out_PFC}.

$$I_{out\_PFC} = \frac{P_{PFC}}{U_{bus} * \eta_{PFC}} = \frac{110W}{450V * 97\%} = 252mA \qquad \text{Equation 36}$$

If we have $U_{bus\_ripple\_pp}$ as bus voltage peak to peak ripple requirement. We could have following equation for bus capacitor C_{bus} calculation:

$$C_{bus} = \sqrt{\left(\frac{1}{2 \bullet \pi \bullet 2 \bullet f_{line} \bullet \frac{U_{bus\_ripple\_pp}}{2}}\right)^2 + ESR^2{}_{cbus} \bullet I_{out\_PFC}} \qquad \text{Equation 37}$$

"ESR_{cbus}" is the ESR of "C_{bus}", which is normally very small and the influence is also very small for a capacitor impedance with large double-line frequency ripple. So it could be neglected and Equation 37 could be approximated to following form:

$$C_{bus} = \frac{I_{out\_PFC}}{2 \bullet \pi \bullet 2 \bullet f_{line} \bullet \frac{U_{bus\_ripple\_pp}}{2}} = \frac{I_{out\_PFC}}{2 \bullet \pi \bullet f_{line} \bullet U_{bus\_ripple\_pp}} \qquad \text{Equation 38}$$

Please note that ICL5101 has an overvoltage protection whose threshold is 109% of rate voltage. That means the target $U_{bus\_ripple\_pp}$ must be lower than 18% of U_{bus}. Normally a safety distance should be hold between peak ripple voltage and the overvoltage protection limit to avoid miss triggering generated by distortion, protection limit tolerance or parameter deviation based on temperature and aging. E.g. we could choose 2.5% as the limit. Then as in our reference design U_{bus} =450V, $U_{bus\_ripple\_pp}$ =11.25V. According to equation 38 we have:

$$C_{bus} == \frac{252mA}{2 * \pi * 50Hz * 11.25V} = 71.3\mu F$$

C_{bus} =71.3uF. For voltage class, with consideration of overvoltage protection threshold, 500V capacitor is required. But it is hard to find a suitable electrolytic capacitor which is from dimension and capacitance point of view suitable for our reference board in this voltage class. Also with consideration of targeting high efficiency and long life, the ESR of the capacitor should be selected as small as possible and the allowed maximum ripple current should have enough margins. So in the end two long life low ESR 150uF/250V electrolytic capacitors are selected to be connected in series here. In the schematic in Chapter 3.1, they are C5 and C8.

PFC Stage Design Guide

To symmetrize the voltage stress on two in series connected capacitors, an in parallel connected voltage divider is used. To reduce the voltage stress on each resistor, 4 resistors are used. They are R_{67}, R_{68}, R_{61} and R_{63}. This voltage divider should be high ohmic to reduce the power loss. In reference design, all four resistors are set to 1M.

4.2.9 Selection of PFC BUS Voltage Sensing Resistor (PFCVS)

For ICL5101, the typical value of reference voltage for bus voltage detection is $V_{PFCVSref}$ = 2.5V see Datasheet chapter 3.4.3. To achieve a 450V bus voltage, the voltage divider consisting of R_{12}, R_{13}, R_{14} and R_{15} should be configured as following:

$$\frac{R_{PFCLow}}{R_{GES}} = \frac{V_{\mathrm{Re}f}}{V_{BUS}} = \frac{R_{PFCLow}}{R_{PFCHigh} + R_{PFCLow}} = R_{PFCLow} = \frac{V_{\mathrm{Re}f} * R_{PFCHigh}}{V_{BUS} - V_{\mathrm{Re}f}} = \frac{2.5V * 4562k\Omega}{450V - 2.5V} = 25.5k\Omega \quad \text{Equation 39}$$

To reduce the voltage stress on each resistor, the high side resistance of the voltage divider is separated to three resistors R_{12}, R_{13} and R_{14}. The total resistance of the voltage divider should be high ohmic enough to reduce the power loss. But also with consideration of the PFCVS Bias Current $-1\mu A < I_{PFCVSBIAS} < 1\mu A$ illustrated in ICL5101's Datasheet, value of R_{15} should not be too large. Otherwise the influence of the Bias Current would be significant to shift the bus voltage level.

In our reference design, $R_{13} = R_{14}$ =2M, R_{12} =562K and R_{15} =25.5K.

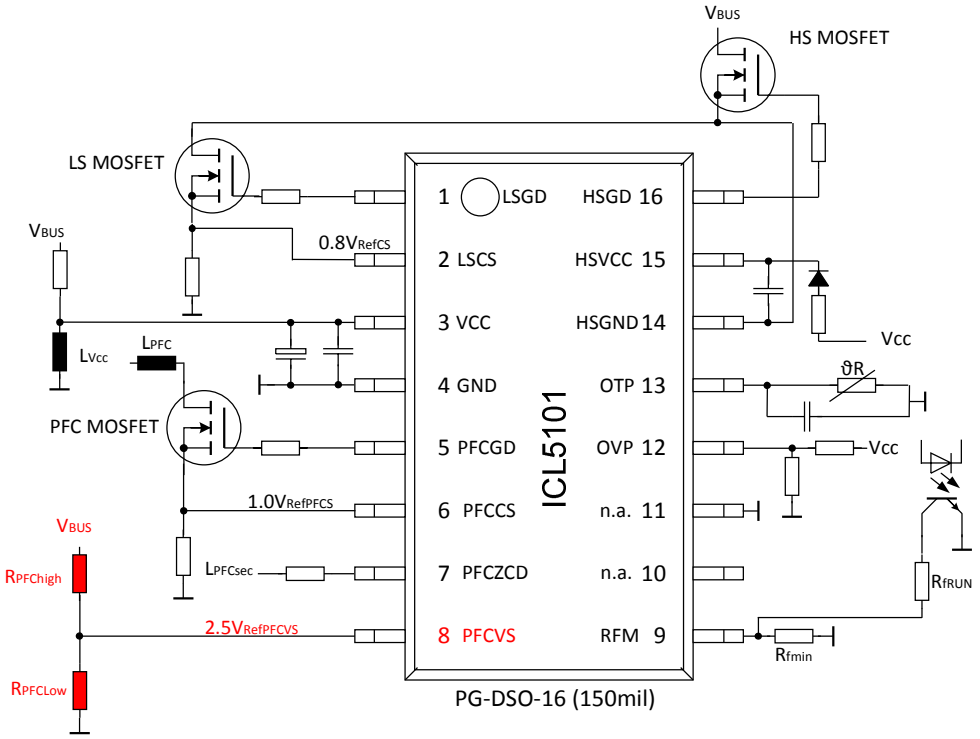

Figure 10 PIN Setup showing the calculated Components in red

5 LLC Stage Design Guide

5.1 LLC Introduction

LLC is a resonant topology. It shifts the operation frequency to achieve a stable output under different input and load conditions. A picture with typical “Gain” vs “Switching Frequency” curves of LLC circuit is shown in Figure 11 Different curves refer to different Quality Factors “Q”, which indicate different loadings. “M(fn, λ ,Q)” is the output voltage to input voltage gain and “fn” is the normalized switching frequency based on the resonant frequency of resonant capacitor and resonant inductor.

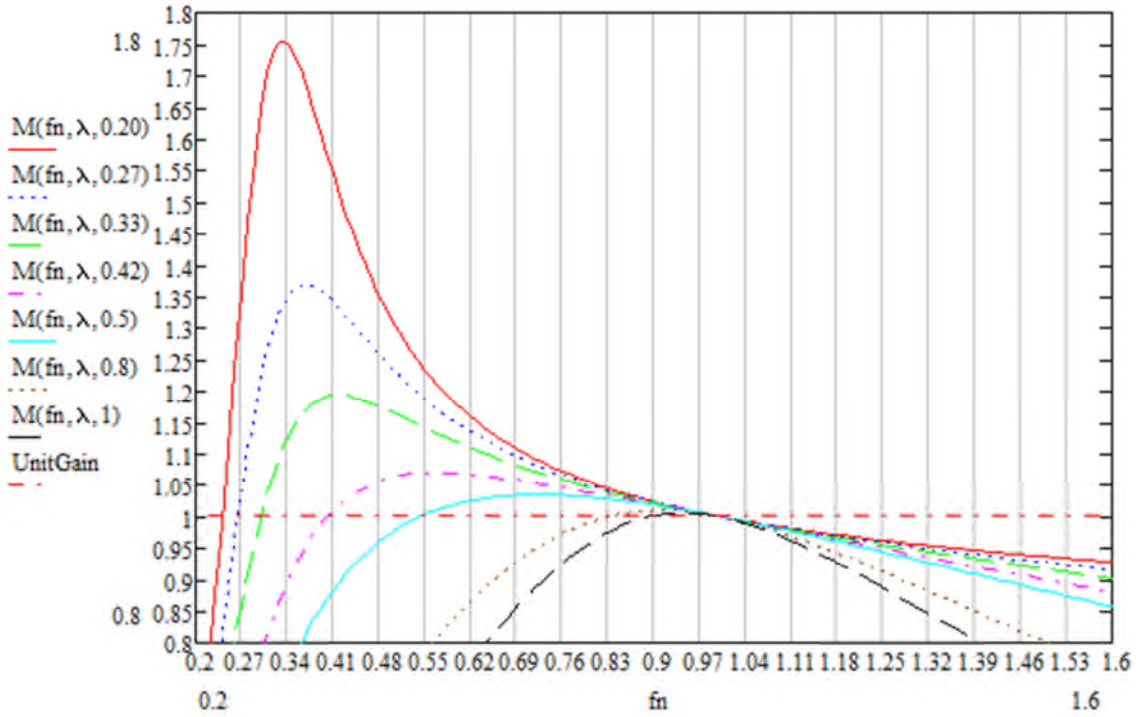

Figure 11 Example Gain Curves of a LLC Circuit

The standard LLC could be in half-bridge or full bridge form. It mainly consists of two (half-bridge) or four (full bridge) power switches, one resonant capacitor, one resonant choke (in many situation it could also be as leakage inductance and integrated in power transformer) and one power transformer. The simplified LLC circuits are shown in Figure 12 and Figure 13.

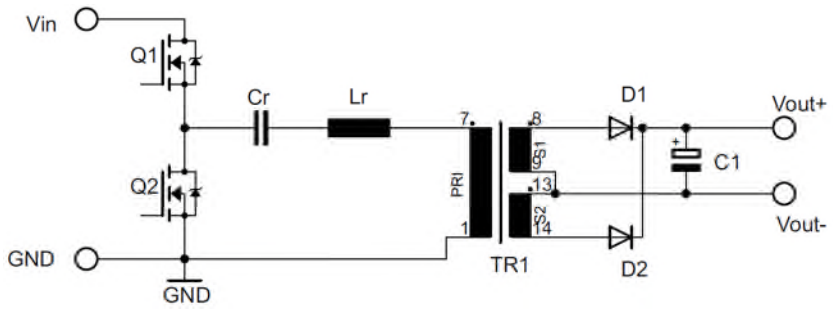

Figure 12 Standard LLC Circuit

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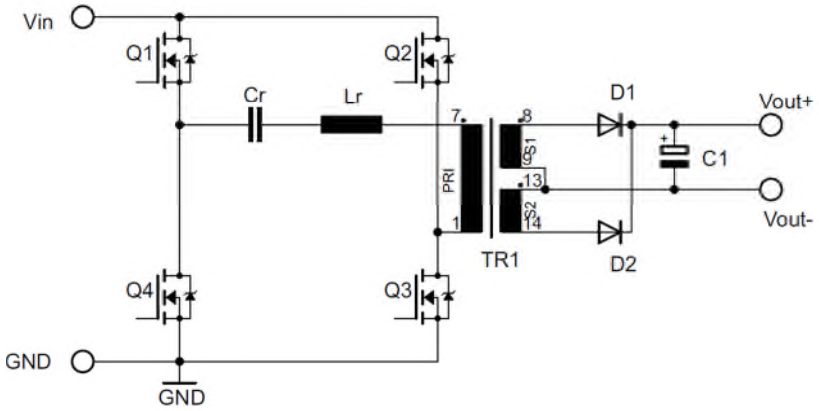

Figure 13 LLC Full Bridge Circuit

Nowadays LLC topology is becoming more and more popular in middle and high power DC/DC converter. Even in converter with power range smaller than 100W, LLC topology could often be seen.

The most important advantage of LLC topology is that it could achieve “ZVS” at wide output power range from full load even down to no load condition, which results high system efficiency.

To design an LLC circuit, the most important thing is to select suitable gain curves so that it could achieve following targets:

1) Small operation frequency variation range around resonant frequency → good for EMI, high efficiency;
2) Small magnetization current → high efficiency;
3) “ZVS” in whole operation range → high efficiency;

5.2 ICL5101 LLC Design Procedure

5.2.1 Selection of LLC Resonant Frequency

When the LLC circuit operates at resonant frequency, it could achieve the highest efficiency and at that point the voltage Gain does not dependent on the load any more. This could be the ideal operation point for LLC circuit. But with consideration of the real operation condition, the coupling between primary and secondary winding of the power transformer is influenced by load condition, the output load could vary under different requirements and the DC-Link voltage also always shows double line frequency ripple. So to achieve a good input and output regulation, an LLC circuit could not operate stably at a fixed resonant frequency. In real application we need to set the LLC circuit to operate in a frequency range around its resonant frequency and this range should be as small as possible. Then how large should the resonant frequency be?

Normally the operation frequency selection is based on the requirement of system efficiency and power density. It also affects EMI result. High switching frequency leads to smaller dimension and allows high power density but it is more difficult to achieve high efficiency and needs a better thermal solution. The maximum switching frequency is normally limited by driver ability. Lower switching frequency is good for EMI and also easier to achieve high efficiency if the dimension is allowed.
The adjustable run frequency of the half-bridge driver of ICL5101 is in the range of 20 kHz to 130 kHz, which could be set by a resistor between “RFM” pin to GND according to following equation:

$$f_{RUN} = \frac{5 \bullet 10^8 \Omega Hz}{R_{RFM}}$$ Equation 40

$$R_{RFM} = \frac{5*10^8 \Omega Hz}{f_{sw\_\min}} = \frac{5*10^8 \Omega Hz}{41.8 kHz} = 11.96 k\Omega$$ calculated via Equation 40

We choose a R_{RFM} = 12.1kΩ Resistor. R_{RFM} is the resistance between “RFM” pin and GND and set the minimum frequency when open loop.

Based on the reference board dimension requirement and also with consideration of EMI effect, we selected our LLC resonant frequency at around 55 kHz. The minimum and maximum operation frequency would then be defined according to the selected LLC Gain curve.

5.2.2 Parameter Selection of LLC Resonant Tank

A simplified LLC resonant circuit with main parameters is shown in Figure 14, which is similar as the circuit in Figure 12 Only the power transformer here is separated to two parts: primary inductor "L_m" and ideal transformer "TR" with turn ratio of "n:1" from primary winding to secondary winding.

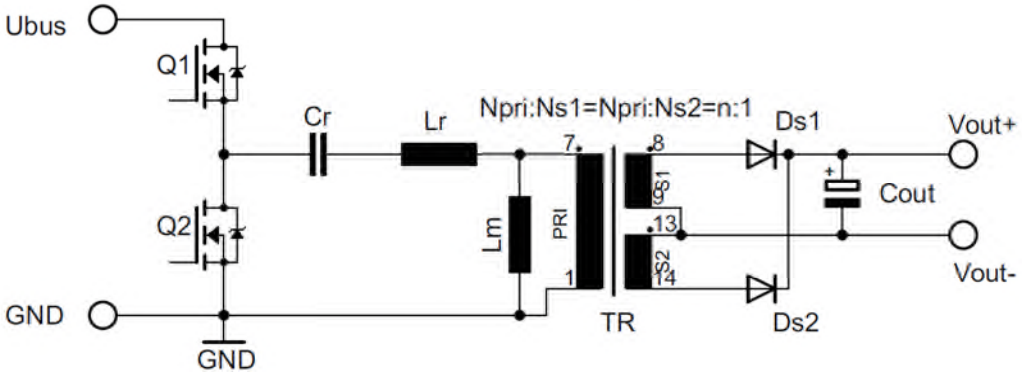

Figure 14 Simplified LLC Resonant Circuit

The steps to select suitable parameters for LLC resonant tank could be abstracted as following:

1) Select turn ratio of power transformer primary winding to secondary winding;
2) Select Quality Factor "Q" for operation point at maximum load on Gain curve plot based on pre-estimated "λ". "λ" is the ratio of resonant inductor "L_r" and transformer primary inductor (also called "magnetizing inductor") "L_m". Different value of "λ" might be tried until suitable Gain curves are selected in the end, which could match the frequency range and efficiency requirement;
3) Calculate and select "C_r", "L_r" and "L_m" according to selected resonant frequency "f_r", Quality Factor "Q" and inductor ratio "λ";
4) Calculate the minimum operation frequency and maximum operation frequency.
5) Calculate the voltage stress on "C_r", the peak current flowing through "L_r" and the peak magnetizing current of the power transformer for resonant capacitor, resonant inductor and power transformer selection and design.

Here let's take the LLC design procedure of 110W/54V reference design as an example.

Step 1):

The turn ratio of the transformer is at first selected according to following equation:

$$n = \frac{U_{bus} \bullet M_{nom\_Sel}}{2 \bullet (U_{out} + U_{F\_Dout})} = \frac{450V \bullet 1.05}{2 \bullet (54V + 0.8V)} = 4.31$$ Equation 41

"M_{nom}" is the wished Gain of LLC circuit at nominal output power at rated input and output voltage. As we know from LLC topology when the operation frequency is at left side of the resonant frequency, the output diodes work in DCM mode it would minimize the diode power loss and increase the efficiency. To ensure the high efficiency, normally "M_{nom}" is selected slightly higher than 1 but not too far away from 1. In the reference design, "M_{nom_Sel}" is selected with the value of 1.05.

"U_{F_Dout}" is the forward voltage of output diode. To increase the efficiency, "U_{F_Dout}" should be as small as possible. For theoretical calculation before we select a concrete diode, the value of "U_{F_Dout}" could be assume as 0.8V, which could anyway not influence the calculation result so much.

The calculation result of equation 41 is $n = 4.311$. Because the transformer coupling is not 100%, when taking the leakage inductance into account, assuming 1% of primary inductance as leakage inductance value, then the effective transformer turns ratio could be calculated as following:

$$n_e = 0.99^{0.5} \bullet n = 4.29 \qquad \text{Equation 42}$$

Step 2):

With effective turns ratio $n_e = 4.29$, we could then calculate back for "M_{nom}". The recalculated value:

$$M_{nom} = \frac{n_e * 2 * (U_{out} + U_F)}{U_{bus}} = \frac{4.29 * 2 * (54V + 0.8V)}{450V} = 1.045 \qquad \text{Equation 42a}$$

With consideration of bus voltage ripple and regulation accuracy, we could assume $U_{bus\_max} = 460V$ and $U_{bus\_min} = 443V$. Then we could calculate the maximum Gain and minimum Gain at nominal output voltage:

$$M_{nom\_max} = \frac{U_{bus}}{U_{bus\_min}} \bullet M_{nom} = 1.061 \qquad \text{Equation 43}$$

$$M_{nom\_min} = \frac{U_{bus}}{U_{bus\_max}} \bullet M_{nom} = 1.022 \qquad \text{Equation 44}$$

Because the output voltage has also regulation accuracy and ripple of approximately ± 2% of V_{OUTnom} = 54V, let's set the target peak output voltage $U_{out\_max} = 54.5V$ and the target minimum output voltage $U_{out\_min} = 53.5V$. Then we would have the absolute maximum Gain:

$$M_{max} = \frac{2 \bullet n_e \bullet (U_{out\_max} + U_F)}{U_{bus\_min}} = 1.07 \qquad \text{Equation 45}$$

and the absolute minimum Gain

$$M_{min} = \frac{2 \bullet n_e \bullet (U_{out\_min} + U_F)}{U_{bus\_max}} = 1.013 \qquad \text{Equation 46}$$

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The inductor ratio is set as $\lambda = 0.09$ (see Equation 47a) after sometimes trying and comparison of different values on the Gain curve plot. In the end according to the LLC transfer function:

$$M\left(f_n, \lambda, Q\right) = \frac{1}{\sqrt{\left(1 + \lambda - \frac{\lambda}{f_n^{\,2}}\right)^2 + Q^2 \bullet \left(f_n - \frac{1}{f_n}\right)^2}}$$

Equation 47

We could have the selected Gain curves plot as in Figure 15:

$$\lambda = \frac{L_r}{L_m}$$

Equation 47a

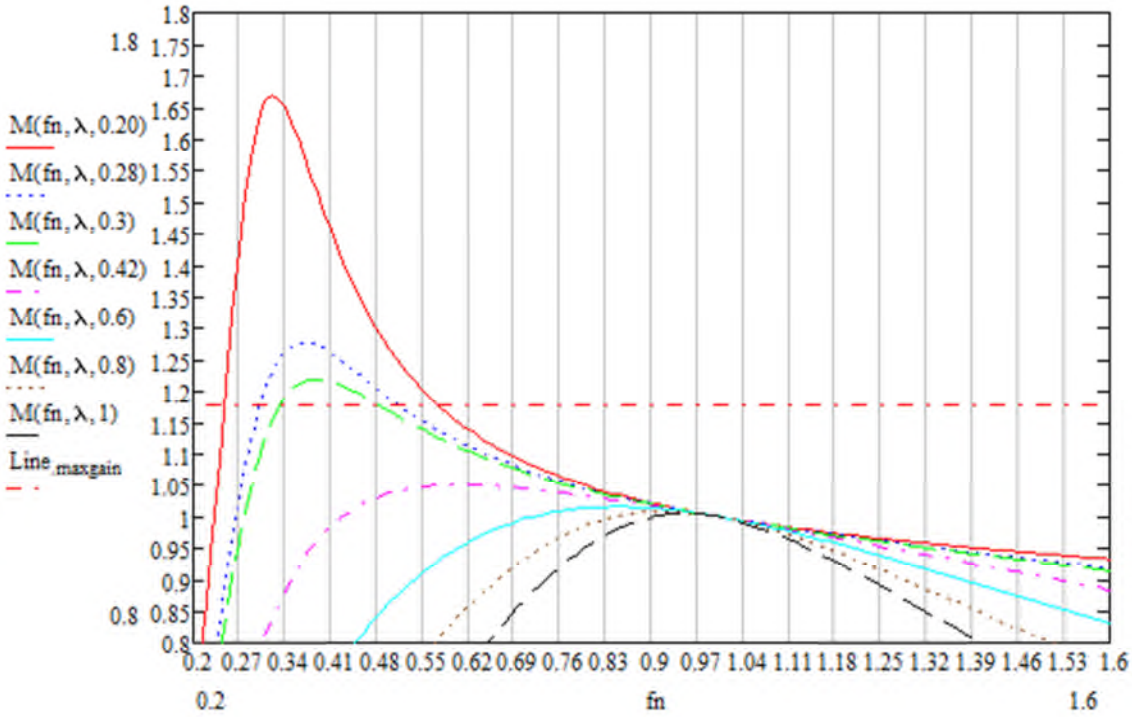

Figure 15 LLC Gain Curve Plot 110W / 54V Reference Board

To ensure “ZVS” at whole output power range with maximum allowed input and output voltage tolerance, when we choose the Gain curve for maximum allowed output power for worst case (minimum input voltage and maximum output voltage) we increase 10% to the above calculated maximum Gain “M_{max}” and draw that line on the Gain curve plot (the red dash-dot line in Figure 15). The Gain curve with the peak a little higher than the 110% “M_{max}” line would then be chosen as the Gain curve for maximum power at worst case. In Figure 15 the green dash line with Q=0.3 is selected.

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Step 3):

$$Q = \frac{Z_r}{R_e} \rightarrow Z_r = Q * R_e$$ Equation 48

$$Z_r = \sqrt{\frac{L_r}{C_r}}$$ Equation 49

$$L_r = C_r * Q^2 * R_e^2$$ Equation 50

"Z_r" is the resonant impedance and "R_e" is the equivalent load resistance at primary side. To calculate "L_r" and "C_r", we need at first to calculate "R_e".

Let's assume resistant output load and no phase shift between the voltage and current at transformer secondary side. The fundamental element of the AC current at secondary winding of the power transformer is:

$$I_{ac}^{F} = \frac{\pi}{2} \bullet I_{out} \bullet \sin(wt)$$ Equation 51

"I_{out}" is LLC output DC current. The fundamental element of square form voltage at secondary winding of the power transformer is:

$$U_{sac}^{F} = \frac{4}{\pi} \bullet U_{out} \bullet \sin(wt)$$ Equation 52

So the nominal equivalent LLC resistance load at primary side could be calculated as:

$$R_{e\_nom} = \frac{U_{sac}^{F}}{I_{ac}^{F}} \bullet n_e^2 = \frac{(U_{out\_nom} + U_F)}{I_{out\_nom}} \bullet \frac{8}{\pi^2} \bullet n_e^2$$ Equation 53

"I_{out_nom}" is the nominal output current.

$R_{e\_nom} = \frac{(54V + 0.8V)}{2037mA} * \frac{8}{\pi^2} * 4.29^2 = 401.3\Omega$ calculated from Equation 53

The resistance of maximum load could be calculated as:

$$R_{e\_max} = \frac{(U_{out\_min} + U_F)}{I_{out\_max}} \bullet \frac{8}{\pi^2} \bullet n_e^2$$ Equation 54

"I_{out_max}" is the required maximum DC output current. With predefined $U_{out\_min} = 53.5V$ (see Equation 46) and $I_{out\_max} = 2.57A$, (Input Parameter) "R_{e_max}" gets the value of about 315Ω.

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$$R_{e\_nom} = \frac{(53.5V + 0.8V)}{2570mA} * \frac{8}{\pi^2} * 4.29^2 = 315.2\Omega$$ calculated from Equation 54

According to equation 48, equation 49 and following resonant frequency equation we can calculate the resonance capacity Cr:

$$f_r = \frac{1}{2 \bullet \pi} \frac{1}{\sqrt{L_r \bullet C_r}} \rightarrow L_r = \frac{1}{f_r^2 * 4 * \pi^2 * C_r}$$ Equation 55

Using Lr from Equation 50 in Equation 55 we can calculate Cr via Equation 55a:

$$C_r^2 = \frac{1}{f_r^2 * 4 * \pi^2 * Q^2 * R_{e\_\max}^2}$$

$$C_r = \frac{1}{f_r * 2 * \pi * Q * R_{e\_\max}} = \frac{1}{55kHz * 2 * \pi * 0.3 * 315} = 30.62nF$$ Equation 55a

Let's take a standard value of 33nF for C_r, and use Equation 55 and calculate the resonance inductivity Lr via Equation 55b:

$$L_r = \frac{1}{f_r^2 * 4 * \pi^2 * C_r} = \frac{1}{55kHz^2 * 4 * \pi^2 * 33nF} = 253.75\mu H$$ Equation 55b

With $\lambda = 0.09$, "L_m" is resulted according to Equation 47a at

$$\lambda = \frac{L_{r\_Pre\_Cal}}{L_{m\_Pre\_Cal}}$$ Equation 55c

$$L_{m\_Pre\_Cal} = \frac{L_{r\_Pre\_Cal}}{\lambda} = \frac{253.75\mu H}{0.09} = 2819\mu H$$ Calculated via Equation 55c

With consideration of 1% leakage inductance (transformer coupling factor) of the power transformer, in reality "L_m" should be

$$\frac{2819\mu H}{0.99} = 2848\mu H$$ Equation 55d

Then the actual "L_r" should be:

$$L_r = L_{r\_Pre\_Cal} - 1\% * L_m = 253.747 - 2848\mu H * 0.01 = 225.267\mu H$$ Equation 56

But in calculation we still need to use the effective value of "L_r" which indicates the total effective resonant inductance.

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Step 4):

Now we could use the selected effective "C_r" and "L_r" to draw the Gain curves and find the operation points for maximum power, nominal power and minimum power in Gain curve plot.

To draw the Gain curves, the "Q" value for different load should be calculated at first. The effective resonant impedance according to Equation 49 $Z_r = \sqrt{\frac{253.747\mu H}{33nF}} = 87.689\Omega$. The "Q" value for nominal load, maximum load and minimum load could be calculated as following:

Nominal load: $Q_{nom} = \frac{Z_r}{R_{e\_nom}}$; Equation 56a

Maximum load: $Q_{\max} = \frac{Z_r}{R_{e\_\max}}$; Equation 56b

Minimum load: $Q_{\min} = \frac{Z_r}{R_{e\_\min}}$. Equation 56c

With $U_{out\_nom} = 450V$ and $I_{out\_nom} = 2.037A$, R_{e_nom} is calculated according to equation 52 and results at 401.234 Ω. $R_{e\_\max} = 315\Omega$. "$R_{e\_\min}$" is calculated according to following equation:

$$R_{e\_\min} = \frac{\left(U_{out\_\max} + U_F\right)}{I_{out\_\min}} \bullet \frac{8}{\pi^2} \bullet n_e^{\,2} \qquad \text{Equation 57}$$

The predefined maximum output voltage is $U_{out\_\max} = 54.5V$. The minimum load condition for the reference board is open output. For calculation we could use a very small output current as replacement. Here we use the output current value when the output power is about 1 μW.

$$R_{e\_\min} = \frac{(54.5V + 0.8V) * 8 * n_e^{\,2}}{18\mu A * \pi^2} = 4.4 * 10^{10}\Omega$$ Calculated via Equation 57

As a result we could have $R_{e\_\min} = 4.4 \bullet 10^{10}\Omega$.

In the end we have $Q_{nom} = 0.219$, $Q_{\max} = 0.278$ and $Q_{\min} = 1.9 \bullet 10^{-9}$. Draw Gain curves for these "Q" values in the Gain curve plot in Figure 16.

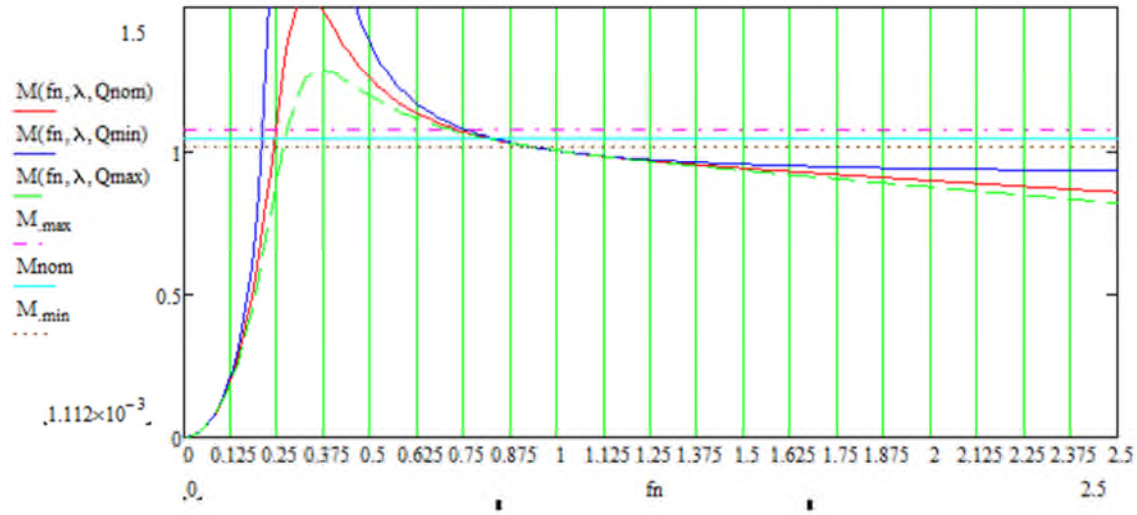

Figure 16 LLC Gain Curve Plot 110W / 54V Reference Board for nom, max and min Power

With drawing the maximum Gain line, nominal operation Gain line and the minimum Gain line also on the plot, the corresponding operation point of "maximum load @U_{bus_min} & U_{out_max}", "nominal load @ U_{bus_nom} & U_{out_nom}" and "minimum load @ U_{bus_max} & U_{out_min}" would be found at the line crossing point of "$M(f_n, \lambda, Q_{max})$ and M_{max}", "$M(f_n, \lambda, Q_{nom})$ and M_{nom}" and "$M(f_n, \lambda, Q_{min})$ and M_{min}" respectively.

According to the plot, the minimum switching frequency happens at operation point "maximum load @ U_{bus_min} & U_{out_max}" with $f_{n\_min} = 0.76$. The absolute switching frequency at this point is then

$$f_{sw\_min} = f_{n\_min} \bullet f_r = 41.8kHz \qquad \text{Equation 57a}$$

The maximum switching frequency happens at operation point "minimum load @ U_{bus_max} & U_{out_min}" with $f_{n\_max} = 0.95$. The absolute switching frequency at this point is then

$$f_{sw\_max} = f_{n\_max} \bullet f_r = 52.25kHz \qquad \text{Equation 57b}$$

The nominal switching frequency at operation point "nominal load @ U_{bus_nom} & U_{out_nom}" with

$f_{n\_nom} = 0.83$ is $f_{sw\_nom} = f_{n\_nom} \bullet f_r = 45.65kHz$ Equation 57c

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Step 5):

To select the voltage class for resonant capacitor "C_r" and define the saturation current for resonant inductor "L_r" and power transformer, we need to know the maximum peak current flowing through the resonant inductor and also the maximum magnetizing current of the power transformer.

As the operation frequency of the maximum power is at the left side of the resonant frequency, system works at DCM mode. The voltage and current waveforms of the LLC circuit are shown in Figure 17.

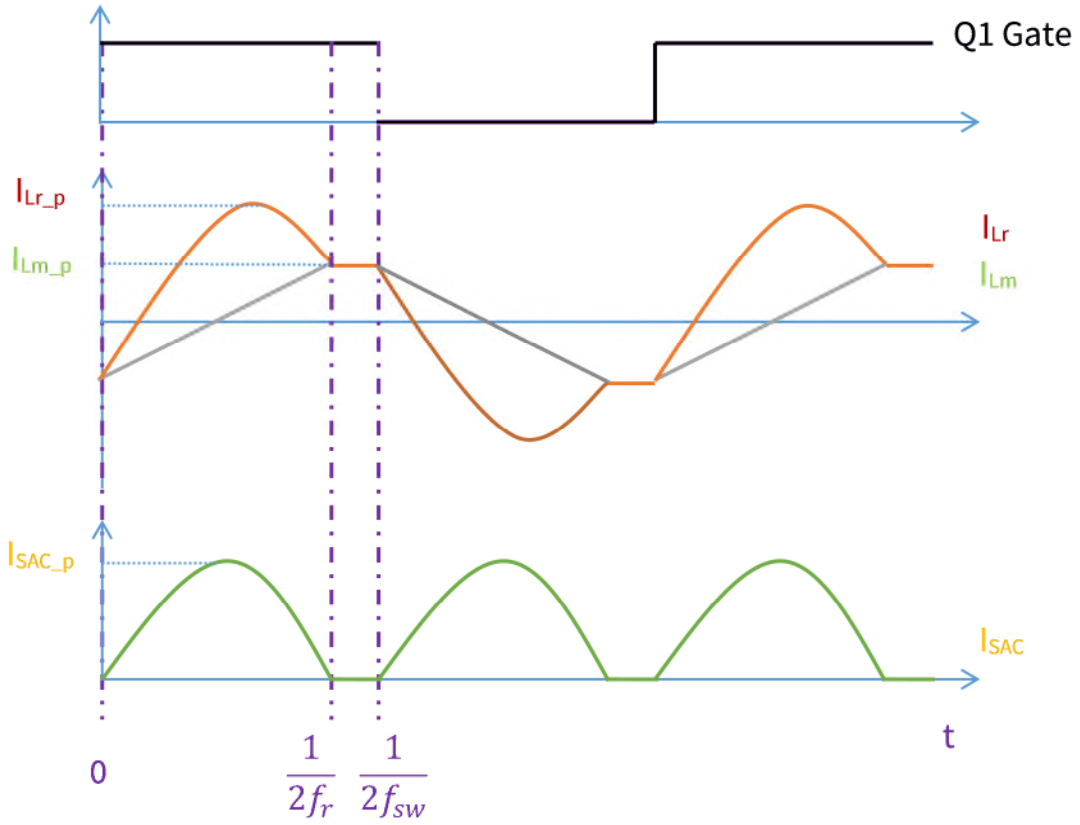

Figure 17 LLC Circuit Voltage and Current waveform in DCM Mode

In approximate calculation dead time could be neglected. The black square wave in the above picture is the Gate signal of the half-bridge high side MOSFET. "I_{Lr}" (dark red), "I_{Lm}" (green) and "I_{SAC}" (orange) is the resonant inductor current, power transformer magnetizing current and power transformer secondary side AC current respectively.

According to above picture, we could have following equation for the magnetizing current "I_{Lm}":

$$I_{Lm}(t) = \begin{cases} (4 \bullet I_{Lm\_p} \bullet f_r \bullet t) - I_{Lm\_p}, if\ 0 < t < \dfrac{1}{2f_r} \\ I_{Lm\_p}, if\ \dfrac{1}{2f_r} \le t \le \dfrac{1}{2f_{sw}} \end{cases} \quad \text{Equation 58}$$

"I_{Lm_p}" is the peak value of the magnetizing current. According to voltage-second rules of inductor, it could be calculated as following:

$$I_{Lm\_p} = \frac{n_e \bullet (U_{out} + U_F)}{4 \bullet L_m \bullet f_{sw}}$$ Equation 59

If we take "U_{out_max}" and "f_{sw_min}" into equation 58:

$$I_{Lm\_p\_max} = \frac{n_e * (U_{out\_max} + U_F)}{4 * L_m * f_{sw\_min}} = \frac{4.29 * (54.5V + 0.8V)}{4 * 2848\mu H * 41.8kHz} = 498.2mA$$ Equation 59a

we could get the maximum peak value of magnetizing current $I_{Lm\_p\_max} = 0.498A$. The absolute limit for the saturation current of the power transformer is then that it should be larger than 0.498A.

For the current in transformer secondary winding, we could have an approximate equation as following:

$$I_{SAC}(t) = \begin{cases} I_{SAC\_p} \bullet \sin(2\pi f_r t), if 0 < t < \frac{1}{2f_r} \\ 0, if \frac{1}{2f_r} \le t \le \frac{1}{2f_{sw}} \end{cases}$$ Equation 60

"I_{SAC_p}" is the peak value of the current in transformer secondary winding. The output current "I_{out}" is the average current of "$I_{SAC}(t)$" in the whole "$\frac{1}{2f_{sw}}$" period. According to energy equilibrium in time range "$\frac{1}{2f_r}$" and in time range "$\frac{1}{2f_{sw}}$", we could have the equation as following:

$$I_{out} \bullet \frac{1}{2f_{sw}} = I_{SAC\_p} \bullet \frac{2}{\pi} \bullet \frac{1}{2f_r}$$ Equation 61

$$I_{SAC\_p\_nom} = \frac{\pi * I_{out} * f_r}{2 * f_{sw}}$$ Equation 62

Take "I_{out_max}" and "f_{sw_min}" into the above equation 62:

$$I_{SAC\_p\_max} = \frac{\pi * I_{out\_max} * f_r}{2 * f_{sw\_min}} = \frac{\pi * 2.57A * 55kHz}{2 * 41.8kHz} = 5.31A$$ Equation 62a

we could have the maximum peak current in secondary winding $I_{sac\_p\_max} = 5.312A$.

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Then we could calculate the peak current in resonant inductor. The general current function in resonant inductor is:

$$I_{Lr}(t) = \frac{I_{SAC}(t)}{n_e} + I_{Lm}(t) \qquad \text{Equation 63}$$

The time point "$t_{\max}$" corresponding to the peak value of "$I_{Lr}(t)$" could be calculated according to following condition:

$$\frac{dI_{Lr}(t)}{dt} = 0 \qquad \text{Equation 64}$$

"$t_{\max}$" is calculated to be:

$$t_{\max} = \frac{\arccos\left(\frac{-2 \bullet I_{Lm\_p} \bullet n_e}{\pi \bullet I_{sac\_p}}\right)}{2 \bullet \pi \bullet f_r} \qquad \text{Equation 65}$$

Take "$I_{Lm\_p\_\max}$" and "$I_{sac\_p\_\max}$" into equation 65:

$$t_{\max} = \frac{\arccos\left(\frac{-2 * I_{Lm\_p\_\max} * n_e}{\pi * I_{sac\_p\_\max}}\right)}{2 * \pi * f_r} = \frac{\arccos\left(\frac{-2 * 0.4985A * 4.29}{\pi * 5.31A}\right)}{2 * \pi * 55kHz} = 5.3\mu s \qquad \text{Equation 65a}$$

According to equation 62 we will have at the maximum a peak current $I_{Lr}(t_{max})$ flowing through resonant inductor as shown in Equation 65b:

$$I_{Lr}(t_{\max}) = \frac{I_{SAC}(t_{\max})}{n_e} + I_{Lm}(t_{\max}) \qquad \text{Equation 65b}$$

The maximum secondary peak current at t_{max} is sinusoidal see Figure 17Figure 14:

$$I_{SAC}(t_{\max}) = I_{SAC\_p\_\max} * \sin(2 * \pi * f_r * t_{\max}) \qquad \text{Equation 65c}$$

$$I_{SAC}(t_{\max}) = 5.31A * \sin(2 * \pi * 55kHz * 5.3\mu s) = 5.135A$$

The maximum primary inductance peak current at t_{max} is linear see Figure 17:

$$I_{Lm}(t_{\max}) = 4 * I_{Lm\_p\_\max} * f_r * t_{\max} - I_{Lm\_p\_\max} \qquad \text{Equation 65d}$$

$$I_{Lm}(t_{\max}) = 4 * 0.4985A * 55kHz * 5.3\mu s - 0.4985 = 0.082A$$

Maximum peak current through resonant inductor $I_{LR(tmax)}$ at t_{max} according to Equation 65b:

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$$I_{Lr}(t_{\max}) = I_{Lr\_p\_\max} = \frac{5.135A}{4.29} + 0.082A = 1.279A$$ Equation 65e

$I_{Lr\_p\_\max} = 1.279A$. The absolute limit for the saturation current of the resonant inductor is then that it should be larger than 1.279A.

The maximum peak voltage on resonant capacitor could be calculated as following:

$$U_{Cr\_p\_\max} = \frac{I_{Lr\_p\_\max}}{2 \bullet \pi \bullet f_{sw\_\min} \bullet C_r} = \frac{1.279A}{2 * \pi * 41.8kHz * 33nFC_r} = 147.588V$$ Equation 66

In reality, 33nF/630V film capacitor is selected as resonant capacitor.

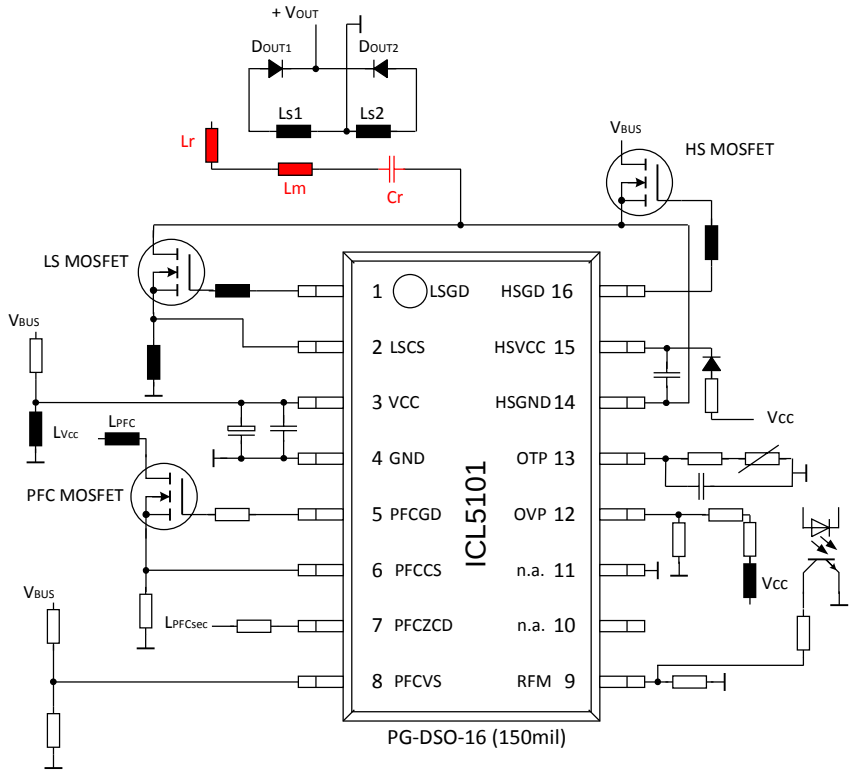

Figure 18 PIN Setup showing the calculated Components in red

5.2.3 ICL5101 Half-Bridge Run Frequency Range setting (RFM)

As described in chapter 5.2.1, the half-bridge run frequency could be set via a resistor between GND and RFM pin 9 according to equation 40.

Based on the calculation in chapter 5.2.2, the designed LLC minimum operation frequency is 41.8 kHz and the maximum operation frequency is 52.25 kHz. We could set the minimum switching frequency via "R_{19}" in the schematic in chapter 3.1. Take 41.8 kHz into equation 40 as "f_{run}" we could $R_{RFM} = 11.96k\Omega$. To have some tolerance margin, "R_{19}" is set at $12.1k\Omega$. With $R_{RFM} = 12.1k\Omega$ calculation back for "f_{run}", it is $41.3kHz$, which is then the minimum allowed switching frequency of the half-bridge.

During normal operation the LLC regulation loop senses the output voltage and feeds back through opto-coupler "OT1" and resistor "R_{23}" to RFM pin 9 in order to adjust the operation frequency. "R_{23}", the saturation voltage "U_{ces}" of opto-coupler and "R_{19}" together set the maximum allowed half-bridge operation frequency in run-mode.

We use VOL617A-3 as opto-coupler for the regulation loop. Its output saturation voltage is V_{CE} = 0.25V. According to the theoretical calculation in chapter 5.2.2, the maximum switching frequency in normal operation in stable state is $f_{sw\_max} = 52.25kHz$. In real operation there could be tolerance and deviation for the switching frequency. Also in unstable state during regulation, the frequency could be higher. So we need leave enough frequency margins for the regulation loop in normal operation in order to prevent a malfunction of the design. But it is also necessary to limit the maximum switching frequency at a certain level, so that during load jump the highest switching frequency could be limited to avoid over regulation and hard switching. In our reference design, we selected a absolut maximum operating frequency of 90kHz for "f_{run_max}", $R_{23} = 9.1k\Omega$ calculated as below.

Then the maximum allowed switching frequency in run-mode has following equation 67 according to Equation 40:

$$f_{RUN\_max} = \frac{5*10^8 \Omega Hz}{R_{RFM\_e}} \qquad \text{Equation 67}$$

For calculating the total effective resistance $R_{RFM\_e} = R_{19} // R_{23}$:

$$R_{RFM\_e} = \frac{5*10^8 \Omega Hz}{f_{RUN\_max}} = \frac{5*10^8 \Omega Hz}{90kHz} = 5.56k\Omega$$

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In run-mode the voltage on RFM pin is V_{RFM} = 2.5V. The total current flowing out of RFM pin could be calculated as:

$$R_{RFM\_e} = \frac{V_{RFM}}{I_{RFM}}$$ Equation 68

$$I_{RFM} = \frac{2.5V}{5.56k\Omega} = 450\mu A$$

Use the following equation 69 in order to calculate R_{23}:

$$I_{RFM} = \frac{U_{REF}}{R_{19}} + \frac{U_{REF} - U_{ces}}{R_{23}}$$ Equation 69

$$R_{23} = \frac{U_{REF} - U_{ces}}{I_{RFM} - \frac{U_{REF}}{R_{19}}} = \frac{2.5V - 0.25V}{450\mu A - \frac{2.5V}{12.1k\Omega}} = 9.24k\Omega$$

We choose the standard value of R_{23} = 9.1kΩ.

The current through the opto-coupler can be calculated as shown below:

$$I_{Opto} = I_{RFM} - I_{19}$$ Equation 69a

$$I_{Opto} = I_{RFM} - \frac{U_{REF}}{R_{19}} = 450\mu - \frac{2.5V}{12.1k\Omega} = 243.3\mu A$$

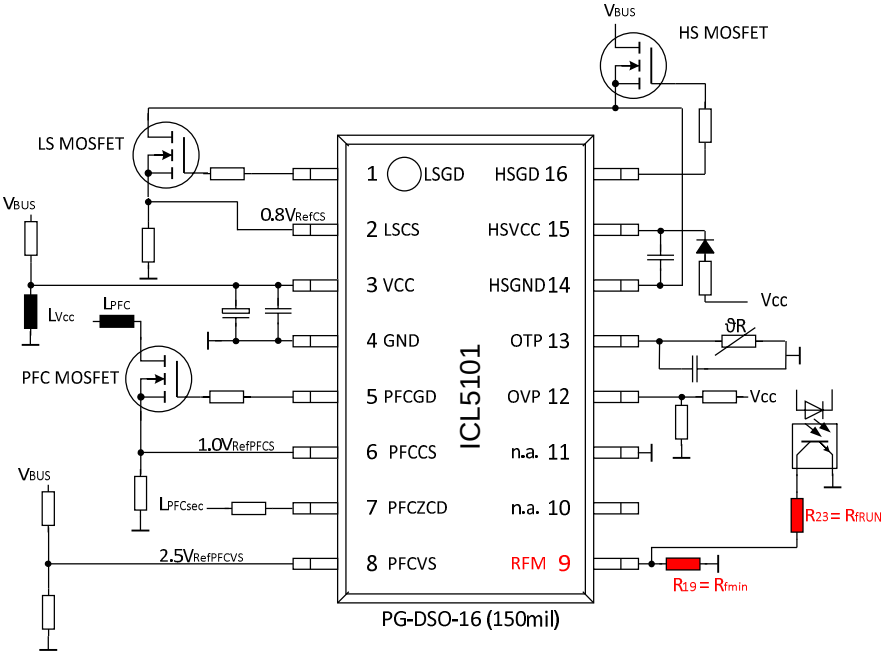

Figure 19 PIN Setup showing the Components in red

5.2.4 Selection of Half-Bridge MOSFET (LSGD / HSGD)

According to the bus voltage level, a 600V MOSFET could be used for this half-bridge LLC circuit.

LLC circuit operates in “ZVS” in normal operation condition. Body diode is conducted before MOSFET turning on. So to select suitable MOSFET for LLC circuit, two most important factors need to be considered: 1) MOSFET power loss; 2) Body diode ability.

1) MOSFET power loss

When we select the MOSFET for LLC circuit, there is no need to consider the MOSFET turning on loss and the “C_{oss}” loss. The conduction loss of the MOSFET at maximum output power could be calculated as following:

$$P_{loss\_LLCMOS\_con} = \frac{1}{2} * I_{Lr\_rms\_\max}{}^{2} * R_{DSon} \qquad \text{Equation 70}$$

“$I_{Lr\_rms\_\max}$” is the effective current flowing through the resonant inductor at maximum output power, which could be calculated as following:

$$I_{Lr\_rms\_\max} = \sqrt{\frac{\int_0^{\frac{1}{2f_{sw\_\min}}} I_{Lr}{}^{2}(t)dt}{\frac{1}{2f_{sw\_\min}}}} \qquad \text{Equation 71}$$

Take “$I_{Lm\_p\_\max}$” and “$I_{sac\_p\_\max}$” into above equation, we could have the exact integrated result $I_{Lr\_rms\_\max} = 0.84A$. For a safety margin we use Equation 71a for the rms current to calculate the conductive power losses using Equation 70:

$$I_{Lr\_rms\_\max} = \frac{\sqrt{2}}{2} * I_{Lr\_\max} = 0.71*1.279A = 0.9A \qquad \text{Equation 71a}$$

R_{DSON} = 1.05Ω should be the value based on 150°C T_j in MOSFET datasheet.

$P_{loss\_LLCMOS\_con} = \frac{1}{2} * 0.90A^2 * 1.05\Omega = 430mW$ Calculated via Equation 70

The MOSFET switching loss at maximum output power could be estimated as following

$$P_{loss\_LLCMOS\_sw} = \frac{1}{2} * I_{Lm\_p\_\max} * t_{troff} * U_{bus\_nom} * f_{sw\_\min} \qquad \text{Equation 72}$$

“I_{MOS_peak}” is the peak current at the moment of MOSFET turning off. According to Figure 17 $I_{MOS\_peak\_\max} = I_{Lm\_p\_\max} * t_{troff}$ is the turning off duration which could be estimated according to the same theory descript in chapter 4.2.4.

For calculating t_{troff} see equation 27 / 28 and 29 or see EXCEL sheet: t_{troff} = 110.4ns

$$P_{loss\_LLCMOS\_sw} = \frac{1}{2} * 0.4985A * 110.4ns * 450V * 41.8kHz = 517.8mW$$ calculated via Equation 72

Gate driving loss could be illustrated as following:

$$P_{loss\_LLCMOS\_drive} = Q_g * U_g * f_{sw\_\min}$$ Equation 73

Note: "Q_g" is Gate charge total.

"U_g" is Gate driver voltage.

$P_{loss\_LLCMOS\_drive} = 28nC * 12V * 41.8kHz = 14mW$ Calculated via Equation 73

The absolute limit for LLC MOSFET selection is also the junction temperature, which should be in the limit of $T_{j\max}$ at the situation of the case temperature stabilized at customer required case temperature T_c. Equation 74 could be applied:

$$T_{j\max} \le T_c + R_{thjc} * \left(P_{loss\_LLCMOS\_con} + P_{loss\_LLCMOS\_SW} + P_{loss\_LLCMOS\_drive}\right) + Z_{thjc} * (P_{loss\_LCCSW\_Tr\_\max})$$ Equation 74

Note: "R_{thjc}" is the junction to case thermal resistance of MOSFET, defines the heating of the MOSFET surface.

"Z_{thjc}"is the transient junction case thermal impedance of MOSFET, which is related with pulse width and duty cycle, which could be checked in the "Max. transient thermal impedance" diagram in MOSFET's datasheet. The calculation of the duty cycle D is giving the parameter for the transient thermal impedance diagram of the MOSFET:

$$D = t_{troff} * f_{sw\_\min}$$ Equation 74a

$$D = 110.4ns * 41.8kHz = 0.0046$$

Using tp2 = 11.1µs @ max frequency of 90kHz and D = 0.0046 < 0.01 in transient thermal impedance diagram of MOSFET (see also below) leads to $Z_{thjc(tp2)}$ = 0.055k/W:

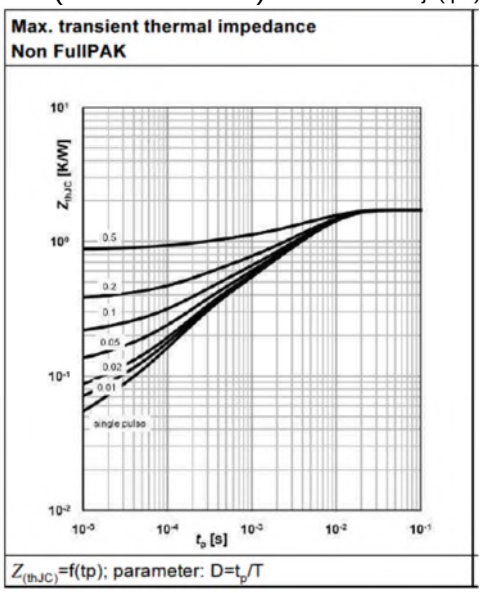

Figure 20 Transient Thermal Impedance Diagram of MOSFET

Equation 74b can be used in order to calculate the $Z_{th(tp2)}$:

$$\frac{Z_{thjc(tp1)}}{Z_{thjc(tp2)}} = \sqrt{\frac{tp1}{tp2}} \qquad \text{Equation 74b}$$

$$Z_{thjc(tp1)} = Z_{thjc(tp2)} * \sqrt{\frac{tp1}{tp2}} = 0.055\frac{K}{W} * \sqrt{\frac{110.4ns}{11.1\mu s}} = 5.5\frac{mK}{W}$$

"$P_{loss\_LLCSW\_Tr\_max}$" is the maximum transient switching off loss at maximum output power:

$$P_{loss\_LLCSW\_Tr\_max} = \frac{1}{2} * I_{Lm\_p\_max} * U_{bus\_nom} \qquad \text{Equation 75}$$

$$P_{loss\_LLCSW\_Tr\_max} = \frac{1}{2} * 0.4985A * 450V = 112.169W$$

$$T_{j\max} \le 105°C + 1.7\frac{K}{W} * (430mW + 517.8mW + 14mW) + 5.5\frac{mK}{W} * 112.169W = 107.2°C$$ from Equation 74

2) Body diode ability

For LLC circuit, as body diode conducts for "ZVS" turning on, the body diode needs then be reverse recovered at first before it could block the reverse direction current. A fast recovery body diode would be preferred for high frequency switching.

For half-bridge application, in abnormal condition, body diode hard commutation could happen. A MOSFET with robust body diode with high dv/dt ability is preferred.

In reference design, Infineon IPD60R450E6 is selected for high and low side switch.

5.2.5 Selection of Heatsink for the Half-Bridge MOSFET (LSGD / HSGD)

For the calculation of the heatsink respective copper area on PCB, we use only $P_{loss\_LLCMOS\_con}$ and $P_{loss\_LLCMOS\_sw}$ the other losses are negligible.

$$R_{thja} = \frac{\Delta T}{P_{loss\_total}} = \frac{T_{J\max} - T_A}{P_{loss\_LLCMOS\_con} + P_{loss\_LLCMOS\_sw}}$$ Equation 75a

- ΔT is only the expected temperature rise of the system without ambient temperature
- $P_{loss\_LLCMOS\_total} = P_{loss\_LLCMOS\_con} + P_{loss\_LLCMOS\_SW}$

$$R_{thja} = \frac{107.1°C - 45°C}{430mW + 517.8mW} = 64.7\frac{K}{W}$$ calculated via Equation 75a

Note:
A copper area on PCB has an estimated Rthja of approximately:

- 3cm² = $64\frac{K}{W}$
- 6cm² = $56\frac{K}{W}$

For the heat dissipator on board we can chose a 3cm² area for the PCB assembled MOS on board.

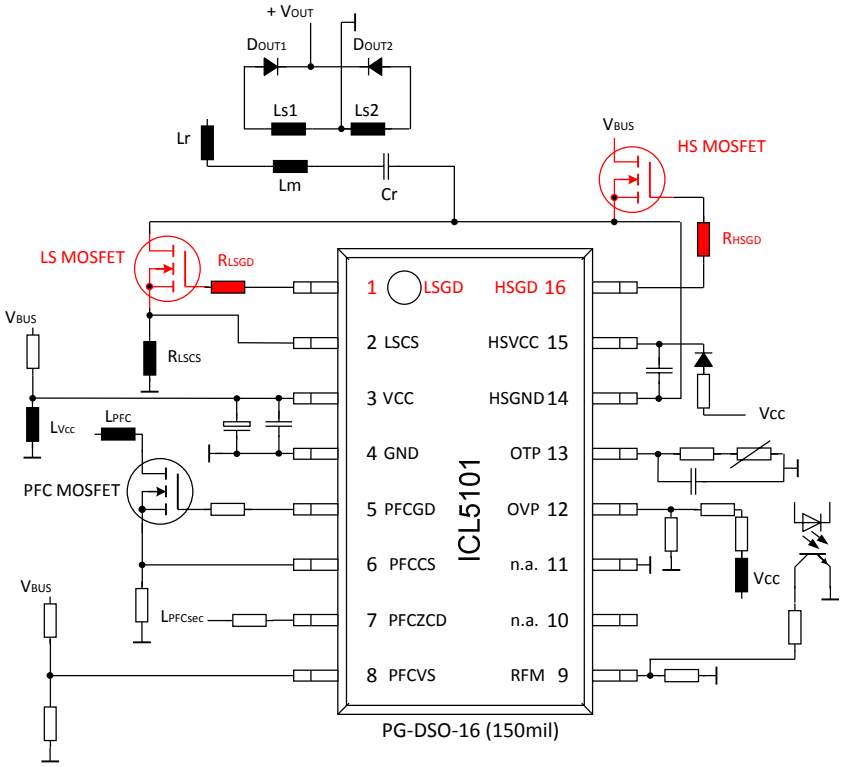

Figure 21 PIN Setup showing the Components in red

5.2.6 Selection of Half-Bridge low side Shunt Resistor (LSCS)

The half-bridge shunt resistor is connected between LSCS pin and GND to sense the current flowing through the low side MOS to achieve half-bridge over current protection. Because during start-up phase the half-bridge frequency decreases from 135kHz towards the minimum operation frequency set by RFM pin until output is stable regulated, during this period some unstable current peak could happen. To avoid miss triggering of over current protection, the protection voltage level of LCSC pin is set higher which is 1.6V during the first 650ms (a brief value) after AC plug in before system goes into run-mode. In run-mode it is set at 0.8V.

We have already known that the maximum peak current flowing through the MOSFET is $I_{Lr\_p\_\max} = 1.279A$, and then we could calculate the shunt resistor as following:

$$R_{lscs} = \frac{V_{LSCSOvC2\_typ}}{I_{Lr\_p\_\max}} = \frac{0.8V}{1.279A} = 0.625\Omega \qquad \text{Equation 76}$$

With consideration of load jump from no load to full load higher current peak may happen. The real "R_{1scs}" is set lower. We set $R_{1scs} = 0.545\Omega$ in our reference design which is separated to 3 resistors (R_{39}, R_{41} and R_{43} in the schematic) for thermal consideration. The peak current of the half-bridge is then allowed for 1.47A. The MOSFET and saturation current of the resonant inductor should be selected and designed accordingly.

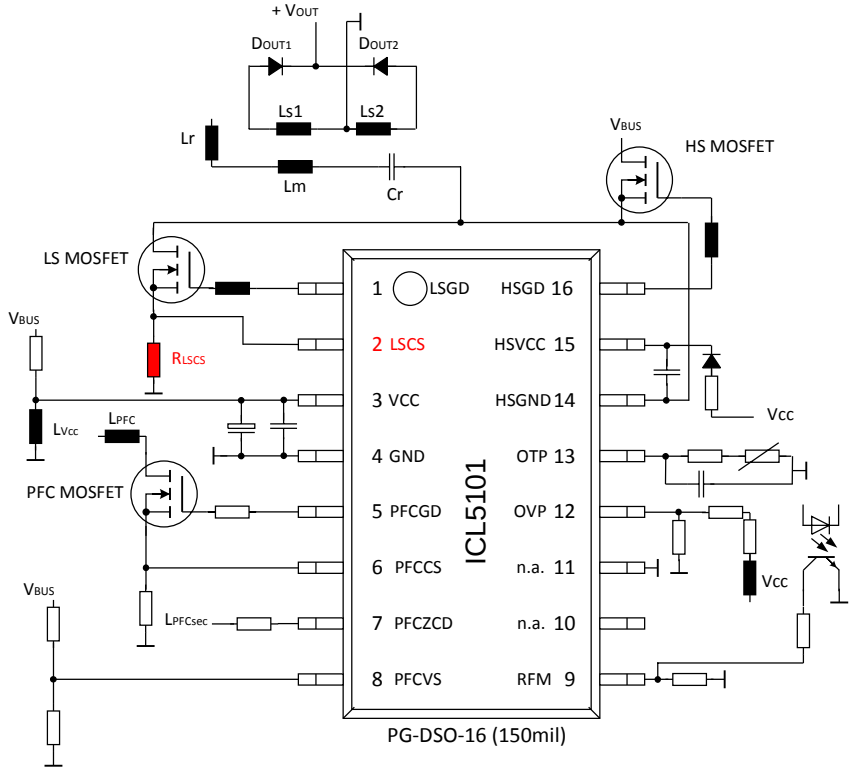

Figure 22 PIN Setup showing the Components in red

5.2.7 Selection of Output Diode

We use full-wave rectification at LLC output in our reference design. The reverse blocking voltage class should be larger than double output voltage. Consider with voltage spike margin, we selected 200V diode.

To achieve a high efficiency, low "V_F" Schottky diode is preferred. The average current of the diode at required case temperature should be larger than half of the maximum DC output current $I_{out\_max} = 2.57A$.

To achieve a low temperature rising and high efficiency, we selected STTH802 as output diode, which allows high average forward current and could result to very low "V_F" at small current condition.
The heat dissipator can be calculated as shown in Equation 75a:

$$R_{thja} = \frac{\Delta T}{P_{loss\_total}} = \frac{T_C - T_A}{I_{out\_max} * V_{FDout}}$$ Equation 76a

$$R_{thja} = \frac{105°C - 45°C}{2.57A * 0.6V} = 38.9\frac{K}{W}$$

5.2.8 Selection of Output Capacitor

The first target for selection output capacitor is to fulfil the output voltage ripple requirement. In our reference design the target maximum allowed peak to peak voltage ripple is $U_{o\_ripple\_pp} = 540mV$.

In normal operation this consists of double-line frequency ripple and the double half-bridge switching frequency ripple. In steady state the maximum ripple happens at maximum output power and lowest switching frequency. As the ripple requirement is for the operation range inside nominal operation power and with nominal voltages, the nominal bus voltage "U_{bus_nom}", nominal output voltage "U_{out_nom}" and nominal output current "I_{out_nom}" will be used here for calculation.

The high frequency peak ripple current "$I_{r\_HF\_p}$" equals to the nominal output current "I_{out_nom}". The high frequency ripple voltage equation could be written as following:

$$\frac{1}{2} \bullet U_{o\_HFripple\_pp} = \sqrt{\left(\frac{1}{2 \bullet \pi \bullet 2 \bullet f_{sw\_nom} \bullet C_{out}}\right)^2 + ESR^2{}_{cout}} \bullet I_{out\_nom} \qquad \text{Equation 77}$$

"$U_{o\_HFripple\_pp}$" is the peak to peak double half-bridge switching frequency voltage ripple. "C_{out}" is the output capacitor. "ESR_{cout}" is the ESR of "C_{out}".

Let's define "$U_{o\_LFripple\_pp}$" as peak to peak value of output double-line frequency voltage ripple. Then we could approximately calculate the total peak to peak value of output voltage ripple as following:

$$U_{o\_ripple\_pp} = 540mV = U_{o\_HFripple\_pp} + U_{o\_LFripple\_pp} \qquad \text{Equation 78}$$

$$U_{o\_LFripple\_pp} = \sqrt{\left(\frac{1}{2 \bullet \pi \bullet 100Hz \bullet C_{out}}\right)^2 + ESR^2{}_{cout}} \bullet I_{r\_100\_pp} \qquad \text{Equation 79}$$

"$I_{r\_100\_pp}$" is the peak to peak value of output double-line frequency ripple current. This ripple current could be approximately calculated according to following equation:

$$I_{r\_100\_pp} = I_{out\_r\max} - I_{out\_r\min} \qquad \text{Equation 80}$$

Assume a constant rated resistance load at output, "$I_{out\_r\max}$" is the transient output current at $U_{out} = U_{out\_nom} + \frac{U_{o\_ripple\_pp}}{2}$. Then "$I_{out\_r\max}$" could be calculated as following:

$$I_{out\_r\max} = \frac{U_{out\_nom} + \frac{U_{o\_ripple\_pp}}{2}}{U_{out\_nom}} \bullet I_{out\_nom} = 2.047A \qquad \text{Equation 81}$$

"$I_{out\_r\min}$" is the transient output current at $U_{out} = U_{out\_nom} - \frac{U_{o\_ripple\_pp}}{2}$. It could be calculated as following:

$$I_{out\_r\min} = \frac{U_{out\_nom} - \frac{U_{o\_ripple\_pp}}{2}}{U_{out\_nom}} \bullet I_{out\_nom} = 2.027A \qquad \text{Equation 82}$$

So according to Equation 80, we have $I_{r\_100\_pp} = 0.02A$.

There are two unknown parameters in Equation 77 and Equation 79 "C_{out}" and it's ESR "ESR_{cout}". Normally for Electrolytic Capacitor, its ESR is strongly related with its capacitance. High efficiency, long life and low temperature rising is the target for our reference design. So for 54V output voltage we selected 100V Electrolytic Capacitor from Rubycon ZLJ series. According to datasheet, the maximum ESR value at 100 kHz at -10°C varies from 5.4 Ω to 0.076 Ω with increasing capacitance. According to Equation 76, Equation 77 and Equation 78 to achieve 540mV output ripple voltage, the ESR should be anyway smaller than $\frac{0.27V}{2.037A} = 0.132\Omega$. If we take $ESR_{cout} = 0.11\Omega$, we will have $C_{out} = 348\mu F$.

Then we need to calculate the total effective RMS output ripple current. The ripple current limit of the selected capacitor should be larger than this effective ripple current.

The total effective RMS ripple current could be calculated as following:

$$I_{r\_effect\_rms} = \sqrt{\left[\left(\frac{I_{r\_100\_rms}}{\eta_{100}}\right)^2 + \left(\frac{I_{r\_HF\_rms}}{\eta_{HF}}\right)^2\right]} \qquad \text{Equation 83}$$

"$I_{r\_100\_rms}$" is the RMS value of the double-line frequency ripple current. "η_{100}" is the capacitor ripple current frequency coefficient for 100Hz. "$I_{r\_HF\_rms}$" is the RMS value of the half-bridge switching frequency ripple current. "η_{HF}" is the capacitor ripple current frequency coefficient for half-bridge switching frequency.

For double-line frequency ripple current, we could approximately assume it has a sinusoidal waveform. The RMS value could then be calculated as:

$$I_{r\_100\_rms} = \frac{I_{r\_100\_pp}}{2 \bullet \sqrt{2}} = 0.007A \qquad \text{Equation 84}$$

The half-bridge frequency ripple current "I_{r_HF}" is a subtraction result of transformer secondary winding current "I_{SAC}" and output DC current "I_{out}". It is shown in Figure 23. The equation at nominal output power and nominal in-and output voltage could be written as following:

$$I_{r\_HF} = \begin{cases} I_{sac\_p\_nom} \bullet \sin(2 \bullet \pi \bullet f_r \bullet t) - I_{out\_nom}, when 0 \le t < \frac{1}{2f_r}; \\ -I_{out\_nom}, when \frac{1}{2f_r} \le t \le \frac{1}{2f_{sw\_nom}} \end{cases} \qquad \text{Equation 85}$$

The secondary winding peak current at nominal condition "$I_{sac\_p\_nom}$" could be calculated according to Equation 62 as following:

$$I_{sac\_p\_nom} = I_{out\_nom} \bullet \frac{f_r}{f_{sw\_nom}} \bullet \frac{\pi}{2} = 3.855A$$ Equation 86

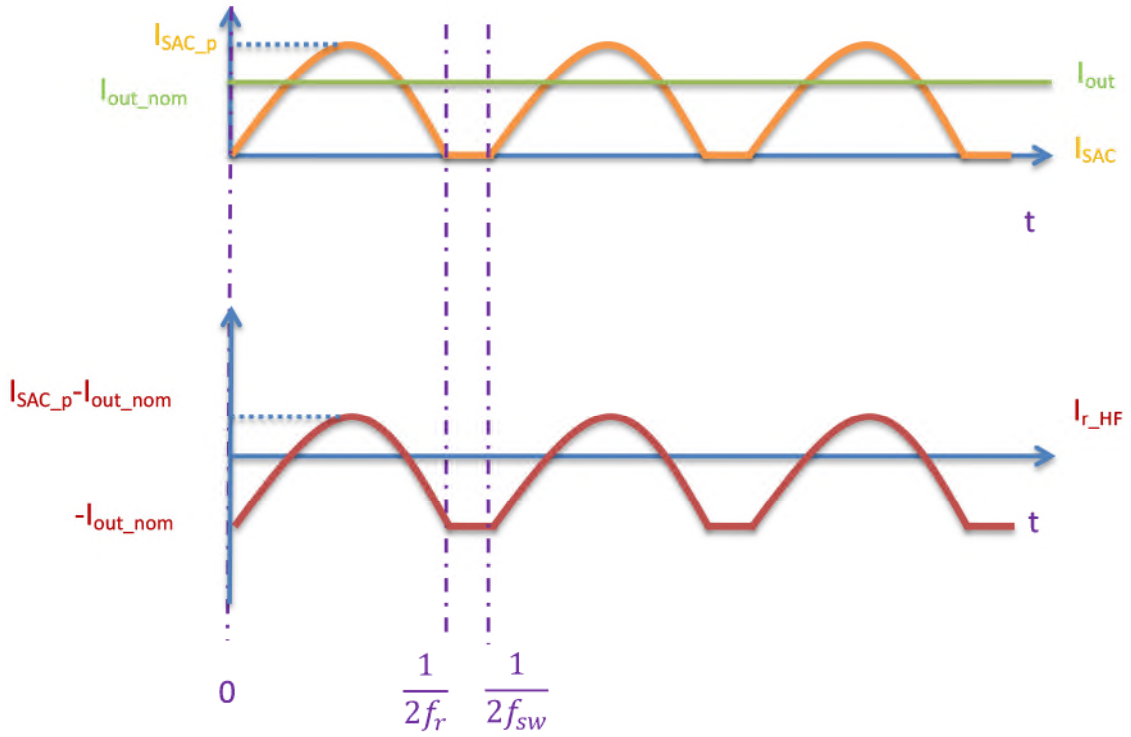

Figure 23 Output Half-Bridge Frequency Ripple Current at nominal Power and Voltage

According to Figure 23 and Equation 85 we could calculate the RMS value of "I_{r_HF}" as following:

$$I_{r\_HF\_rms} = \sqrt{\frac{\int_0^{\frac{1}{2f_{sw\_nom}}} I^2_{r\_HF} \bullet dt}{\frac{1}{2f_{sw\_nom}}}} = 1.421A$$ Equation 87

The ripple current frequency coefficient could be found in capacitor's datasheet. The frequency coefficient table abstracted from datasheet is shown in Table 3.

◆MULTIPLIER FOR RIPPLE CURRENT

Frequency (Hz)		120	1k	10k	100k≦
Coefficient	8.2~33μF	0.42	0.70	0.90	1.00
	47~270μF	0.50	0.73	0.92	1.00
	330~680μF	0.55	0.77	0.94	1.00
	820~1800μF	0.60	0.80	0.96	1.00
	2200~8200μF	0.70	0.85	0.98	1.00

Table 3 Ripple Current Frequency Coefficient Table of Rubycon ZLJ Series Electrolytic Capacitor

So according to Table 3, for a capacitance of "$348\mu F$" we have $\eta_{100} = 0.55$ and $\eta_{HF} = 0.94$. Take all the value into Equation 83 we could have $I_{r\_effect\_rms} = 1.511A$. According to datasheet, with consideration of board dimension, we could select the $330\mu F$ capacitor with dimension of "$\phi D \bullet L = 12.5mm \bullet 35mm$". Its maximum ESR at 100kHz at -10°C is 0.11Ω. The output effective RMS ripple current is then nearly only half of the ripple current limit specified in the datasheet. This ripple current margin is required for a long life design.

When we take $330\mu F$ back into Equation 78, we have $U_{o\_ripple\_pp} = 0.545V$.

To ensure the output voltage ripple to be inside the range of limit and also to filter the conducted noise, an extra "LC" filter is connected after the output capacitor. It builds up a voltage divider for the high frequency ripple, which is also the main ripple at output. To ensure a high efficiency, a small HF inductor is normally used here. If we have $L_{o\_filter} = 4.7\mu H$ and want to suppress the output voltage ripple to be $\frac{1}{10}$ of the ripple on "C_{out}", we would have following equation:

$$\frac{U_{filter\_ripple\_pp}}{U_{o\_ripple\_pp} - U_{filter\_ripple\_pp}} = \frac{\sqrt{\left[\frac{1}{2\pi \bullet 2 \bullet f_{sw\_nom} \bullet C_{o\_filter}}\right]^2 + ESR^2_{cfilter}}}{\sqrt{\left(2\pi \bullet 2 \bullet f_{sw\_nom} \bullet L_{o\_filter}\right)^2 + RS^2}} = \frac{1}{9} \quad \text{Equation 88}$$

"RS" is the series resistance of the filter inductor. It could be neglected here. Also for $\left[\frac{1}{2\pi \bullet 2 \bullet f_{sw\_nom} \bullet C_{o\_filter}}\right]^2$, in double half-bridge switching frequency range, it could be neglected. "C_{o_filter}" is the output filter capacitor. The simplified equation of Equation 88 is as following:

$$\frac{U_{filter\_ripple\_pp}}{U_{o\_ripple\_pp} - U_{filter\_ripple\_pp}} = \frac{ESR_{cfilter}}{2\pi \bullet 2 \bullet f_{sw\_nom} \bullet L_{o\_filter}} = \frac{1}{9} \quad \text{Equation 89}$$

So we could have the calculation result: $ESR_{cfilter} = 0.3\Omega$. According to Rubycon ZLJ series datasheet, we selected $100\mu F$ as C_{o_filter}.

For EMI optimization, if necessary, the value of "L_{o_filter}" and "C_{o_filter}" could be adjusted.

5.2.9 Design of Regulation Loop (RFM)

In our reference design, like most of galvanic isolated circuits, we use Opto-coupler and AZ431 (the same function as TL431) to build up the feedback loop and the Error Amplifier.

From Chapter 5.2.3 we know that the maximum current flowing through the output of the opto-coupler "OT1" when using R23 = 9.1kΩ (calculated via Equation 69 in Chapter 5.2.3):

$$I_{OT1\_o\_\max} = \frac{V_{RFM\_typ} - V_{CE\_opto}}{R_{23}} = \frac{2.5V - 0.25V}{9.1k\Omega} = 247\mu A \qquad \text{Equation 90}$$

Because the "CRT" of VOL617-3T is from 100% to 200%, the maximum needed current at primary side of the opto-coupler is $I_{OT1\_p\_\max} = 250\mu A$.

The voltage reference AZ431 needs about 1mA as minimum current for regulation. So the current flowing through "R_{45}" should be not smaller than 1.25mA.

Because the maximum allowed cathode voltage of AZ431 is $40V < U_{out} = 54V$, to protect AZ431 a "$9.1V$" Zener-diode is used to be connected from "R_{45}" to GND. Let's reserve a current of $250\mu A$ for Zener-diode voltage clamping using. Then the total current flowing through "R_{45}" is $1.5mA$. "R_{45}" could be calculated as:

$$R_{45} = \frac{V_{OUT} - V_{D16}}{I_{KA\min} + I_{opto} + I_{D16}} = \frac{54V - 9.1V}{1.0mA + 250\mu A + 250\mu A} = 30k\Omega \qquad \text{Equation 91}$$

The supply resistor of the TL431 reference diode we calculate as followed:

$$R_{46} = \frac{V_{FTL431}}{I_{KA\min}} = \frac{0.7V}{1.0mA} = 700\Omega \qquad \text{Equation 91a}$$

Choose the next lower value of: R_{46} = 680Ω

The reference voltage of AZ431 is 2.5V. To regulate the output voltage at 54V, we set the voltage divider, which consists of "R_{50}" parallel to "R_{53}" and "R_{52}" shown in the schematic. According to equation 92 we define at first the value of R_{50} // R_{53} to 6.2kΩ and recalculate R_{52}:

$$R_{52} = R_{50//53} * \frac{V_{OUT}}{V_{REFTel431}} = 6.2k\Omega * \frac{54V}{2.5V} = 127k\Omega \qquad \text{Equation 92}$$

The low side resistance of the voltage divider is separated to two in parallel connected resistors to set the voltage divider more precisely.

Normally to achieve a high efficiency design, we need to set the voltage divider resistance as high as possible. But in reality, the current "I_{ref}" flowing into REF pin of the AZ431 has influence on the output voltage and it also varies with changing of the ambient temperature. The real output voltage equation could be written as following:

The larger "R_{52}" is the larger influence of "I_{ref}" on the output voltage. So the voltage divider resistance could not be set too large. In our reference design, we selected $R_{52} = 127k\Omega$, $R_{50} = 7.5k\Omega$ and $R_{53} = 34k\Omega$ in the end.

For error signal compensation network, we used "PIDT1" circuit, which provides us large freedom to optimise the system performance.

The target for setting the negative feedback compensation network is to achieve a stable system and a fast enough time response to input and output change. But normally these two targets conflicts with each other.

A negative feedback loop already provides -180° phase shift without compensation network. To avoid system self-resonant and to achieve a stable working system, the additional compensation network phase shift should be smaller than -180° before system loop Gain reaches one. "180°+ phase shift of compensation network" could be defined as phase margin. To achieve high system stability, large phase margin of the feedback loop should be ensured. But in the other side large phase margin slows down the time response. 60° is normally considered to be the optimum value for phase margin.

To choose the most suitable parameters for compensation network, at first a system modeling without feedback loop needs to be done to get the system transfer function. Then the Bod Plot for Amplitude and Phase need to be plotted. According to the Bod Plot, a suitable compensation network with suitable Bod Plot form could be defined base on the above descript criteria. In the end, the parameters still need to be tested and adjusted after real testing. For detailed info regarding system modeling and compensation network setting could refer to [7] and [8].

6 VCC Supply Circuit Design

6.1 Fast Start-Up VCC Circuit using Hysteresis

6.1.1 Fast Start-Up (VCC)

For LED application, a total system Start-Up time from AC-plug-in to output light is required to be shorter than 500ms. As our reference design could be applied as front stage converter for system bus voltage suppling, the Start-Up time from AC-plug-in to output voltage reaching 54V is required to be shorter than 200ms. With consideration of high efficiency, a fast Start-Up circuit, which could be disabled after system starting, is then required.

Look into Schematic in Chapter 3.1, the fast Start-Up circuit consists of "R_7", "R_8", "R_{18}", "Q_9", "R_{40}", "R_{47}", "D_4", "R_{48}", "Q_{10}", "D_5" and "R_{44}".

"Q_9" is 600V depletion MOS BSP135. It is normally on at zero Gate-Source voltage. The minimum Gate-Source threshold voltage of "Q_9" is $V_{GS(th)\_\min} = -2.1V$.

The fast Start-Up principle is that when AC input is plugged in the VCC capacitors "C_{18}" and "C_7" begins to be charged by a maximum current flowing through "Q_9" limited by "R_{40}". This current could be set relative large so that the VCC capacitors could be charged very quickly. When the voltage on VCC capacitor reaches IC turn-on threshold, IC begins to operate. The VCC voltage will then start to be supplied by LLC transformer auxiliary winding "$T2/2$" through "D_{12}", "R_{42}" and the linear regulator consisting of "R_1", "D_3", "Q_1" and "D_{10}". As long as the voltage on the capacitor "C_3" before the linear regulator reaches the voltage level (set by "R_{44}" and "D_5", by reaching this voltage, it should be considered as successfully building up of VCC supplying via self-biasing through transformer auxiliary winding.) for turning-on of "Q_{10}", the Gate voltage of "Q_9" is pulled low by "Q_{10}" via "R_{48}". The Gate-Source voltage of "Q_9" is then reverse-biased, which is resulted by voltage divider "$R47$" and "R_{48}". "Q_9" is then turned off and this fast Start-Up circuit is automatically disabled.

"R_7", "R_8" and "R_{18}" limit the VCC-start-up inrush current. According to BSP135 datasheet, the allowed power dissipation at $T_a = 100°C$ is about 0.7W. If take R_{dson} at $T_j = 150°C$ into calculation, we could calculate the maximum allowed continuous Drain-Source current as following:

$$I_{d\_\max\_Q9} = \sqrt{\frac{P_{DisBsp135}}{R_{DAON150°C}}} = \sqrt{\frac{0.7W}{138\Omega}} = 71mA \qquad \text{Equation 93}$$

The maximum input voltage is 305VAC for our reference design. So the maximum allowed total resistance of "R_7", "R_8" and "R_{18}" could be calculated as following:

$$R_{total\_vccsu} = \frac{305V \bullet \sqrt{2}}{71mA} = 6.07k\Omega \qquad \text{Equation 94}$$

VCC Supply Circuit Design

So we set $R_7 = R_8 = R_{18} = 2.2k\Omega$ to reserve about 10% margin. The absolute maximum drain current flowing through "Q_9" is then limited at

$$I_{d\_max\_Q9} = \frac{305V \bullet \sqrt{2}}{6.6k\Omega} = 65mA \qquad \text{Equation 95}$$

To utilize the maximum allowed drain current range to achieve a maximum charging current, we could set "R_{40}" to zero. If we want to set the charging current at a certain level, "R_{40}" could also be calculated according to following equation:

$$R_{40} = \frac{V_{GS(th)\_min}}{I_{d\_Q9}} = \frac{2.1V}{65mA} = 32\Omega \qquad \text{Equation 96}$$

"D_4" is used to clamp the VCC voltage at Start-Up phase. According to ICL5101 datasheet, the absolute allowed maximum VCC voltage is 18V. So for "D_4" 15V Zener Diode is selected. So at Start-Up, in worst case VCC voltage is clamped at $15V + 2.1V = 17.1V$.

"R_{47}" is used here to build a negative Gate-Source voltage when there is current flowing via "$R47$" to "D_4". With consideration of efficiency, "R_{47}" should be set as large as possible. But to ensure "D_4" to have enough current for voltage clamping, some hundreds of approximately 200 μA current would be preferred.

$$R_{47} = \frac{V_{GS(th)\_min}}{I_{D4}} \frac{2.1V}{200\mu A} = 10.5k\Omega \qquad \text{Equation 96a}$$

In the end "$R47$" is set at $10k\Omega$, which results in a maximum current of about $\frac{2.1V}{10k\Omega} = 210\mu A$ flowing through "D_4".

To reduce the power dissipation when "Q_{10}" is turned on, "R_{48}" is used here together with "$R47$" in series to reduce the current flowing through "Q_{10}". At the meantime, the voltage divider built from "R_{48}" and "R_{47}" should ensure the Gate-Source voltage to be larger than $V_{GS(th)\_min}$ when "Q_{10}" is on. So "R_{48}" could also be set at $10k\Omega$. The Gate-Source voltage is then reverse-biased at half-VCC voltage which is larger enough to turn off "Q_9".

According to datasheet the maximum VCC turn-off threshold is 11V. As long as the voltage at "VSS" in the schematic is larger than "11V+Forward voltage of D_{10}+V_{BE} of Q_1", we could assume that the VCC supplying from transformer auxiliary winding is successfully built up and the Start-Up circuit could be disabled. To take a safety margin, we selected 13V Zener Diode for "D_5". So when the "VSS" voltage reaches about 13.6V, the Start-Up circuit is turned off.
A linear voltage regulator is required from "VSS" to "VCC", because the voltage supplied from transformer auxiliary winding varies a lot when output power changes. The absolute maximum allowed voltage for VCC is only 18V. So we choose 16V Zener Diode for "D_3" to clamp the maximum VCC voltage during running at "16V-0.6V-0.6V=14.8V".

6.1.2 VCC Chip Supply Voltage Hysteresis

ICL5101 can latch up the IC when some main failures are detected. But for our reference design, we want always to have Auto-Restart after failure detection. So we need to make the VCC voltage to be able to drop under UVLO level. To achieve this target we need a Hysteresis to reactivate the Start-Up circuit when VCC is under UVLO level.

For this, "R_{85}", "D_9", "Q_{12}", "D_{13}", "R_{49}", "R_9" and "C_6" are used to build the hysteresis circuit.

We detect VCC voltage directly as trigger signal for turning-on "Q_9" again. After "VSS" voltage reaches the threshold to turn on "Q_{10}", "Q_{12}" is then also turned on by VCC via "R_{85}", "D_9", "D_{13}" and "R_{49}" through "Q_{10}". Then if failure happens and half-bridge stops, "VSS" will not be supplied anymore and drops below the threshold again, "D_5" will also not conduct anymore. But "Q_{10}" stays on through the path built by "Q_{12}", "D_9" and "R_{85}" supplied by VCC. Only when the VCC voltage drops below the threshold set by "$V_{R85} + V_{z\_D9} + V_{be\_Q12} + V_{F\_D13} + V_{R49} + V_{ce\_Q10}$", "$Q_{12}$" is turned off. Then "$Q_{10}$" will be also turned off and "Q_9" is turned on again. Fast Start-Up circuit is activated again. When "$V_{R85} + V_{z\_D9} + V_{be\_Q12} + V_{F\_D13} + V_{R49} + V_{ce\_Q10}$" is set lower than VCC UVLO level, an expected hysteresis is achieved for turning on and off Start-Up circuit.

Note: "V_{R85}": voltage drop on R_{85};
"V_{z_D9}": Zener clamping voltage of D_9;
"V_{be_Q12}": Base-Emitter voltage of Q_{12};
"V_{F_D13}": Forward voltage of D_{15};
"V_{R49}": voltage drop on R_{49};
"V_{ce_Q10}": Collector-Emitter voltage of Q_{10};

The lowest VCC UVLO threshold is 10V according to datasheet. Assuming $V_{be\_Q12} = 0.6V$, $V_{F\_D13} = 0.6V$ and $V_{ce\_Q10} = 0.3V$, we could set $V_{z\_D9} = 8.2V$. The Start-Up circuit restart threshold is then set below VCC UVLO.

6.2 VCC Chip Supply Voltage in RUN Mode (VCC)

In Run-Mode the VCC voltage is supplied by LLC transformer auxiliary winding through a linear voltage regulator circuit as descript in Chapter 6.1.1.

The output voltage reflects to auxiliary winding divided by turn ratio $n_{aux} = \frac{N_s}{N_{aux}}$.

Note: "N_s": half of total secondary winding number;
"N_{aux}": auxiliary winding number

To achieve a short Start-Up time the turn ratio should be hold as small as possible. But with consideration of high efficiency, the turn ratio should not be too small. In our circuit we have already a fast Start-Up circuit. So after testing we set n_{aux} at around 2.5, which make the reflected voltage on auxiliary winding at around 20V.

6.3 High Side Supply Voltage (HVCC / HVGND)

High Side MOSFET at half-bridge has floating GND, which is the middle point of the half-bridge and its voltage varies between "U_{bus}" and GND. To drive the High-Side MOSFET the ICL5101 has HSGD (High-Side Gate Driver) Pin which is supplied by HSVCC (High-Side VCC) Pin internally.

To supply the HSVCC an external boot strap circuit could be used. It consists of "D_{11}", "R_{28}" and "C_{14}".

"C_{14}" is connected between HSVCC Pin and HSGND Pin as HSVCC capacitor which is charged through "D_{11}" and "R_{28}" by VCC when half-bridge low side MOSFET is turned on. As the energy is only used to drive High-Side MOSFET, normally 100nF capacitor is enough.

When High-Side MOSFET is turned on HSGND voltage is equal to "U_{bus}". A 600V Ultra-Fast Diode is need for "D_{11}". As the required energy is small, 1A is enough. MURS160 is used in our reference design.

"R_{28}" is used here to limit the peak charging current also to prevent miss triggering of half-bridge over current at LSCS Pin at the moment half-bridge low side MOSFET is switched on. 10Ω resistor is used in our reference design.

7 Output Over Voltage Protection

7.1 Output Over Voltage Protection using IC (OVP PIN 12)

As descript in Chapter 6.2 the voltage on LLC transformer auxiliary winding reflects the output voltage divided by turn ratio $n_{aux} = \frac{N_s}{N_{aux}}$. So we could detect the output over Voltage at primary side by monitoring the voltage on the auxiliary winding using IC OVP Pin.

To achieve an effective OVP function and to ensure the safety of the system, the minimum detection threshold of the OVP Pin needs to be taken as the OVP detection threshold. According to Datasheet, the minimum AC OVP current threshold $I_{ovp\_min} = 186\mu A$, it is a Peak to Peak value. During design we will take the peak value for components value calculation.

So the first equation could be written as following:

$$\frac{V_{aux\_ovp} - V_{ovp}}{R_{ovp}} = \frac{I_{ovp\_min}}{2} + \frac{V_{ovp}}{R_{29}} \qquad \text{Equation 97}$$

Note: "V_{aux_ovp}": Reflected voltage of output over voltage level at auxiliary winding;
"V_{ovp}": Voltage on OVP Pin when OVP is detected;
"R_{ovp}": Sum of "R_{33}" and "R_{37}";

Because the IC checks at every Start-Up the present of a $12\mu A$ current flowing into OVP Pin and without this current OVP would be triggered, OVP Pin should be disabled at Start-Up phase. To deactivate the OVP Pin at Start-Up phase the voltage on OVP Pin should be kept below the minimum voltage on OVP Pin for enabling OVP monitoring, $V_{ovpEnable\_min}$, which is 350mV listed in datasheet. The maximum current flowing out of OVP Pin at Start-Up phase is $I_{ovpsource\_max} = 5\mu A$. Based on this, the second equation could be written as following:

$$\frac{V_{ovpEnable\_min}}{\frac{R_{ovp} \bullet R_{29}}{R_{ovp} + R_{29}}} = I_{ovpsource\_max} \qquad \text{Equation 98}$$

There is an internal series resistor of about 5kΩ to an internal voltage source of about 600mV at the OVP Pin (not specified in the datasheet). So at the moment OVP is detected, the voltage on OVP Pin could be calculated as following:

$$V_{ovp} = \frac{I_{ovp\_min}}{2} \bullet 5k\Omega + 600mV = 1.06V \qquad \text{Equation 99}$$

So "R_{ovp}" and "R_{29}" could be calculated from Equation 97 and Equation 98. The real "R_{29}" value should be chosen to be smaller than calculated value to make sure the OVP Pin is deactivated during Start-Up phase.

Output Over Voltage Protection

Take our reference design as calculation example:

The output OVP level is set at $V_{out\_ovp} = 58V$ and the turn ratio of the secondary to aux winding is 13:5, V_{aux_ovp} could be calculated as:

$$V_{aux\_ovp} = V_{out\_ovp} * \frac{1}{n_{aux}}$$

$$V_{aux\_ovp} = 58V * \frac{5}{13} = 22.31V$$

Equation 99a

So according to Equation 97 and Equation 98 we could have following two equations:

$$\frac{22.3V - 1.06V}{R_{ovp}} = \frac{186\mu A}{2} + \frac{1.06V}{R_{29}} \text{ and } \frac{350mV}{\frac{R_{ovp} \bullet R_{29}}{R_{ovp} + R_{29}}} = 5\mu A$$

So as a result we achieve:

$$R_{ovp} = \frac{V_{aux\_ovp}}{\frac{I_{ovp\_\min}}{2} + \frac{V_{ovp} * 5\mu A}{350mA}} = \frac{22.3V}{\frac{186\mu A}{2} + \frac{1.06V * 5\mu A}{350mA}} = 206.2k\Omega$$

Equation 99b

and set the calculated ROVP in:

$$R_{29} = \frac{R_{ges} \bullet R_{OVP}}{R_{ovp} + R_{ges}} = \frac{\frac{350mV}{5\mu A} \bullet 206.2k\Omega}{206.2k\Omega + \frac{350mV}{5\mu A}} = 106k\Omega$$

Equation 99c

In reality "R_{29}" could be set at $100k\Omega$, and $R_{33} = R_{37} = \frac{R_{ovp}}{2} = 103k\Omega$.

The theoretical calculation provides only a basic reference for OVP setting. For choosing practical OVP resistance in the real circuit, it should be fine-tuned, because of the coupling effect of the transformer. Note: to disable OVP set PIN 12 to IC GND.

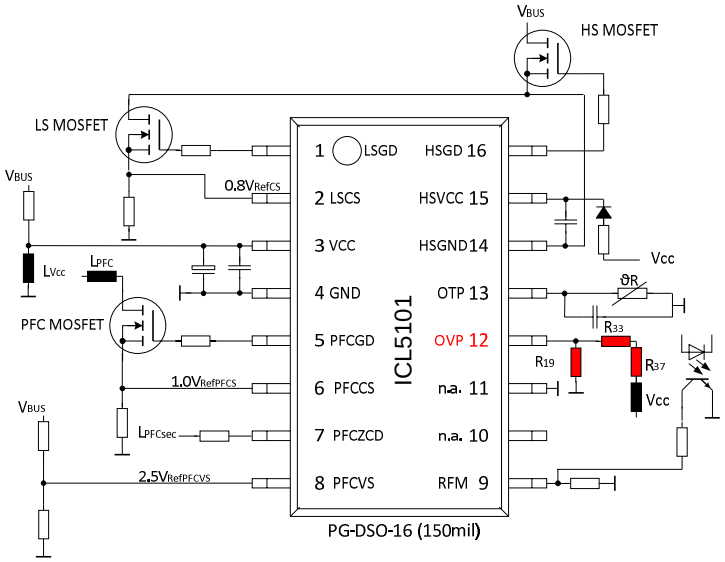

Figure 24 PIN Setup showing the Components in red

7.2 Output Over Voltage Protection using external Circuit (RFM)

With IC OVP Pin, Over Voltage Protection could be achieved at primary side. It saves cost and board area. But because of transformer coupling effect, the protection could not be set very precisely.

With request of a precise output Over Voltage Protection, an external OVP circuit with Hysteresis could be applied. In the schematic, "R_{27}", "R_{54}", "R_{59}", "Q_6", "R_{55}", "C_{27}", "U_6", "D_8", "R_{57}", "R_{58}", "R_{56}", "Q_4", "R_{78}", "R_{60}", "Q_2", "R_{30}" and "$OT2$" build together this external OVP circuit with Hysteresis.

"U_6" AZ431 is used here as voltage reference. When the "U_{out}" is still under "V_{ovp}", the voltage built by voltage divider (consist of "R_{27}", "R_{54}" and "R_{59}") on reference Pin of AZ431 is lower than internal 2.5V reference voltage. Then the cathode voltage of AZ431 is high, which is clamped by Zener Diode "D_8" at 15V. "Q_4" and "Q_6" are turned on by the voltage divider "R_{57}" and "R_{58}". With "on" status of "Q_6", "R_{59}" is paralleled to "R_{54}". This builds a low resistance for the low side of the voltage divider. With "on" status of "Q_4", Base voltage of "Q_2" is pulled down so that "Q_2" is turned off and the opto-coupler is in OFF mode. So that "Q_{11}" could stay "on" because its Base is supplied by VCC through "R_{22}". System could normally work.

When "U_{out}" becomes to "V_{ovp}", the voltage on reference Pin of AZ431 reaches 2.5V. The cathode voltage of AZ431 is then also drops to nearly 2.5V. The Gate voltage of "Q_4" and "Q_6" become low so that "Q_4" and "Q_6" are turned off. At the moment "Q_6" is turned off, "R_{59}" is decoupled from "R_{54}". The low side resistance of the voltage divider is then enlarged. So that to reduce the reference voltage to be lower than 2.5V again a lower "U_{out}" is required. With this method, a Hysteresis is achieved. At the moment "Q_4" is turned off Base voltage of "Q_2" is pulled high by voltage divider built from "R_{56}", "R_{78}" and "R_{60}". Then "Q_2" is turned on and "$OT2$" conducted. Then at the primary side of "$OT2$" the Base of "Q_{11}" is pulled low and "Q_{11}" is turned off. The path from OTP Pin to GND is cut off. This results an infinite large resistance between OTP Pin and GND Pin. In normal operation, there is a current flowing out of OTP Pin. The voltage on OTP Pin then rises. As long as the voltage on OTP Pin reaches over 3.2V for longer than $620\mu s$, system is stopped. Restart of the system could be triggered by "U_{out}" dropping below the OVP hysteresis level or VCC dropping below UVLO level.

In our reference design, external OVP circuit is used and OVP Pin is set through "R_{19}" to GND.

8 Over Temperature Protection (OTP)

The OTP function for ICL5101 could be realized via OTP Pin. In Run-Mode when the voltage on OTP Pin 13 is exceeding 3.2V for longer than $620\mu s$ the system will be stopped. During Start-Up when UVLO or $10.5V < VCC < 14.1V$ the OTP threshold is at 1.6V.

A resistor "R_{25}" and two PTCs are connected in series between OTP Pin 13 and GND in order to achieve the temperature monitoring and protection. PTCs could be put anywhere on the board to measure the temperature of the wished area – the detection of the hot spot is flexible.

To calculate the value for "R_{25}" and PTCs we need to consider the high temperature and low temperature condition. Also we need to consider the different thresholds for Start-Up phase and Run-Mode. Target is to avoid miss triggering of OTP at room temperature and to achieve correct triggering of OTP at high temperature.

At room temperature, the worst case happens in Start-Up phase. The maximum OTP current $I_{OTP3} = 26.6\mu A$ and the minimum OTP threshold voltage is $V_{OTP1} = 1.546V$ are considered. The value of PTC could be neglected in the calculation, only few ohms at room temperature. Then we have following Equation:

$$R_{25} \le \frac{V_{OTP1} - V_{ce\_Q11}}{I_{OTP3}} = \frac{1.546V - 0.3V}{26.6\mu A} = 46.84k\Omega \qquad \text{Equation 100}$$

"V_{ce_Q11}" is the collector-emitter voltage of "Q_{11}". In the end we selected $R_{25} = 47K\Omega$.

When the temperature reaches the OTP level in Run-Mode, the maximum OTP current is still $I_{OTP3} = 26.6\mu A$. The typical OTP threshold voltage changes to $V_{OTP3} = 3.2V$. So we could calculate the total resistance "R_{OTP}" between OTP Pin and GND as following:

$$R_{OTP} = \frac{V_{OTP3} - V_{ce\_Q11}}{I_{OTP3}} = \frac{3.2V - 0.3V}{26.6\mu A} = 109k\Omega \qquad \text{Equation 101}$$

The resistance of each PTC at the wished protection temperature should be:

$$R_{62} + R_{77} = R_{OTP} - R_{25} = 109k\Omega - 47k\Omega = 62k\Omega \qquad \text{Equation 101a}$$

In our reference design, we split our PTC resistance in two serial R62 and R77:

$$R_{62} = R_{77} = \frac{62k\Omega}{2} = 31k\Omega$$

Over Temperature Protection (OTP)

We choose for temperature limitation at the absolute hot spot on our PCB: 115°C. So in the end we selected “B59701A0100A062” from EPCOS.

Note:
C_{11} is a filter capacitor and has a fixed value of 22nF / 50V

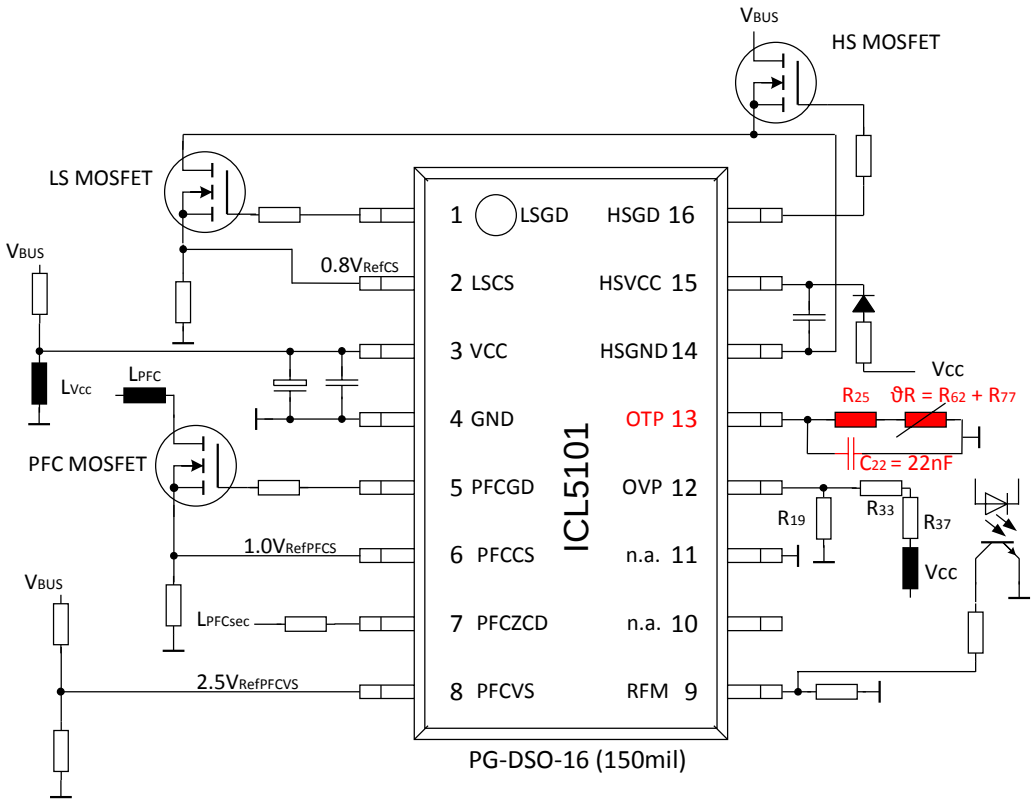

Figure 25 PIN Setup showing the Components in red

9 Reference

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Date	Version	Changed by	Change Description
2015.11.06	1.1		Adjustment to Design Tool V1.1

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