# Demystifying the Paralleling of IGBT Modules 

## Paralleling power devices is of general interest. It helps to increase the power rating of inverter systems very easily. Paralleling becomes even more essential for the new modular semiconductor concept of $X H P^{\mathrm{TM}} 2$ and $X H P^{\mathrm{TM}} 3$ which open up a new degree in flexibility.

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This type of module supports and simplifies the design of new converters by enabling an easy scalability of the output power. Besides the power module characteristics, the system and bus bar design, the routing of the load conductor and the gate-driver characteristics have significant impact on the current sharing between paralleled devices. A certain deviation of losses, resulting in different junction temperatures among the power modules, is the result. A current derating will be defined in order to operate the paralleled power modules safely within their specification.

Below, an analytical approach will be described, which, by means of key influential device parameters, provides e.g. the maximum deviation of switching losses dependent on the number of paralleled modules. By determining the maximum current imbalance and considering the safe-operating-area (SOA) limits, a corresponding derating can be defined.

## Design of experiments for $\mathbf{n = 2}$

In order to evaluate the most influential parameters a measurement DOE with two modules in parallel has been carried out to assess the collector-current mismatch and the difference of losses. The dependencies between device parameter deviations and resulting loss mismatches are summarized in figure 1.


Figure 1: Differences of switching losses for two modules in parallel with respect to the most influential parameters

$$
\begin{align*}
& \Delta E_{\text {rec }}=f\left(\Delta V_{F}\right)  \tag{1}\\
& \Delta E_{\text {on }}=f\left(\Delta V_{F}, \Delta V_{P}\right)  \tag{2}\\
& \Delta E_{\text {off }}=f\left(\Delta V_{C E}, \Delta t_{\text {dvoff }}\right) \tag{3}
\end{align*}
$$

The turn-off delay time $t_{\text {dvoff }}$ is the time between $90 \% \mathrm{~V}_{\mathrm{GE}}$ and $10 \%$ of the rising $\mathrm{V}_{\mathrm{CE}}$ during IGBT turn-off. The difference between two modules $\Delta \mathrm{t}_{\text {dvoff }}$ has only a slight impact on $\Delta \mathrm{E}_{\text {off }}$, but a significant impact regarding the safe operating area (SOA) of the IGBTs.


Figure 2: Difference in turn-off current DIcoff,dyn depending on the difference in turn-off delay time Dtdvoff

In figure 2 the difference in turn-off current $\Delta \mathrm{I}_{\text {coff,dyn }}$, i.e. the current at which $\mathrm{V}_{\mathrm{CE}}$ equals the DC-link voltage, is shown as a function of $\Delta \mathrm{t}_{\text {dvoff }}$, revealing an almost linear dependency. With increasing $\Delta \mathrm{t}_{\mathrm{dvoff}}$, the $\Delta \mathrm{I}_{\text {coff,dyn }}$ increases due to a voltage difference between the modules that leads to a circulating current and a corresponding current mismatch. In order to stay within the SOA, the $\Delta t_{\text {dvoff }}$ has to be limited.

The set of regression functions (1) to (3) describe the differences of dynamic losses for two modules switched in parallel. The differences in conduction losses are described by the differences in output characteristics of the IGBTs and diodes. With respect to the chosen values for the selection parameters $\Delta \mathrm{V}_{\mathrm{F}}, \Delta \mathrm{V}_{\mathrm{CE}}, \Delta \mathrm{V}_{\mathrm{P}}$ and $\Delta \mathrm{t}_{\text {dvoff }}$, and taking into account a certain duty cycle, thermal impedances and cooling conditions, the differences in total IGBT and diode losses as well as the junction temperatures can be calculated. Knowing the distribution of the parameters, they can be applied to a Monte-Carlo simulation, and their impact on switching and conduction losses quantified. Furthermore, the adherence of the SOA by mismatched currents can be verified.

## Analytical approach for $\mathrm{n} \geq 2$

Determining the current mismatch for paralleled modules with regard to their individual characteristics via a DoE is manageable as long as the number of paralleled devices is rather low. In order to predict the mismatch for multiple paralleled modules, an analytical approach is needed. A figure of merit $f_{X}(4)$ has been defined describing the devia-
tion for a given parameter $X$. $f_{X}$ reaches its maximum for the smallest $X_{\text {avg }}$ and the largest $\Delta X$. The minimum $X_{a v g}$ for $n$ modules is given by equation (5). (5) inserted into (4) results in (6), which is a universal equation for $f_{\text {Xmax }}$ in dependence of $n$. For $n \rightarrow \infty$, the limiting value is obtained according to (7). Figure 3 shows $f_{X \max }$ in dependence of $n$ for a difference of $5 \%$ and $10 \%$ between $X_{\max }$ and $X_{\min }$.

$$
\begin{align*}
& f_{X}=\frac{\Delta X}{X_{a v g}}=\frac{X_{\max }-X_{a v g}}{X_{a v g}}  \tag{4}\\
& X_{a v g}=\frac{X_{\max }+(n-1) \cdot X_{\min }}{n}  \tag{5}\\
& f_{X \max }=\frac{X_{\max }-X_{\min }}{X_{\min }+\frac{X_{\max }}{n-1}}  \tag{6}\\
& f_{X \max }=\frac{X_{\max }-X_{\min }}{X_{\min }}
\end{align*}
$$



Figure 3: $f_{X \max }=f(n)$ describes the worst-case $f_{X}$ according to (4)
The on-state current mismatch between two modules is determined by characteristics, that schematically can be simplified to a voltage source $\left(V_{0}\right)$ connected in series to a resistance $\left(R_{d}\right)$. In case of a positive di/dt, the voltage drop across the corresponding leg inductances of the paralleled device results in a negative feedback. The higher the positive di/dt, the higher the inductive voltage drop, and therefore, the lower the mismatch. Negative di/dt will result in a positive feedback, however, declining currents in the on-state are in general less critical in terms of losses or SOA.

Hence, for a worst-case on-state scenario, the leg inductance is negligible. According to (6), the difference in on-state currents of $n$ modules reaches its maximum $f_{\text {imax }}$ if $(n-1)$ modules with $R_{d 1}=\ldots$ $=R_{d(n-1)}=R_{d m a x}$ are carrying a low current in parallel to a single module with $R_{d n}=R_{d m i n}$ carrying a higher current. (6) can be rewritten as (8), an expression that depends on the individual module currents and the number of paralleled modules $n$.

$$
\begin{equation*}
f_{i \max }=\frac{i_{\max }-i_{\min }}{i_{\min }+\frac{i_{\max }}{n-1}} \tag{8}
\end{equation*}
$$

$R_{d}$ and $V_{0}$ are sufficiently linear depending on the $V_{C E s a t}$ or $V_{F}$, and therefore can be obtained for differing on-state characteristics by a linear regression function. (8) delivers the maximum current mismatch for $n$ paralleled modules. According to figure 3 , the maximum current mismatch for $n=6$ modules and $\Delta i=i_{\max }{ }^{-i_{\min }}=10 \%$ amounts to $f_{i m a x} \approx 8 \%$. Assuming a typical selection of modules with various $R_{d}$ and $\mathrm{V}_{0}$ values, the individual module currents can be calculated ac-
cording to Kirchhoff's law, and the current mismatch $f_{i}$ is given by (4). Once the individual $R_{d}$ and $V_{0}$ have been determined, the mismatch of switching losses can be determined too.


Figure 4: a) Simplified on-state characteristics for two modules with different $V_{\text {CEsat }} ;$ b) Trade-off curve; c) $E_{\text {off }}=f(i C)$ for two modules with different $V_{\text {CEsat }}$

Figure 4a shows the output characteristics of two IGBTs with different $V_{C E s a t}$, i.e. with different $R_{d}$ and $V_{0}$. The difference in $V_{C E s a t}$ leads to different $E_{\text {off }}$ values due to their trade-off characteristics (figure $4 b$ ) at the same current, e.g. $I_{\text {Cnom. }}$. Hence, module-specific $E_{\text {off }}=f\left(i_{C}\right)$ values are obtained (figure 4c). By determining the worst-case module currents of the parallel IGBTs ( $\mathrm{i}_{\mathrm{Cmax}}$ and $\mathrm{i}_{\mathrm{Cmin}}$ ), also $\mathrm{E}_{\text {off,max }}$ and $\mathrm{E}_{\text {off,min }}$, hence $f_{\text {Eoff }}$ can be calculated.

This approach is sufficient as long as the desired value depends mainly on one variable. In this example, it has been assumed that $\mathrm{E}_{\text {off }}$ depends only on $V_{\text {CEsat }}$. This approach is also valid for determining $\Delta \mathrm{E}_{\text {rec }}$ and $\mathrm{f}_{\text {Erec }}$. Since $\Delta \mathrm{E}_{\text {on }}$ depends on $\Delta \mathrm{V}_{\mathrm{F}}$ as well as $\Delta \mathrm{V}_{\mathrm{P}}$ (figure 1), a trade-off $E_{o n}=f\left(V_{F}, V_{P}\right)$ has to be considered for determining the appropriate relation $\mathrm{E}_{\mathrm{on}}=\mathrm{f}\left(\mathrm{i}_{\mathrm{C}}\right)$.


Figure 5: Correlation of $f_{\text {Eoff }}$ for $n=2$ modules of the analytical approach ( $x$ axis) and the regression function obtained by the DoE (y axis). The module parameters were diced randomly according to their distribution.

In figure 5, the correlation of fEoff for $\mathrm{n}=2$ of the regression function determined via the DoE and the analytical approach are shown. The slope is almost one, indicating a sufficient correlation and validity of the analytical approach. Nevertheless, the correlation reveals an increasing scattering for larger $\mathrm{f}_{\text {Eoff. }}$. This is due to the fact that the analytical approach does not consider the impact of $\Delta \mathrm{t}_{\text {dvoff }}$ on $\Delta \mathrm{E}_{\text {off }}$, which is rather low, but essential for the DoE regression function in order to
achieve a sufficiently good fit. Furthermore, the $\Delta t_{\text {dvoff }}$ has not been restricted to a certain value in the diced configuration of parameters, which is required in order to stay within a defined SOA.





Figure 6: $f_{\text {Eoff }} f_{\text {Erec }}$ and $f_{\text {Eon }}$ calculated according to (4) for sets of six module

Secondary effects, such as a circulating current between paralleled devices during switching as an effect of $\mathrm{V}_{\mathrm{CE}}$ differences, cannot be considered. In measurements, they are inevitably included. Considering them is challenging, and would unnecessarily obstruct the simplicity of the suggested analytical approach.

## Probability of a worst-case set of $\mathbf{n}=\mathbf{6}$ modules

Based on end test data of XHP ${ }^{\text {TM }} 3$ half-bridge modules, the probability of occurrence for $\mathrm{f}_{\text {Eoff }}, \mathrm{f}_{\text {Erec }}$ and $\mathrm{f}_{\text {Eon }}$ has been calculated. A worst-case set of e.g. six modules is obtained, when $f_{X}$ in (4) reaches the maximum, i.e. five modules have a $\mathrm{V}_{\mathrm{CEsat}}$ or $\mathrm{V}_{\mathrm{F}}$ at the lower limit while the sixth module has a respective value at the upper limit. For the selection criteria applied here, data of sets of six XHP 3 halfbridge modules were investigated. $\mathrm{f}_{\text {Eoff }}, \mathrm{f}_{\mathrm{Erec}}$ and $\mathrm{f}_{\text {Eon }}$ are calculated and depicted in figure 6. The respective values on the x-axis are given in \%. The analysis reveals that the difference in switching losses within the sets of six modules is always $<10 \%$. Since the losses are distributed similar to that of a Gaussian distribution, it is possible to define an upper limit for $f X$ to fulfil a probability of occurrence, e.g. $\leq 100 \mathrm{ppm}$. For the data shown, this is fulfilled for $\mathrm{f}_{\text {Eoff }} \leq 11.6 \%$, $\mathrm{f}_{\text {Erec }} \leq 9.4 \%$ and $\mathrm{f}_{\text {Eon }} \leq 8.4 \%$.
Beside the deviations in device characteristics, the surrounding conditions like DC busbar symmetry, placement of the load cable, gate-drive parasitics, or the cooling concept can have an impact on the mismatch among the paralleled devices. They should be carefully evaluated as well.

## Summary

By means of a DoE, the most influential parameters describing the differences in module behavior due to paralleling have been determined. Besides the differences in on-state characteristics which impact static current sharing, differences in switching delay time have to be considered to comply with the SOA. All differences in voltage between paralleled devices, either in on-state or during switching, provoke current imbalances due to circulating currents among the modules. An analytical approach has enabled us to predict the behavior of multiple devices connected in parallel, and to define selection criteria to ensure the reliable use of paralleled modules. Infineon XHP ${ }^{\text {тм }}$ devices for paralleling are grouped and supplied according to these criteria.
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