15 W 12 V 5 V SMPS demo board with ICE5QR4780BG

DEMO_5QR4780BG_15W1

About this document

Scope and purpose

This document is an engineering report that describes a universal-input 15 W 12 V 5 V off-line Flyback converter using the latest fifth-generation Infineon Quasi-Resonant (QR) CoolSET™ ICE5QR4780BG, which offers high-efficiency, low-standby power with selectable entry and exit standby power option, wide V_{CC} operating range with fast start-up, robust line protection with input Over-Voltage Protection (OVP) and brown-out and various protections for a highly reliable system. This demo board is designed for users who wish to evaluate the performance of ICE5QR4780BG and its ease-of-use.

Intended audience

This document is intended for power supply design/application engineers, students, etc., who wish to design low-cost and highly reliable systems for off-line SMPS, either auxiliary power supplies for white goods, PCs, servers and TVs, or enclosed adapters for Blu-ray players, set-top boxes, games consoles, etc.

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1 Abstract

This application note is an engineering report for the 15 W 12 V 5 V demo board designed in a QR Flyback converter topology using the fifth-generation QR CoolSET™, ICE5QR4780BG. The target applications of ICE5QR4780BG are either auxiliary power supplies for white goods, PCs, servers and TVs, or enclosed adapters for Blu-ray players, set-top boxes, games consoles, etc. With the CoolMOS™ integrated in this IC, it greatly simplifies the design and layout of the PCB. The improved new digital frequency reduction with proprietary QR operation offers lower EMI and higher efficiency for a wide AC range by reducing the switching frequency difference between low- and high-line. The enhanced Active Burst Mode (ABM) power enables flexibility in standby power operation range selection and QR operation during ABM. As a result, the system efficiency over the entire load range is significantly improved compared to conventional free-running QR converters implemented with only maximum switching frequency limitation at light load. In addition, numerous adjustable protection functions have been implemented in ICE5QR4780BG to protect the system and customize the IC for the chosen application. In case of failure modes, like brown-out or line over-voltage, V_{CC} over/under-voltage, open control-loop or over-load, output over-voltage, over-temperature, V_{CC} short-to-ground, the device enters protection mode. By means of the cycle-by-cycle Peak Current Limitation (PCL), the dimensions of the transformer and the current rating of the secondary diode can both be optimized. Thus, a cost-effective solution can be easily achieved.

2 Demo board

This document contains the list of features, power supply specifications, schematics, Bill of Material (BOM) and transformer construction documentation. Typical operating characteristics such as performance curve and scope waveforms are shown at the end of the report.

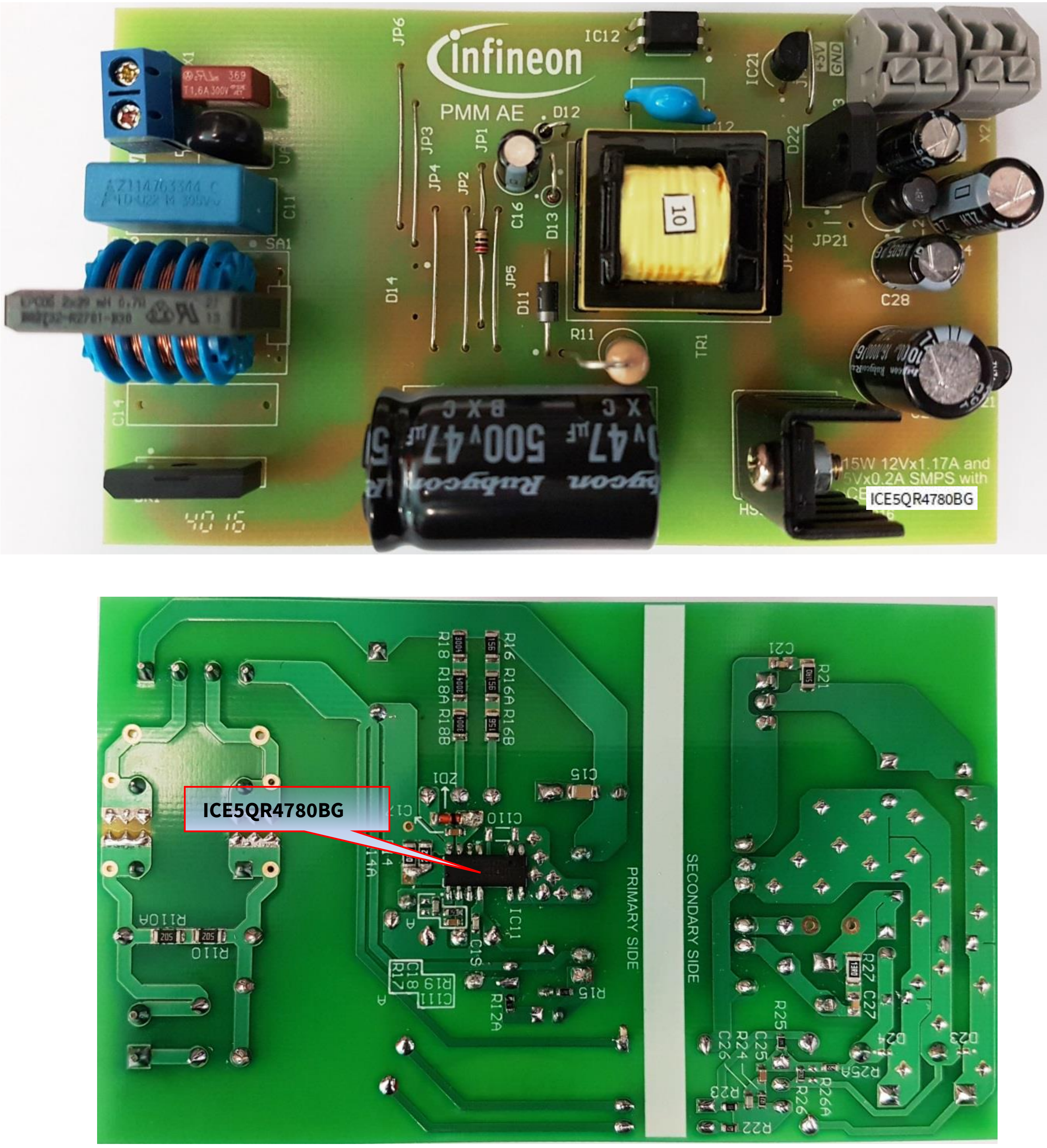


Figure 1 DEMO_5QR4780BG_15W1

3 Specifications of the demo board

Table 1 Specifications of DEMO_5QR4780BG_15W1

Input voltage and frequency	85 V AC (60 Hz) ~ 300 V AC (50 Hz)
Output voltage, current and power	(12 V x 1.16 A) + (5 V x 0.2 A) = 15 W
Dynamic load response (5 V at 0.2 A and 12 V load change from 10 percent to 100 percent, slew rate at 0.4 A/µs, 100 Hz)	±5 percent of nominal output voltage
Output ripple voltage (full load, 85 V AC ~ 300 V AC)	5 $V_{ripple\_p\_p}$ less than 100 mV 12 $V_{ripple\_p\_p}$ less than 100 mV
Active-mode four-point average efficiency (25 percent, 50 percent, 75 percent, 100 percent load)	More than 84 percent at 115 V AC and 230 V AC
No-load power consumption	Less than 100 mW at 230 V AC
Conducted emissions (EN 55022 class B)	Pass with 6 dB margin for 115 V AC and 6 dB margin for 230 V AC
ESD immunity (EN 61000-4-2)	Special level (±14 kV for contact and ±16 kV air discharge)
Surge immunity (EN 61000-4-5)	Installation class 4 (±2 kV for line-to-line and ±4 kV for line-to-earth)
Form factor case size (L x W x H)	(110 x 66 x 27) mm^3

Note: *The demonstrator board is designed for dual-output with cross-regulated loop feedback (FB). It may not regulate properly if loading is applied only to single-output. If the user wants to evaluate for single-output (12 V only) condition, the following changes are necessary on the board.*

1. Remove D22, L22, C28, C210, R25A (to disable 5 V output). 2. Change R26 to 10 kΩ and R25 to 38 kΩ (to disable 5 V FB and enable 100 percent weighted factor on 12 V output).

Since the board (especially the transformer) is designed for dual-output with optimized cross-regulation, single-output efficiency might not be optimized. It is only for IC functional evaluation under single-output condition.

4 Circuit description

4.1 Line input

The AC-line input side comprises the input fuse F1 as over-current protection. The choke L11, X-capacitor C11 and Y-capacitor C12 act as EMI suppressors. Optional spark-gap devices SA1, SA2 and varistor VAR can absorb HV stress during a lightning surge test. A rectified DC voltage (120 ~ 424 V DC) is obtained through the bridge rectifier BR1 together with bulk capacitor C13.

4.2 Start-up

To achieve fast and safe start-up, ICE5QR4780BG has been implemented with start-up resistor and V_{CC} short-to-GND protection. When V_{VCC} reaches the turn-on voltage threshold 16 V, the IC begins with a soft-start. The soft-start implemented in ICE5QR4780BG is a digital time-based function. The preset soft-start time is 12 ms with four steps. If not limited by other functions, the peak voltage on Current Sense (CS) pin will increase step by step from 0.3 V to 1 V finally. After the IC turns on, the V_{CC} voltage is supplied by auxiliary windings of the transformer. V_{CC} short-to-GND protection is implemented during the start-up time.

4.3 Integrated MOSFET and PWM control

ICE5QR4780BG is comprised of a power MOSFET and the proprietary new QR controller, which enables higher average efficiency and low EMI. This integrated solution greatly simplifies the circuit layout and reduces the cost of PCB manufacturing. The PWM switch-on is determined by the zero-crossing detection input signal and the value of the up/down counter. The PWM switch-off is determined by the FB signal V_{FB} and the CS signal V_{CS}. ICE5QR4780BG also performs all necessary protection functions in Flyback converters. Details about the information mentioned above are illustrated in the product datasheet.

4.4 RCD clamper circuit

A clamper network (R11, C15 and D11) dissipates the energy of the leakage inductance and suppresses ringing on the SMPS transformer.

4.5 Output stage

There are two outputs on the secondary side, 12 V and 5 V. The power is coupled out via Schottky diodes D21 and D22. The capacitors C22 and C28 provide energy buffering followed by the L-C filters L21-C24 and L22-C210 to reduce the output ripple and prevent interference between SMPS switching frequency and line frequency. Storage capacitors C22 and C28 are designed to have an internal resistance (ESR) as small as possible to minimize the output voltage ripple caused by the triangular current.

4.6 Feedback (FB) loop

For FB, the output is sensed by the voltage divider of R26, R25, R25A and compared to IC21 (TL431) internal reference voltage. C25, C26 and R24 comprise the compensation network. The output voltage of IC21 (TL431) is converted to the current signal via optocoupler IC12 and two resistors R22 and R23 for regulation control.

4.7 Primary-side peak-current control

The MOSFET drain-source current is sensed via external resistor R14 and R14A. Since ICE5QR4780BG is a current mode controller, it would have a cycle-by-cycle primary current and FB voltage control, which can ensure the maximum power of the converter is controlled in every switching cycle.

For a QR Flyback converter, the maximum possible output power is increased when a constant current limit value is used for all the line input voltage range. This is usually not desired as this will increase the cost of the transformer and output diode in case of output over-power conditions.

Internal current limitation with line-dependent V_{CS} curve and the proprietary new QR switching which reduces switching frequency difference between minimum and maximum line are implemented in the ICE5QR4780BG. As a result, the maximum output power can be easily limited versus the input voltage.

4.8 Digital frequency reduction

During normal operation, the switching frequency for ICE5QR4780BG is digitally reduced with decreasing load. At light load, the MOSFET will be turned on not at the first minimum drain-source voltage time, but on the n^{th}. The counter is in the range of 1 to 8 for low-line and 3 to 10 for high-line, which depends on FB voltage in a time-base. The FB voltage decreases when the output power requirement decreases, and vice versa. Therefore, the counter is set by monitoring voltage V_{FB}. The counter will be increased with low V_{FB} and decreased with high V_{FB}. The thresholds are preset inside the IC.

4.9 Active Burst Mode (ABM)

ABM entry and exit power (two levels) can be selected in ICE5QR4780BG. Details are illustrated in the product datasheet. ABM power level 1 is used in this demo board (R17 = open). At light-load condition, the SMPS enters into ABM with QR switching. At this stage, the controller is always active but the V_{VCC} must be kept above the switch-off threshold. During ABM, the efficiency increases significantly and at the same time it supports low ripple on V_{out} and fast response on load jump.

For determination of entering ABM operation, three conditions apply:

1. The FB voltage is lower than the threshold of V_{FB_EBLX}
2. The up/down counter is 8 for low-line and 10 for high-line, and
3. A certain blanking time (t_{FB_BEB} = 20 ms)

Once all of these conditions are fulfilled, the ABM flip-flop is set and the controller enters ABM operation. This multi-condition determination for entering ABM operation prevents mis-triggering of ABM, so that the controller enters ABM only when the output power is really low during the preset blanking time.

During ABM, the maximum CS voltage is reduced from V_{CS_N} to V_{CS_BLX} so as to reduce the conduction loss and the audible noise. In ABM, the FB voltage is changing like a sawtooth between V_{FB_BOFF} and V_{FB_BON}.

The FB voltage immediately increases if there is a high load jump. This is observed by one comparator. As the current limit is 31/35 percent during ABM a certain load is needed so that FB voltage can exceed V_{FB_LB}. After leaving ABM, maximum current can now be provided to stabilize V_{out}. In addition, the up/down counter will be set to 1 (low-line) or 3 (high-line) immediately after leaving ABM. This is helpful to decrease the output voltage undershoot.

5 Protection features

Protection is one of the major factors to determine whether the system is safe and robust. Therefore, sufficient protection is necessary. ICE5QR4780BG provides a comprehensive protection to ensure the system is operating safely. The protections include line over-voltage, brown-out, V_{CC} over-voltage and under-voltage, over-load, output over-voltage, over-temperature (controller junction) and V_{CC} short-to-GND. When those faults are found, the system will enter protection mode. Once the fault is removed, the system resumes normal operation. A list of protections and failure conditions are shown in the table below.

Table 2 Protection functions of ICE5QR4780BG

Protection function	Failure condition	Protection mode
Line over-voltage	V_{VIN} more than 2.9 V	Non-switch auto-restart
Brown-out	V_{VIN} less than 0.4 V	Non-switch auto-restart
V_{CC} over-voltage	V_{VCC} more than 25.5 V	Odd-skip auto-restart
V_{CC} under-voltage	V_{VCC} less than 10 V	Auto-restart
Over-load	V_{FB} more than 2.75 V and lasts for 30 ms	Odd-skip auto-restart
Output over-voltage	V_{ZCD} more than 2 V and lasts for 10 consecutive pulses	Odd-skip auto-restart
Over-temperature (junction temperature of controller chip only)	T_J more than 140°C with 40°C hysteresis to reset	Non-switch auto-restart
V_{CC} short-to-GND (V_{VCC} = 0 V, $R_{StartUp}$ = 50 MΩ and V_{DRAIN} = 90 V)	V_{VCC} less than 1.1 V, $I_{VCC\_Charge1}$ ≈ 0.2 mA	Cannot start up

6 Circuit diagram

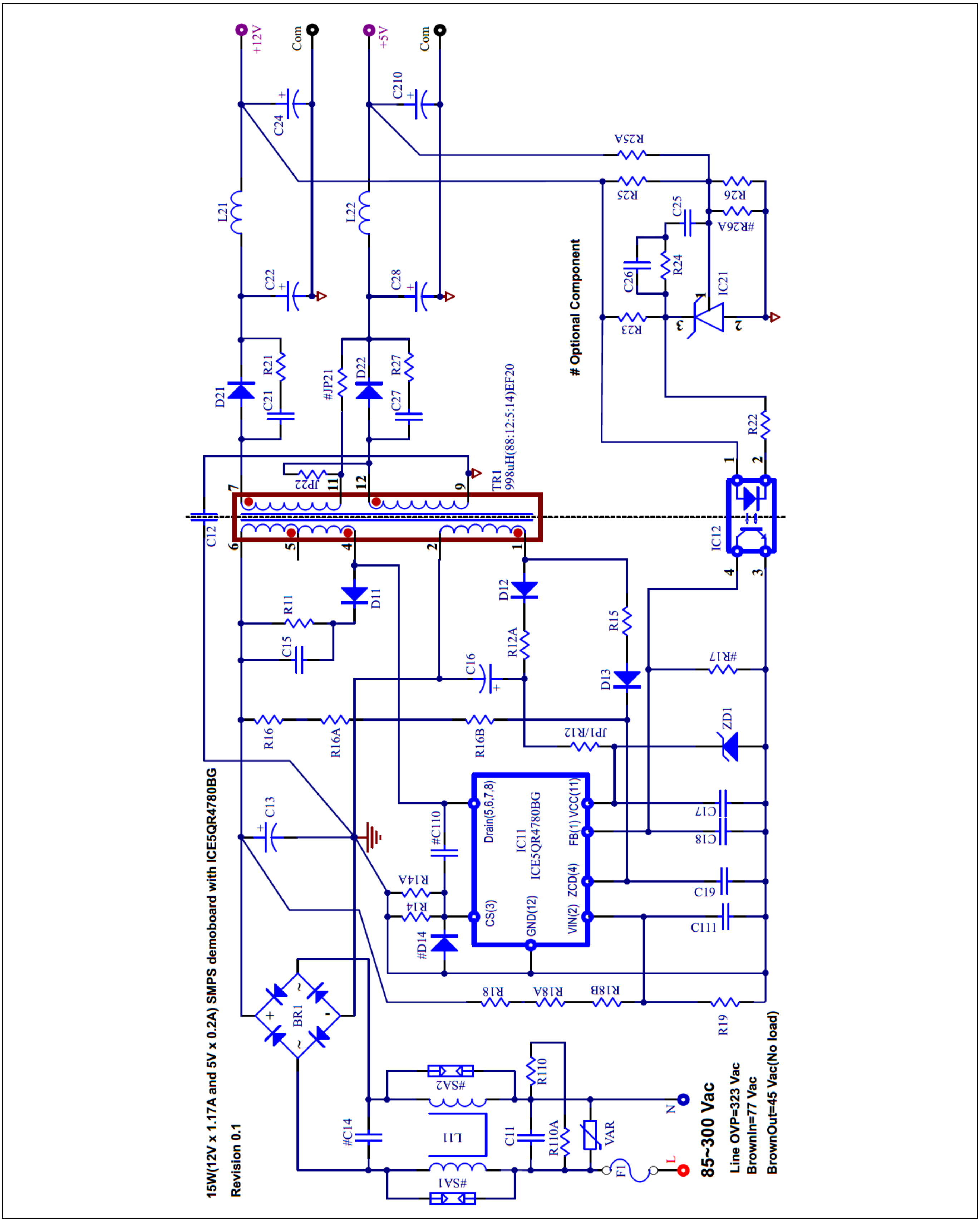


Figure 2 Schematic of DEMO_5QR4780BG_15W1

Note: General guideline for layout design of printed circuit board (PCB):

1. *Star ground at bulk capacitor C13: all primary grounds should be connected to the ground of bulk capacitor C13 separately in one point. It can reduce the switching noise going into the sensitive pins of the CoolSET™ device effectively. The primary star ground can be split into four groups as follows:*
    i. *Combine signal (all small-signal grounds connecting to the CoolSET™ GND pin such as filter capacitor ground C17, C18, C19, C111 and optocoupler ground) and power ground (CS resistor R14 and R14A)*
    ii. *V_{CC} ground includes the V_{CC} capacitor ground C16 and the auxiliary winding ground, pin 2 of the power transformer*
    iii. *EMI return ground includes Y capacitor C12*
    iv. *DC ground from bridge rectifier, BR1*
2. *Filter capacitor close to the controller ground: filter capacitors, C17, C18, C19 and C111 should be placed as close to the controller ground and the controller pin as possible so as to reduce the switching noise coupled into the controller.*
3. *High-voltage traces clearance: high-voltage traces should be spaced far enough apart from nearby traces. Otherwise, arcing could occur.*
    i. *400 V traces (positive rail of bulk capacitor C13) to nearby trace: more than 2.0 mm*
    ii. *600 V traces (drain voltage of CoolSET™ IC11) to nearby trace: more than 2.5 mm*
4. *Recommended minimum 232 mm^2 copper area at drain pin to add on PCB for better thermal performance.*
5. *Power loop area (bulk capacitor C13, primary winding of the transformer TR1 (pins 4 and 6), IC11 drain pin, IC11 CS pin and CS resistor R14/R14A) should be as small as possible to minimize the switching emissions.*

7 PCB layout

7.1 Top side

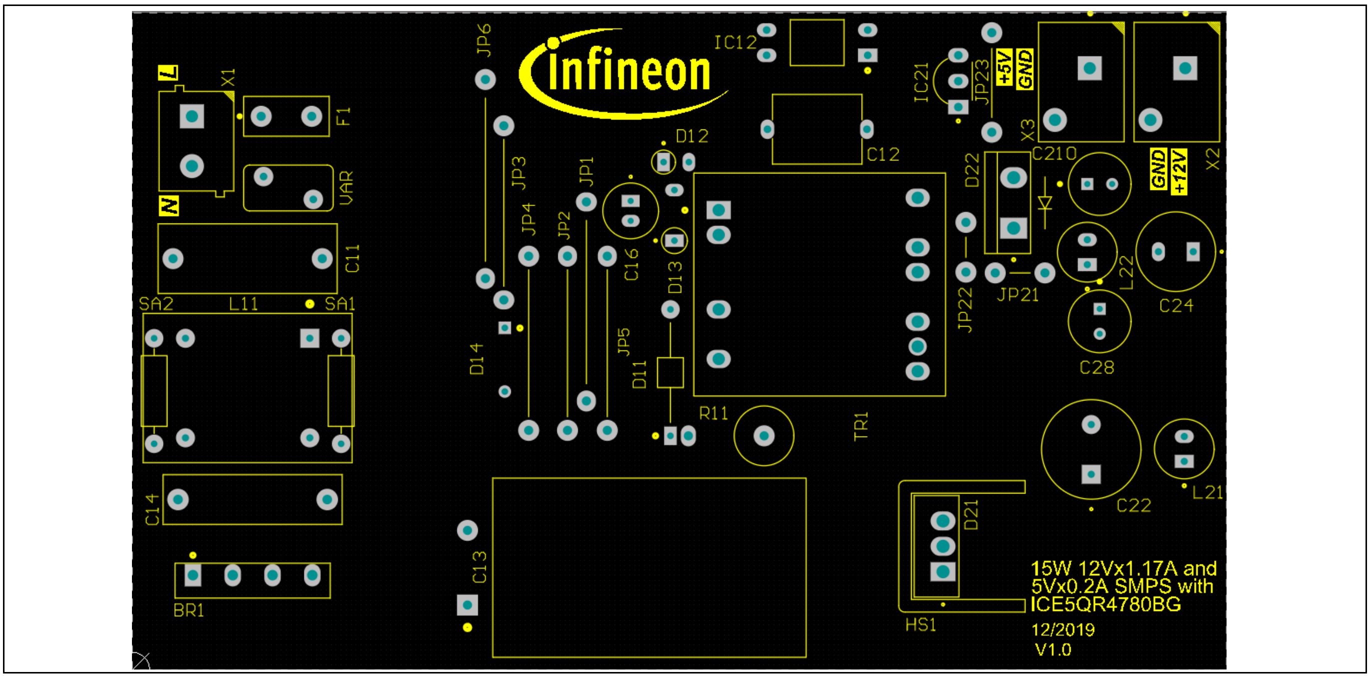


Figure 3 Top-side component legend

7.2 Bottom side

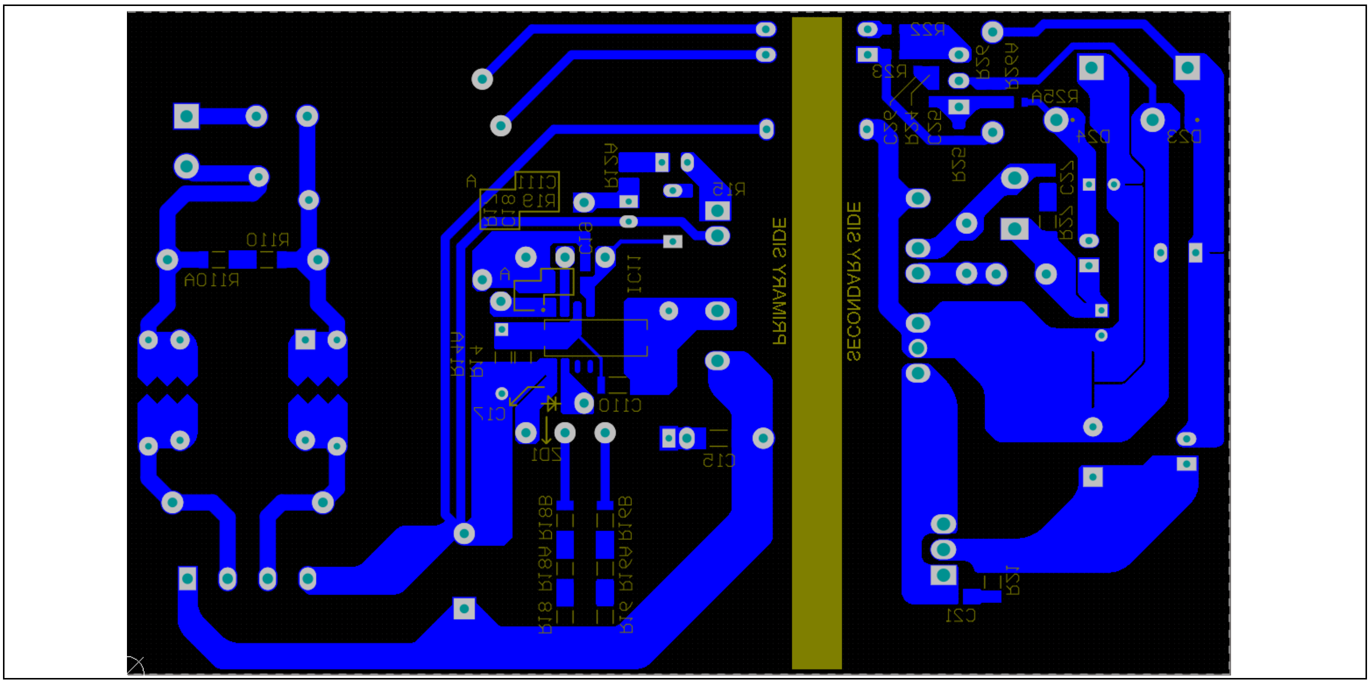


Figure 4 Bottom-side component legend

8 Bill of Materials (BOM)

Table 3 BOM

No.	Designator	Description	Part number	Manufacturer	Quantity
1	BR1	600 V/1 A	S1VBA60	Shindengen	1
2	C11	0.22 µF/305 V	B32922C3224	Epcos	1
3	C12	1 nF/500 V	DE1E3RA102MA4BQ	Murata	1
4	C13	47 µF/500 V	500BXC47MEFC18X31.5	Rubycon	1
5	C15	1 nF/1000 V	GRM31BR73A102KW01#	Murata	1
6	C16	22 µF/50 V	50PX22MEFC5X11	Rubycon	1
7	C17	100 nF/50 V	GRM188R71H104KA93D	Murata	1
8	C18, C26	1 nF/50 V	GRM1885C1H102GA01D	Murata	2
9	C19	120 pF/50 V	GRM1885C1H121GA01D	Murata	1
10	C111	22 nF/50 V	GCM188R71H223KA37D	Murata	1
11	C21, C27	1 nF/100 V	GRM2162C2A102JA01#	Murata	2
12	C22	1000 µF/16 V	16ZLH1000MEFC10X16	Rubycon	1
13	C24	470 µF/16 V	16ZLH470MEFC8X11.5	Rubycon	1
14	C25	220 nF/50 V	GRM188R71H224KAC4D	Murata	1
15	C28	330 µF/10 V	10ZLH330MEFC6.3X11	Rubycon	1
16	C210	330 µF/10 V	10ZLH330MEFC6.3X11	Rubycon	1
17	D11	1 A/800 V	UF4006		1
18	D12	0.2 A/200 V	1N485B		1
19	D13	0.2 A/150 V/50 ns	FDH400		1
20	D21	20 A/100 V	STPS20M100SFP		1
21	D22	10 A/45 V	VFT1045BP		1
22	F1	1.6 A/300 V	36911600000		1
23	HS21	Heatsink	577202B00000G		1
24	IC11	ICE5QR4780BG	ICE5QR4780BG	Infineon	1
25	IC12	Optocoupler	SFH617A-3		1
26	IC21	Shunt regulator	TL431BVLPG		1
27	JP2, JP3, JP4, JP5, JP6, JP22, JP23	Jumper			7
28	L11	39 mH/0.7 A	B82732R2701B030	Epcos	1
29	L21	2.2 µH/4.3 A (or 3.3 µH/4.0 A)	7447462022 (or 7447462033)	Wurth Electronics	1
30	L22	4.7 µH/4.2 A (or 6.8 µH/3.3A)	7447462047 (or 7447462068)	Wurth Electronics	1
31	R11	68 kR/2 W/350 V	ERG-2SJ683A	Panasonic	1
32	JP1/R12	27 Ω			1
33	R12A	0 Ω (0603)			1
34	R14	2.2 R/0.33 W/±1 percent	ERJ8BQF2R2V	Panasonic	1
35	R14A	2 R/0.33 W/±1 percent	ERJ8BQF2R0V	Panasonic	1
36	R15	27 k Ω ±1 percent (0603)			1
37	R16, R16A, R16B	15 MR/0.25 W/5 percent	RC1206JR-0715ML		3
38	R18, R18A, R18B	3 MR/0.25 W/1 percent	RC1206FR-073ML		3
39	R19	58.3 kR/0.1 W/0.5 percent	RT0603DRE0758K3L		1
40	R110, R110A	2 MΩ/5 percent/200 V	RC1206JR-072ML		2

41	R21	51 R/0.25 W/±1 percent	ERJ8ENF51R0V	Panasonic	1
42	R22	820 Ω (0603)			1
43	R23	1.2 kΩ (0603)			1
44	R24	12 kΩ (0603)			1
45	R25	16 kΩ (0603)			1
46	R25A	6.2 kΩ (0603)			1
47	R26	2.5 kΩ (0603)			1
48	R27	13 R/0.25 W/±1 percent	ERJ8ENF13R0V	Panasonic	1
49	TR1	998 µH	750343074(Rev 0.2)	Wurth Electronics	1
50	Test point of FB, V_{IN}, CS, ZCD, drain, V_{CC}, GND	Test point	5010		7
51	VAR	0.3 W/320 V	ERZE07A511	Panasonic	1
52	ZD1	22 V Zener			1
53	Con (L N)	Connector	691102710002	Wurth Electronics	1
54	Con (+12 V com), Con (+5 V com)	Connector	691 412 120 002B	Wurth Electronics	2

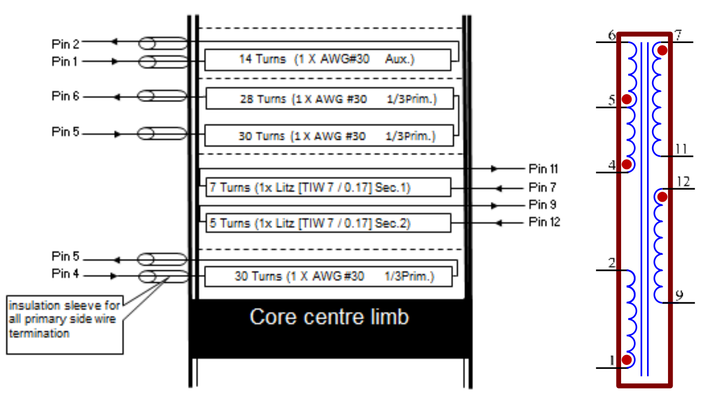
9 Transformer construction

Core and materials: EE20/10/6 (EF20), TP4A (TDG)

Bobbin: 070-5643 (14-pin, THT, horizontal version)

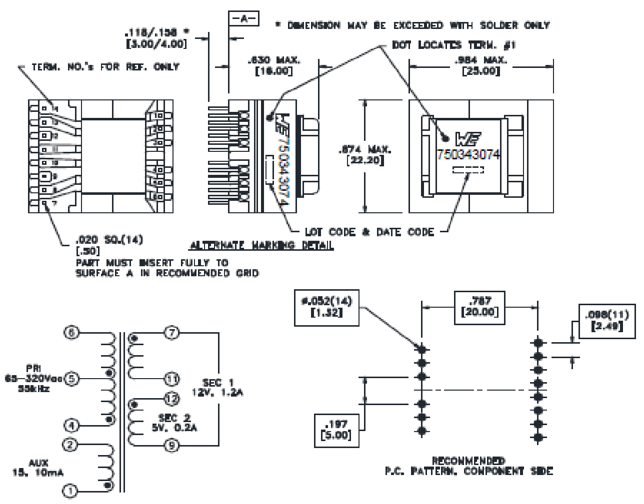
Primary inductance: Lp = 998 µH (±10 percent), measured between pin 4 and pin 6

Manufacturer and part number: Wurth Electronics Midcom (750343074)



Start	Stop	No. of turns	Wire size	Layer
4	5	30	1XAWG#30	1/3 Primary
12	9	5	1 x Litz [TIW 7 / 0.17]	Secondary 2
7	11	7	1 x Litz [TIW 7 / 0.17]	Secondary 1
5	6	58	1XAWG#30	2/3 Primary
1	2	14	1XAWG#30	Auxiliary

CUSTOMER TERMINAL	RoHS	LEAD(Pb)--FREE
Sn 96%, Ag 4%	Yes	Yes



ELECTRICAL SPECIFICATIONS @ 25° C unless otherwise noted:

PARAMETER		TEST CONDITIONS	VALUE
D.C. RESISTANCE	1-2	@20°C	0.250 ohms max.
D.C. RESISTANCE	4-6	@20°C	1.320 ohms max.
D.C. RESISTANCE	7-11	@20°C	0.040 ohms max.
D.C. RESISTANCE	12-9	@20°C	0.025 ohms max.
INDUCTANCE	4-6	50kHz, 100mV, Ls	998.0uH ±10%
LEAKAGE INDUCTANCE	4-6	tie(1+2+7+9+11+12),100kHz, 100mV, Ls	9uH typ., 15uH max.
DIELECTRIC	6-7	tie(2+4, 11+12), 3750VAC, 1 second	
DIELECTRIC	7-core	tie(11+12), 3750VAC, 1 second	
TURNS RATIO		(4-6):(1-2)	6.29:1, ±2%
TURNS RATIO		(4-6):(7-11)	12.57:1, ±2%
TURNS RATIO		(4-6):(12-9)	17.6:1, ±2%

GENERAL SPECIFICATIONS:

OPERATING TEMPERATURE RANGE: -40°C to +125°C including temp rise.

Designed to comply with the following requirements as defined by IEC60950-1, EN60950-1, UL60950-1/CSA60950-1 and AS/NZS60950.1:

- Reinforced Insulation for a primary circuit at a working voltage of 320Vrms, Overvoltage Category II.

Wire insulation & RoHS status not affected by wire color. Wire insulation color may vary depending on availability.

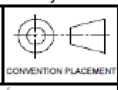
DFM		Packaging Specifications	 CONVENTION PLACEMENT	Tolerances unless otherwise specified:	DRAWING TITLE
DATE		Method: Tray		Angles: ±1° Decimals: ±.005 [.13]	TRANSFORMER
ENG	NWA	PKG-0736		Fractions: ±1/64 Footprint: ± .001 [.03]	PART NO. 750343074
REV.	02			This drawing is dual dimensioned. Dimensions in brackets are in millimeters.	SPECIFICATION SHEET 1 OF 1
DATE	2016-03-16				

Figure 5 Transformer structure

10 Test results

10.1 Efficiency, regulation and output ripple

Table 4 Efficiency, regulation and output ripple

Input (V AC/Hz)	P_{in} (W)	V_{out1} (V DC)	I_{out1} (A)	V_{ORPP1} (mV)	V_{out2} (V DC)	I_{out2} (A)	V_{ORPP2} (mV)	P_{out} (W)	Efficiency η (percent)	Average η (percent)	OLP P_{in} (W)	OLP I_{out12V} (Fixed 5 V at 0.2 A) (A)
85 V AC/ 60 Hz	0.043	4.92	0.000	10.9	12.16	0.000	44.8				25.18	1.52
	0.083	4.79	0.006	38.4	12.50	0.000	28.2	0.03				
	9.172	4.96	0.060	9.0	12.05	0.600	26.9	7.53	82.07			
	4.562	4.93	0.050	9.1	12.14	0.290	21.1	3.77	82.54	82.76		
	9.030	4.93	0.100	9.6	12.14	0.580	42.2	7.53	83.40			
	13.667	4.92	0.150	10.2	12.15	0.880	38.4	11.43	83.60			
	18.620	4.93	0.200	11.5	12.13	1.170	41.6	15.18	81.51			
115 V AC/ 60 Hz	0.046	4.92	0.000	10.9	12.16	0.000	46.7				27.97	1.79
	0.092	4.79	0.006	38.4	12.50	0.000	26.9	0.03				
	8.973	4.96	0.060	8.3	12.06	0.600	31.4	7.53	83.96			
	4.563	4.93	0.050	8.3	12.13	0.290	18.6	3.76	82.49	83.16		
	9.018	4.94	0.100	8.3	12.10	0.580	22.4	7.51	83.30			
	13.692	4.94	0.150	9.0	12.11	0.880	21.3	11.40	83.24			
	18.142	4.93	0.200	8.3	12.12	1.170	24.3	15.17	83.60			
230 V AC/ 50 Hz	0.071	4.92	0.000	11.5	12.17	0.000	49.9				28.68	1.87
	0.118	4.79	0.006	30.1	12.51	0.000	21.1	0.03				
	9.020	4.96	0.060	10.2	12.05	0.600	27.5	7.53	83.45			
	4.612	4.94	0.050	10.2	12.12	0.290	44.8	3.76	81.57	83.35		
	9.050	4.93	0.100	9.6	12.13	0.580	32.6	7.53	83.19			
	13.580	4.93	0.150	10.2	12.15	0.880	38.4	11.43	84.18			
	17.970	4.94	0.200	9.6	12.13	1.170	30.1	15.18	84.47			
265 V AC/ 50 Hz	0.083	4.92	0.000	12.8	12.17	0.000	49.3				29.57	1.95
	0.131	4.78	0.006	41.0	12.52	0.000	30.7	0.03				
	9.161	4.96	0.060	10.2	12.05	0.600	27.0	7.53	82.17			
	4.672	4.94	0.050	10.2	12.11	0.290	43.5	3.76	80.46	82.52		
	9.151	4.93	0.100	9.6	12.13	0.580	32.6	7.53	82.27			
	13.670	4.93	0.150	10.2	12.13	0.880	36.5	11.41	83.50			
	18.087	4.93	0.200	9.6	12.12	1.170	30.7	15.17	83.85			
300 V AC/ 50 Hz	0.098	4.92	0.000	12.8	12.17	0.000	50.6				30.35	1.99
	0.139	4.79	0.006	39.0	12.50	0.000	30.1	0.03				
	9.215	4.96	0.060	9.6	12.06	0.600	28.8	7.53	81.75			
	4.868	4.93	0.050	10.2	12.16	0.290	23.7	3.77	77.50	81.20		
	9.267	4.94	0.100	9.6	12.12	0.580	32.0	7.52	81.19			
	13.806	4.93	0.150	10.2	12.14	0.880	35.8	11.42	82.74			
	18.192	4.94	0.200	10.2	12.12	1.170	30.1	15.17	83.38			

Minimum load condition : 5 V at 6 mA

Typical load condition : 5 V at 60 mA and 12 V at 0.6 A

Maximum load condition : 5 V at 200 mA and 12 V at 1.17 A

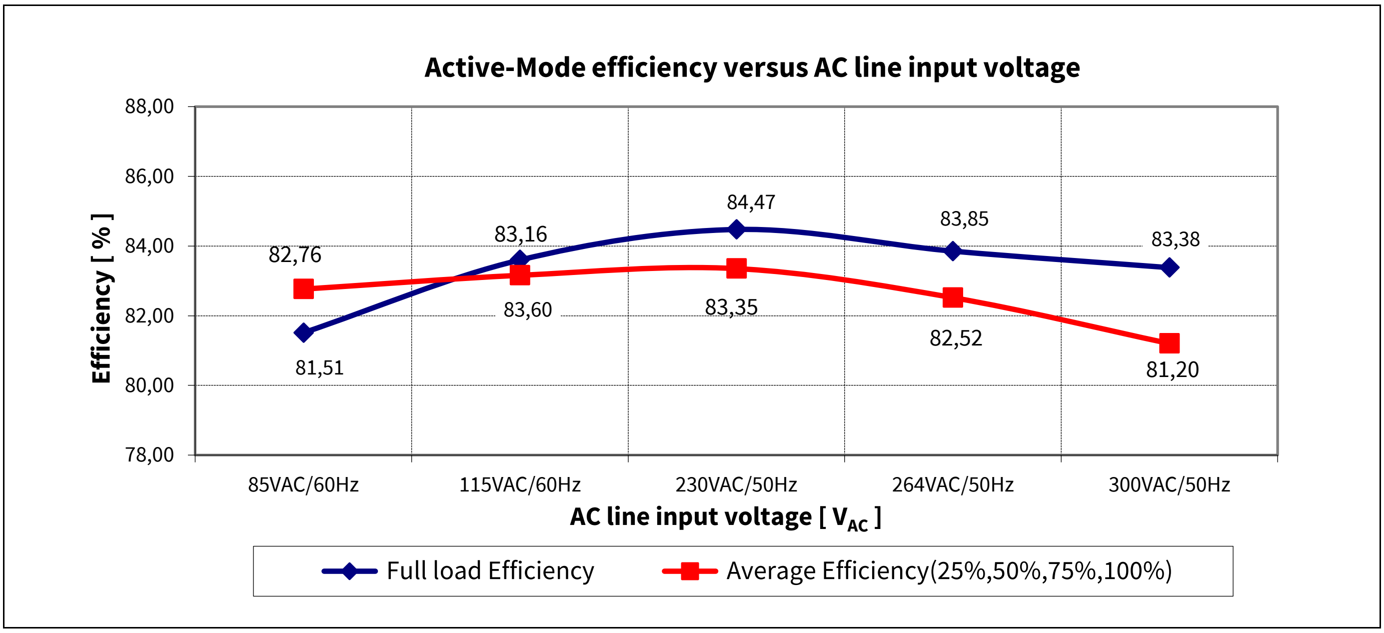


Figure 6 Efficiency vs. AC-line input voltage

10.2 Standby power

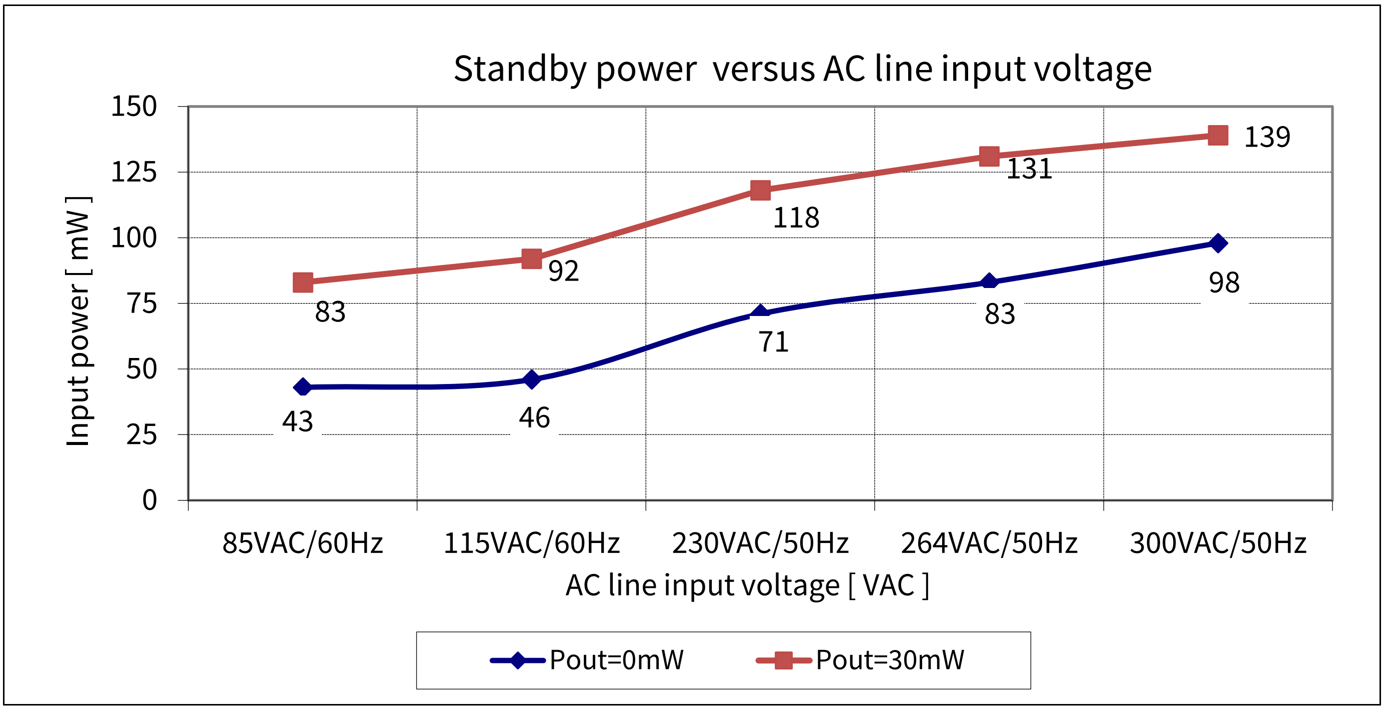


Figure 7 Standby power at no load and 30 mW load vs. AC-line input voltage (measured by Yokogawa WT210 power meter – integration mode)

10.3 Line regulation

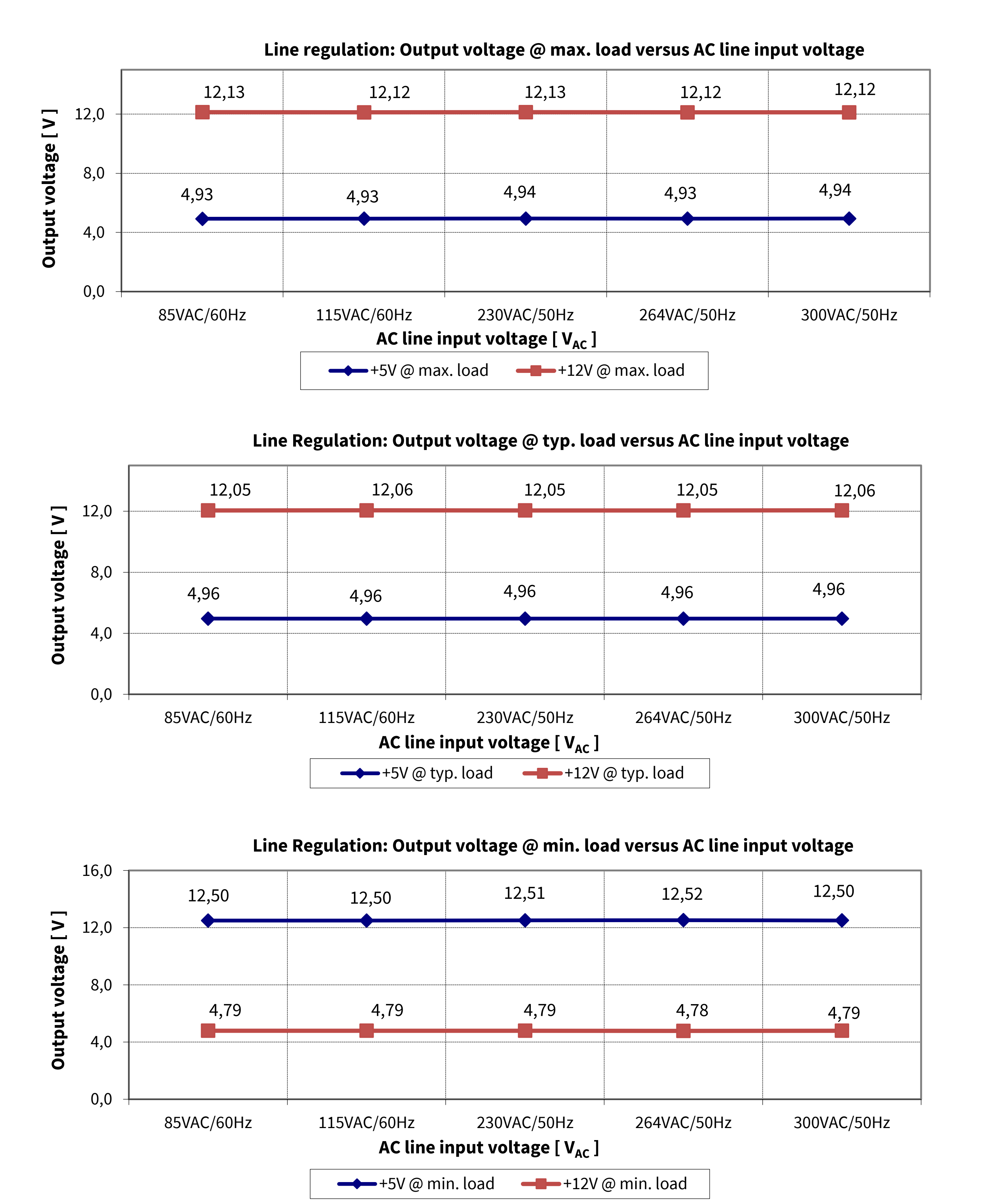


Figure 8 Line regulation V_{out} at full load vs AC-line input voltage

10.4 Load regulation

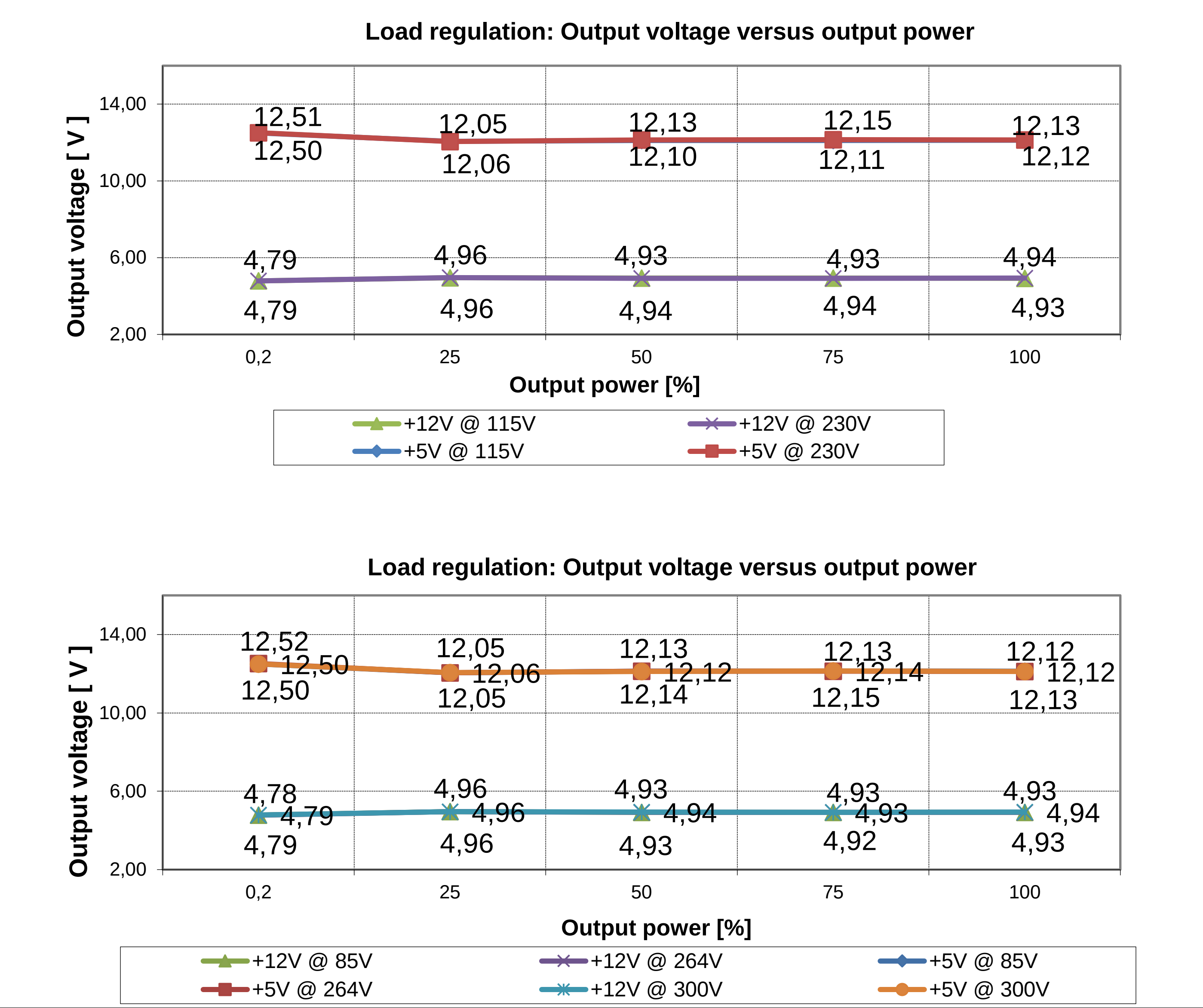


Figure 9 Load regulation V_{out} vs. output power

10.5 Maximum input power

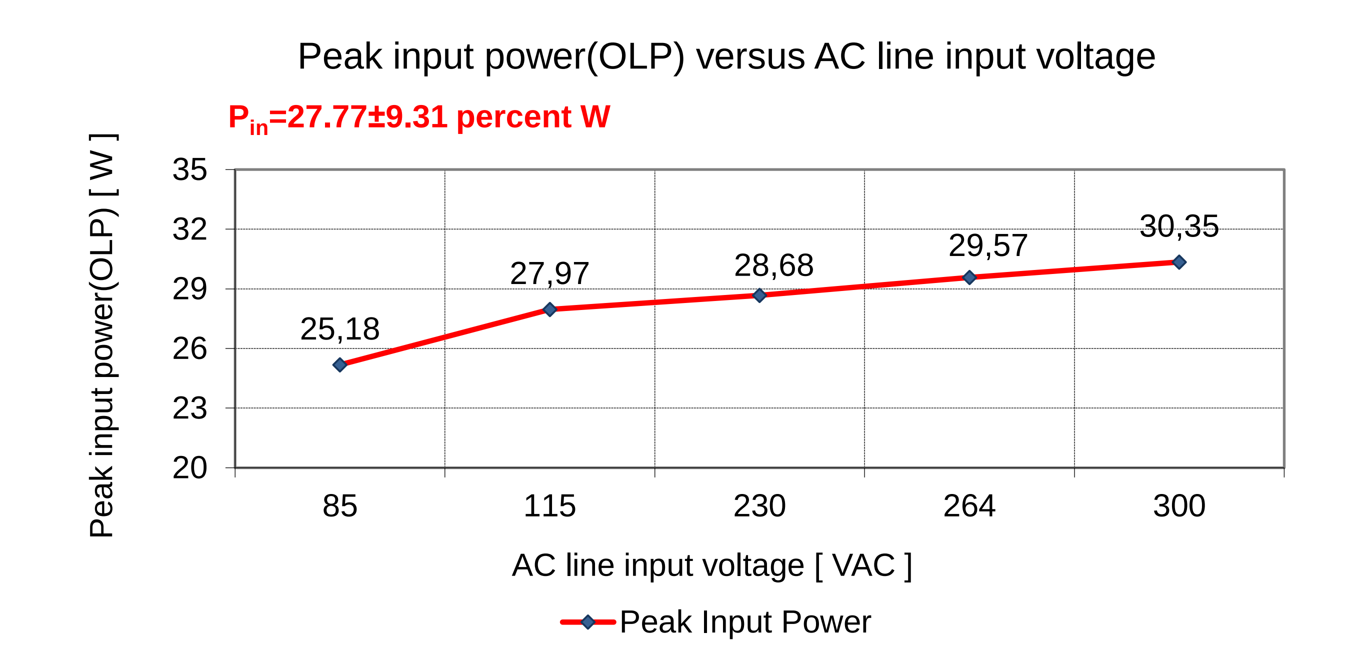


Figure 10 Maximum input power (before over-load protection) vs. AC-line input voltage

10.6 ESD immunity (EN 61000-4-2)

Pass EN 61000-4-2 special level (±14 kV for contact discharge and (±16 kV air discharge).

10.7 Surge immunity (EN 61000-4-5)

Pass EN 61000-4-5 installation class 4 (±2 kV for line-to-line and ±4 kV for line-to-earth).[1]

10.8 Conducted emissions (EN 55022 class B)

The conducted EMI was measured by Schaffner (SMR4503) and followed the test standard of EN 55022 (CISPR 22) class B. The demo board was set up at maximum load (15 W) with input voltage of 115 V AC and 230 V AC.

[1] PCB spark gap distance needs to reduce to 0.5 mm and C13 change to 120 µF.

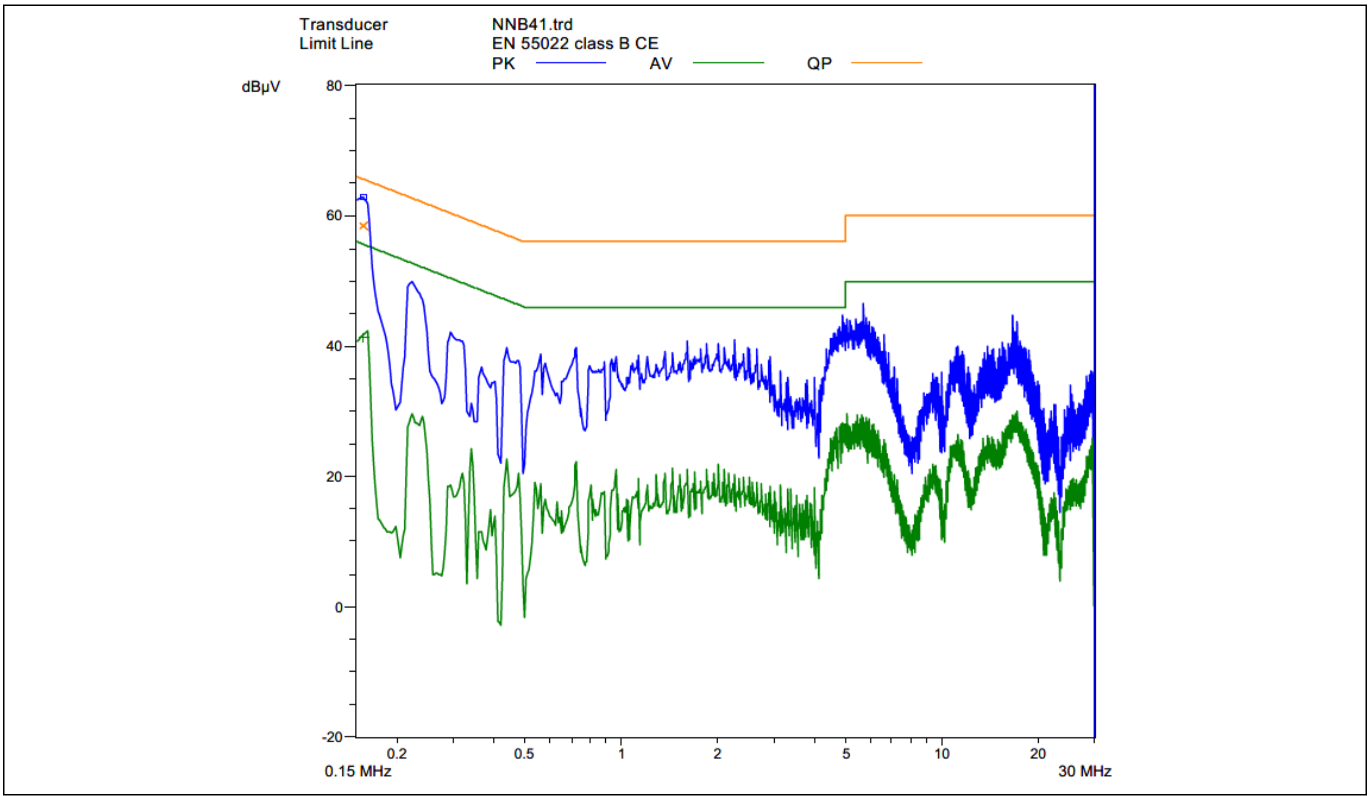


Figure 11 Conducted emissions (line) at 115 V AC and maximum load

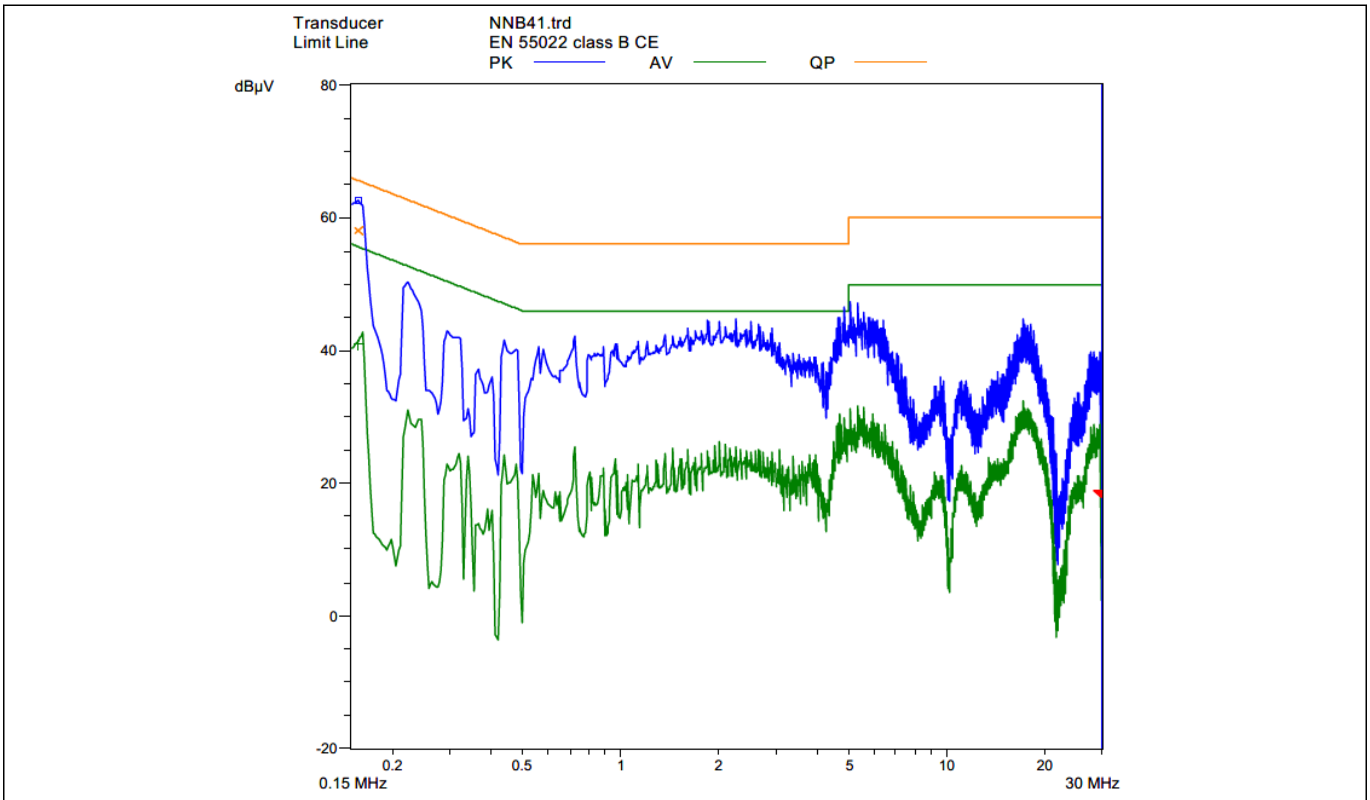


Figure 12 Conducted emissions (neutral) at 115 V AC and maximum load

Pass conducted emissions EN 55022 (CISPR 22) class B with 6 dB margin for quasi-peak measurement at low-line (115 V AC).

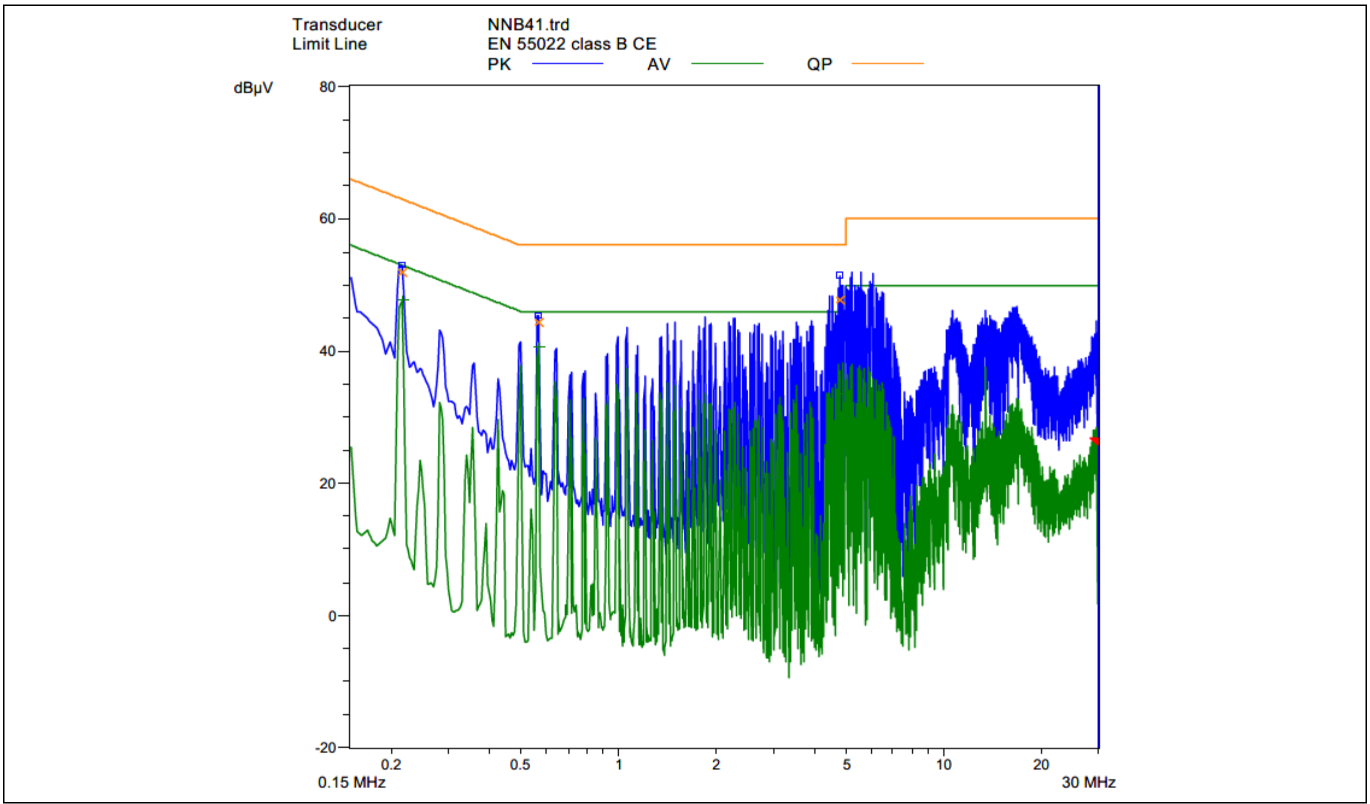


Figure 13 **Conducted emissions (line) at 230 V AC and maximum load**

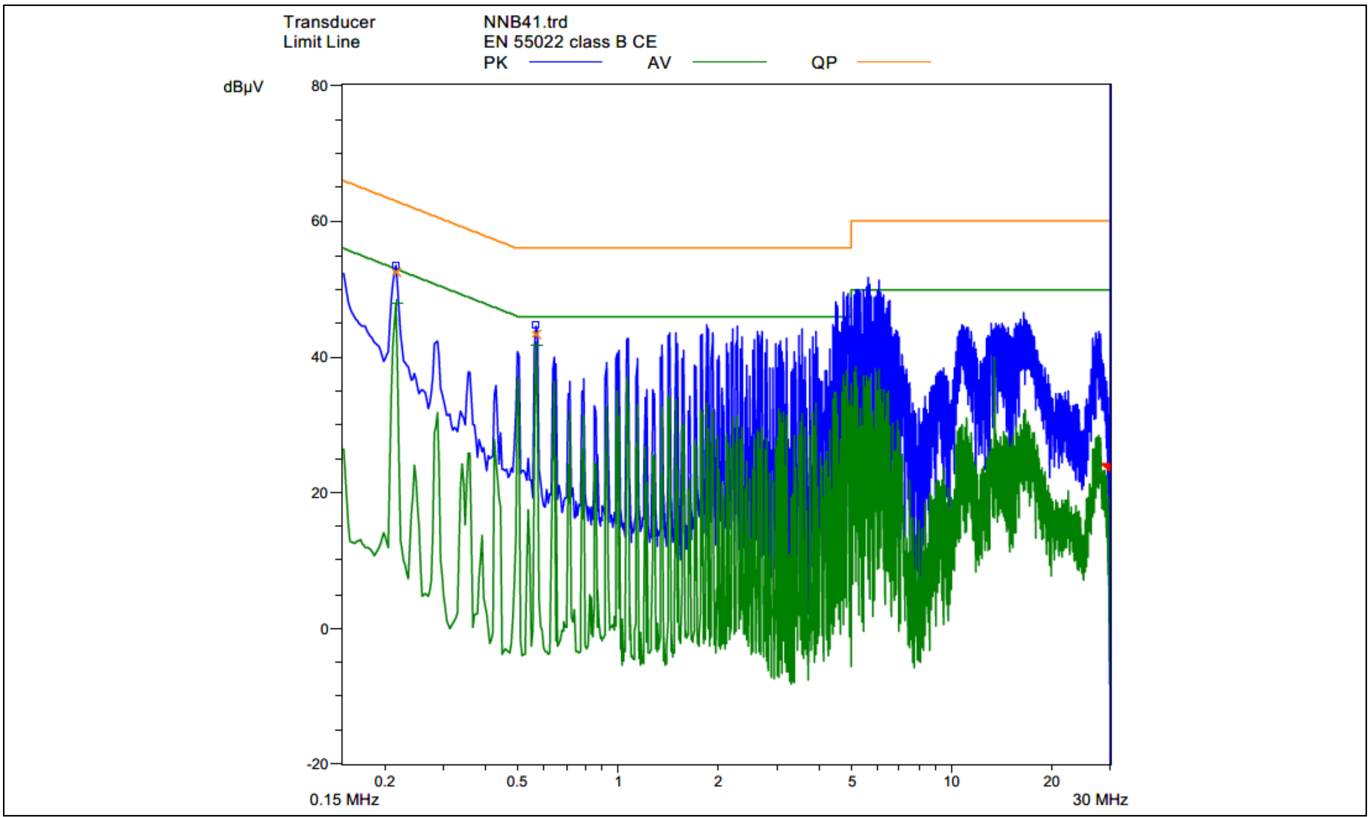


Figure 14 **Conducted emissions (neutral) at 230 V AC and maximum load**

Pass conducted emissions EN 55022 (CISPR 22) class B with 6 dB margin for quasi-peak measurement at high-line (230 V AC).

10.9 Thermal measurement

The thermal test of the open-frame demo board was done using an infrared thermography camera (FLIR-T62101) at ambient temperature 25°C. The measurements were taken after one hour running at full load.

Table 5 Hottest temperature of demo board

No.	Major component	85 V AC (°C)	300 V AC (°C)
1	IC11 (ICE5QR4780BG)	75.9	54.9
2	R14A (CS resistor)	49.6	43.5
3	TR1 (transformer)	51.7	61.3
4	BR1 (bridge diode)	46.8	30.5
5	R11 (clamper resistor)	49.1	51.3
6	L11 (choke)	43.8	28.7
7	D21 (secondary diode)	43.9	50.8
8	D22 (secondary diode)	37.4	40.3
9	Ambient	25.0	25.0

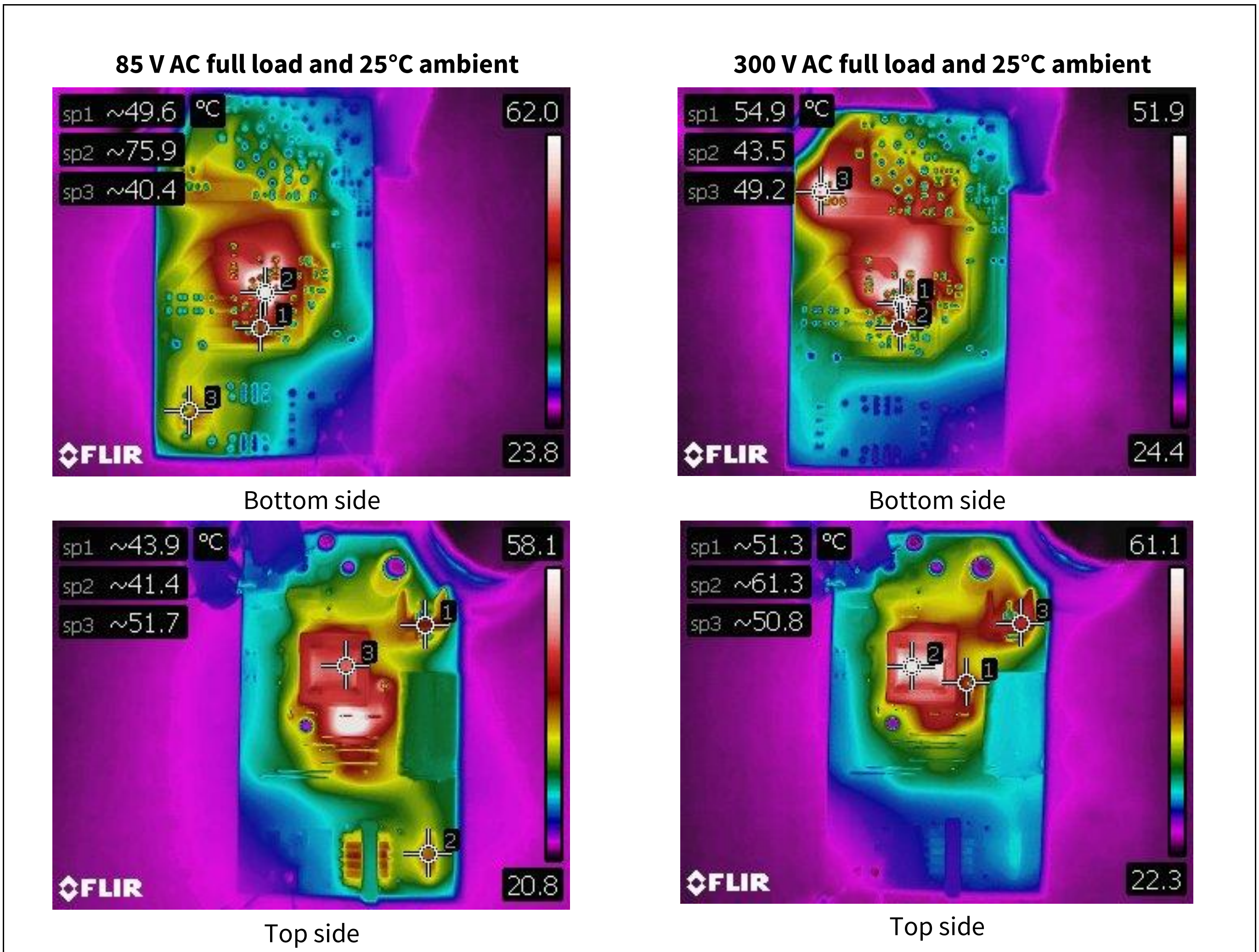
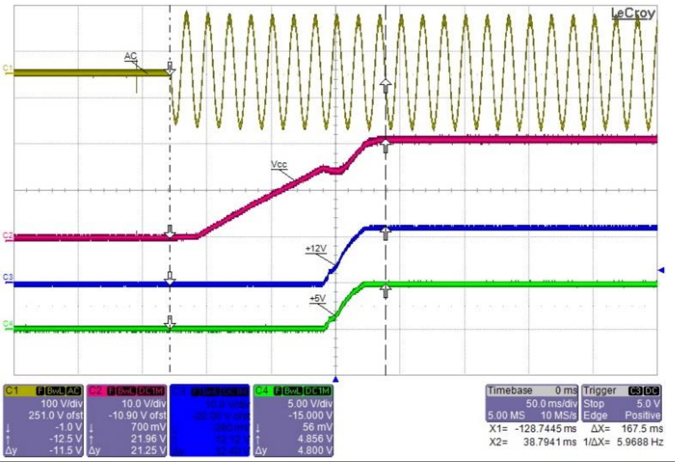


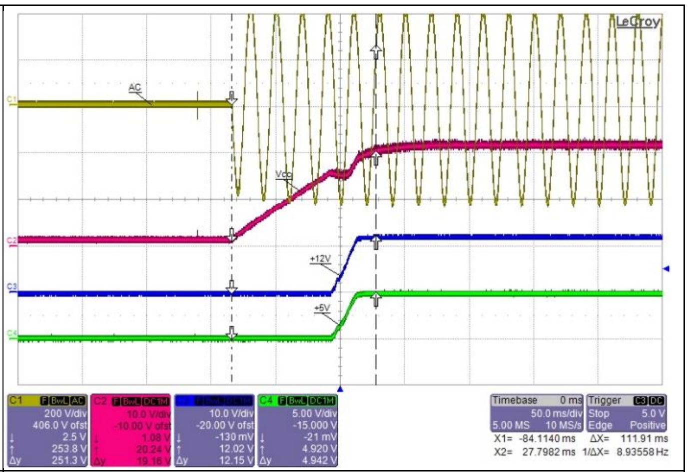
Figure 15 Infrared thermal image of DEMO_5QR4780BG_15W1

11 Waveforms and scope plots

All waveforms and scope plots were recorded with a Teledyne LeCroy 606Zi oscilloscope.

11.1 Start up at low/high AC-line input voltage with maximum load

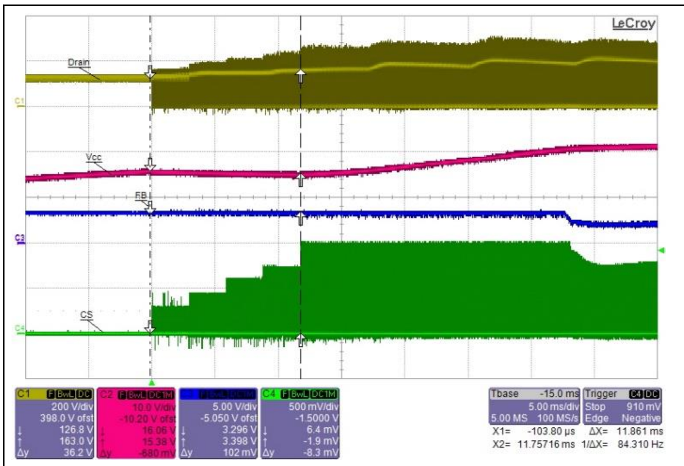


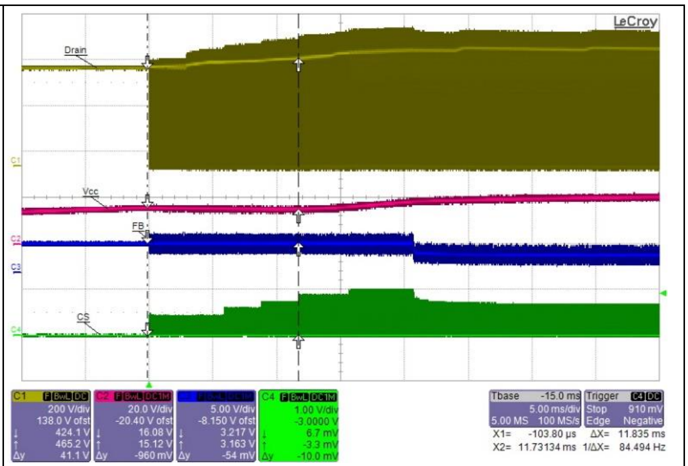


C1 (yellow) : AC-line voltage (V AC) C2 (purple) : Supply voltage (V_{VCC}) C3 (blue) : 12 V output voltage (V_{out12}) C4 (green) : 5 V output voltage (V_{out5})	C1 (yellow) : AC-line voltage (V AC) C2 (purple) : Supply voltage (V_{VCC}) C3 (blue) : 12 V output voltage (V_{out12}) C4 (green) : 5 V output voltage (V_{out5})
Start-up time at 85 V AC and maximum load ≈ 168 ms	Start-up time at 300 V AC and maximum load ≈ 112 ms

Figure 16 Start-up

11.2 Soft-start





C1 (yellow) : Drain voltage (V_D) C2 (purple) : Supply voltage (V_{VCC}) C3 (blue) : FB voltage (V_{FB}) C4 (green) : CS voltage (V_{CS})	C1 (yellow) : Drain voltage (V_D) C2 (purple) : Supply voltage (V_{VCC}) C3 (blue) : FB voltage (V_{FB}) C4 (green) : CS voltage (V_{CS})
Soft-start time at 85 V AC and maximum load ≈ 12 ms	Soft-start time at 300 V AC and maximum load ≈ 12 ms

Figure 17 Soft-start

11.3 Drain and Current Sense (CS) voltage at maximum load

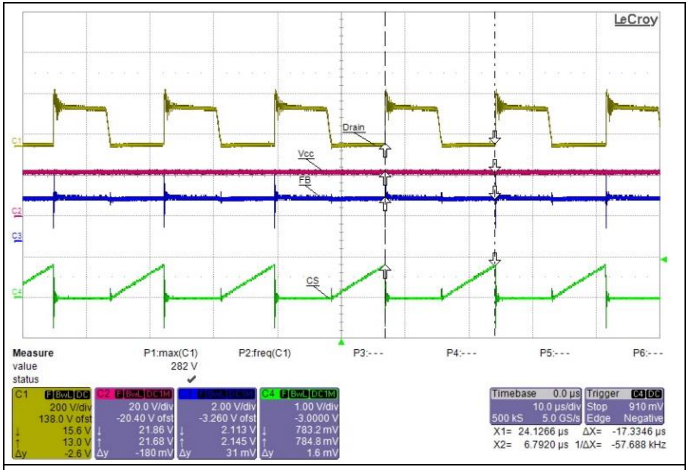
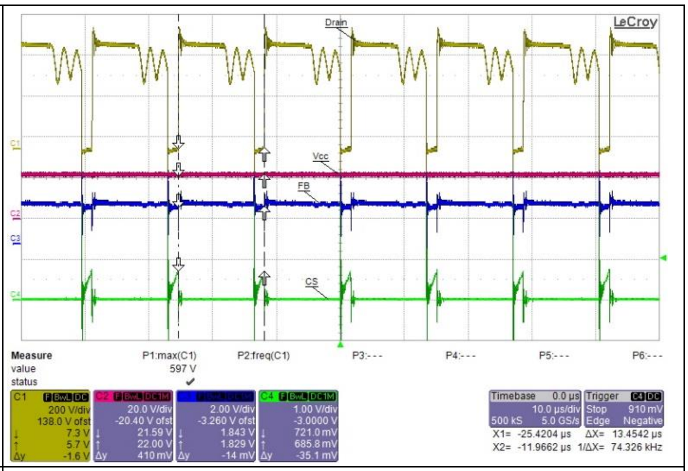
	
C1 (yellow) : Drain voltage (V_D) C2 (purple) : Supply voltage (V_{VCC}) C3 (blue) : FB voltage (V_{FB}) C4 (green) : CS voltage (V_{CS})	C1 (yellow) : Drain voltage (V_D) C2 (purple) : Supply voltage (V_{VCC}) C3 (blue) : FB voltage (V_{FB}) C4 (green) : CS voltage (V_{CS})
V_{Drain_peak} at 85 V AC ≈ 282 V with first zero crossing and f_S ≈ 58 kHz	V_{Drain_peak} at 300 V AC ≈ 597 V with third zero crossing and f_S ≈ 74 kHz

Figure 18 Drain and CS voltage at maximum load

11.4 Zero crossing point during normal operation

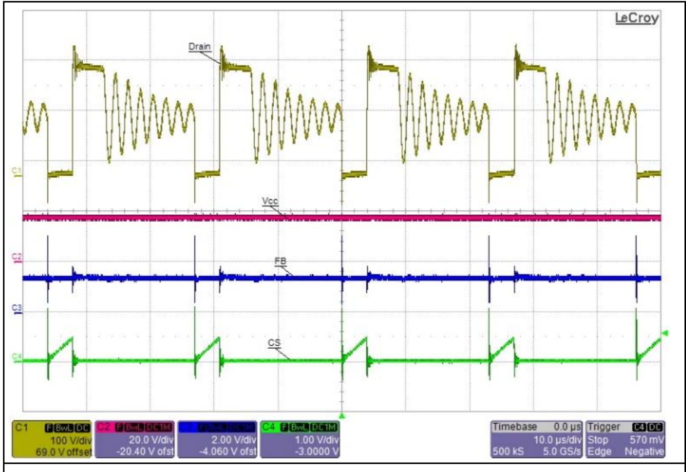
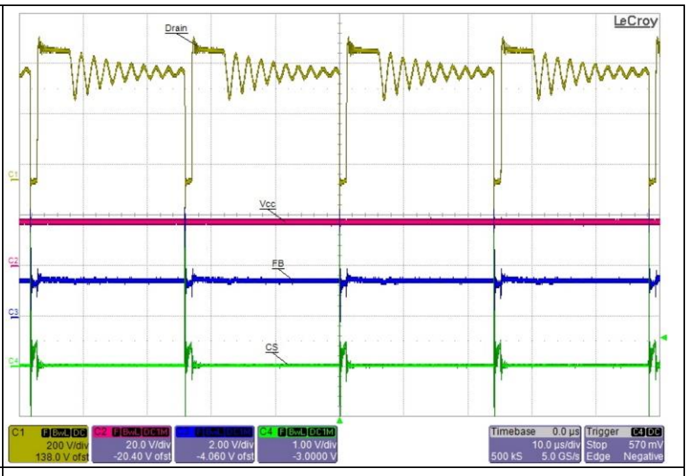
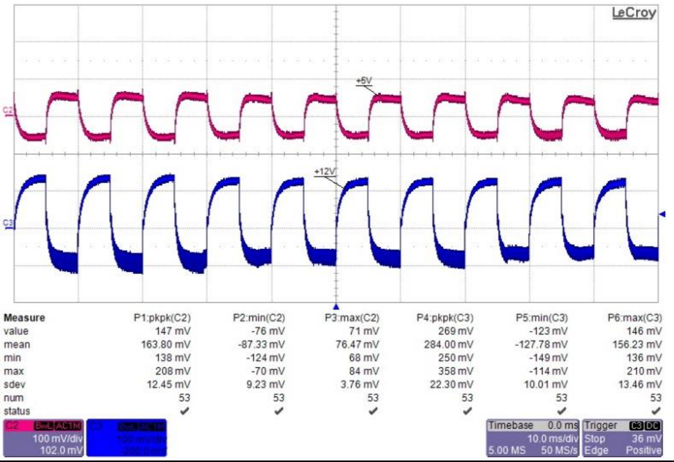
	
C1 (yellow) : Drain voltage (V_D) C2 (purple) : Supply voltage (V_{VCC}) C3 (blue) : FB voltage (V_{FB}) C4 (green) : CS voltage (V_{CS})	C1 (yellow) : Drain voltage (V_D) C2 (purple) : Supply voltage (V_{VCC}) C3 (blue) : FB voltage (V_{FB}) C4 (green) : CS voltage (V_{CS})
Eighth zero crossing at 85 V AC and 25 percent load (5 V x 0.05 A + 12 V x 0.29 A) (zero crossing varies from 1 ~ 8 for low-line)	Tenth zero crossing at 300 V AC and 25 percent load (5 V x 0.05 A +12 V x 0.29 A) (zero crossing varies from 3 ~ 10 for high-line)

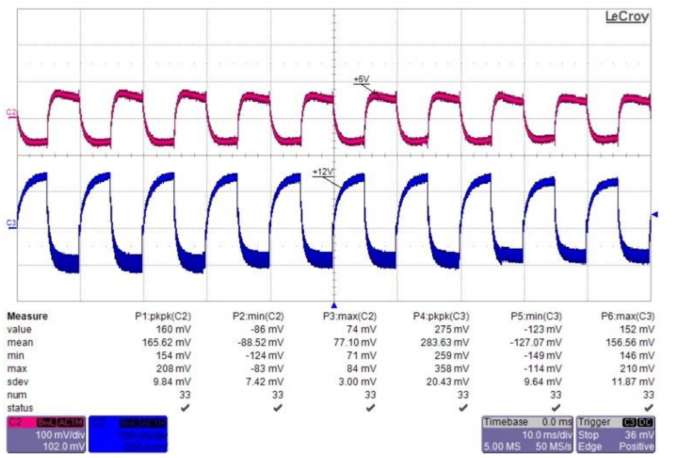
Figure 19 Zero crossing

11.5 Load-transient response (dynamic load from 10 percent to 100 percent)



C2 (purple) : 5 V output ripple voltage (V_{out5})
C3 (blue) : 12 V output ripple voltage (V_{out12})

5 $V_{ripple\_pk\_pk}$ at 85 V AC ≈ 147 mV
12 $V_{ripple\_pk\_pk}$ at 85 V AC ≈ 269 mV
(85 V AC, 12 V load change from 10 percent to 100 percent and 5 V at 200 mA load, 100 Hz, 0.4 A/µs slew rate)
Probe terminal end with decoupling capacitor of 0.1 µF (ceramic) and 1 µF (electrolytic), 20 MHz filter

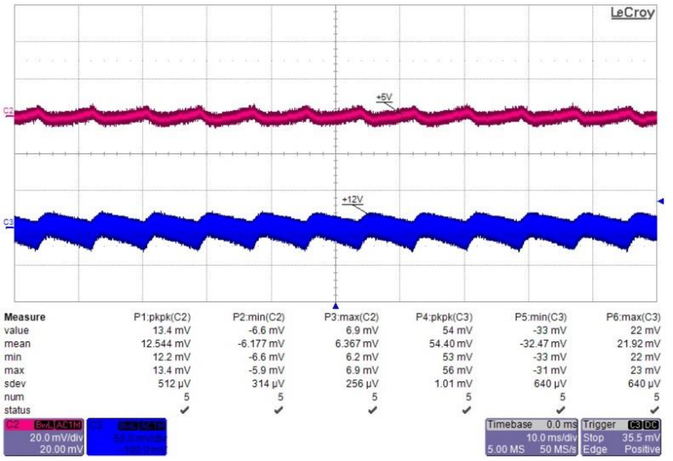


C2 (purple) : 5 V Output ripple voltage (V_{out5})
C3 (blue) : 12 V Output ripple voltage (V_{out12})

5 $V_{ripple\_pk\_pk}$ at 300 V AC ≈ 160 mV
12 $V_{ripple\_pk\_pk}$ at 85 V AC ≈ 275 mV
(300 V AC , 12 V load change from 10 percent to 100 percent and 5 V at 200 mA load, 100 Hz, 0.4 A/µs slew rate)
Probe terminal end with decoupling capacitor of 0.1 µF (ceramic) and 1 µF (electrolytic), 20 MHz filter

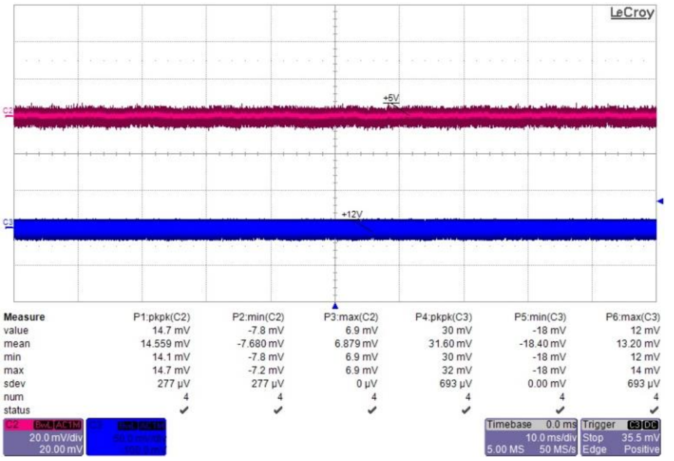
Figure 20 Load-transient response

11.6 Output ripple voltage at maximum load



C2 (purple) : 5 V output ripple voltage (V_{out5})
C3 (blue) : 12 V output ripple voltage (V_{out12})

5 $V_{ripple\_pk\_pk}$ at 85 V AC ≈ 13.4 mV
12 $V_{ripple\_pk\_pk}$ at 85 V AC ≈ 54 mV
Probe terminal end with decoupling capacitor of 0.1 µF (ceramic) and 1 µF (electrolytic), 20 MHz filter



C2 (purple) : 5 V output ripple voltage (V_{out5})
C3 (blue) : 12 V output ripple voltage (V_{out12})

5 $V_{ripple\_pk\_pk}$ at 300 V AC ≈ 14.7 mV
12 $V_{ripple\_pk\_pk}$ at 300 V AC ≈ 30 mV
Probe terminal end with decoupling capacitor of 0.1 µF (ceramic) and 1 µF (electrolytic), 20 MHz filter

Figure 21 Output ripple voltage at maximum load

11.7 Output ripple voltage at burst mode 1 W load

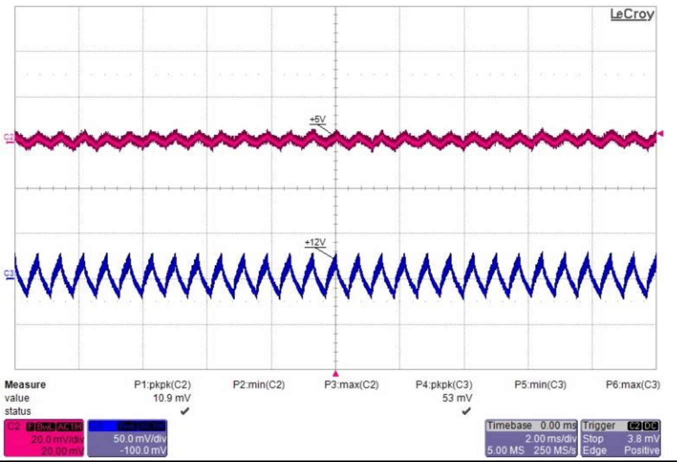
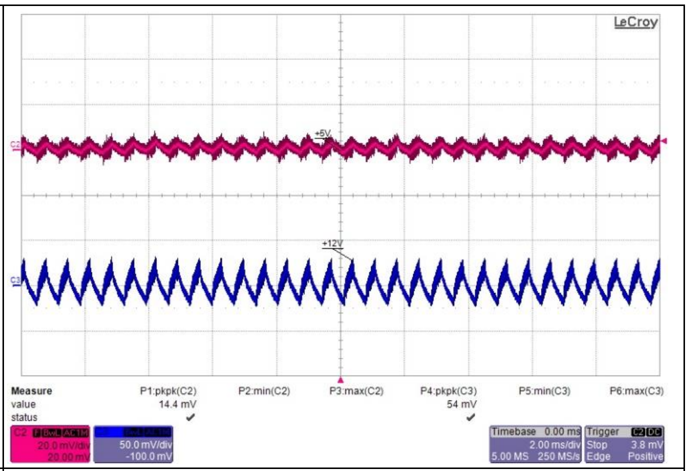
	
C2 (purple) : 5 V output ripple voltage (V_{out5}) C3 (blue) : 12 V output ripple voltage (V_{out12})	C2 (purple) : 5 V output ripple voltage (V_{out5}) C3 (blue) : 12 V output ripple voltage (V_{out12})
5 $V_{ripple\_pk\_pk}$ at 85 V AC ≈ 10.9mV 12 $V_{ripple\_pk\_pk}$ at 85 V AC ≈ 53 mV Load: 5 V at 6 mA and 12 V at 80 mA Probe terminal end with decoupling capacitor of 0.1 µF (ceramic) and 1 µF (electrolytic), 20 MHz filter	5 $V_{ripple\_pk\_pk}$ at 300 V AC ≈ 14.4 mV 12 $V_{ripple\_pk\_pk}$ at 300 V AC ≈ 54 mV Load: 5 V at 6 mA and 12 V at 80 mA Probe terminal end with decoupling capacitor of 0.1 µF (ceramic) and 1 µF (electrolytic), 20 MHz filter

Figure 22 Output ripple voltage at burst mode 1 W load

11.8 Entering ABM

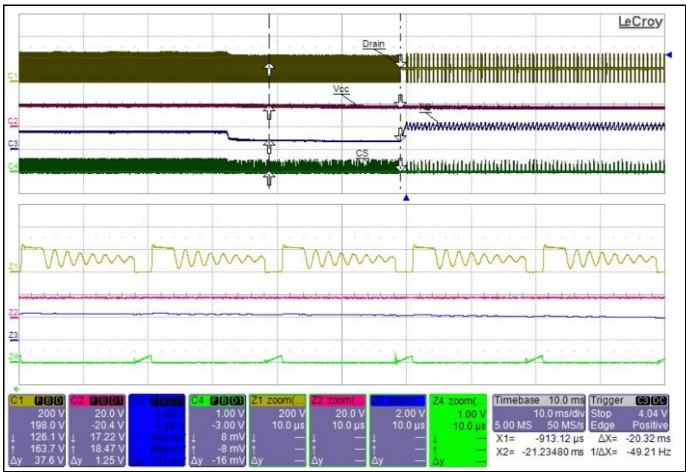
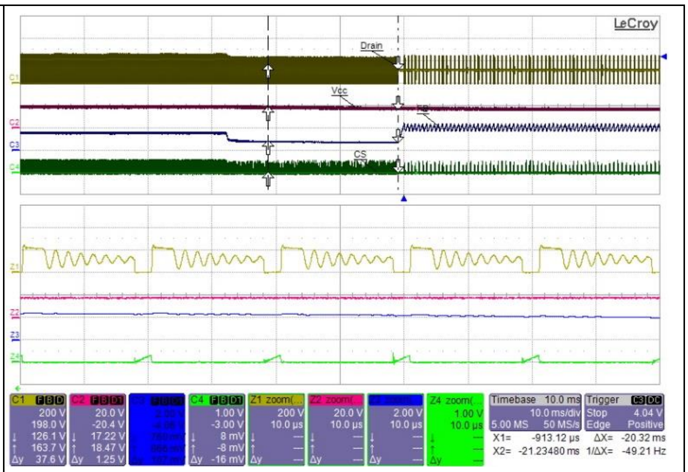
	
C1 (yellow) : Drain voltage (V_D) C2 (purple) : Supply voltage (V_{VCC}) C3 (blue) : FB voltage (V_{FB}) C4 (green) : CS voltage (V_{CS})	C1 (yellow) : Drain voltage (V_D) C2 (purple) : Supply voltage (V_{VCC}) C3 (blue) : FB voltage (V_{FB}) C4 (green) : CS voltage (V_{CS})
Condition to enter ABM level 1: V_{FB} less than 0.9 V, N_{ZC} = 8 and $t_{blanking}$ = 20 ms (load change from 5 W to 0.5 W at 85 V AC)	Condition to enter ABM level 1: V_{FB} less than 0.9 V, N_{ZC} = 10 and $t_{blanking}$ = 20 ms (load change from 5 W to 0.5 W at 300 V AC)

Figure 23 Entering ABM

11.9 During ABM

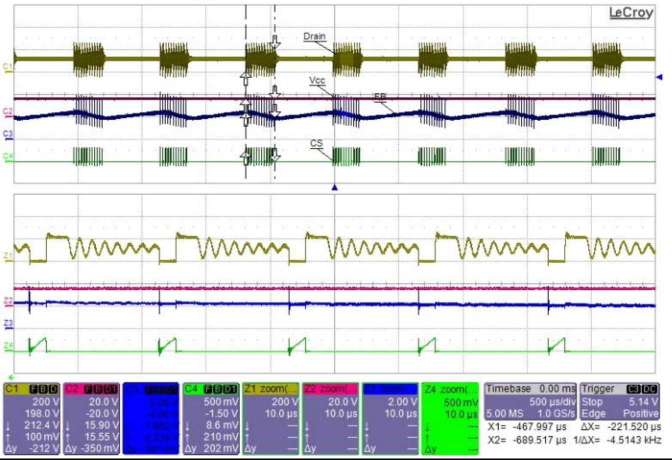
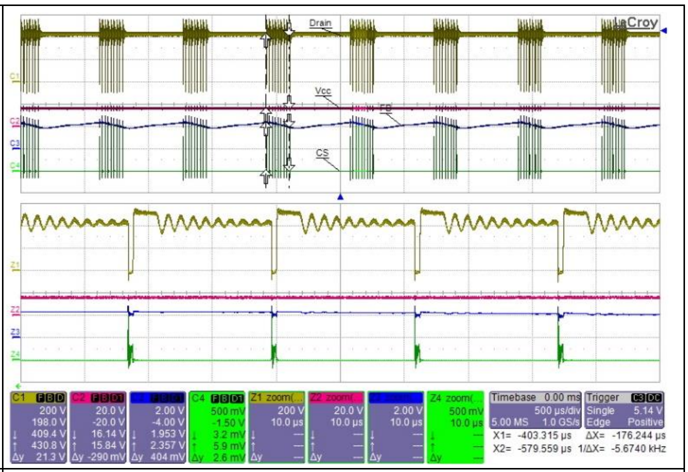
	
C1 (yellow) : Drain voltage (V_D) C2 (purple) : Supply voltage (V_{VCC}) C3 (blue) : FB voltage (V_{FB}) C4 (green) : CS voltage (V_{CS})	C1 (yellow) : Drain voltage (V_D) C2 (purple) : Supply voltage (V_{VCC}) C3 (blue) : FB voltage (V_{FB}) C4 (green) : CS voltage (V_{CS})
During ABM level 1: V_{FB_BOn} = 2.4 V, V_{FB_BOff} = 2.0 V, V_{CSBLP} = 0.31 V, N_{ZC} = 8 (0.5 W at 85 V AC)	During ABM level 1: V_{FB_BOn} = 2.4 V, V_{FB_BOff} = 2.0 V, V_{CSBLP} = 0.31 V, N_{ZC} = 10 (0.5 W at 300 V AC)

Figure 24 During ABM

11.10 Leaving ABM

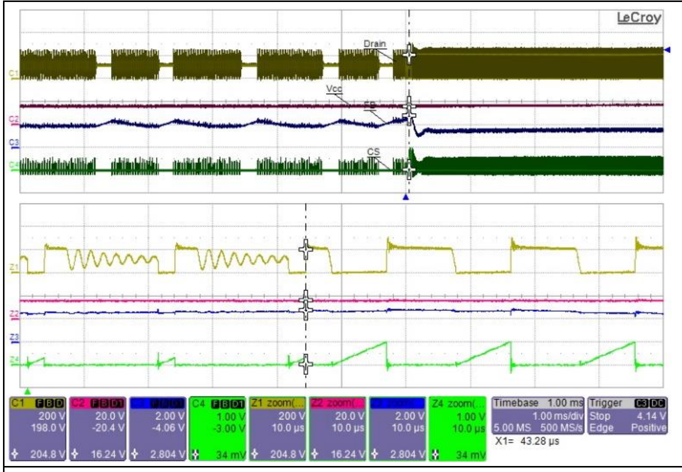
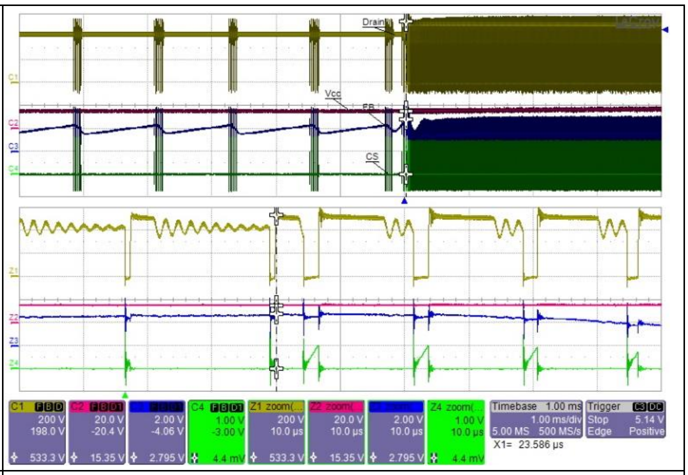
	
C1 (yellow) : Drain voltage (V_D) C2 (purple) : Supply voltage (V_{VCC}) C3 (blue) : FB voltage (V_{FB}) C4 (green) : CS voltage (V_{CS})	C1 (yellow) : Drain voltage (V_D) C2 (purple) : Supply voltage (V_{VCC}) C3 (blue) : FB voltage (V_{FB}) C4 (green) : CS voltage (V_{CS})
Condition to leave ABM level 1: V_{FB} more than 2.75 V (load change from 0.5 W full load at 85 V AC)	Condition to leave ABM level 1: V_{FB} more than 2.75 V (load change from 0.5 W full load at 300 V AC)

Figure 25 Leaving ABM

11.11 Line Over-Voltage Protection (OVP) (non-switch auto-restart)

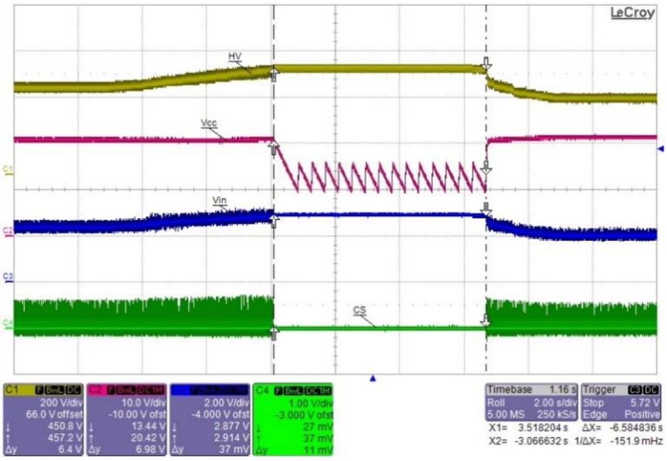
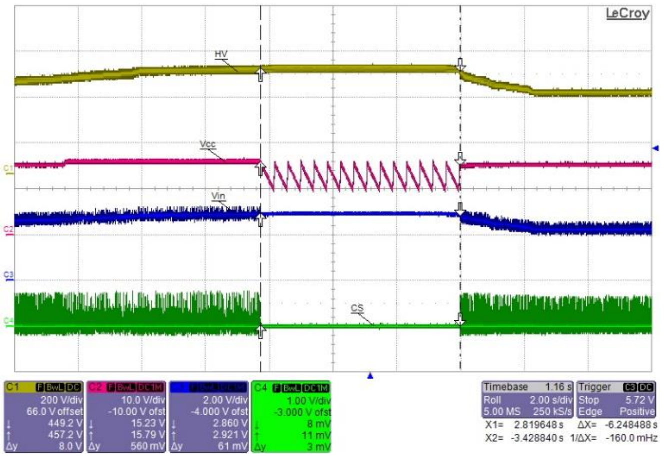
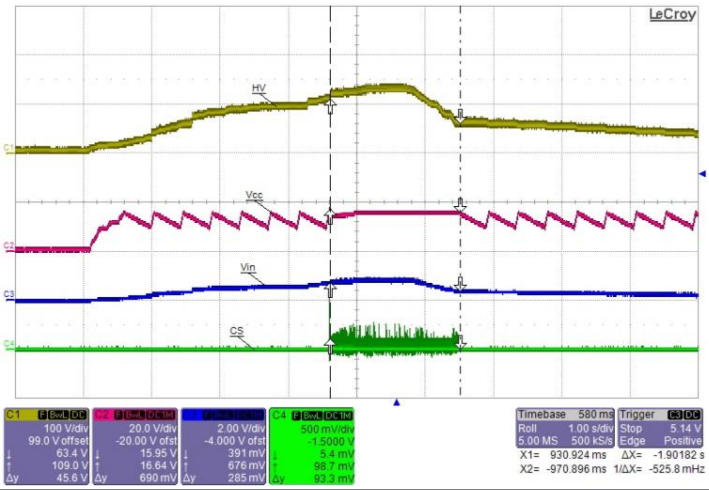
	
C1 (yellow) : Bulk voltage (V_{Bulk}) C2 (purple) : Supply voltage (V_{VCC}) C3 (blue) : V_{IN} voltage (V_{VIN}) C4 (green) : CS voltage (V_{CS})	C1 (yellow) : Bulk voltage (V_{Bulk}) C2 (purple) : Supply voltage (V_{VCC}) C3 (blue) : V_{IN} voltage (V_{VIN}) C4 (green) : CS voltage (V_{CS})
Condition to detect line OVP: V_{VIN} more than 2.9 V Condition to reset line OVP: V_{VIN} less than 2.9 V	
Gradually increase AC-line voltage at full load until line OVP detect and decrease AC-line until line OVP reset.	Gradually increase AC-line voltage at 1 W load (ABM) until line OVP detect and decrease AC-line until line OVP reset.

Figure 26 Line OVP

11.12 Brown-out protection (non-switch auto-restart)



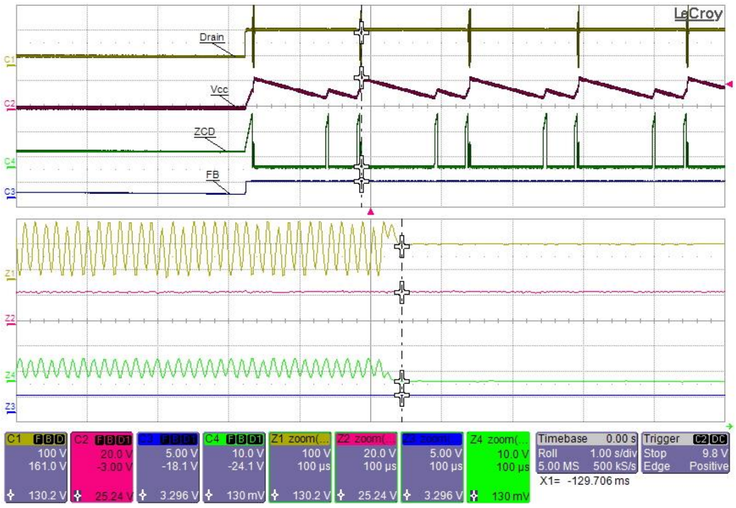
C1 (yellow)	: Bulk voltage (V_{Bulk})
C2 (purple)	: Supply voltage (V_{VCC})
C3 (blue)	: V_{IN} voltage (V_{VIN})
C4 (green)	: CS voltage (V_{CS})

Condition to reset brown-out protection (brown-in): V_{VIN} more than 0.66 V (V_{BULK} more than 100 V DC [≈ 77 V AC])
Condition to detect brown-out protection: V_{VIN} less than 0.4 V (V_{BULK} less than 61 V DC [≈ 45 V AC])

(Gradually increase AC-line voltage at 1 W load until system start and reduce the line until brown-out detect)

Figure 27 Brown-out protection

11.13 V_{CC} OVP (odd-skip auto-restart)

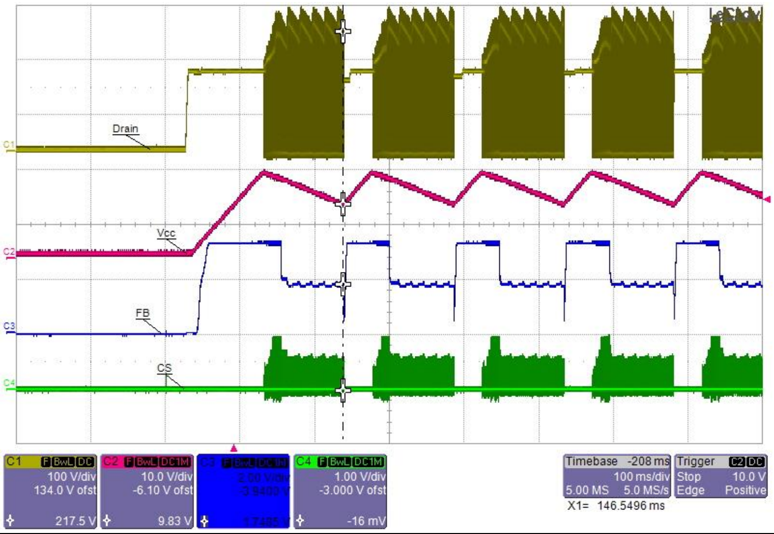


C1 (yellow) : Zero Crossing Detection (ZCD) voltage (V_{ZCD})
C2 (purple) : Supply voltage (V_{VCC})
C3 (blue) : FB voltage (V_{FB})
C4 (green) : ZCD voltage (V_{ZCD})

Condition to enter V_{VCC} OVP: V_{VCC} more than 25.5 V
(85 V AC and disable output OVP detection at ZCD pin, short R26, open ZD1)

Figure 28 V_{CC} OVP

11.14 V_{CC} Under-Voltage Protection (UVP) (auto-restart)

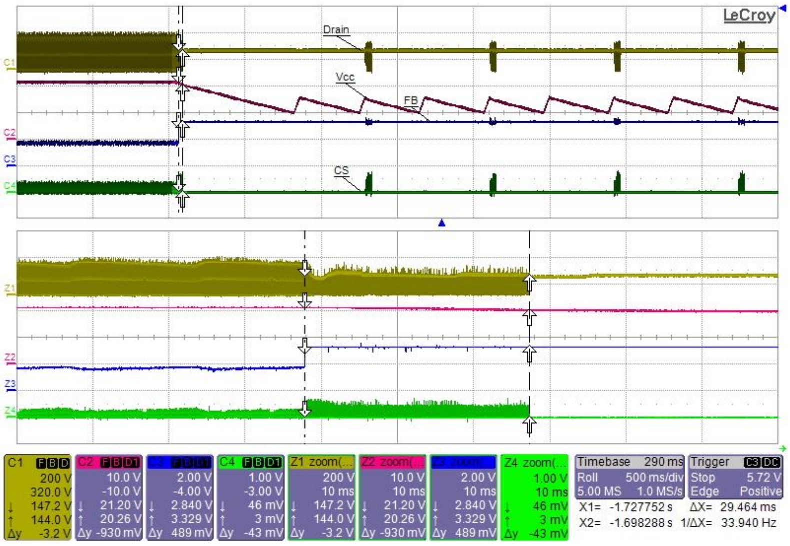


C1 (yellow) : Drain voltage (V_D)
C2 (purple) : Supply voltage (V_{VCC})
C3 (blue) : FB voltage (V_{FB})
C4 (green) : CS voltage (V_{CS})

Condition to enter V_{CC} UVP: V_{CC} less than 10 V
(Remove R12A and power on the system with full load at 85 V AC)

Figure 29 V_{CC} UVP

11.15 Over-load protection (odd-skip auto-restart)

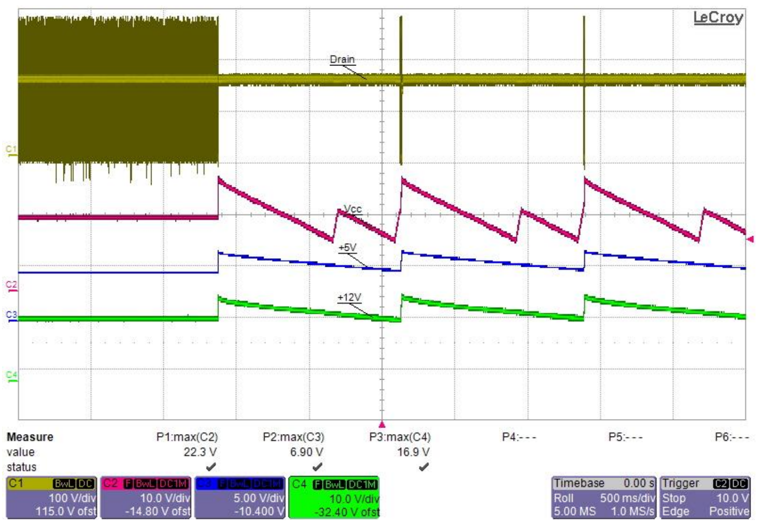


C1 (yellow) : Drain voltage (V_D)
C2 (purple) : Supply voltage (V_{VCC})
C3 (blue) : FB voltage (V_{FB})
C4 (green) : CS voltage (V_{CS})

Condition to enter over-load protection: V_{FB} more than 2.75 V and lasts for 30 ms blanking time
(12 V output load change from full load to short at 85 V AC)

Figure 30 Over-load protection

11.16 Output OVP (odd-skip auto-restart)

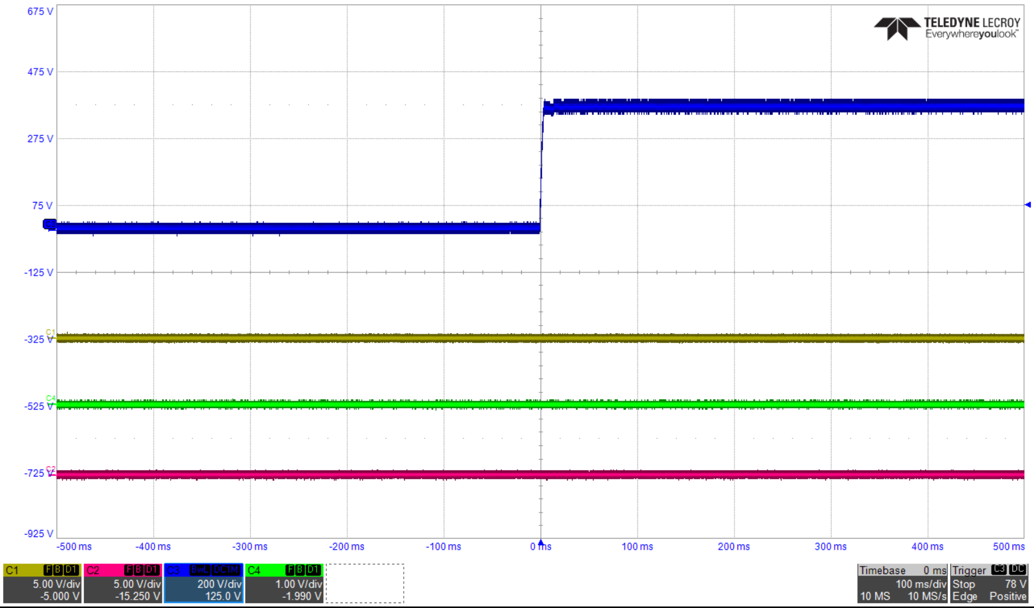


C1 (yellow) : Drain voltage (V_D)
C2 (purple) : Supply voltage (V_{VCC})
C3 (blue) : 5 V output voltage (V_{out5})
C4 (green) : 12 V output voltage (V_{out12})

Condition to enter output OVP: V_{out12} more than 16.8 V; V_{out5} more than 7 V
(85 V AC, short R26 during system operation at no load)

Figure 31 Output OVP

11.17 V_{CC} short-to-GND protection



C1 (yellow) : FB voltage (V_{FB})
C2 (purple) : V_{CC} voltage (V_{VCC})
C3 (blue) : Drain voltage (V_D)
C4 (green) : CS voltage (V_{CS})

Condition to enter V_{CC} short-to-GND: if V_{CC} is less than V_{VCC_SCP} → I_{VCC} = $I_{VCC\_Charge1}$
(Short V_{CC} pin-to-GND and measure the AC input current, I_{in} ≈ 22.4 mA and input power is ≈ 38.6 mW at 264 V AC)

Figure 32 V_{CC} short-to-GND protection

12 References

[1] ICE5QRxx80BG datasheet, Infineon Technologies AG

[2] AN-201609_PL83_026-fifth-generation Quasi-Resonant Design Guide

Revision history

Document version	Date of release	Description of changes
V1.0	13-03-2020	First release

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