ILD8150/ILD8150E

LED driver IC for high power LEDs with hybrid dimming down to 0.5%

Features

- DC/DC buck with hysteretic current regulation
- Output current up to 1.5 A DC
- Integrated 80 V high-side MOSFET switch with low R_{ON}
- Hybrid dimming to 0.5% of the target current
- Wide operating voltage range 8 V to 80 V
- Cycle-by-cycle current limitation
- Under-voltage lockout
- Thermal protection
- Flicker free operation
- Digital soft-start
- Pull-down transistor to avoid LED glowing

Potential applications

- Electronic Control Gear (ECG) for LED luminaries

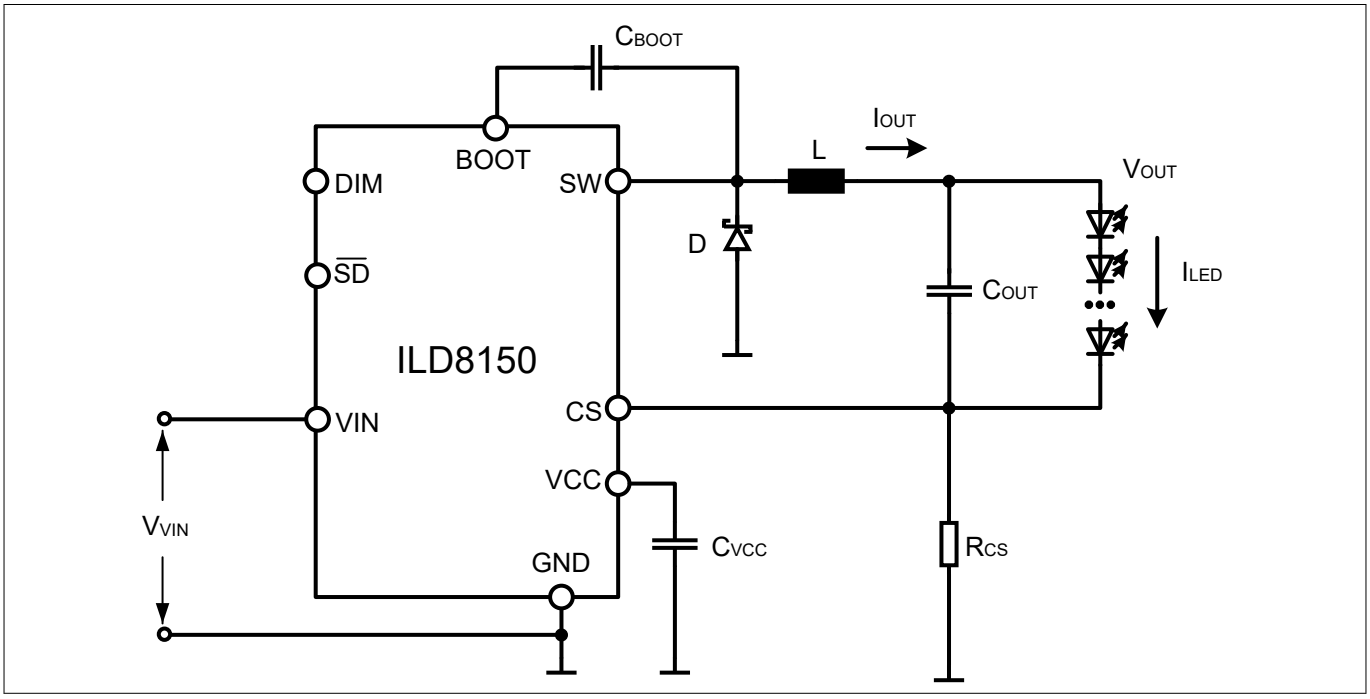


Figure 1 DC/DC buck constant current

Product validation

- Qualified for industrial applications according to the relevant tests of JEDEC47/20/22.

Product type	Package
ILD8150	PG-DSO-8
ILD8150E	PG-DSO-8 with exposed pad

Description

The ILD8150 is a 80 V DC/DC converter IC for LED applications to drive high-power LEDs. For applications operating close to SELV limits it provides a high safety voltage margin. The buck LED driver IC is tailored for LEDs in general lighting applications with average currents up to 1.5 A using a high-side integrated switch. A complete set of features and protections provide a well fit for professional LED lighting solutions.

Performance and innovation

The hysteretic current control provides an extremely fast regulation and stable LED current combined with good EMI performance. The efficiency of the LED driver is remarkable high due to the low R_{ON} of the internal switch.

Hybrid dimming is an Infineon unique one-pin dimming method that combines analog dimming and PWM dimming of the LEDs current in one hybrid dimming curve.

A PWM input signal between 250 Hz and 20 kHz controls dimming of the LEDs current in analog mode from 100 percent to 12.5 percent and 12.5 percent to 0.5 percent in hybrid mode with flicker-free modulation frequency of 3.4 kHz. The digital PWM dimming detection with high resolution makes it the perfect match for microcontroller and high quality dimming applications.

The IC supply is directly driven from the primary stage and the low-power shut down contributes to a very high stand-by system efficiency.

High output current accuracy from device to device under all loads and input voltages conditions makes it perfect for tunable white and flat panel designs where current must be identical string to string.

Protection

A wide range of operating supply voltage from 8 V to 80 V DC enables a wide use in many applications and provides a good margin when bus voltage exceeds shortly the SELV limits.

The soft-start function protects the primary stage from abrupt current request.

The over temperature protection is triggered when the junction temperature exceeds the temperature threshold turning off the output stage. The output stage turns on again when the junction temperature falls below the temperature threshold.

Under voltage lock-out protects the bootstrap voltage and the hysteretic design ensures cycle-by-cycle current limitation.

Table of contents

Features . . . 1
Potential applications . . . 1
Description . . . 2
Table of contents . . . 3
1 Functional block diagram . . . 4
2 Pin configuration . . . 5
3 Functional description . . . 6
3.1 Buck controller features . . . 6
3.1.1 Output current regulation . . . 6
3.1.2 Dimming . . . 6
3.1.3 Digital soft-start . . . 8
3.1.4 Low power mode . . . 9
3.2 Protection features . . . 10
3.2.1 Over-temperature protection . . . 10
3.2.2 Under-voltage protection . . . 10
4 Thermal and electrical characteristics . . . 11
4.1 Package characteristics . . . 11
4.2 Absolute maximum ratings . . . 11
4.3 Operating conditions . . . 12
4.4 Electrical characteristics . . . 13
5 Package dimensions . . . 16
Revision history . . . 18
Disclaimer . . . 19

1 Functional block diagram

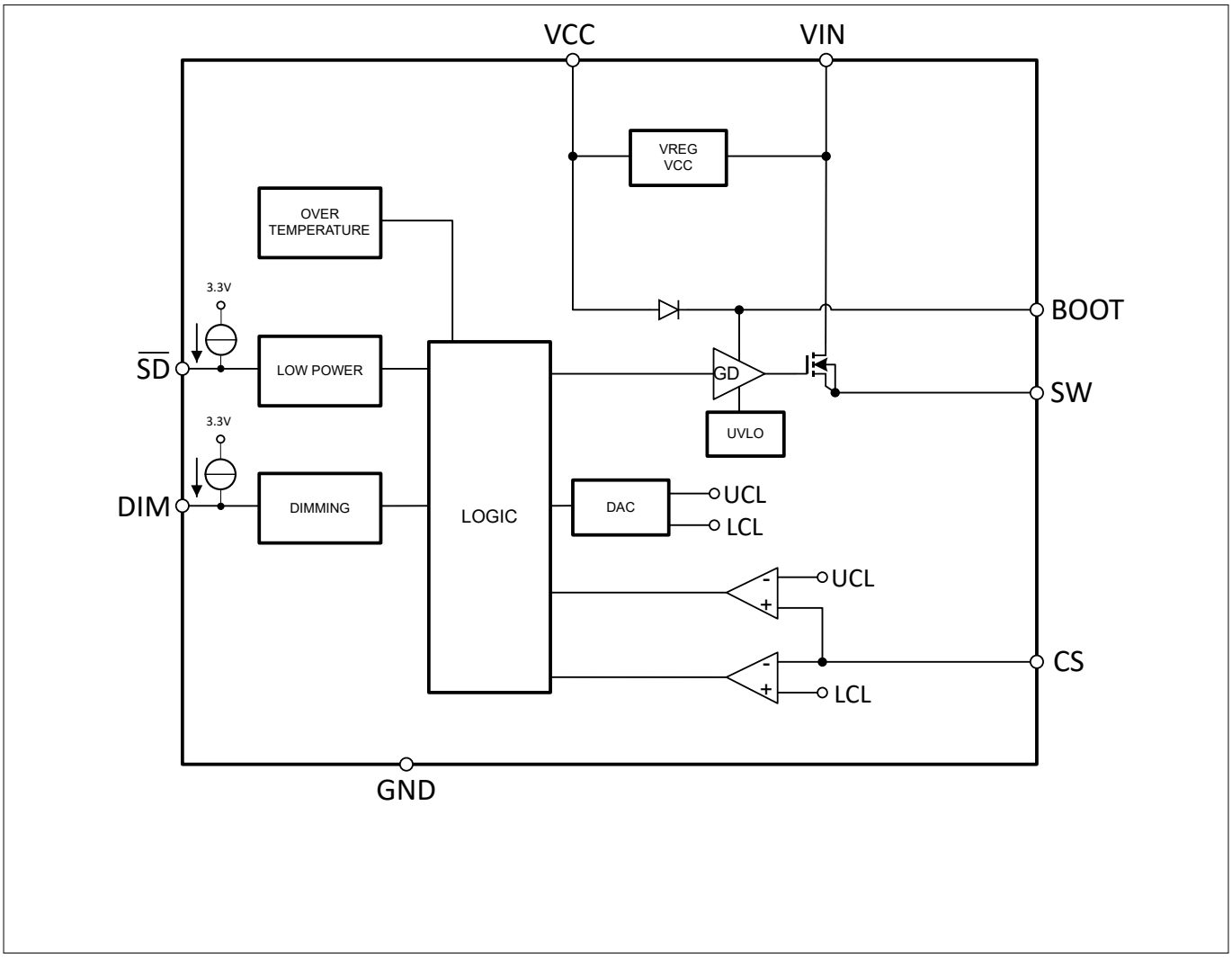


Figure 2 Block diagram

2 Pin configuration

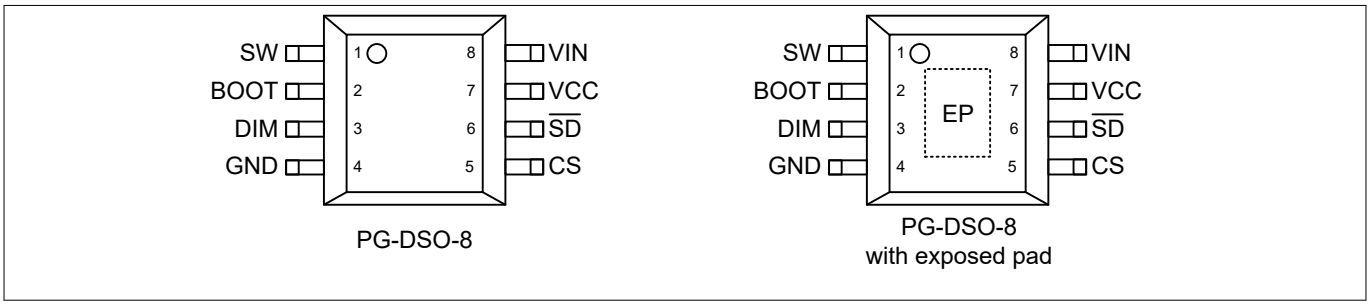


Figure 3 Pin-out

Both PG-DSO-8 and PG-DSO-8 with exposed pad have the same pin-out. The exposed pad is internally not connected.

Table 1 Pin functions

Name	No.	Function
SW	1	Internal switch output.
BOOT	2	Internal switch driver bootstrap, connect to bootstrap capacitor.
DIM	3	Input for PWM dimming (internally pulled-up).
GND	4	Ground.
CS	5	Current sense feedback.
SD (neg.)	6	Shutdown (internally pulled-up).[1)]
VCC	7	Output of the internal regulator, connect to bypass capacitor.
VIN	8	Input voltage.
EP[2)]	9	Exposed pad, connect to GND (internally not connected).

1 To use the shutdown functionality 3.3 V must be provided externally at DIM pin.
2 PG-DSO-8 with exposed pad only.

3 Functional description

This chapter provides a summary of the integrated functions and features, and describes the relationships between them. The parameters and equations are based on typical values at T_A = 25 °C.

3.1 Buck controller features

3.1.1 Output current regulation

The hysteretic control allows fast and always stable output current and guarantees an intrinsic cycle-by-cycle over-current protection.

The pin CS feeds back the voltage level on the current sense resistor R_{CS} to the hysteretic controller. The hysteretic controller implements two voltage thresholds V_{CSH} and V_{CSL}. When the CS voltage crosses above the V_{CSH} threshold the internal switch turns-off. When the CS voltage crosses below the V_{CSL} the internal switch turns-on. The thresholds V_{CSH} and V_{CSL} determine the output current peak-to-peak ripple $I_{OUT,RIPPLE} = (V_{CSH} - V_{CSL})/R_{CS}$. The target LEDs current is the undimmed average current determined by the formula $I_{LED,AVG} = V_{CS,AVG}/R_{CS}$ with $V_{CS,AVG} = (V_{CSH} + V_{CSL})/2$. The continuous-conduction-mode (CCM) timings are $t_{ON} = (I_{OUT,RIPPLE} \bullet L)/(V_{VIN} - V_{OUT})$ and $t_{OFF} = (I_{OUT,RIPPLE} \bullet L)/V_{OUT}$.

Figure 4 show the CCM output current waveform.

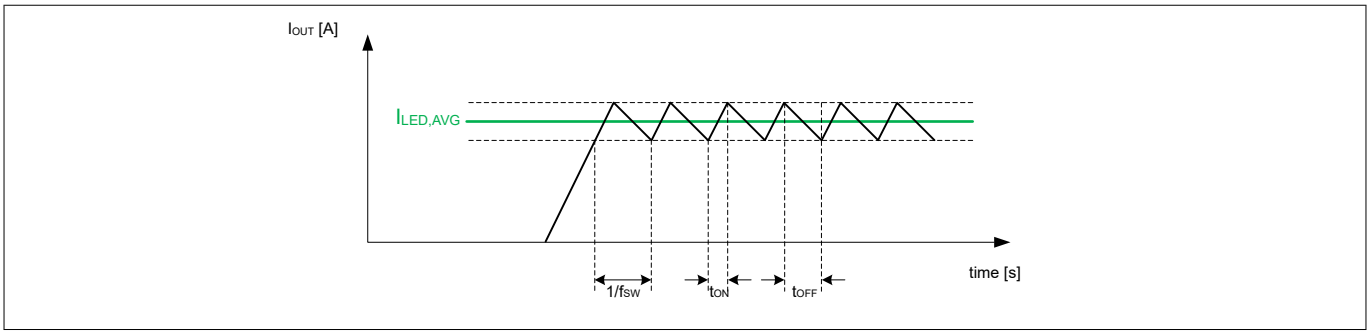


Figure 4 Output current waveform

3.1.2 Dimming

In analog dimming the output current is proportional to the internal CS reference voltage and the output current varies analogically between 100% and 12.5% of the target output current. Hybrid dimming applies below 12.5% of the target output current so that the output current is stable at 12.5% and amplitude modulated. The modulation signal has a frequency of typically 3.4 kHz to satisfy the IEEE1789-2015 recommendation for no observable flicker in light.

Figure 5 shows the mapping between the input PWM duty cycle and the output current as a ratio of the target output current. Figure 8 shows the detail of dim-to-off.

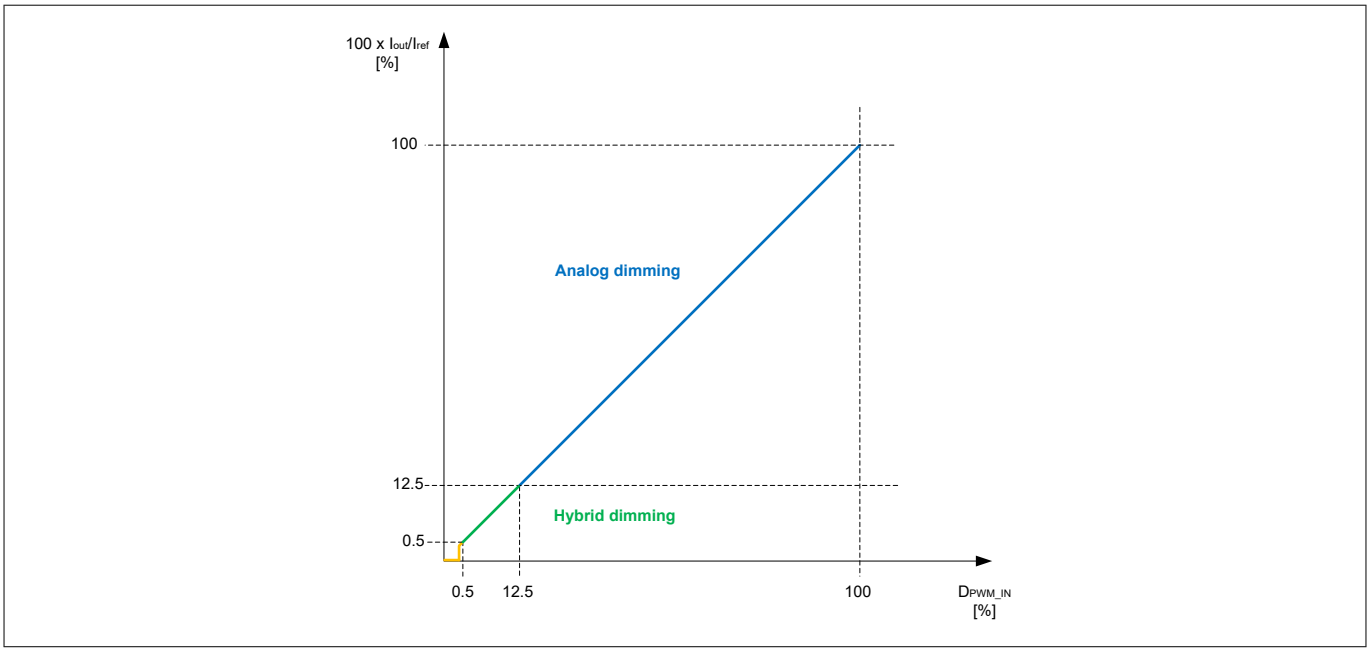


Figure 5 Hybrid dimming curve

Figure 6 shows the output current in analog dimming.

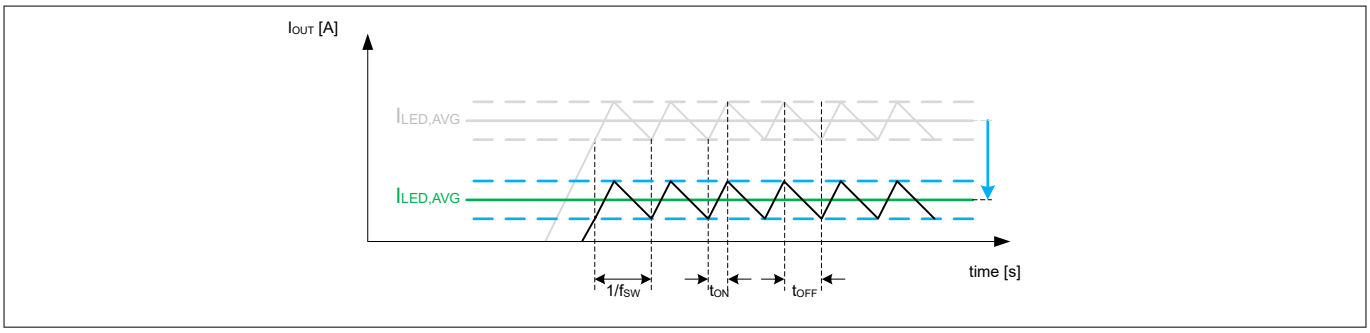


Figure 6 Output current waveform in analog dimming at two dimming levels

Figure 7 shows the output current in hybrid dimming.

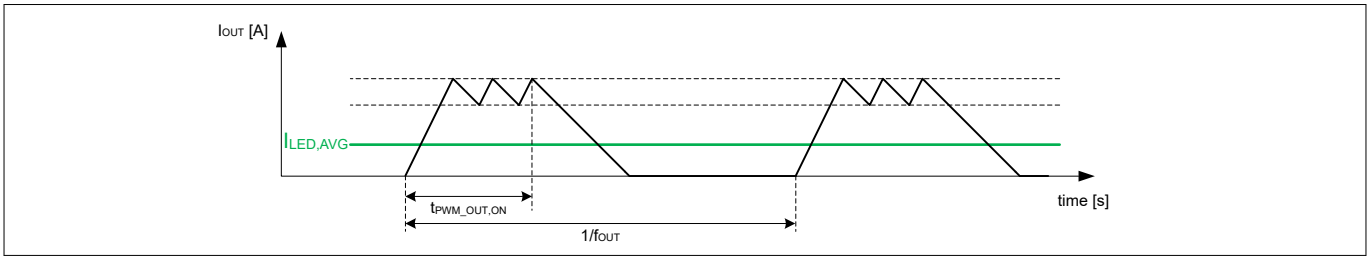


Figure 7 Output current waveform in hybrid dimming

The ILD8150 turns the output stage respectively off when the PWM dimming input signal duty cycle is less than $D_{PWM_IN,OFF}$ and on when the PWM dimming input signal duty cycle is higher than $D_{PWM_IN,ON}$. The two dim-to-off levels create a hysteresis that avoids unstable states at the on/off boundary.

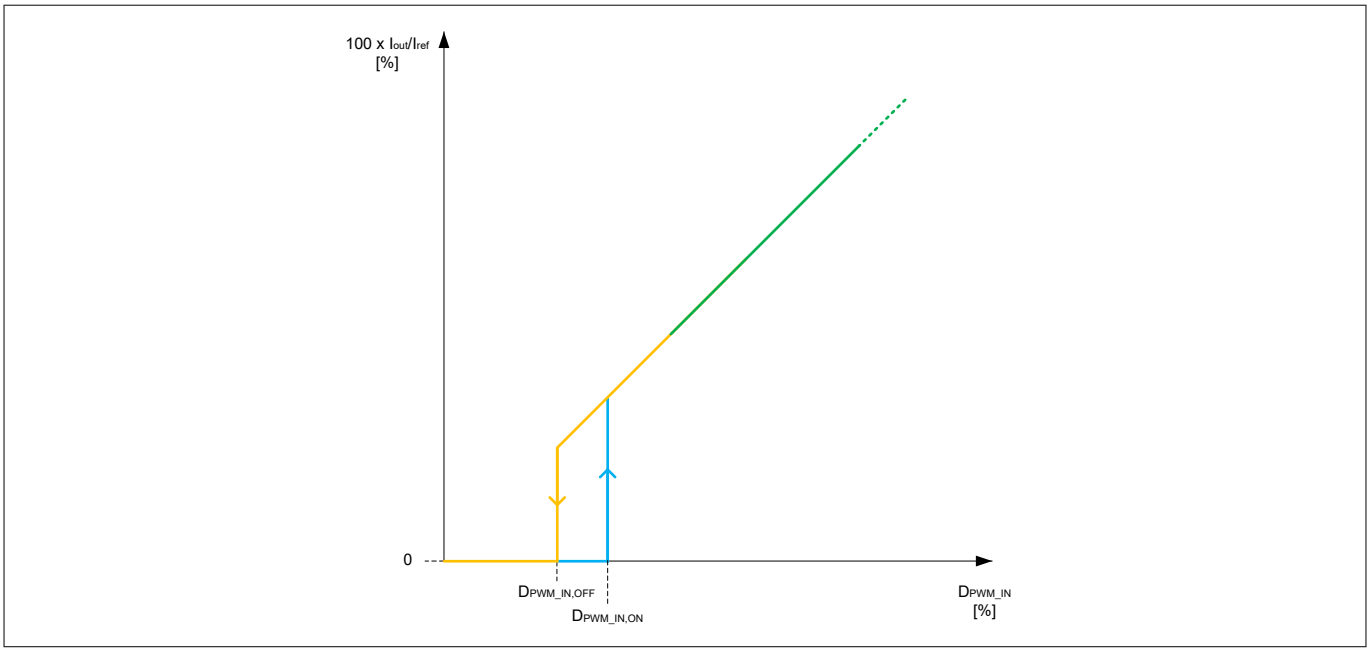


Figure 8 Dimming curve dim-to-off detail

The ILD8150 evaluates the PWM dimming input signal duty cycle D_{PWM_IN} at the DIM pin. In analog dimming the duty cycle maps to a proportional CS reference voltage. In hybrid dimming the duty cycle maps to a hybrid dimming duty cycle using the hybrid dimming curve. The hybrid dimming frequency is fixed and does not relate to the input PWM frequency.

Figure 9 shows the details of the input PWM signal where $D_{PWM_IN} = t_{PWM_IN,ON} \bullet f_{INPUT}$.

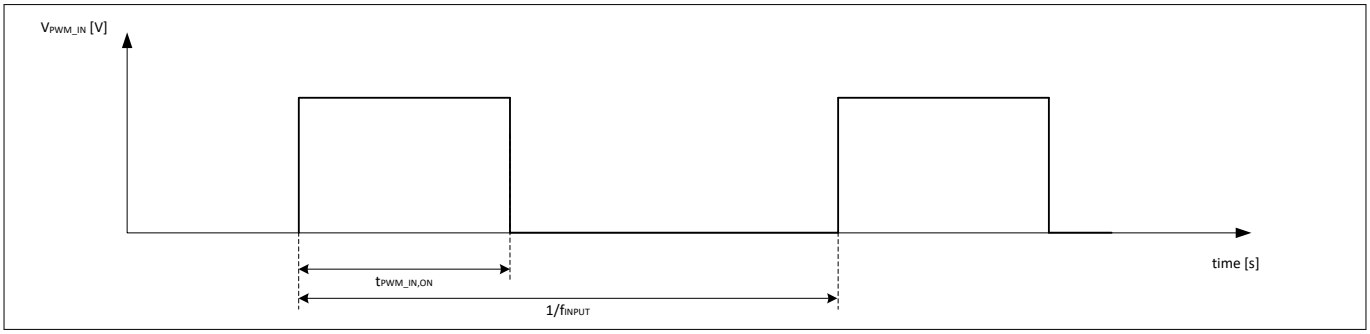


Figure 9 Input PWM signal

3.1.3 Digital soft-start

Soft-start is a feature that smooths output current transients during start-up.

Output current smoothing is digitally managed by the IC and applies in case of abrupt dimming changes. When the IC goes to dim-to-off the output current smoothing applies resulting in a soft-stop behavior. Benefits are the avoidance of under shoots or over shoots at primary side reflecting in a stable power regulation and reduction of components stress.

Digital soft-start uses of the PWM dimming signal. The PWM duty cycle sets the target dimming level and the PWM frequency sets the speed to reach that level. To lower PWM frequencies correspond a slower soft-start, to higher PWM frequencies correspond a faster soft-start. The output current ramps up to the target value in a determined soft start time t_{SS}. t_{SS} is defined as the time to reach the desired dimming level from a change in the PWM dimming signal. The number of steps of the soft-start ramp may vary depending on the actual and the target dimming level.

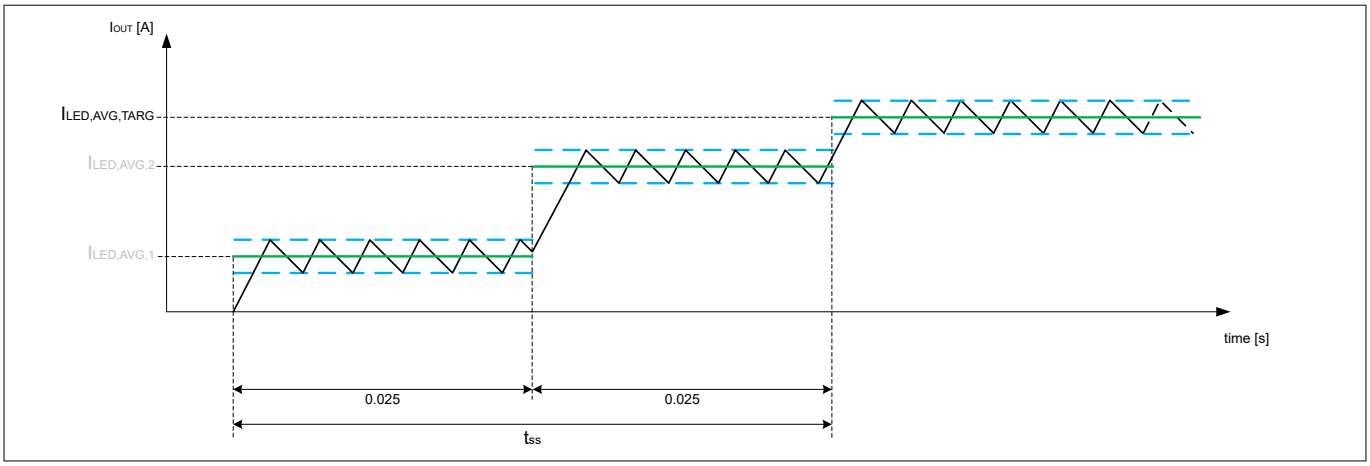


Figure 10 Digital soft-start

Figure 10 shows the output current soft-start in case of 100% dimming or DIM pin open (internally pulled-up).

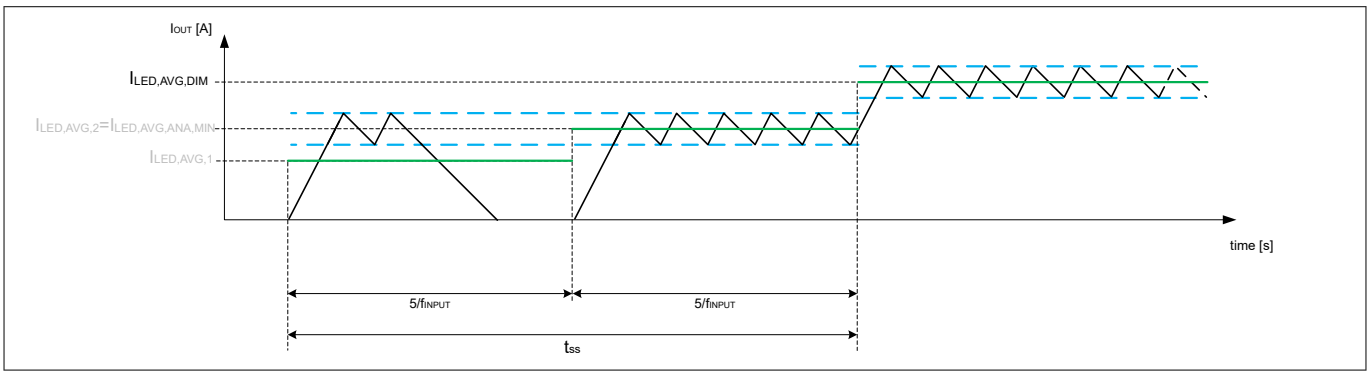


Figure 11 Digital soft-start in dim-mode

Figure 11 shows the output current soft-start in case of PWM dimming signal applied at the DIM pin.

Note: Output current smoothing does not affect the output current for small variations of the dimming signal e.g. to create light fading effects.

3.1.4 Low power mode

If the shut-down signal (SD neg.) is driven low for more than t_{SD_LO} the low power mode is active. If the shut-down signal is held high for more than t_{SD_HI} the IC resumes from low power mode. $-I_{SD,HPU}$ dynamic current is needed to turn the IC into low power mode, then the current changes into static $-I_{SD,LPU}$. DIM pin needs to be driven externally with at least $V_{DIM,SD}$ voltage during low power mode.

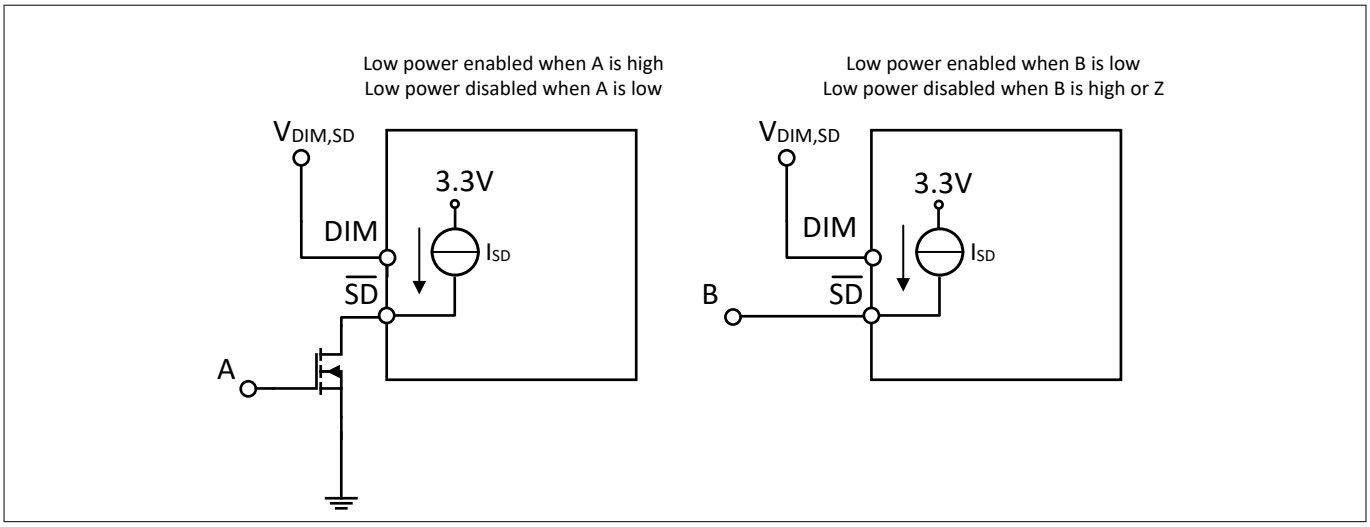


Figure 12 Shut-down signal interfacing

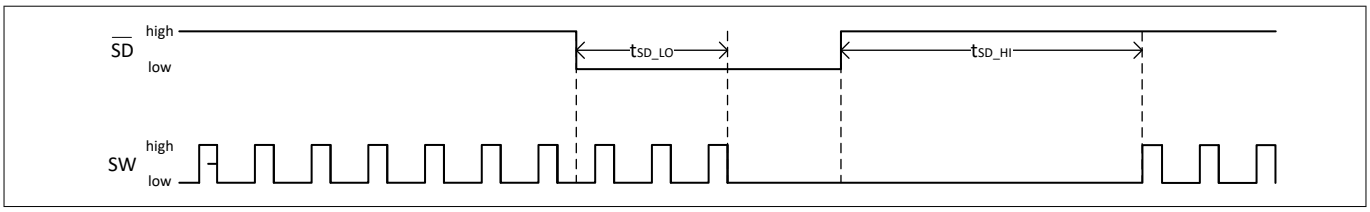


Figure 13 Shut-down timings

3.2 Protection features

3.2.1 Over-temperature protection

The over-temperature protection turns off the output stage when the junction temperature exceeds the temperature threshold $T_{OT,OFF}$. When the junction temperature falls below the temperature threshold $T_{OT,ON}$ the output stage turns on again.

In case of over-temperature the IC stops switching and waits for the over-temperature condition to disappear. The low power mode is not entered in case of over-temperature.

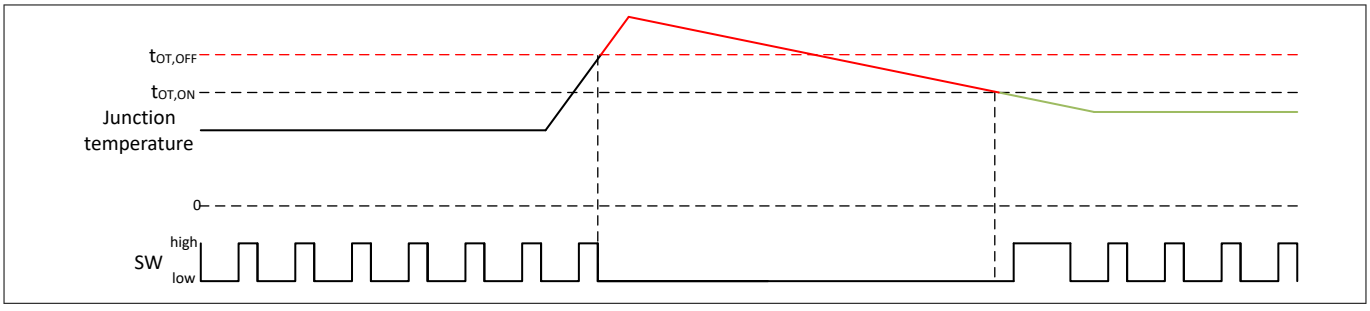


Figure 14 Over-temperature protection reaction

3.2.2 Under-voltage protection

The gate driver implements an under-voltage lock-out (UVLO) protection at high-side that switches-off the gate driver in case of BOOT under voltage (e.g. due to wrong bootstrap capacitor selection or incorrect system dimensioning).

In case of gate driver UVLO, the switch activity is interrupted in order to reload the bootstrap capacitor charge.

4 Thermal and electrical characteristics

This chapter describes the thermal and electrical characteristics of the ILD8150.

4.1 Package characteristics

Table 2 Package characteristics

Parameter	Symbol	Limit values		Unit	Remarks
		min	max		
Thermal resistance for PG-DSO-8 junction-to-ambient	R_{thJA}	—	*170*	K/W	JEDEC 1s0p no cooling area, for 345 mW power dissipation, T_A = 90 °C
	R_{thJA}	—	*135*	K/W	JEDEC 1s0p 100 mm² cooling area, for 440 mW power dissipation, T_A = 90 °C
Thermal resistance for PG-DSO-8 junction-to-case top	$R_{thJCtop}$	—	*42*	K/W	for 440 mW power dissipation, T_A = 90 °C
Thermal resistance for PG-DSO-8 with exposed pad junction-to-ambient	R_{thJA}	—	*160*	K/W	JEDEC 1s0p no cooling area, for 372 mW power dissipation, T_A = 90 °C
	R_{thJA}	—	*90*	K/W	JEDEC 1s0p 100 mm² cooling area, for 635 mW power dissipation, T_A = 90 °C
Thermal resistance for PG-DSO-8 with exposed pad junction-to-case top	$R_{thJCtop}$	—	*60*	K/W	for 635 mW power dissipation, T_A = 90 °C

4.2 Absolute maximum ratings

Attention**: **Stresses above the values listed below may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit. These values are not tested during production test.

Table 3 Absolute maximum ratings

Parameter	Symbol	Limit values		Unit	Remarks
		min	max		
Junction temperature	T_J	—	165	°C	
Storage temperature	T_S	–65	150	°C	
Soldering temperature	T_{SOLD}	—	260	°C	

(table continues...)

Table 3 (continued) Absolute maximum ratings

Parameter	Symbol	Limit values		Unit	Remarks
		min	max		
Latch-up	I_{LU}	—	100	mA	[3] Pin voltages acc. to abs. max. ratings
ESD HBM [4]	V_{HBM}	—	2000	V	[5]
ESD CDM	V_{CDM}	—	500	V	[6]
Voltage at pin SW	V_{SW}	–1.3	90	V	t_{Pulse} < 100 ns
Voltage at pin BOOT	V_{BOOT}	V_{SW}	90[7]	V	Voltage internally supplied to BOOT pin
Voltage at pin DIM	V_{DIM}	–0.3	3.6	V	
Voltage at pin CS	V_{CS}	–0.3	1.5	V	
Voltage at pin SD	V_{SD}	–0.3	3.6	V	
Voltage at pin VCC	V_{VCC}	–0.3	9	V	Voltage internally supplied to VCC pin
Voltage at pin VIN	V_{VIN}	–0.3	90	V	

4.3 Operating conditions

The recommended operating conditions are shown for which the DC electrical characteristics are valid.

Table 4 Operating conditions

Parameter	Symbol	Limit values		Unit	Remarks
		min	max		
Junction temperature	T_J	–40	150	°C	
VIN pin voltage	V_{VIN}	8	80	V	

3 Latch-up according to JEDEC JESD78D, T_A= 85°C.
4 Two different classes of ESD protection elements are implemented within ILD8150/ILD8150E: 1. ESD protection at pin VS will be triggered if the voltage at pin VS rises by more than 5 V with a slew rate of more than 5 V/µs. This condition is met during an ESD event, but might also occur if the LED driver gets hotplugged into a power supply and the VS blocking capacitor has a too small capacitance. ESD protection will remain triggered as long as the slewrate condition is met. If the ESD protection gets triggered while VS is supplied the IC might be damaged. 2. ESD protection at all other pins is triggered once the connected voltage signal exceeds a threshold higher than the maximum voltage rating specified for each pin. No preventions regarding slew rate control need to be taken for these pins..
5 ESD-HBM according to JEDEC JS-001.
6 ESD-CDM according to JEDEC JS-002.
7 The voltage difference between BOOT and SW pins must never exceed 9 V.

4.4 Electrical characteristics

The DC electrical characteristics provide the spread of values applicable within operating conditions (see chapter 4.3).

Typical values represent the median values related to T_A = 25 °C.

Table 5 DC electrical characteristics

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
Integrated switch and driver						
VIN pin to SW pin ON resistance	R_{ON}	—	290	—	mΩ	I_{SW}=200 mA[8]
	R_{ON}	—	—	545	mΩ	I_{SW}=200 mA and T_J=150 °C[8]
	R_{ON}	—	330	—	mΩ	I_{SW}=200 mA [9]
	R_{ON}	—	—	585	mΩ	I_{SW}=200 mA and T_J=150 °C [9]
Gate-driver under-voltage lock-out (turn-off)	$V_{GD_UVLO,OFF}$	—	3.6	—	V	V_{GD}=V_{BOOT}-V_{SW}
Gate-driver under-voltage lock-out (turn-on)	$V_{GD_UVLO,ON}$	—	3.7	—	V	V_{GD}=V_{BOOT}-V_{SW}
Supply						
Voltage internally supplied to VCC pin	V_{VCC}	—	—	7.3	V	
VIN pin operating current in dim-to-off	I_{VIN_DO}	—	—	2.3	mA	V_{DIM}=0 V
VIN pin operating current in shutdown	I_{VIN_SD}	—	—	100	µA	V_{SD}=0 V and V_{DIM}=3.3V provided externally[10]
	I_{VIN_SD}	—	—	140	µA	V_{SD}=0 V and V_{DIM}=3.3V provided externally[11]
VIN under-voltage lock-out (turn-off)	$V_{VIN_UVLO,OFF}$	—	7.1	—	V	
VIN under-voltage lock-out (turn-on)	$V_{VIN_UVLO,ON}$	—	7.5	—	V	
Shutdown						
SD pin input high voltage	$V_{SD,IH}$	2.1	—	—	V	
SD pin input low voltage	$V_{SD,IL}$	—	—	1.0	V	
SD pin, reduced pull-up current during shutdown	$-I_{SD,LPU}$	—	—	3.0	µA	V_{SD}=0 V V_{DIM}>$V_{DIM,SD}$ provided externally
SD pin, initial pull-up current to start shutdown	$-I_{SD,HPU}$	—	48	71	µA	V_{SD}>$V_{SD,IH}$ V_{DIM}>$V_{DIM,SD}$ provided externally

(table continues...)

8 PG-DSO-8
9 PG-DSO-8 with exposed pad
10 Tested at V_{VIN}=8 V.
11 Tested at V_{VIN}=80 V.

Table 5 (continued) DC electrical characteristics

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
DIM pin low power mode current	$I_{DIM,SD}$	—	52	105	µA	V_{SD}=0 V
DIM pin low power mode voltage	$V_{DIM,SD}$	3.1	—	—	V	V_{SD}=0 V
Regulation						
CS reference voltage high	V_{CSH}	379	390	401	mV	undimmed
CS reference voltage low	V_{CSL}	320	330	340	mV	undimmed
CS reference voltage hysteresis	$HYST_{CS}$	7	—	—	%	peak-to-average $HYST_{CS} = 100x\frac{V_{CSH}-V_{CSL}}{V_{CSH}+V_{CSL}}$
Dimming						
DIM pin input high voltage	$V_{DIM,IH}$	2.1	—	—	V	
DIM pin input low voltage	$V_{DIM,IL}$	—	—	1.0	V	
Input low current (internal pull-up)	$-I_{DIM,LPU}$	—	—	65	µA	V_{DIM}=0 V

The values in switching characteristics are verified by design and not tested in production test.

Table 6 Switching characteristics

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
Integrated switch and driver						
Undimmed average switch current	$I_{SW,AVG}$	—	—	1.5[12)]	A	selectable using CS shunt resistor
Switching frequency	f_{SW}	—	—	2	MHz	
Shutdown						
SD pin stable high	t_{SD_HI}	20	—	—	ms	time to begin of SW turn-on (low power mode exit)
SD pin stable low	t_{SD_LO}	5	—	—	µs	time to begin of SW turn-off (low power mode entry)
Regulation						
Delay from V_{CS} crossing to begin of SW turn-off or turn-on	t_{CSSW}	—	—	120	ns	
Dimming						

(table continues...)

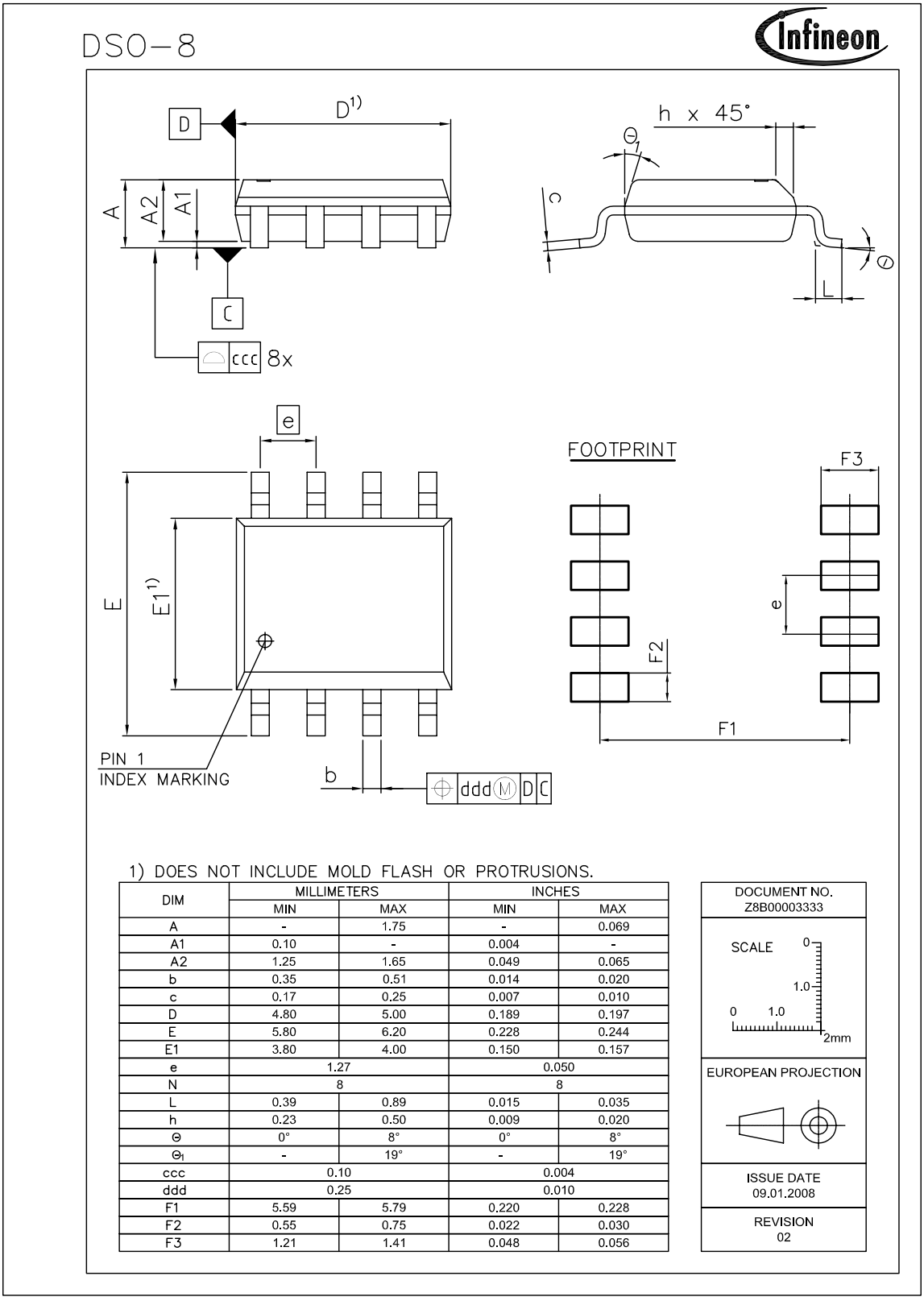
12 The system must be capable of dissipating the power.

Table 6 (continued) Switching characteristics

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
Output current hybrid dimming frequency	f_{OUT}	3060	3400	3740	Hz	
Input PWM frequency	f_{INPUT}	250	—	20000	Hz	
Input PWM recognizable duty cycle	D_{PWM_IN}	0	—	100	%	
Input PWM duty cycle dim-to-off (turn-off)	$D_{PWM_IN,OFF}$	—	0.45	—	%	
Input PWM duty cycle dim-to-off (turn-on)	$D_{PWM_IN,ON}$	—	0.5	—	%	
Input PWM recognizable duty cycle accuracy	A_{PWM_IN}	—	$\pm 2^{-14}$	—	LSB^{-1}	f_{INPUT}=1 kHz
Over-temperature protection						
Thermal shutdown threshold (turn-off)	$T_{OT,OFF}$	153	—	161	°C	
Thermal shutdown threshold (turn-on)	$T_{OT,ON}$	138	—	146	°C	
Thermal shutdown hysteresis	$T_{OT,HYST}$	15	—	—	°C	
Soft-start						
Soft-start time in dimming	t_{SS}	—	—	10/ f_{INPUT}	s	
Soft-start time undimmed	$t_{SS,100\%}$	—	—	50	ms	

5 Package dimensions

The package dimensions of PG-DSO-8 and PG-DSO-8 with exposed pad are provided.



1) DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	-	1.75	-	0.069
A1	0.10	-	0.004	-
A2	1.25	1.65	0.049	0.065
b	0.35	0.51	0.014	0.020
c	0.17	0.25	0.007	0.010
D	4.80	5.00	0.189	0.197
E	5.80	6.20	0.228	0.244
E1	3.80	4.00	0.150	0.157
e	1.27		0.050	
N	8		8	
L	0.39	0.89	0.015	0.035
h	0.23	0.50	0.009	0.020
Θ	0°	8°	0°	8°
Θ1	-	19°	-	19°
ccc	0.10		0.004	
ddd	0.25		0.010	
F1	5.59	5.79	0.220	0.228
F2	0.55	0.75	0.022	0.030
F3	1.21	1.41	0.048	0.056

DOCUMENT NO.
Z8B00003333

SCALE 0 1.0 0 1.0 2mm

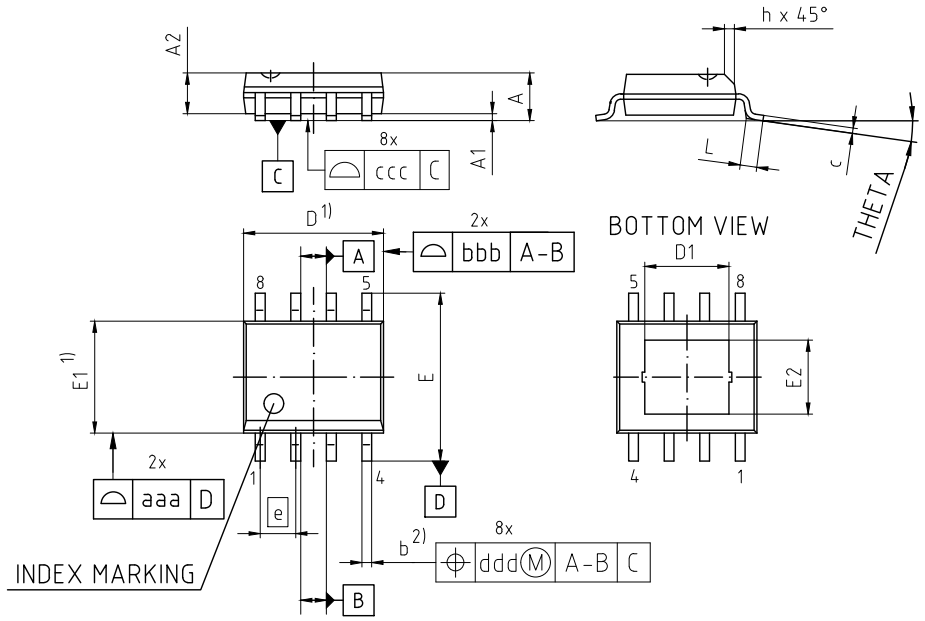
EUROPEAN PROJECTION

ISSUE DATE
09.01.2008

REVISION
02

Figure 15 Package dimensions for PG-DSO-8

Package dimensions



1) DOES NOT INCLUDE PLASTIC OR METAL PROTRUSION OF 0.15 MAX. PER SIDE
2) DAMBAR PROTRUSION SHALL BE MAXIMUM 0.1 mm TOTAL IN EXCESS OF LEAD WIDTH.

DIMENSIONS	MILLIMETERS	
	MIN.	MAX.
A	-	1.70
A1	0.00	0.10
A2	1.45	
b	0.32	0.50
c	0.19	0.25
D	4.80	5.10
D1	2.80	3.20
E	5.80	6.20
E1	3.80	4.00
E2	2.45	2.85
e	1.27	
h	0.35	
L	0.39	0.99
THETA	0°	8°
aaa	0.10	
bbb	0.10	
ccc	0.08	
ddd	0.20	

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Figure 16 Package dimensions for PG-DSO-8 with exposed pad

Revision history

Major changes since previous revision

Revision history

Reference	Description
V1.0	First release
V1.1	Absolute maximum ratings changed (V_{SW} min)
V1.2	R_{ON} split for T_A = 25 °C and T_J = 150 °C
V1.3	$-I_{SD,HPU}$, $I_{DIM,LPI}$ and $V_{DIM,SD}$ added, SD pin behavior described
V1.4	ESD protection described
V1.5	Absolute maximum rating for V_{SW} updated

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